United States Patent

Ezaki

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[54] CORE DRIVE AND BIASING SYSTEM

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[30] **Foreign Application Priority Data**

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[52] **U.S. Cl.**.....**340/166 R**, 340/174 TB

[51] **Int. Cl.**.....**H04q 9/00**

[58] **Field of Search**.....340/166, 173, 174 TB

[56] **References Cited**

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[57] **ABSTRACT**

A read/write drive circuit for a circuit having a driver and a plurality of read/write circuit units connected in parallel thereto, wherein when one desired circuit unit is driven with a potential of one polarity, a potential of the opposite polarity is applied to other circuit units, thereby preventing a flow of current through the other circuit units and through an inadvertent ground path including stray capacitances. A higher speed operation is feasible because no charging current flows through the other circuit units that are not driven.

4 Claims, 4 Drawing Figures

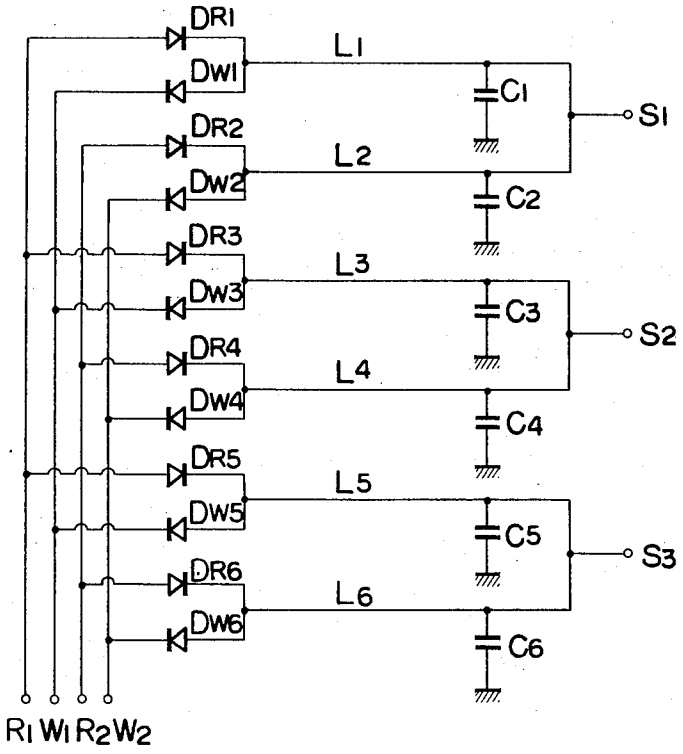


FIG. 1

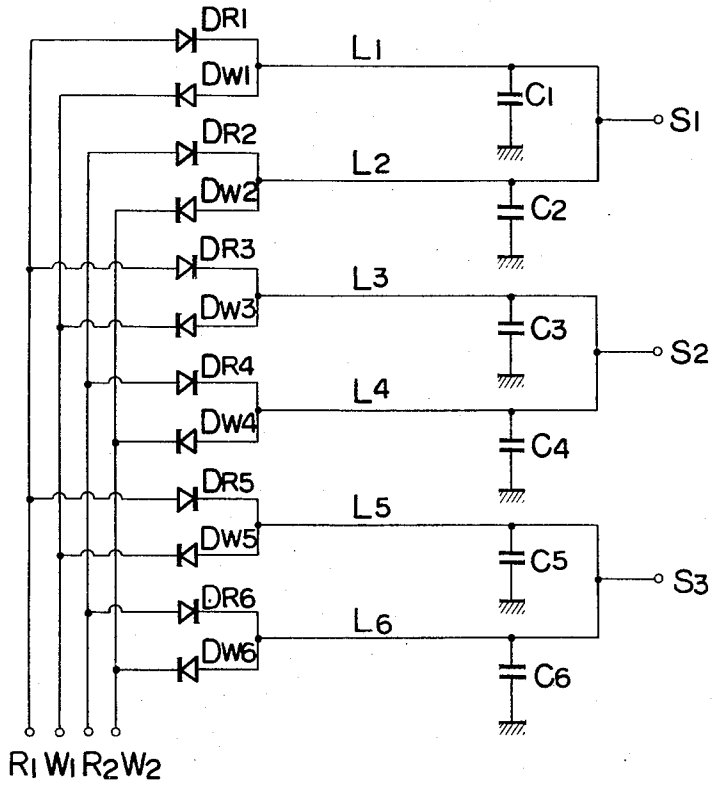

DR1
DW1
L1
C1
S1
DR2
L2
DW2
C2
DR3
L3
DW3
C3
S2
DR4
L4
DW4
C4
DR5
L5
DW5
C5
S3
DR6
L6
DW6
C6
R1 W1 R2 W2

FIG. 2

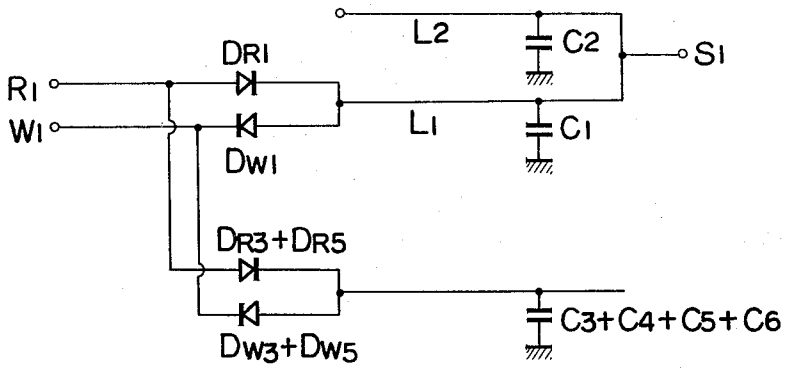

L2
C2
S1
DR1
R1
W1
L1
C1
DW1
DR3+DR5
C3+C4+C5+C6
DW3+DW5

FIG. 3

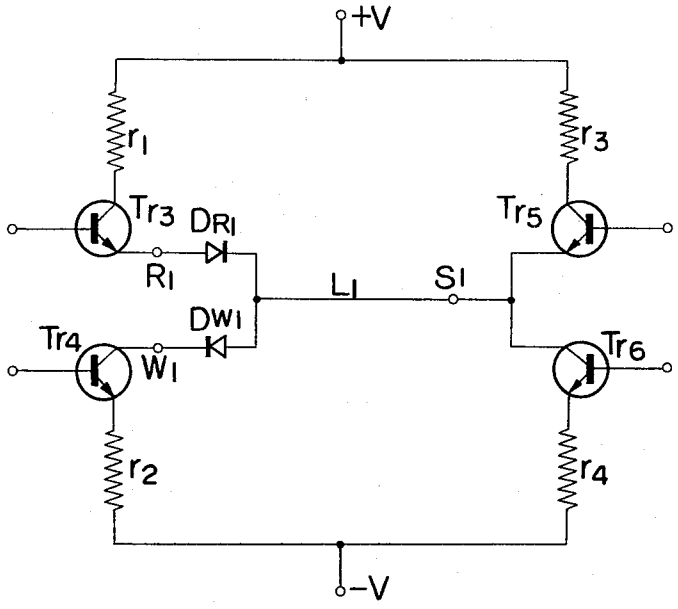
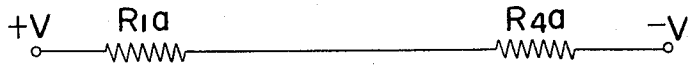


FIG. 4



CORE DRIVE AND BIASING SYSTEM

BACKGROUND OF THE INVENTION

The present invention relates to generally a read/write drive circuit and more particularly to a drive circuit in which a plurality of read/write drive circuits are connected in parallel to a common driver.

In the conventional core matrix driving, an electrostatic capacitance forming a ground path between a drive wire and the ground presents always a serious problem. In a drive circuit in which a plurality of drive circuit units are connected in parallel to a common driver, upon driving a desired drive wire, it is charged to a capacitance equivalent to that between the drive wire and the ground.

In this case, other drive wires are also charged. Upon completion of driving, the charge may be discharged through for example bias resistors, but since the discharge time is always large, a high speed operation is very difficult.

SUMMARY OF THE INVENTION

The present invention relates to a read/write driving system having a plurality of read/write circuit units connected in parallel to a common driver, in which a desired circuit unit is driven with a potential of one polarity while to the other circuits units that are not driven are applied a potential of the opposite polarity.

One of the objects of the present invention is to attain a higher speed operation of a core matrix.

According to one embodiment of the present invention, the collectors of a read-out drive transistor and a write switching transistor are connected through load resistors to a positive voltage source while the emitters of the above transistors are connected to a read-out terminal and a switch terminal respectively. In a similar manner, the emitters of a write drive transistor and a read-out switching transistor are connected through load resistors to a negative voltage source while the collectors of the above transistors are connected to a write terminal and the switch terminal respectively. The resistance of the load resistors on the side of the positive voltage source is selected to be higher than that of the load resistors on the side of the negative voltage source. Therefore, when one selected circuit unit is driven, a potential at the connections of other parallel circuit units becomes lower than the ground potential so that the one selected circuit unit that is driven is applied with a potential of one polarity while the other units, with a potential of the opposite polarity. Therefore, no current flows through the other units that are not driven and the drive wires of the other units are not charged. Each of the circuit units includes a diode so that one of said diodes is forward biased while the remainder are actively back biased by maintaining the anode voltage less than ground.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a circuit diagram of a core matrix read/write driving circuit;

FIG. 2 is an equivalent circuit of FIG. 1 for explanation of the operation thereof;

FIG. 3 is a circuit diagram in accordance with the present invention illustrating one drive wire and a driving section; and

FIG. 4 is an equivalent circuit of the circuit of FIG. 3 for explanation of the operation thereof.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a circuit diagram of a core matrix driving circuit consisting of two pairs of read-out drivers and write drivers and three switch matrix. The drive wires L_1 to L_5 pass through memory cores (not shown) and one end of each drive wire is connected to parallel circuits each consisting of a pair of first diodes Dr_1 to Dr_6 and second diodes Dw_1 to Dw_6 respectively. The other ends of the drive wires L_1 and L_2 are connected to a switch terminal S_1; the other ends of drives wires L_3 and L_4, to a switch terminal S_2; and the other ends of drive wires L_5 and L_6, to a switch terminal S_3. The anodes of the write pulse drive diodes Dr_1, Dr_3 and Dr_5 are connected to a common read-out terminal R_1 while the anodes of the write pulse drive diodes Dr_2, Dr_4 and Dr_6 are connected to a common read-out terminal R_2. The cathodes of diodes Dr_1–Dr_6 are connected to their respective drive wires L_1 to L_6. In a similar manner but reversed with respect to the diode connections, the write pulse drive diodes Dw_1, Dw_3 and Dw_5 are connected to a common write terminal W_1 while the write pulse drive diodes Dw_2, Dw_4 and Dw_6 are connected to a common write terminal W_2. Reference characters C_1 to C_6 designate the grounding capacitances of the drives wires L_1 to L_6 respectively.

FIG. 2 shows an equivalent circuit of the circuit shown in FIG. 1 when the drive wire L_1 is used for write drive. In order to drive the read-out pulse drive diode Dr_1 into conduction, a positive voltage is impressed from the read-out terminal R_1. In this case, both of the read-out pulse drive diodes Dr_3 and Dr_5 are driven into conduction and the grounding capacitors C_3, C_4, C_5 and C_6 are also charged. Upon completion of the read-out, the capacitors C_3 to C_6 are discharged through bias resistors or the like, but the discharging time interval is very long so that it is very difficult to realize high-speed driving.

In FIG. 3 illustrating a circuit diagram of one drive wire and its driving section of one embodiment of the present invention, both of a read-out drive transistor Tr_3 and a write-in switching transistor Tr_5 have their collector electrodes connected to a positive voltage source +V through load resistors r_1 and r_3 respectively while their emitter electrodes are connected to a read-out terminal R_1 and a switch terminal S_1 respectively. In a similar manner, the emitters of a write drive transistor Tr_4 and a read-out switching transistor Tr_6 are connected to a negative voltage source −V through load resistors r_2 and r_4 respectively while their collector electrodes are connected to a write terminal W_1 and the switch terminal S_1 respectively. A reference character S_1 designates a drive wire.

FIG. 4 is an equivalent circuit of the circuit shown in FIG. 3 when the drive wire L_1 is used for read-out drive. In this circuit, the load resistor r_1 may be approximated to a resistor R_{1a} while the load resistor r_4, to a resistor R_{4a}. Assume in this circuit that a voltage between the drive wire L_1 and the ground be E, then

$$E = V - R_{1a} I \tag{1}$$

$$E = -V + R_{4a} I \tag{2}$$

where I is the current flowing through the drive wire L_1; and

$$R_{1a} > R_{4a} \text{ so that } R_{1a} I > R_{4a} I.$$

From Eqs. (1) and (2),

$$2E = R_{4a} I - R_{1a} I < 0$$

Hence,

$$E < 0.$$

This means that $R_{1a} > R_{4a}$ is the condition for obtaining $E<0$.

When the potential of the drive wire L_1 is negative relative to the ground potential, a negative potential is applied to the terminals of the diodes Dr_3 and Dr_5 connected to the terminal R_1 as is readily seen from FIG. 2, so that neither of the diodes Dr_3 and Dr_5 are driven into conduction. Consequently, the capacitors C_3 to C_6 are not charged.

The present invention has been so far described only regarding to the case in which the drive wire L_1 is used for read-out drive, but it will be readily understood from the foregoing that other drive wires are used for read-out and write drives in a similar manner as described above. It will be understood that the system in accordance with the present invention is not only employed for driving a core matrix but also for an ordinary transmission line.

It will be seen that in the transmission line driving system in accordance with the present invention, no charging current is flown into a circuit that is not driven so that a high-speed driving may be realized.

I claim:

1. A read and write drive circuit system for a plurality of read and write drive circuits for a core memory, said plurality of read drive circuits including groups of diodes having their anodes connected together to respective read drive lines, said plurality of write drive circuits including groups of diodes having their cathodes connected together to respective write drive lines, voltage divider means having points connected to respective ones of said read and write drive lines, and selection means for selectively forward biasing one diode of one of said groups of diodes and reversely biasing the remainder of the diodes of the group, at least one of the divider points being maintained at a voltage level less than ground when a corresponding read line is energized and being maintained at a voltage level greater than ground when a corresponding write line is energized so that said forward biased diode carries current to the core memory while the remainder of the diodes of the selected group are actively back biased to prevent stray capacitance between the cathode of read diodes and ground and between the anode or write diodes and ground from being inadvertently charged.

2. A read and write drive circuit system as set forth in claim 1, wherein said selection means comprises a first driving transistor having collector and emitter terminals, and a second switching transistor having collector and emitter terminals, a source of positive voltage and a source of negative voltage, said voltage divider comprising a first load resistor connected between said source of positive voltage and said collector of said first driving transistor, and a second load resistor connected between the emitter of said second switching transistor and said source of negative voltage, said anode of the diode of said selected drive circuit being connected to the emitter of said first drive transistor and said cathode of said diode of said selected drive circuit being coupled to the collector of said second switching transistor.

3. A read and write drive circuit system as set forth in claim 2, wherein the magnitude of said positive and negative voltages are equal and the equivalent resistance between said emitter of said first driving transistor and said source of positive voltage is greater in value than the equivalent resistance between said collector of said second switching transistor and said source of negative potential.

4. A read and write drive circuit system as set forth in claim 3, comprising a read line and a corresponding write line and a switch terminal energized for pairs of corresponding read and write lines, a second driving transistor having emitter and collector terminals, said emitter of said first driving transistor and said collector of said second driving transistor connected to said read and write lines respectively, a first switching transistor having emitter and collector terminals, a third load resistor connected between the emitter of said second driving transistor and said source of negative voltage, a fourth load resistor connected between said collector of said first switching transistor and said source of positive voltage, said collector of said second switching transistor and said emitter of said first switching transistor connected together and to said switch terminal, and a write diode having an anode and a cathode, said anode of said write diode coupled to said switch terminal and said cathode of said write diode connected to said collector of said second driving transistor.

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