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Title: ELECTROSTATIC DISCHARGE COMPLIANT PATTERNED ADHESIVE TAPE

Abstract: The present disclosure relates to the field of fabricating microelectronic devices, wherein a microelectronic device substrate, such as a microelectronic wafer, may be thinned by a backgrinding process using a patterned adhesive tape that reduces slurry seepage and adhesive contamination while also reducing the potential of electrostatic discharge damage. The patterned adhesive tape may comprise a base film and adhesive material patterned on the base film such that an edge or periphery portion of the microelectronic device substrate may contact the adhesive material, but substantially no adhesive material contacts interconnectors formed on the microelectronic device substrate. The base film of the patterned adhesive tape may have an electrically conductive coating or layer, or may be electrically conductive itself to reduce the potential of electrostatic discharge damage during the backgrinding process.

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BACKGROUND

Embodiments of the present description generally relate to the field of microelectronic device fabrication and, more particularly, to thinning of microelectronic wafers with a backgrinding process.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 illustrates a microelectronic device substrate having a plurality of microelectronic dice on an active surface thereof, as known in the art.

FIG. 2 illustrates a side cross-sectional view of an adhesive tape applied over an active surface of a microelectronic device substrate prior to a backgrinding process, wherein an adhesive material of the adhesive tape substantially encapsulates interconnectors disposed on the active surface of the microelectronic device substrate, as known in the art.

FIG. 3 illustrates a side cross-sectional view of the structure of FIG. 2 after the backgrinding process, as known in the art.

FIG. 4 illustrates a side cross-sectional view of an adhesive tape applied over an active surface of a microelectronic device substrate, wherein an adhesive material of the adhesive tape substantially encapsulates an upper portion of interconnectors disposed on the active surface of the microelectronic device substrate (illustrated after the backgrinding process), as known in the art.

FIG. 5 illustrates a side cross-sectional view of an adhesive tape applied over an active surface of a microelectronic device substrate, wherein an adhesive material of the adhesive tape contacts a top portion of the interconnectors disposed on the active surface of the microelectronic device substrate (illustrated after the backgrinding process), as known in the art.
FIG. 6 illustrates a film-side oblique view of a patterned adhesive tape according to an embodiment of the present description.

FIG. 7 illustrates an adhesive-side view of the patterned adhesive tape of FIG. 8, according to an embodiment of the present description.

FIG. 8 illustrates a side cross-sectional view of the patterned adhesive tape, according to an embodiment of the present description applied over an active surface of a microelectronic device substrate.

FIG. 9 illustrates a side cross-sectional view of the inset A of FIG. 8, according to an embodiment of the present description.

FIG. 10 illustrates a side cross-sectional view of the inset A of FIG. 8, according to another embodiment of the present description.

FIG. 11 illustrates a side cross-sectional view of the inset A of FIG. 8, according to a still another embodiment of the present description.

FIG. 12 illustrates a side cross-sectional view of the inset A of FIG. 8, according to a further embodiment of the present description.

FIG. 13 is flow diagram of a process of backgrinding a microelectronic device substrate utilizing a patterned adhesive tape according to an embodiment of the present description.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only
by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and those elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

Embodiments of the present description relate to the field of fabricating microelectronic devices, wherein a microelectronic device substrate, such as a microelectronic wafer, may be thinned by a backgrinding process using a patterned adhesive tape that reduces slurry seepage and adhesive contamination while also reducing the potential of electrostatic discharge damage.

In the production of microelectronic devices, integrated circuitry may be formed in and/or on microelectronic device substrates. As shown in FIG. 1, a single microelectronic device substrate 100, such as a silicon or a silicon-germanium wafer, may contain a plurality of substantially identical integrated circuits (not shown) forming a plurality of microelectronic dice 102, such as microprocessors, chipsets, graphics devices, wireless devices, memory devices, application specific integrated circuits, or the like, on an active surface 104 of the microelectronic device substrate 100. Each of the microelectronic dice 102 may include a plurality of interconnectors 112, such as solder bumps or pillars, which may be in electrical contact with the integrated circuits (not shown) of their respective microelectronic dice 102. As will be understood to those skilled in the art, the interconnectors 112 may be used to connect the microelectronic dice 102 to external device or components (not shown). The interconnectors 112 may be any appropriate electrically conductive material, including but not limited to lead/tin alloys, such as tin/lead solder, such as 63% tin / 37% lead solder, or lead-free solders, such as pure tin or high tin content alloys (e.g. 90% or more tin), such as tin/bismuth, eutectic tin/silver, ternary tin/silver/copper, eutectic tin/copper, and similar alloys. The fabrication processes for the integrated circuits (not shown) and the interconnectors 112 are well known in the art and will not be discussed herein in the interest of brevity.

In a wafer backgrinding process (also known as 'wafer thinning' or 'backlapping'), a portion of a back surface 106 (see FIG. 2) of the microelectronic device substrate 100, which opposes the microelectronic device substrate active surface 104, is removed to reduce its thickness (see thickness $T_1$ for FIG. 2 prior to wafer backgrinding and thickness $T_2$ in FIG. 3 after wafer backgrinding). Wafer backgrinding is not necessary in the fabrication of the microelectronic dice 102 themselves, but as the desire to make microelectronic devices thinner
for use in smart cards, memory sticks, smart phones, portable music players, and other compact
electronic products, it has become an advantageous process.

As shown in FIGs. 2 and 3, in the backgrinding process, an adhesive tape 122 may be
applied over the microelectronic device substrate active surface 104 prior to the backgrinding
process to provide support thereof during the backgrinding process and to protect the
microelectronic device substrate 100 from mechanical damage and contamination during the
backgrinding process. The adhesive tape 122 may be comprised of a base film 124 and a layer
of adhesive material 126. The backgrinding process may be conducted with a backgrinding tool
comprising grinding wheels (bounded abrasive particle) and a cooling fluid. After the
backgrinding process, the microelectronic device substrate 100 is removed from the adhesive
tape 122 and sent for further processing.

As shown in FIGs. 2 and 3, the attachment of the adhesive tape 122 to the microelectronic
device substrate active surface 104 may include the adhesive material layer 126 substantially
encapsulating the interconnectors 112 and substantially covering the microelectronic device
substrate active surface 104. This arrangement may be referred to as “full-bump encapsulation”.
However, residual adhesive may remain on the microelectronic device substrate active surface
104 and/or interconnectors 112 after the removal of the adhesive tape 122, particularly at a
periphery or edge portion 108 proximate an edge 110 of the microelectronic device substrate 100
and in areas of a high density/tight pitch interconnector 112 pattern. Such, residual adhesive can
result in defects in the microelectronic dice 102, as will be understood to those skilled in the art.

As shown in FIG. 4, in order to reduce residual adhesive contamination, the attachment of
the adhesive tape 122 to the microelectronic device substrate active surface 104 may comprise a
portion of the adhesive material layer 126 in contact with the microelectronic device substrate
edge portion 108 and in contact with a top portion 114 of each interconnector 112 and an upper
portion of each interconnector 112 proximate the top portion 114 thereof. This arrangement may
be referred to as "partial bump lamination" and may be effectuated by reducing the thickness of
the adhesive material layer 126 and/or reducing the adhesive properties of the adhesive material
layer 126. Although with the adhesive tape 122 of FIG. 4, it may be possible to reduce or
substantially eliminate adhesive residue on the microelectronic device substrate active surface
104, it may result in adhesive residue on the interconnector 112.

As shown in FIG. 5, in order to further reduce residual adhesive contamination, the
attachment of the adhesive tape 122 to the microelectronic device substrate active surface 102
may comprise a portion of the adhesive material layer 126 in contact with the microelectronic
device substrate edge portion 108 and in contact with the top portion 114 of each
interconnector 112. This arrangement is referred to as "bump lop lamination" and maybe effectuated by further reducing the thickness of the adhesive material layer 126 and/or further reducing the adhesive properties of the adhesive material layer 126.

However, reducing the thickness of the adhesive material layer 126 and/or reducing the adhesive properties of the adhesive material layer 126 may increase the risk of seepage backgrinding slurry between the adhesive material layer 126 and the microelectronic device substrate active surface 104. Backgrinding slurry is a combination of process cooling fluid and particles from the grinding wheel due to wear. Such backgrinding slurry contamination can result in defects in the microelectronic dice 102, as will be understood to those skilled in the art. Moreover, with a desire to increase the number of microelectronic dice 102 (see FIG. 1) on each microelectronic device substrate 100, the space around the microelectronic device substrate edge portion 108 is reduced, which reduces the available contact area between the adhesive material layer 126 and the microelectronic device substrate active surface 104. Thus, the reduction in contact area and the reduction in the adhesive material thickness may significantly increase the risk of seepage of the backgrinding slurry between the adhesive material layer 126 and the microelectronic device substrate active surface 104.

Thus, the prevention of adhesive residue is at odds with the prevention of slurry seepage, because to eliminate the adhesive residue on microelectronic device substrate active surface 102 and/or interconnectors 112, modulus properties of the adhesive material layer 126 have to be increased and, to eliminate the occurrence of slurry seepage, the adhesion properties of the adhesive material layer 126 have to be increased, which means the modulus properties of adhesive material layer 126 have to be decreased. Therefore, the materials property of the adhesive tape 122 cannot be optimally balanced.

Furthermore, the tape lamination process (e.g. attaching the microelectronic device substrate 100 to the adhesive tape 122 prior the backgrinding process) and the de-lape process (e.g. removing the wafer after the backgrinding process) may generate an electrostatic charge within the adhesive tape 122. If this electrostatic charge discharges through the interconnectors 112, the discharge can damage the integrated circuits, such as copper traces and interlayer dielectric layers (not shown) of their respective microelectronic dice 102 (see FIG. 1), as will be understood those skilled in the art.

In an embodiment of the present disclosure, a patterned adhesive tape 200 may be comprised of a base film 202 and an adhesive material layer 204 disposed therein on, with at least one opening 212 patterned through an adhesive material layer 204, as shown in FIGs. 6 and 7. As shown in FIG. 8, an intermediate structure 210 may be formed by attaching a
microelectronic device substrate 100 to the adhesive material layer 204. The adhesive material layer openings 212 may be patterned, such that the microelectronic device substrate edge portion 108 may contact the adhesive material layer 204, but substantially no portion of the adhesive material layer 204 contacts the interconnectors 112, as shown in FIG. 8. Such an arrangement may substantially reduce adhesive residue contamination and/or backgrinding slurry seepage. With regard to adhesive residue contamination reduction, having substantially no portion of the adhesive material layer 204 contacting the interconnectors 112, means that substantially no adhesive residue will result on the interconnectors 112. With regard to backgrinding slurry seepage reduction, having the adhesive material layer 204 only contacting the microelectronic device substrate edge portion 108 will allow for the use of the adhesive material layer 204 having of low modulus and high tackiness to achieve an effective seal, which may significantly reduce or prevent slurry seepage during the backgrinding process.

In one embodiment, the opening 212 through the adhesive material layer 204 may be substantially circular. In another embodiment, the opening 212 may be sized such that the microelectronic device substrate edge portion 108 which contacts the adhesive material layer 204 has a width of about equal to or less than about 3 mm. In still another embodiment, the opening 212 may be sized such that the microelectronic device substrate edge portion 108 which contacts the adhesive material layer 204 has a width of about equal to or less than about 2 mm. The adhesive material layer 204 may be an ultra-violet light curable adhesive. In one embodiment, the adhesive material layer 204 may have an adhesion greater than about 4500 mN / 25 mm.

Referring back to FIG. 6, at least one alignment mark 214 may be formed on the base film 202 of the patterned adhesive tape 200 to allow appropriate positioning of the microelectronic device substrate 100 (see FIG. 8) in relation to the openings 212 of the patterned adhesive tape 200.

In one embodiment of the present description, the base film 202 may include an electrically conductive element therein as a mechanism for electrostatic discharge. As will be understood to those skilled in the art, the electrically conductive element may be grounded such that any electrostatic charge that may be built-up during the attachment of the patterned adhesive tape 200 to the microelectronic device substrate 100 and/or during the removal of the microelectronic device substrate 100 from the patterned adhesive tape 200 may be discharged.

In one embodiment shown in the FIG. 8, the base film 202 itself may be the electrically conductive element. The electrically conductive base film 202 may comprise any electrically conductive material, including but not limited to, conducting polymers (such as polyphenylenes,
polypyrrenes, polyazulenes, polynaphthalenes, polyacetylenes, poly p-phenylene vinylenes, poly
cyrrroles, polycarbazoles, polyindoles, polya/epines, polyanilines, polythiophenes, poly(3,4-
ethylendioxythiophene)s, poly(p-phenylene sul ft de)s, functionalized polyethylene oxides, ionomers, and ionic conductive polymers), or may contain conductive fillers, including but not limited to, metal coated glass, aluminum doped zinc oxide, nickel-coated graphite, fluorine-

In another embodiment shown in FIG. 9, the base film 202 may comprise a support film 220 and an electrically conductive coating or film 230, as the electrically conductive element. The support film 220 may comprise any appropriate material, including but not limited to, polymer materials. The electrically conductive film 230 may comprise any electrically conductive material, including but not limited to, conducting polymers (such as polyphenylenes, polypyrrenes, polyazulenes, polynaphthalenes, polyacetylenes, poly p-phenylene vinylenes, polypyrroles, polycarbazoles, polyindoles, polya/epines, polyanilines, polythiophenes, poly(3,4-
ethylendioxythiophene)s, poly(p-phenylene sulfide)s, functionalized polyethylene oxides, ionomers, and ionic conductive polymers), or may contain conductive fillers, including but not limited to, metal coated glass, aluminum doped zinc oxide, nickel-coated graphite, fluorine-
doped tin oxide, nickel graphite, indium tin oxide, silver particles, tin panicles, and the like. As shown in FIG. 9, the electrically conductive film 220 may be disposed between a first surface 222 of the support film 220 and the adhesive material layer 204. As shown in FIG. 10, the electrically conductive film 230 may be disposed proximate a second surface 224 of the support film 220 (opposing the support film first surface 222 and the adhesive material layer 204). It is understood that the base film 202 may comprise a plurality of layers of support film 220 and/or a plurality of layers of electrically conductive film 230. Such multiple layers within the base film 202 may allow for the tuning of the mechanical properties of the base film 202 for use in ultra-thin wafer thinning (e.g. thinning to less than about 200 µm).

In order to minimize stress and have sufficient support of the microelectronic device substrate 100 during the backgrinding process, a height H of the interconnector 112 may be approximately the same as a thickness T of the adhesive material layer 204, as shown in FIGs. 9 and 10.

In another embodiment of the present description, with ultra-thin substrate thinning, due to no adhesive in the bump area during thinning, there may not be sufficient support for microelectronic device substrate 100. Therefore, as shown in FIG. 11, a compliant layer 240 may be disposed proximate the support film first surface 222, such that the compliant layer 240 at least partially (e.g., either partially (shown) or fully) encapsulates the interconnectors 112, to
provide additional support. The use of the compliant layer 240 may result in lower shear stresses on the microelectronic device substrate edge portion 108 (see FIG. 8) with more uniform stress transferred across an entire contact surface between the patterned adhesive tape 200 and the microelectronic device substrate 100, as will be understood to those skilled in the art. The compliant layer 240 may include any appropriate material, including but not limited to a soft polymer layer, such as an ultraviolet light curable adhesive, pre-cured elastomer, and the like. It is understood that the compliant layer 240 should be selected such that it does not leave residual use during the removal through the base film 

electrically conductive element, as defined in block 340.

As shown in FIG. 12, the compliant layer 240 may itself be the electrically conductive element or may contain the electrically conductive element, such as electrically conductive particles 250, dispersed therein, to act as an electrostatic discharge means. The electrically conductive particles 250 may include, but is not limited to, metal coated glass, aluminum doped zinc oxide, nickel-coated graphite, fluorine-doped tin oxide, nickel graphite, indium tin oxide, silver particles, tin particles, and the like. Furthermore, as also shown in FIG. 12, the electrically conductive particles 250 may also be contained within the support film 220 to have the support film 220 to act as an electrostatic discharge means in addition to or in lieu of the electrically conductive particles 250 in the compliant layer 240.

It is understood the subject matter of the present description can including combination of layer of support films 220, electrically conductive film 230, and compliant layers 240.

An embodiment of one process of thinning a microelectronic device substrate using the patterned adhesive tape of the present description is illustrated in a flow diagram 300 of FIG. 13. As defined in block 310, an adhesive tape may be formed with a base film and an adhesive material layer disposed thereon with at least one opening patterned through the adhesive material layer, wherein the base film includes an electrically conductive element. A microelectronic device substrate, having a plurality of interconnects extending from an active surface thereof, may be attached to the patterned adhesive tape, such that an edge or periphery of the microelectronic device substrate active surface adheres to the adhesive material layer proximate the opening with the plurality interconnectors extending into the adhesive material layer opening, and wherein any electrostatic charge generated during the adhering of the microelectronic device substrate is discharged through the base film electrically conductive element, as defined in block 320. As defined in block 330, the microelectronic device substrate may be thinned by removing a portion of the microelectronic device substrate from a back surface thereof. The microelectronic device substrate may then be removed from the patterned adhesive tape while discharging any electrostatic charge generated during the removal through the base film electrically conductive element, as defined in block 340.
It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 8-13. The subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art. Furthermore, the subject matter may also be used in any appropriate application outside of the microelectronic device fabrication field.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.
What is claimed is:

1. A patterned adhesive tape comprising:
   a base film including an electrically conductive element; and
   an adhesive material layer disposed proximate a first surface of the base film with at least
   one opening patterned through the adhesive material layer, wherein the at least one opening is
   adapted to adhere to an edge portion of a microelectronic device substrate.

2. The patterned adhesive tape of claim 1, wherein the base film comprises a conductive
   polymer.

3. The patterned adhesive tape of claim 1, wherein the electrically conductive element
   comprises electrically conductive particles dispersed within the base film.

4. The patterned adhesive tape of claim 1, wherein the base film comprises a support film
   and an electrically conductive film as the electrically conductive element.

5. The patterned adhesive tape of claim 4, wherein the support film comprises a polymer
   film.

6. The patterned adhesive tape of claim 4, wherein the electrically conductive film
   comprises a conductive polymer.

7. The patterned adhesive tape of claim 4, wherein the electrically conductive film is
   disposed on a first surface of the support film with at least a portion thereof between the support
   film and the adhesive material layer.

8. The patterned adhesive tape of claim 4, wherein the electrically conductive film is
   disposed on a second surface of the support film opposing the adhesive material layer on a first
   surface of the support film.
9. The patterned adhesive tape of claim 1, wherein the base film further includes a compliant layer disposed adjacent the adhesive material layer, wherein a portion of the compliant layer is exposed within the at least one opening.

10. The patterned adhesive tape of claim 9, wherein the electrically conductive element comprises electrically conductive particles dispersed within the compliant layer.

11. An intermediate structure comprising:
   a base film including an electrically conductive element;
   an adhesive material layer disposed on the base film having at least one opening patterned therethrough; and
   a microelectronic device substrate having active surface, a edge portion proximate an edge of the microelectronic device substrate, and a plurality of interconnectors extending from the microelectronic device substrate active surface, wherein the microelectronic device edge portion is adhered to the adhesive material layer and wherein the plurality of interconnectors extend into the at least one opening.

12. The intermediate structure of claim 11, wherein a height of the plurality of interconnectors is approximately the same as a thickness of the adhesive material layer.

13. The intermediate structure of claim 12, wherein the base film comprises conductive polymer.

14. The intermediate structure of claim 11, wherein the electrically conductive element comprises electrically conductive particles dispersed within the base film.

15. The intermediate structure of claim 11, wherein the base film comprises a support film and an electrically conductive film as the electrically conductive element.

16. The intermediate structure of claim 15, wherein the support film comprises a polymer film.

17. The intermediate structure of claim 15, wherein the electrically conductive film comprises a conductive polymer.
18. The intermediate structure of claim 15, wherein the electrically conductive film is disposed on a first surface of the support film with at least a portion thereof between the support film and the adhesive material layer.

19. The intermediate structure of claim 15, wherein the electrically conductive film is disposed on a second surface of the support film opposing the adhesive material layer on a first surface of the support film.

20. The intermediate structure of claim 11, wherein the base film further includes a compliant layer disposed adjacent the adhesive material layer, wherein a portion of the compliant layer is exposed within the at least one opening and wherein the compliant layer at least partially encapsulates the plurality of interconnectors.

21. The intermediate structure of claim 20, wherein the electrically conductive element comprises electrically conductive particles dispersed within the compliant layer.

22. The intermediate structure of claim 11, wherein the base film further includes an alignment mark.

23. A method of thinning a microelectronic device substrate comprising:

   forming a patterned adhesive tape with a base film and an adhesive material layer disposed thereon with at least one opening patterned through the adhesive material layer, wherein the base film includes an electrically conductive element;

   adhering an edge portion of an active surface of a microelectronic device substrate to the adhesive material layer proximate the adhesive material layer opening, wherein a plurality of interconnectors disposed on the microelectronic substrate active surface extend into the adhesive material layer opening, and wherein any electrostatic charge generated during the adhering of the microelectronic device substrate is discharged through the base film electrically conductive element;

   removing a portion of the microelectronic device substrate from a back surface thereof; and
removing the microelectronic device substrate from the patterned adhesive tape while discharging any electrostatic charge generated during the removal through the base film electrically conductive element.

24. The method of claim 23, wherein removing the portion of the microelectronic device substrate comprises backgrinding the microelectronic device substrate back surface.

25. The method of claim 23, wherein forming the patterned adhesive tape with the base film and the adhesive material layer disposed thereon comprises forming a thickness of the adhesive material layer that is approximately the same as a height of the plurality of interconnectors on the microelectronic device substrate.

26. The method of claim 23, wherein forming a patterned adhesive tape includes forming a compliant layer disposed adjacent the adhesive material layer, wherein a portion of the compliant layer is exposed within the at least one opening and wherein adhering the microelectronic device substrate includes the compliant layer at least partially encapsulating the plurality of interconnectors.

27. The method of claim 23, wherein adhering the edge portion of the active surface of the microelectronic device substrate to the adhesive material layer proximate the adhesive material layer opening further comprises aligning the microelectronic device substrate to the adhesive material layer opening with at least one alignment mark on the base film.
FIG. 1 (Prior Art)
Start

310
Forming a patterned adhesive tape with a base film and an adhesive material layer disposed thereon with at least one opening patterned through the adhesive material layer, wherein the base film includes an electrically conductive element

320
Adhering an edge portion of an active surface of a microelectronic device substrate to the adhesive material layer proximate the adhesive material layer opening, wherein a plurality of interconnectors disposed on the microelectronic substrate active surface extend into the adhesive material layer opening, and wherein any electrostatic charge generated during the adhering of the microelectronic device substrate is discharged through the base film electrically conductive element

330
Thinning the microelectronic device substrate by removing a portion of the microelectronic device substrate from a back surface thereof

340
Removing the microelectronic substrate from the patterned adhesive tape while discharging any electrostatic charge generated during the removal through the base film electrically conductive element

End

FIG. 13
A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/301(2006.01)i, H01L 21/304(2006.01)1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/301; B24B 7/30; C09J 7/02; B24B 1/00; B32B 7/12; B24B 49/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: backgrinding; adhesive tape; opening; conductive element; electrostatic charge

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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Further documents are listed in the continuation of Box C.

See patent family annex.

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
26 SEPTEMBER 2012 (26.09.2012)

Date of mailing of the international search report
27 SEPTEMBER 2012 (27.09.2012)

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan
City, 302-70 1, Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
Lee Seok Joo
Telephone No. 82-42-818-8681

Form PCT/ISA/210 (second sheet) (July 2009)
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