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(54) Magnetic Bubble Memory Control

(57) In a magnetic bubble memory control apparatus comprising a magnetic bubble memory controller (BMC) 1 for controlling the operating sequence of magnetic bubble memories and data controllers (DC) 2 for controlling the data flow to and from the memories, respective output buffers of the data controllers are each as in Figure 4 and connected to a common bus line 5*a* and operated in an open drain mode during each operation of the memories to check the plurality of data controllers for data abnormality. On detection of abnormality, the output buffers are operated in a tristate mode to check sequentially the data controllers for state to locate the abnormality. On confirmation of the absence of abnormality, the sequential check is omitted.

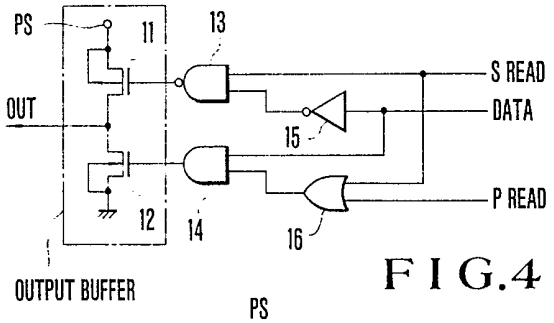

FIG.4

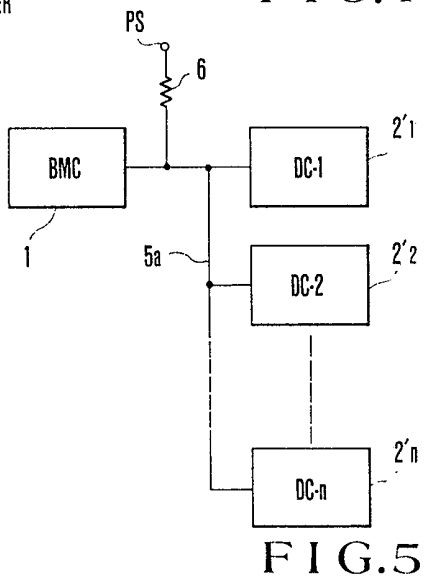

FIG.5

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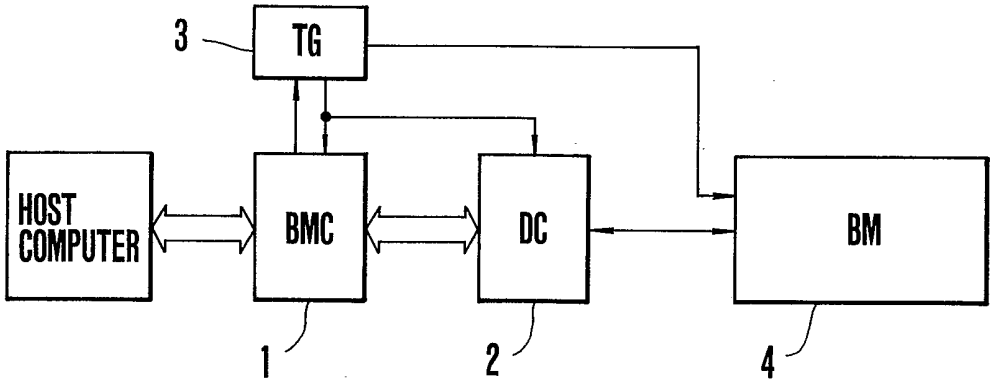

FIG.1
PRIOR ART

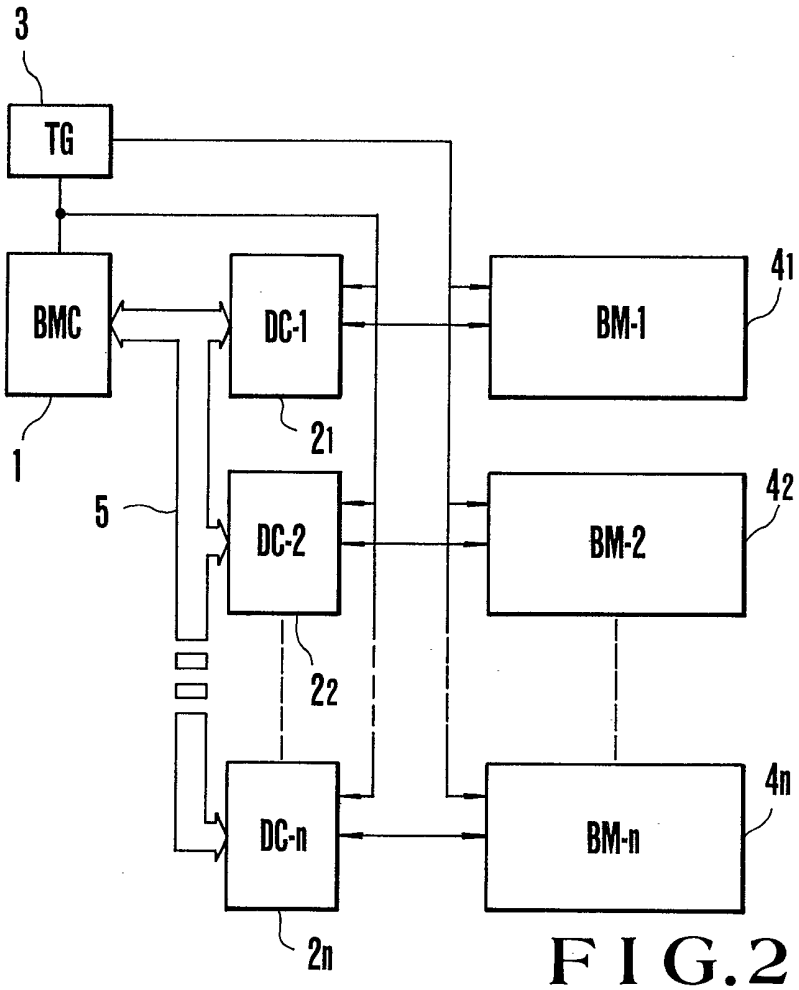

FIG.2
PRIOR ART

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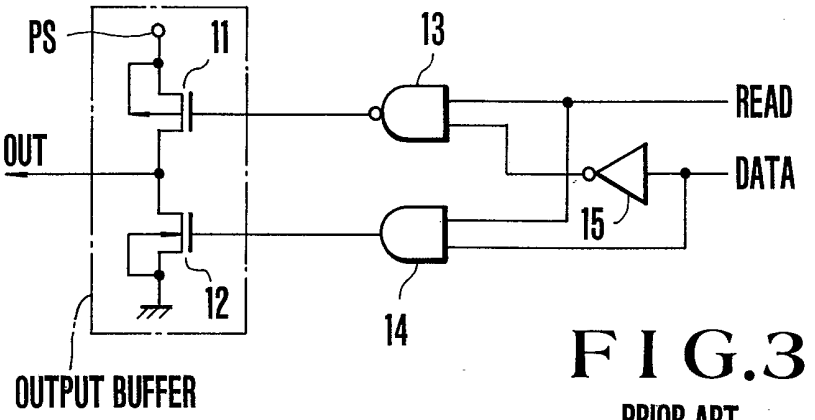

FIG.3
PRIOR ART

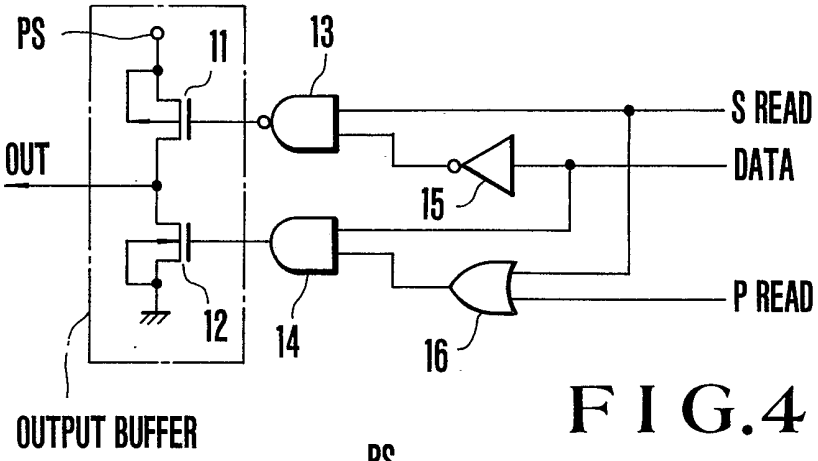

FIG.4

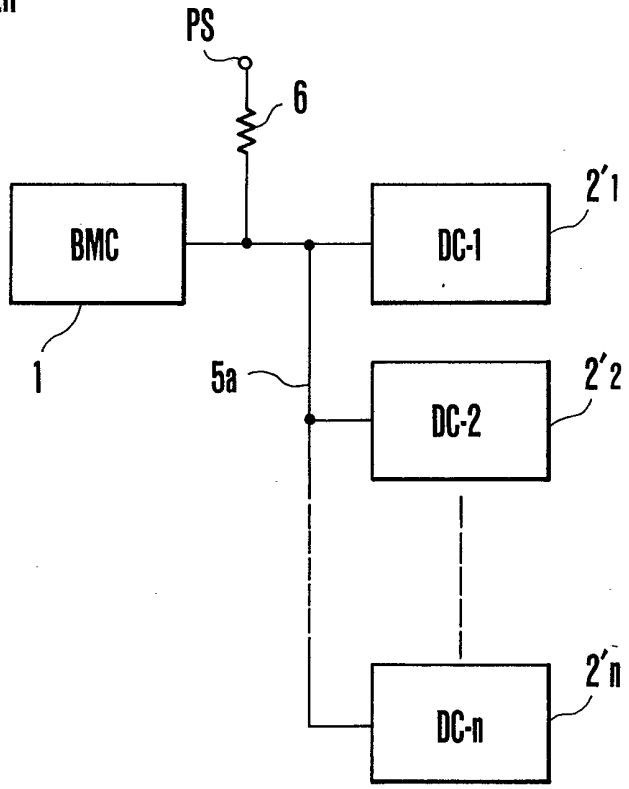

FIG.5

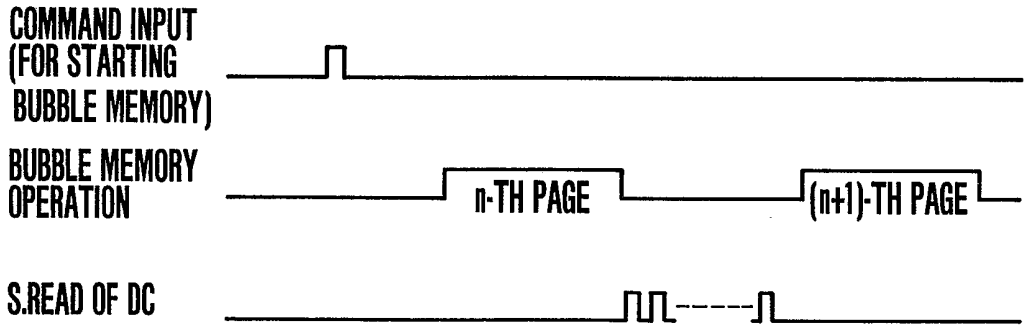

FIG.6
PRIOR ART

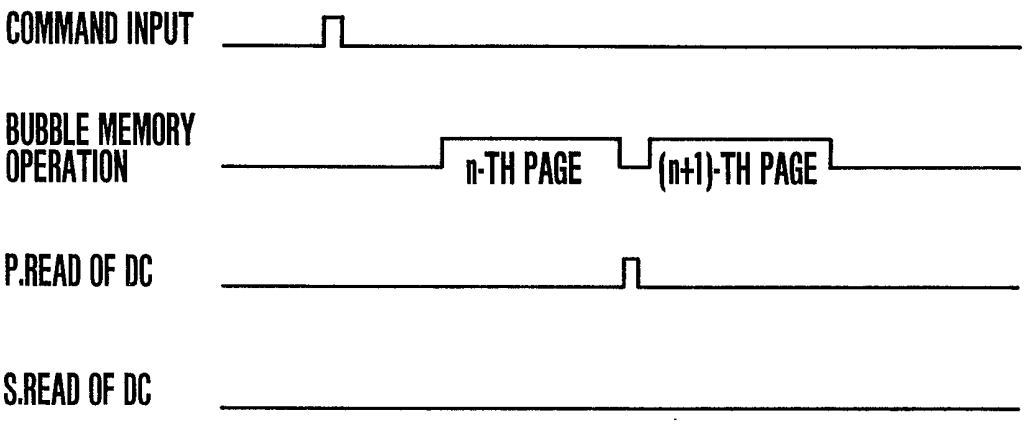

FIG.7

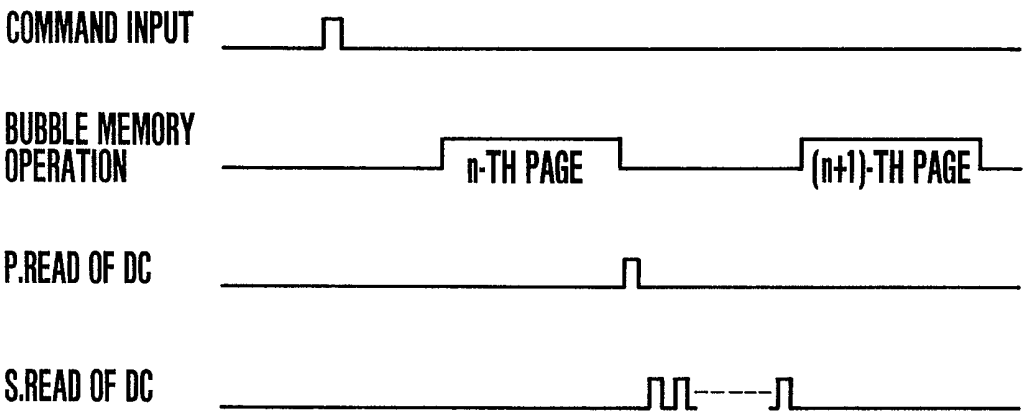

FIG.8

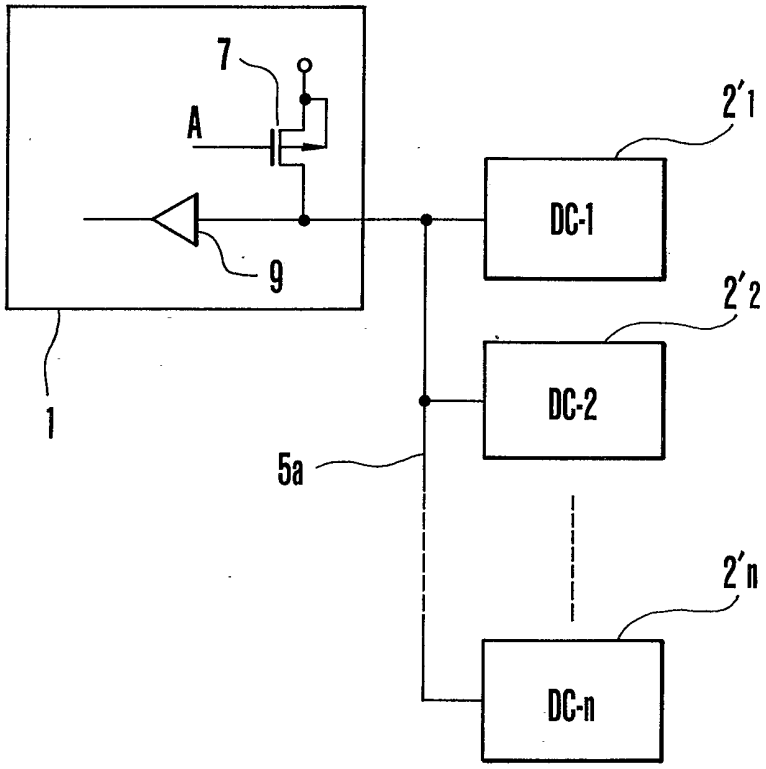

FIG.9

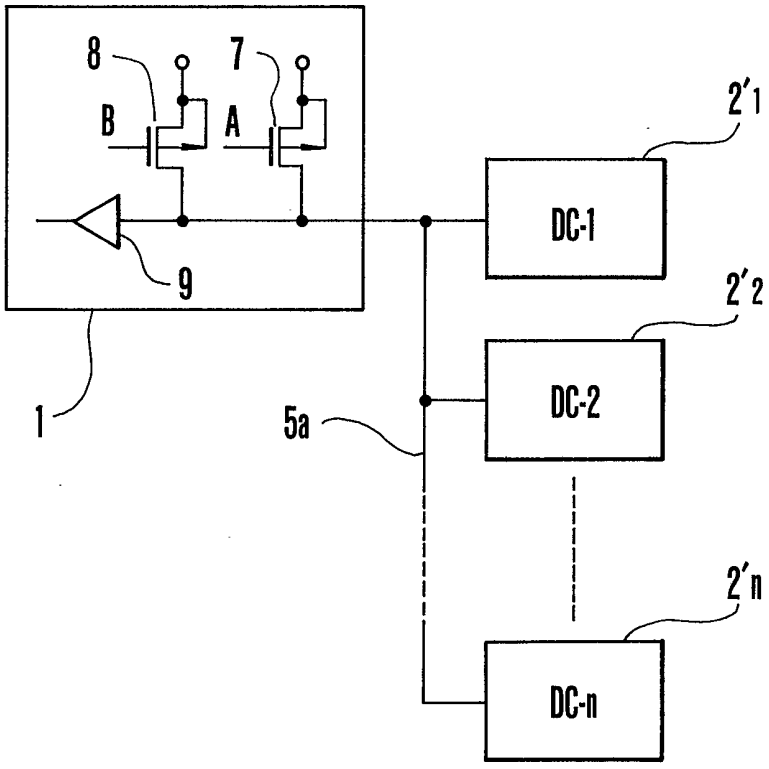

FIG.10

SPECIFICATION

Magnetic Bubble Memory Control Apparatus and Method for Control Thereof

This invention relates to a magnetic bubble memory control apparatus and to a method for the control of the magnetic bubble memory. More particularly, this invention relates to an output buffer suitable for reading out registers in a plurality of data controllers during the control of the plurality of data controllers by the use of a magnetic bubble memory controller and to a method for the control of the output buffer.

Generally, a magnetic bubble memory apparatus is comprised of a magnetic bubble memory device, a magnetic bubble memory including direct peripheral circuits for directly giving and receiving signals to and from the magnetic bubble memory device, and a magnetic bubble memory control circuit for controlling the direct peripheral circuits.

Fig. 1 is an essential block diagram illustrating a typical configuration of a magnetic bubble memory apparatus of this class. In Fig. 1 reference numeral 1 denotes a bubble memory controller (hereinafter simply referred to as "BMC"). The BMC 1 serves to give and receive data to and from a host computer, decode instructions from the host computer, and control a magnetic bubble memory. Denoted by reference numeral 2 is a data controller (hereinafter simply referred to as "DC"). This DC 2 has a buffer for the data to be transferred to the magnetic bubble memory and serves to control the data so transferred. Denoted by 3 is a timing generator (hereinafter simply referred to as "TG"). This TG 3 serves to generate timings required for the operation of the magnetic bubble memory. In this setup, the DC 2 and the TG 3 are controlled by the BMC 1. By 4 is denoted a magnetic bubble memory (hereinafter simply referred to as "BM") serving as a memory unit operated by the control signal received from the TG 3. The BM 4 contains in the interior thereof a magnetic bubble memory device and direct peripheral circuits such as a coil driver, a sense amplifier, and a function pulse driver. The transfer of data to the BM is carried out by the DC 2.

In the configuration described above, the BMC 1, on receiving an instruction from the host computer, issues relevant control signals to the TG 3 and the DC 2. In the meantime, the DC 2 receives from the host computer the data to be written in the BM 4, which data is temporarily stored in the data buffer and transferred to the BM 4 in accordance with the operation of the BM 4. During the read-out of data, the data of the BM 4 is transferred to the data buffer of the DC 2 and the host computer reads out the data of the data buffer. For each operation of the transfer of one page of data to the BM 4, namely, whenever one page of data is written into the BM 4 or one page of data is read out of the BM 4, the data of the BM 4 is checked by the check circuit in the DC 2 to detect the presence or absence of abnormality in the data. The outcome of this check is temporarily stored in the register within the DC 2. The BMC 1 examines one series of data for each operation to confirm absence of abnormality in the data and reads the register in the DC 2 for the purpose of enabling the host computer to sense the outcome of the confirmation. In the typical configuration illustrated in Fig. 1, just one DC 2 is connected to one BMC 1. Thus, the read-out of the register poses no serious problem.

When the magnetic bubble memory apparatus is designed in a large capacity, it becomes necessary to have a plurality of BM's 4 connected and operated all at once. In this case, since a plurality of pieces of magnetic bubble memory data cannot be simultaneously connected to the DC 2, it also becomes necessary to connect and control as many DC's 2 as the BM's 4 which are operated at the same time.

Fig. 2 is an essential block diagram illustrating a typical large-capacity magnetic bubble memory apparatus having a plurality of DC's connected therein. The apparatus of Fig. 2 has a configuration wherein n DC's 2_1—2_n are parallelly connected to permit simultaneous operation of n BM's 4_1—4_n.

In this configuration, the DC 2_1 controls the data of the BM 4_1, the DC 2_2 controls the data of the BM 4_2, and, by the same token, each of the subsequent DC's controls the data of each of the subsequent BM's in one to one correspondence. Then, the control of n DC's is effected by the BMC 1 in much the same way as in the configuration of Fig. 1. To confirm the absence of abnormality in data for each operation, therefore, the BMC 1 effects the read-out of all the registers in a total of n DC's 2_1 to 2_n. As a way of reading these registers through the BMC 1 in this case, there has been heretofore adopted a method of reading the registers in the DC's 2_1 to 2_n sequentially from the DC 2_1 through the DC 2_n. To be more specific, the data of the registers in the DC's 2_1 to 2_n have been read out by the use of data bus 5 connected to the individual DC's 2_1 to 2_n. The output buffers for the individual DC's 2_1 to 2_n have heretofore been designed in a tristate construction so that the output buffers of only the selected DC's are allowed to assume an active state and, depending on the contents of the relevant registers, set the state of the data bus to the "H" or "L" level. In this case, since the output buffers of the unselected DC's remain in an OFF state, the contents of the registers of the unselected DC's will never interfere with those of the data bus.

Fig. 3 is a circuit diagram illustrating a typical conventional configuration wherein a tristate buffer is formed by using CMOS's. In Fig. 3, an output OUT is connected to the drains of a PMOS transistor 11 and an NMOS transistor 12 and the sources of these transistors 11, 12 are connected respectively to a power source PS and the ground, thereby forming a tristate fundamental circuit generally adopted in the art. The gate of

the PMOS transistor 11 is connected to the output of a NAND gate 13 and the gate of the NMOS transistor 12 is connected to the output of an AND gate 14. The signal DATA fed from the register (not shown) within the aforementioned DC is connected to the AND gate 14 and to the NAND gate 13 via an inverter 15. The signal READ used to read out the register of the DC is connected to the inputs of the NAND gate 13 and the AND gate 14.

In the circuit configurated as described above, when the register within the DC is read out, the signal READ is generated only in the selected DC's and allowed to assume the state "H". The signal READ in the unselected DC's is in the state "L". Since the gate of the PMOS transistor 11 is in the state of "H" and the gate input of the NMOS transistor 12 in the state of "L" where the signal READ is in the state of "L", both the transistors 11, 12 are in the OFF state. As the signal READ is shifted to the state of "H", either of the PMOS transistor 11 and the NMOS transistor 12 assumes the ON state and the signal OUT assumes the state of "H" or "L", depending on the state of the signal DATA. To be specific, the NMOS transistor 12 assumes the ON state and the signal OUT the state of "L" where the signal DATA is in the state of "H". On the other hand, the PMOS transistor 11 assumes the ON state and the signal OUT the state of "H" where the signal DATA is in the state of "L".

When the contents of the registers in the DC's which possess an output buffer of such a tristate construction as illustrated in Fig. 3 are read out, it has been necessary for the BMC 1 to select the DC's one by one and effect the read-out sequentially in the order of DC 2_1, DC 2_2, ... DC 2_n as described above. This is because when the read-out is effected parallelly from the plurality of DC's, the outputs interfere with one another to jeopardize the accuracy of the operation of the apparatus. When the plurality of DC's are connected as described above, therefore, there ensues the disadvantage that the operation of the BM must be limited because the read-out of the contacts of the registers in the DC's requires much time.

This invention, initiated for the purpose of overcoming the aforementioned drawbacks suffered by the conventional apparatus, aims to improve the read-out operation of the registers in the data controllers in a magnetic bubble memory apparatus having a plurality of data controllers connected therein.

The conventional magnetic bubble memory control apparatus has suffered from the disadvantage in that since the read-out of the contents of the registers in the plurality of data controllers necessitates sequential selection of the plurality of data controllers one by one, the read-out operation consumes much time. To shorten the time required for the read-out, it becomes necessary to simultaneously read the registers of the plurality of data controllers. When the read-out is effected at once on all the data controllers where the output buffer is in a tristate construction, however, since the contents of data differ from one data controller to another, the signals OUT from some of the data controllers may be in the state of "H" and those from the other data controllers in the state of "L". Consequently, outputs of different levels are generated through the medium of the data bus and the overall level of the data bus becomes instable and the output transistors of some of the data controllers are short-circuited to the output transistors of the other data controllers. The present invention, therefore, is characterized by controlling the output buffer of the data controllers so that the output buffer will assume an open drain construction while the read-out is effected in a simultaneous manner.

Fig. 1 through Fig. 3 are essential block diagrams illustrating typical conventional magnetic bubble memory control apparatuses;

Figs. 4 and 5 are essential block diagrams illustrating a typical magnetic bubble memory control apparatus of the present invention;

Fig. 6 is a time chart for illustrating the operation of the conventional magnetic bubble memory control apparatus;

Figs. 7 and 8 are time charts for illustrating the operation of the magnetic bubble memory control apparatus in accordance with the present invention;

Fig. 9 is an essential block diagram illustrating another embodiment of the magnetic bubble memory control apparatus in accordance with this invention; and

Fig. 10 is an essential block diagram illustrating yet another embodiment of the magnetic bubble memory control apparatus of the present invention.

Fig. 4 is a circuit diagram illustrating the configuration of an output buffer for data controllers as involved in the magnetic bubble memory control apparatus in accordance with this invention. Parts like the parts of Fig. 3 are denoted by like symbols. In Fig. 4, a signal S READ and a signal P READ are used as signals for controlling the read-out of data. Here, the signal S READ means signal used for the purpose of selecting data controllers and effecting the read-out of the registers of the selected data controllers. The signals R READ of only the selected data controllers assume the state of "H". When some of the data controllers are selected for the read-out, the signals S READ of the unselected data controllers assume the state of "L". On the other hand, the signal P READ is a signal which assumes the state of "H" when the read-out is effected at once on the plurality of data controllers. The signals P READ of all the data controllers invariably assume the state of "H". The signals S READ constitute themselves input signals to the NAND gate 13, the signals S READ and the signals P READ constitute themselves inputs to an OR gate 16, and the outputs from the OR gate 16 from inputs to the AND gate 14. In the other respect, the operation

of the apparatus of Fig. 4 is similar to the operation of the apparatus of Fig. 3.

The circuit constructed as described above is operated as follows. During the parallel read-out of the data controllers, the signals P READ assume the state of "H" and, consequently, the NMOS transistor 12 assumes the state of ON or OFF, depending on the state of the signal DATA. When the signal DATA is in the state of "H", for example, the NMOS transistor 12 assumes the ON state. When the signal DATA is in the state of "L", the NMOS transistor 12 assumes the OFF state. In the case of the PMOS transistor 11, the signals S READ assume the state of "L" without reference to the level of the signals P READ. During the parallel read-out, the PMOS transistor 11 assumes the OFF state. At the time of parallel read-out, therefore, the signal OUT assumes the state of OFF and the NMOS transistor 12 the state of ON or vice versa, depending on the contents of the registers. This condition is equivalent to the condition in which only the NMOS transistor 12 is connected and, at the time of parallel read-out, this NMOS transistor 12 exclusively assumes the state of either ON or OFF, depending on the contents of data and no PMOS transistor 11 is present. In other words, the condition is equivalent to an open drain output of the NMOS transistor 12.

On the other hand, in the case of selective read-out of data controllers, since the control is effected by the signal S READ, the signal OUT is issued in a tristate form.

Fig. 5 is an essential circuit diagram illustrating the connection between a magnetic bubble memory controller (hereinafter simply referred to as "BMC") 1 and a plurality of data controllers (hereinafter simply referred to as "DC") 2′ each having the construction illustrated in Fig. 4 where the configuration involves connection of the plurality of data controllers $2'_1, 2'_2, \ldots 2'_n$. Parts like the parts of Fig. 2 are denoted by like symbols. The magnetic bubble memory (BM) and the timing generator (TG) which have no direct bearing upon the read-out of the registers within the DC's are omitted from the diagram. While the data bus 5 illustrated in Fig. 2 is composed of a plurality of signal lines, the diagram of Fig. 5 shows only one signal line for the convenience of illustration and is designated as a data bus 5a. Denoted by 6 is a resistor. This resistor 6 has one end thereof connected to the data bus 5a and the other end thereof to a power source PS. In this case, the NMOS transistor 12 is adapted so that the impedance generated while the transistor 12 is in the state ON will be amply smaller than the resistance of resistor 6. The signal level of the data bus 5a, therefore, shifts to "L" when any one of the NMOS transistors 12 for DC-1 through DC-n is caused to assume the ON state.

In the circuit configurated as illustrated in Fig. 5, while the BMC 1 is in the process of parallel read-out of the registers in the DC's $2'_1, 2'_2, \ldots 2'_n$, the outputs of the DC's $2'_1, 2'_2, \ldots 2'_n$ are in the state of OFF and the NMOS transistor 12 is in the state of ON. Where normality of the data series has been confirmed by the signal P READ and the outputs of all the DC's $2'_1, 2'_2 \ldots 2'_n$ are invariably in the state of OFF, the data bus 5a connected by the resistor 6 to the power source is shifted to the level of "H". The data bus 5a is shifted to the level "L" as described above, when any one of the NMOS transistors 12 happens to assume the state of ON.

When the contents of the registers are fixed so that, on occurrence of abnormality in the data series, the signal DATA illustrated in Fig. 4 will assume the level of "H", the data bus 5a at the time of parallel read-out assumes the level of "L" on sensing abnormality in the data series in any of the DC's $2'_1$ through $2'_n$. The data bus 5a, therefore, assumes the level of "H" only when it senses no abnormality in any of the DC's $2'_1$ through $2'_n$. By the arrangement described above, the BMC 1 is enabled to discern the occurrence of abnormality in the data series by a single read-out and, as the result, the time required for the read-out is shortened.

More particularly, in the conventional configuration, when the bubble memory has started to operate in response to the command input from the host computer as shown in Fig. 6, the plurality of DC's are subjected to sequential read-out (S. READ) one by one for each operation of the transfer of one page of data, or generally between the n-th page and the (n+1)-th page. Thus, much time elapses over the interval between the two pages. In accordance with the present invention, the time required over the interval between the n-th page and the (n+1)-th page is notably decreased because the detection of abnormality in the data series is effected by a single parallel read-out (P READ) of the DC's as illustrated in Fig. 7 and, in the absence of abnormality, the sequential read-out (S READ) is omitted. Since abnormality occurs very rarely, the absence of abnormality is confirmed by a single parallel read-out (P READ) in virtually all cases.

Only when there occurs abnormality, it becomes necessary to pinpoint the particular DC that is causing the abnormality. This detection is accomplished by simply selecting DC's by the parallel read-out P READ to set the relevant registers ready for the read-out, and subsequently sequentially selecting and reading out the DC's by S READ similarly to the conventional apparatus. In this case, the data can be read out as tristate outputs similarly to the conventional apparatus.

When the apparatus is designed from the beginning in an open drain construction, selective read-out of the DC's can be obtained. When the read-out is carried out in the open drain construction, however, flow of electric current from the resistor 6 shown in Fig. 5 to the DC's whose outputs happen to be on the level of "L" if the outputs are on the level of "L". In the foregoing embodiment of this invention, a circuit has been explained using CMOS transistors. Since the CMOS transistors are characterized by their ability to operate with low power consumption, it

is important to avoid using them in a manner that is liable to entail addition to the power consumption. In the read-out of the contents of the registers in the DC's, therefore, unless parallel read-out is effected as when the time required for read-out is desired to be shortened, namely when selective read-out is effected on the DC's, it is desirable to feed out the data in tristate and disconnect the resistor 6 from the bus line 5a during the course of read-out.

Fig. 9 is an essential circuit diagram illustrating another embodiment of this invention. In the circuit of this diagram, in place of the resistor 6 of Fig. 5 serving to pull up the bus line 5a to a higher potential, a PMOS transistor 7 is used within the BMC 1. Denoted by 9 is a BMC input circuit including an input buffer. The gate signal A which is connected to the gate of this PMOS transistor 7 assumes the level of "L" only during the parallel read-out of the DC's. Otherwise, this signal assumes the level of "H". The PMOS transistor 7, therefore, assumes the state of ON during the parallel read-out of the DC's and provided the same operation and effect similarly to the resistor 6 described above. In contrast, in the case of the operation of selective read-out of the DC's, the PMOS transistor 7 assumes the state of OFF and the level of the data bus 5a is determined by the output of the selected DC and the increase in power consumption due to the resistor 6 can be avoided.

Fig. 10 is an essential circuit diagram illustrating a further embodiment of the present invention. In the circuit of this diagram, a second PMOS transistor 8 is connected in parallel to the first PMOS transistor 7 within the BMC 1. This second PMOS transistor 8 is characterized by having amply lower impedance while it is in the state of ON than the first PMOS transistor 7. In the apparatus of Fig. 6, during the parallel read-out of the DC's, the level of the data bus 5a must be shifted by the PMOS transitor 7 from "L" to "H" if all the outputs are in the state OFF. A magnitude of about 200 PF must be considered for the stray capacity connected to the data bus 5a, although this stray capacity is widely variable with the number of DC's connected. The time required for the BMC 1 to effect the read-out of the DC's $2'_1$ through $2'_n$ is of the order of about 500 ns. For the level of the data bus 5a to be shifted by the PMOS transistors 7, 8 from "L" to "H" within about 500 ns, therefore, the PMOS transistor 7 requires about 1 K of impedance while it is in the state of ON. On the other hand, the impedance which the NMOS transistor used in the output buffer for the DC's $2'_1$ through $2'_n$ has while it is in the state of ON must be amply smaller than the impedance of the PMOS transistor 7 while it is in the state of ON. Thus, the impedance of the NMOS transistor is required to fall in the range of 10 to 100. To provide such low impedance, the NMOS transistor inevitably acquires a large size and proves impracticable. The second PMOS transistor 8 is incorporated for the purpose of solving the drawback mentioned above. Only during one half of the time required for the parallel read-out, the gate signal B of the second PMOS transistor 8 is kept on the level "L" and in the state of ON and the level of the data bus 5a is kept pulled up to "H". On elapse of the half of the time mentioned above, the level of the gate signal B is returned to "H", that of the gate signal A is shifted to "L", the second PMOS transistor 8 is set to the ON state, and the first PMOS transistor 7 is set to the ON state. Since the impedance of the second PMOS transistor 8 while the transistor is in the state of ON is fixed at an amply small magnitude, the shift of the data bus 5a from "L" to "H" completes rapidly. After the shift of the level to "H" is completed, the first PMOS transistor is relied on to keep the "H" level. Thus, no problem ensues when the impedance of the first PMOS transistor 7 during the ON state is fixed at such a large magnitude of about 100 K. In the embodiment of Fig. 7, the size of the NMOS transistor used to determine the level "L" during the parallel read-out of the DC's $2'_1$ through $2'_n$ in the open drain construction has only to be considered with respect to the first PMOS transistor 7 and the impedance during the ON state is permitted to be fixed in the range of 1 to 10 K. Thus, the size of the NMOS transistor can be reduced to a practicable level.

The foregoing embodiments of this invention has been described as incorporating the data buffer for data controllers in an open drain construction. The use of the data buffer in the open drain construction is not an exclusive requirement for this invention. Naturally, this invention brings about entirely the same effect as described above even when an open collector is used instead.

As described above, this invention enables the contents of the registers in the plurality of data controllers to be parallelly read out when necessary. Thus, it brings about an oustanding effect of enabling magnetic bubble memories to be operated at high speed and, for the purpose of selective operation of data controllers, permitting use of tristate outputs, and notably lowering the power consumption for the control circuit.

CLAIMS

1. A magnetic bubble memory control apparatus comprising a magnetic bubble memory controller for controlling the operating sequence of a plurality of magnetic bubble memories, a plurality of data controllers for controlling the flow of data from said memories, and read-out control means for effecting read-out of registers within said data controllers by said magnetic bubble memory controller, said read-out control means being operable to cause an output buffer associated with each of said plurality of data controllers to be operated in an open drain mode when parallel read-out is effected from said registers and to cause said output buffer associated with a particular said data controller to be operated in a tristate mode when selective

read-out is effected from the register of said particular data controller.

2. A magnetic bubble memory control apparatus according to claim 1, wherein a first transistor for retaining the level of a data bus serving to connect said magnetic bubble memory controller to said data controllers is disposed within said magnetic bubble memory controller and said first transistor is set to the ON state during parallel read-out of said registers within said data controllers.

3. A magnetic bubble memory control apparatus according to claim 2, wherein a second transistor having a lower impedance during the ON state than said first transistor is disposed in parallel with said first transistor within said magnetic bubble memory controller and said second transistor is kept in the ON state during the first half of the cycle of parallel read-out of the registers within said data controllers.

4. A method for the control of magnetic bubble memories in a magnetic bubble memory control apparatus comprising a magnetic bubble memory controller for controlling the operating sequence of magnetic bubble memories, and data controllers for controlling the flow of data from said memories, said method comprising a first step of causing, during P READ for each operation of said magnetic bubble memories, an output buffer associated with each of said plurality of data controllers connected to a common bus line to be operated in an open drain mode to check said plurality of data controllers for abnormality; and a second step of causing, on detection of abnormality, said output buffer to be shifted from said open drain mode to a tristate mode and sequentially checking said data controllers for state; and a third step of omitting said second step on confirmation of the absence of abnormality and bringing said one operation to completion.

5. A magnetic bubble memory control apparatus substantially as described herein with reference to Figs. 4, 5 and 7 to 10 of the accompanying drawings.

6. A method according to claim 4 and substantially as described herein with reference to Figs. 4, 5 and 7 to 10 of the accompanying drawings.

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