

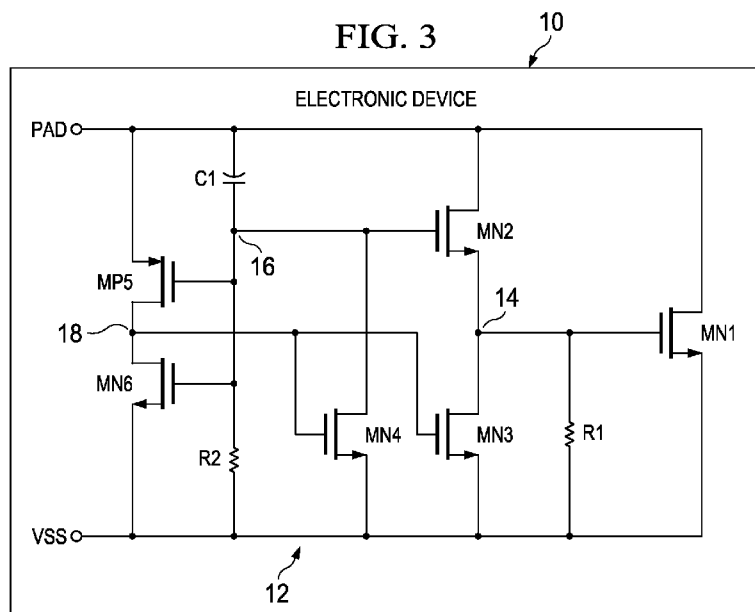


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[Continued on next page]

(54) **Title:** ELECTRONIC DEVICE AND METHOD FOR PROTECTING AGAINST DAMAGE BY ELECTROSTATIC DISCHARGE

FIG. 3



(57) **Abstract:** An electronic device with a protective circuit against damage by electrostatic discharge includes a discharge current path (channel MN1) connectable between an input (PAD) to be protected and a ground pin (VSS). An enabling circuit (C1, R2) outputs a control signal (16) for connecting the discharge current path in the event of an electrostatic discharge. A deactivating circuit (MN3, MP5, MN6) which deactivates the enabling circuit during operation of the electronic device is controlled by the inverted control signal. A method of protecting an electronic device against damage by electrostatic discharge includes providing a control signal for connecting a discharge current path between an input to be protected and a ground pin in the event of an electrostatic discharge. An inverted control signal is applied to the inverted control signal to a deactivating circuit. The inverted control signal prevents connection of the discharge current path between the input to be protected and ground during operation of the electronic device.

**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

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ELECTRONIC DEVICE AND METHOD FOR PROTECTING AGAINST DAMAGE BY ELECTROSTATIC DISCHARGE

[0001] This relates to an electronic device comprising a protective circuit against damage by electrostatic discharge and to a method of protecting an electronic device against damage by electrostatic discharge.

BACKGROUND

[0002] Many electronic circuits may be severely damaged by electrostatic discharge (ESD). An electrostatic discharge on an input pin of an electronic component, especially a CMOS component, may lead to a current in the chip which is much higher than the currents for which the circuit is designed. The high current locally overheats the component and destroys parts of the chip structures.

[0003] A first prior art solution is shown in FIG.1. A pin PAD is to be protected against an electrostatic discharge by a protective circuit. The protective circuit comprises a transistor MN1 the transistor channel of which is connected between the pin PAD and a pin VSS. Transistor MN1 is designed to support electrostatic discharge currents through its channel.

[0004] Pin PAD may be a pad to which a supply voltage is applied when the circuit which is protected by the protective circuit works normally. VSS may be a pin which is connected to ground.

[0005] A resistor R1 is connected between the gate of transistor MN1 and pin VSS. A transistor MN2 is connected with one side of the transistor channel to pin PAD and with the other side of the channel to the gate of transistor MN1. A transistor MN3 is connected with one side of the transistor channel to the gate of transistor MN1, and with the other side of the transistor channel to the pin VSS. Transistors MN2 and MN3 are connected in series between the pins PAD and

VSS. An interconnection node between transistors MN2 and MN3 is connected to the gate of transistor MN1.

[0006] A series connection between a capacitor C1 and a resistor R2 is connected between pin PAD and pin VSS. One side of capacitor C1 is connected to pin PAD and the other side of capacitor C1 is connected to the gate of transistor MN2 and to one side of resistor R2. The other side of resistor R2 is connected to pin VSS.

[0007] A transistor MN4 is connected with one side of the transistor channel to the interconnection node between capacitor C1 and resistor R2 and with the other side to pin VSS. A pin V_OFF is connected to the gate of transistor MN3 and to the gate of transistor MN4.

[0008] When the component or chip comprising the prior art protective circuit according to FIG.1 is handled before being mounted to a circuit board no supply voltages are applied to the pins PAD and V_OFF (V_OFF should be pulled to ground level).

[0009] In the event of an electrostatic discharge on pin PAD there is a sudden voltage rise on PAD. An electrostatic discharge pulse lasts generally only about 1 microsecond. The prior art protective circuit functions as a dV/dt -trigger or transient clamp. Through capacitor C1 a voltage VRC on the gate of transistor MN2 rises also very fast. The rise time of the voltage VRC can be controlled by the RC time constant $\tau_1 = C1 * R2$.

[0010] Voltage VRC on the gate of transistor MN2 causes it to conduct and the voltage at pin PAD leads to a voltage VG on the gate of transistor MN1. Transistor MN1 conducts and a discharge current can flow from pin PAD to pin VSS through the transistor channel of transistor MN1 without destroying the protected circuit.

[0011] Transistor MN2 functions as an auxiliary transistor to main transistor MN1 ensuring that enough current is provided to turn on transistor MN1 very fast. Once the protected circuit which is not shown in FIG.1 is inserted including the protective circuit into an electronic device, for example mounted on a circuit board, and used normally, the protective circuit risks to disturb the normal

function of the electronic device. During normal function of the protected circuit transistor MN1 must not conduct. Or in other words, it is not desired that a short circuit via transistor MN1 occurs, once the voltage supply connected between pin PAD and pin VSS.

[0012] In the first prior art solution as shown in FIG.1 an additional pin V_OFF is provided to which during normal operation of the protected circuit an external control voltage V_OFF is applied. The voltage applied to pin V_OFF is applied directly to the gates of transistors MN3 and MN4 so that the channels of transistors MN3 and MN4 are conducting. With transistors MN3 and MN4 conducting, the gate voltage VRC of transistor MN2 and the gate voltage VG of transistor MN1 can not rise sufficiently anymore to switch transistors MN1 and MN2 and the protective circuit is disabled.

[0013] A disadvantage of the first prior art solution, which is widely used, is that an additional control voltage V_OFF is needed. Usually, the additional control voltage is provided by a further voltage supply. The top level routing of the entire integrated circuit comprising the protective circuit becomes more difficult as additional voltage lines are needed.

[0014] A further disadvantage is that the two supply voltages, the supply voltage between PAD and VSS and the supply voltage for V_OFF, may power up with different time constants. If the voltage V_OFF powers up later or slower than the voltage across PAD and VSS, a high current flows through MN1 during this delay time. This could damage the circuit or even the whole chip.

[0015] A second prior art solution is shown in FIG.2. In the schematic diagram in FIG.2 those components are provided with the same reference signs which are already included in the schematic diagram of the first prior art solution in FIG.1. The circuit according to the second prior art solution is only explained insofar as it differs from the first prior art solution.

[0016] The circuit according to FIG.2 also comprises transistors MN1, MN2, MN3 and MN4 which are interconnected and connected to a pin PAD and a pin VSS as the corresponding transistors in FIG.1. Furthermore, a capacitor C1 and resistors R1 and R2 are also interconnected in the same way.

[0017] The second prior art solution avoids the use of a separate voltage V_{OFF} . Instead, a series connection of a resistor R3 and a capacitor C2 is connected between pin PAD and pin VSS. One side of capacitor C2 is connected to pin VSS and the other side of capacitor C2 is connected to the gates of transistors MN3 and MN4 and to one side of resistor R3. The other side of resistor R3 is connected to pin PAD.

[0018] Resistor R3 and capacitor C2 form together a low pass filter with an RC time constant $\tau_2 = R3 * C2$. In the event of an electrostatic discharge the time constant τ_2 and the low pass filter characteristic in general prevent building up of a gate voltage on the gates of transistors MN3 and MN4. Transistors MN3 and MN4 remain non-conducting and a gate voltage VRC switches transistor MN2. With the transistor channel of transistor MN2 conducting a gate voltage on the gate of transistor MN1 switches transistor MN1 and the electrostatic discharge current flows through the transistor channel of transistor MN1 between PAD and VSS as in the first prior art solution.

[0019] Once the protected circuit is inserted to an electronic device, for example mounted on a circuit board, and used normally, the low pass filter formed by resistor R3 and capacitor C2 will lead during the much slower power up process to a gate voltage on transistors MN3 and MN4 so that the transistors MN3 and MN4 are conducting and no gate voltages build up on the gates of transistors MN1 and MN2. Once the voltage on PAD is the constant supply voltage of the electronic device or the electronic circuit to be protected, the gate voltage on transistors MN3 and MN4 will remain constant and transistors MN3 and MN4 are conducting.

[0020] The time constant τ_2 must be greater than the time constant τ_1 which triggers the circuit in case of an electrostatic discharge pulse. If the time constant τ_2 is too low, a gate voltage will build up on the gates of transistors MN3 and MN4 which is sufficient to switch these transistors before a gate voltage on gates of transistors MN1 and MN2 is sufficient to make the channels of these two transistors conductive. In this case the protective circuit does not work in the event of an electrostatic discharge and the circuit to be protected could be

damaged. If the time constants τ_1 and τ_2 are chosen too close together, it is possible that the ESD protection is switched off too early. Therefore, the selection of the time constants is critical and may lead to failure of the circuit.

[0021] A further disadvantage of the second prior art solution is the additional silicon area needed for resistor R3 and capacitor C2. Capacitors and resistors are space-consuming components which are much larger than transistors. In an embodiment, the silicon area required may be around 2,600 μm^2 .

SUMMARY

[0022] It is a general object of the invention to provide a protective circuit protecting against damage by electrostatic discharge which may be deactivated during normal operation of the protected circuit without the need to provide an additional voltage supply and requiring less silicon area.

[0023] In one aspect of the invention an electronic device (for example an integrated semiconductor circuit) is provided comprising a protective circuit against damage by electrostatic discharge. The protective circuit may include a discharge current path which is configured to be coupled between an input to be protected and a ground pin. There may be an enabling circuit configured to output a control signal for enabling the discharge current path in the event of an electrostatic discharge. A deactivating circuit can be configured to deactivate the enabling circuit during operation of the electronic device. The deactivating circuit may be controlled by the inverted control signal.

[0024] The control signal which is used to connect the discharge current path or in other words to enable the discharge current path in the event of an electrostatic discharge is used in inverted form for deactivating the protective circuit during normal operation of the electronic device.

[0025] In an embodiment of the invention, the discharge current path may comprise a first transistor. The control signal may be applied to the control gate of the first transistor. It is known in the art to design a transistor to support a maximal current.

[0026] In a further embodiment, the enabling circuit may comprise a high pass filter which is coupled between the input to be protected and ground. The control signal may then depend on the output signal of the high pass filter.

[0027] A high pass filter may be designed to have a time constant adapted to the time response of an ESD event. Using a high pass filter provides a dV/dt -trigger responding to fast voltage rises as they occur during ESD events. As the control signal depends on the output signal of the high pass filter, only voltage signals having a short rise time will result in a control signal. The much slower power up provides a voltage rise which does not cause a control signal.

[0028] In an embodiment, the high pass filter may comprise a series connection of a resistor and a capacitor. Such a high pass filter only needs very few components.

[0029] In an embodiment, the deactivating circuit comprises a second transistor and an inverter. The inverter may be coupled to receive the control signal at an inverter input. The inverter is further coupled to output the inverted control signal to a control gate of the second transistor. The inverter is adapted to provide the inverted control signal needed to control the deactivating circuit.

[0030] In a further embodiment, the inverter comprises a third and a fourth transistor. The channels of the third and fourth transistors may be connected in series between the input to be protected and the ground pin. The gates of the third and the fourth transistor may then form the inverter input. This means that only two transistors are needed to provide the inverted control signal. The inverted control signal may be used to deactivate the enabling circuit. The silicon area needed for a transistor is much smaller than the silicon area required for a capacitor or for a resistor.

[0031] In an embodiment, the channel of the second transistor may be coupled between an output of the enabling circuit and the ground pin. A control signal output from the enabling circuit may then be led directly to ground via the channel of the second transistor. In this case the control signal cannot activate the discharge current path.

[0032] In a further aspect of the invention, a method of protecting an electronic device against damage by electrostatic discharge is provided. The method may comprise the following steps: providing a control signal for connecting a discharge current path between an input to be protected and a ground pin in the event of an electrostatic discharge. This means that the discharge current path is only connected between input and ground pin in an ESD event. Whether the discharge current path is connected or not is controlled by the control signal.

[0033] A further step is providing an inverted control signal. The inverted control signal may be applied to a deactivating circuit. The inverted control signal may be configured to prevent connection of the discharge current path between the input to be protected and the ground pin during operation of the electronic device.

BRIEF DESCRIPTION OF DRAWINGS

[0034] FIG. 1 shows a schematic circuit diagram of a protective circuit according to a first solution in the prior art;

[0035] FIG. 2 shows a schematic circuit diagram according to a second prior art solution; and

[0036] FIG. 3 shows a representative schematic of an electronic device according to the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0037] FIG. 3 shows a representative schematic of an electronic device according to the invention. In the embodiment shown an electronic device 10 comprises a protective circuit 12.

[0038] In the embodiment shown components which are already used in the prior art solutions have the same reference signs.

[0039] The protective circuit 12 comprises a transistor MN1 which may be an NMOS transistor. Transistor MN1 is connected with its channel between an input pin PAD which is to be protected against an ESD event and a ground pin designated by VSS. Transistor MN1 provides as first transistor a discharge current path according to the invention. The channel or discharge current path is

conducting respectively enabled or not conducting respectively disabled between the input PAD and the ground pin in accordance with a voltage applied to the gate of transistor MN1. The gate of transistor MN1 is connected via a resistor R1 to pin VSS.

[0040] A series connection of the channels of a transistor MN2 and transistor MN3 is connected between the input PAD and the pin VSS. Transistors MN2 and MN3 may be NMOS transistors. An interconnection node 14 between transistors MN2 and MN3 is connected to the gate of transistor MN1. Transistor MN3 can be a second transistor in the wording of the claims.

[0041] A series connection between a capacitor C1 and a resistor R2 is connected between pin PAD and pin VSS. Capacitor C1 is connected with one side to pin PAD and with the other side to resistor R2. Resistor R2 is connected with the other side to pin VSS. An interconnection node 16 between capacitor C1 and resistor R2 is connected to the gate of transistor MN2.

[0042] A transistor MN4 which may be an NMOS transistor is connected with its channel between the interconnection node 16 and pin VSS.

[0043] A series connection between a transistor MP5 which may be a PMOS transistor and a transistor MN6 which may be an NMOS transistor is connected between pin PAD and pin VSS. The source of transistor MP5 is connected to pin PAD and the drain of transistor MP5 is connected to the drain of transistor MN6. Transistor MN6 is connected with its source to pin VSS. An interconnection node 18 between transistor MP5 and transistor MN6 is connected to the gate of transistor MN4 and to the gate of transistor MN3. The gate of transistor MP5 and the gate of transistor MN6 are connected to interconnection node 16 between capacitor C1 and resistor R2. Transistors MP5 and MN6 form, as a third and fourth transistor together, an inverter. The gates of transistors MP5 and MN6 form an input of the inverter and interconnection node 18 forms an output of the inverter.

[0044] In operation, a discharge current path is provided by the channel of transistor MN1 between pin PAD to be protected against an electrostatic discharge and pin VSS when the voltage applied to the gate of transistor MN1 is

such that the transistor channel is conductive. In other words, the gate voltage of transistor MN1 enables or disables the discharge current path.

[0045] An enabling circuit is formed by a high pass filter formed by capacitor C1 and resistor R2. At their interconnection node 16 an enabling signal or control signal for connecting the discharge current path is provided.

[0046] A deactivating circuit is formed by second transistor MN3 and the inverter comprising transistors MP5 and MN6. In the embodiment shown, the deactivating circuit further comprises transistor MN4. If transistor MN3 is conductive, the gate voltage of MN1 drops to VSS. If MN4 is conductive, the gate voltage of transistor MN2 drops to VSS. In other words MN3 and MN4 can deactivate transistors MN1 and MN2.

[0047] Transistors MN3 and MN4 become conductive by applying an adequate gate signal. The gate signal is provided on interconnection node 18 between transistors MP5 and MN6, in other words at the output of the inverter formed by transistors MP5 and MN6. The signal on interconnection node 18 is the inverted control signal of interconnection node 16.

[0048] The inverted control signal is applied to the gates of transistors MN3 and MN4. When transistors MN3 and MN4 are conducting they deactivate enabling of the discharge current path.

[0049] In the event of an electrostatic discharge, the voltage on pin PAD rises very fast. Capacitor C1 is in the beginning not charged so that the voltage on the gate of transistor MN2 rises also very fast and the channel of transistor MN2 turns on quickly. A current flows from pin PAD through the channel of transistor MN2 and via interconnection node 14 through resistor R1 to VSS. This means that the gate voltage of transistor MN1 rises very fast and the discharge current path through transistor MN1 is enabled.

[0050] It is to be understood that transistor MN2 is an auxiliary transistor which is not essential for the invention and transistor MN4 is only needed to deactivate the auxiliary transistor MN2. The use of MN2 allows reducing the capacitance of capacitor C1 while still providing sufficiently high current in order

to switch transistor MN1 quickly. The discharge current can pass securely transistor MN1 without damaging the electronic device.

[0051] Once the protective circuit is mounted on a circuit board or integrated into an electronic device and a normal power up of a supply voltage on pin PAD occurs, the voltage rises much slower than in an ESD event. Due to the high pass filter characteristic of C1 and R2, the power rises only slowly at interconnection node 16. Interconnection node 16 is connected to the gates of transistors MP5 and MN6 which form an inverter input. While the voltage at interconnection node 16 is low transistor MP5 is conductive and transistor MN6 is non-conductive. As transistor MP5 is conductive, the voltage at interconnection node 18 becomes essentially the same voltage than the voltage on pin PAD. Interconnection node 18 forms the inverter output. The signal at interconnection node 18 is the inverted signal of the signal at interconnection node 16, i.e. when the voltage at interconnection node 16 is low, the voltage at interconnection node 18 is high.

[0052] The voltage at interconnection node 18 is applied to the gates of transistors MN3 and MN4. Transistors MN3 and MN4 become conductive and the voltage at interconnection node 16 between capacitor C1 and resistor R2 drops. This means that the enabling circuit formed by capacitor C1 and resistor R2 is deactivated because there may be no control signal enabling the discharge current path.

[0053] This means when there is a slow voltage rise on PAD or a constant voltage on PAD transistors MN3 and MN4 are conductive and transistors MN1 and MN2 cannot become conductive.

[0054] The voltage at interconnection node 16 respectively on the gate of transistor MN2 falls with the $R2 \cdot C1$ time constant.

[0055] During normal operation of the electronic device, the voltage on pin PAD is generally constant and capacitor C1 blocks current flow. Transistors MN3 and MN4 remain conductive and the electrostatic discharge current path remains disabled.

[0056] It is important to realize that no additional RC time constant is needed with the inventive circuit and no further voltage supply is required.

[0057] For the realization of an inverter comprising a PMOS transistor MP5 and an NMOS transistor MN6 as described with reference to the embodiment shown in FIG.3, only a silicon space or a silicon area of 440 μm^2 is needed to support the self-deactivation. Compared to the 2,300 μm^2 needed for an additional RC circuit this means an area reduction of over 80 % in this embodiment.

[0058] Those skilled in the art to which this relates will appreciate that modifications may be made to the described example embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

1. An electronic device comprising:
a protective circuit against damage by electrostatic discharge, the protective circuit including:
a discharge current path configured to be connectable between an input to be protected and a ground pin;
an enabling circuit configured to output a control signal for enabling the discharge current path in the event of an electrostatic discharge;
a deactivating circuit configured to deactivate the enabling circuit during operation of the electronic device;
wherein the deactivating circuit is controlled by an inverted control signal.
2. The electronic device according to claim 1, wherein the discharge current path comprises a first transistor and wherein the control signal acts upon the control gate of the first transistor.
3. The electronic device according to claim 1, wherein the enabling circuit comprises a high-pass filter coupled between the input to be protected and ground and wherein the control signal is the output signal of the high-pass filter.
4. The electronic device according to claim 2, wherein the enabling circuit comprises a high-pass filter coupled between the input to be protected and ground and wherein the control signal is the output signal of the high-pass filter.
5. The electronic device according to claim 3, wherein the high-pass filter comprises a series connection of a resistor and a capacitor and wherein an interconnection node between the resistor and the capacitor is coupled to the control gate of the first transistor.

6. The electronic device according to claim 4, wherein the high-pass filter comprises a series connection of a resistor and a capacitor and wherein an interconnection node between the resistor and the capacitor is coupled to the control gate of the first transistor.

7. The electronic device according to claim 1, wherein the deactivating circuit comprises a second transistor and an inverter, the inverter being coupled to receive the control signal at an inverter input and to output the inverted control signal to a control gate of the second transistor.

8. The electronic device according to claim 2, wherein the deactivating circuit comprises a second transistor and an inverter, the inverter being coupled to receive the control signal at an inverter input and to output the inverted control signal to a control gate of the second transistor.

9. The electronic device according to claim 3, wherein the deactivating circuit comprises a second transistor and an inverter, the inverter being coupled to receive the control signal at an inverter input and to output the inverted control signal to a control gate of the second transistor.

10. The electronic device according to claim 4, wherein the deactivating circuit comprises a second transistor and an inverter, the inverter being coupled to receive the control signal at an inverter input and to output the inverted control signal to a control gate of the second transistor.

11. The electronic device according to claim 5, wherein the deactivating circuit comprises a second transistor and an inverter, the inverter being coupled to receive the control signal at an inverter input and to output the inverted control signal to a control gate of the second transistor.

12. The electronic device according to claim 6, wherein the deactivating circuit comprises a second transistor and an inverter, the inverter being coupled to receive the control signal at an inverter input and to output the inverted control signal to a control gate of the second transistor.

13. The electronic device according to claim 7, wherein the inverter comprises a third and a fourth transistor, the channel of the third transistor and the channel of the fourth transistor being connected in series between the input to be protected and the ground pin and the gates of the third and the fourth transistor forming the inverter input.

14. The electronic device according to claim 8, wherein the inverter comprises a third and a fourth transistor, the channel of the third transistor and the channel of the fourth transistor being connected in series between the input to be protected and the ground pin and the gates of the third and the fourth transistor forming the inverter input.

15. The electronic device according to claim 9, wherein the inverter comprises a third and a fourth transistor, the channel of the third transistor and the channel of the fourth transistor being connected in series between the input to be protected and the ground pin and the gates of the third and the fourth transistor forming the inverter input.

16. The electronic device according to claim 10, wherein the inverter comprises a third and a fourth transistor, the channel of the third transistor and the channel of the fourth transistor being connected in series between the input to be protected and the ground pin and the gates of the third and the fourth transistor forming the inverter input.

17. The electronic device according to claim 11, wherein the inverter comprises a third and a fourth transistor, the channel of the third transistor and the channel of the fourth transistor being connected in series between the input to be protected

and the ground pin and the gates of the third and the fourth transistor forming the inverter input.

18. The electronic device according to claim 12, wherein the inverter comprises a third and a fourth transistor, the channel of the third transistor and the channel of the fourth transistor being connected in series between the input to be protected and the ground pin and the gates of the third and the fourth transistor forming the inverter input.

19. The electronic device according to claim 7, wherein a channel of the second transistor is coupled between an output of the enabling circuit and the ground pin.

20. A method of protecting an electronic device against damage by electrostatic discharge, the method comprising:

providing a control signal for connecting a discharge current path between an input to be protected and a ground pin in the event of an electrostatic discharge;

providing an inverted control signal;

applying the inverted control signal to a deactivating circuit;

wherein the inverted control signal is configured to prevent connection of the discharge current path between the input to be protected and ground during operation of the electronic device.

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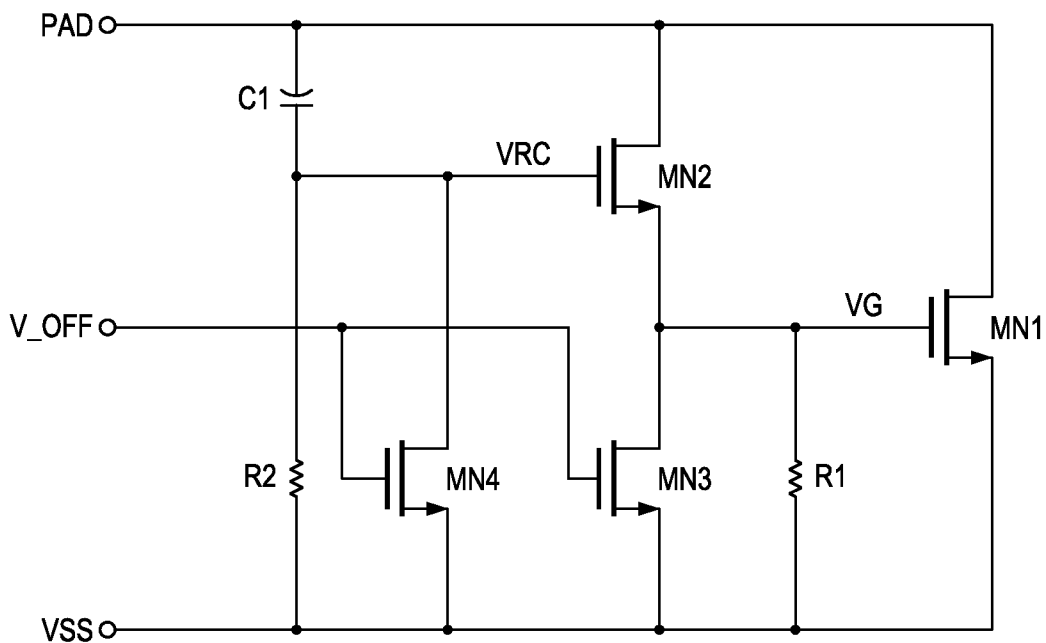
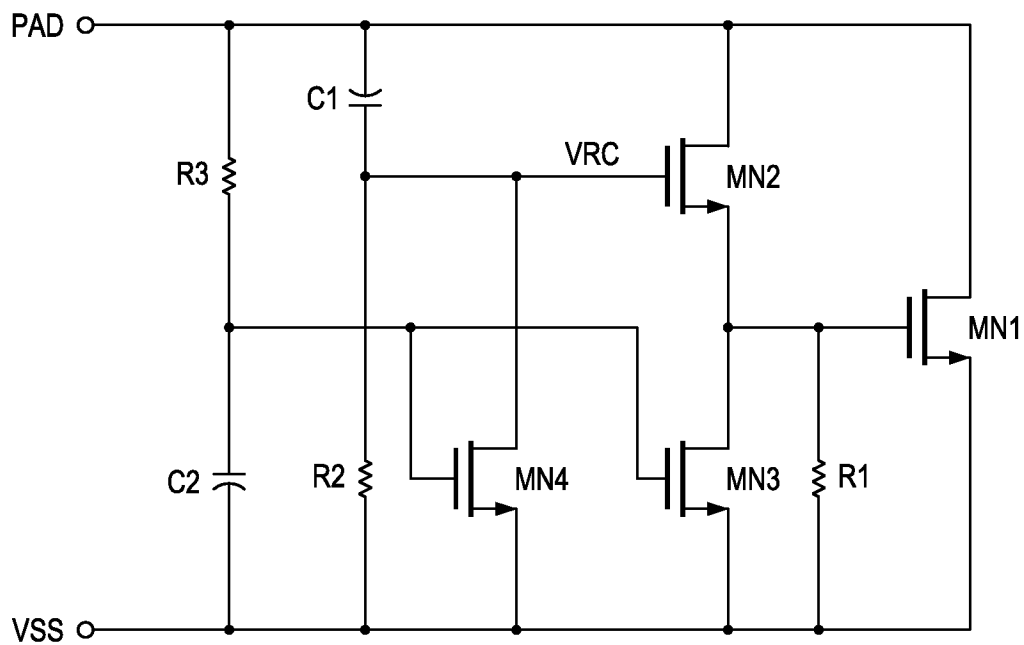
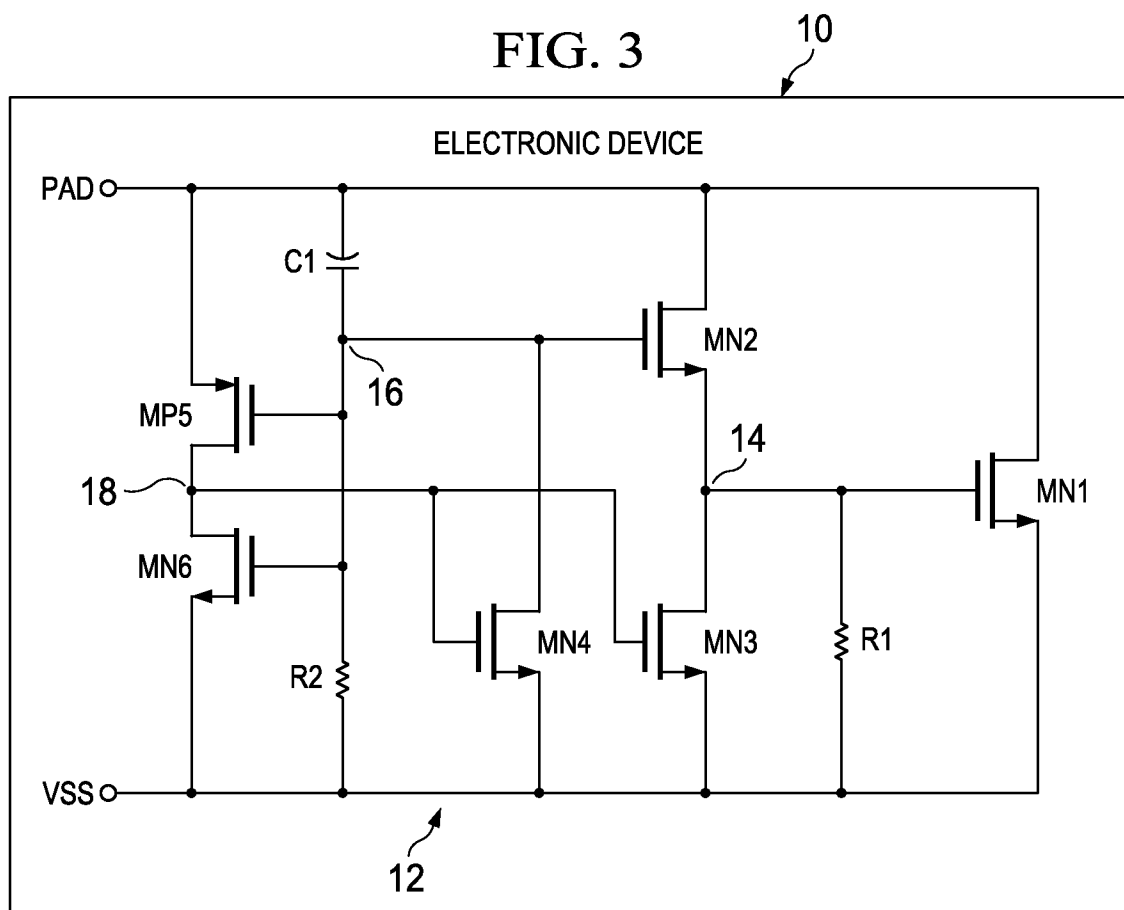
FIG. 1
(PRIOR ART)**FIG. 2**
(PRIOR ART)

FIG. 3



A. CLASSIFICATION OF SUBJECT MATTER**H01L 27/04(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/04; H01L 23/60; H02H 9/04; H02H 9/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: electrostatic, protect, circuit, invert, signal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007-0109697 A1 (YOON J. HUH) 17 May 2007 See abstract, paragraphs [0014]-[0021] and figure 1.	1-2, 7-8, 19-20
Y		3-6, 9-18
Y	US 2004-0125521 A1 (CRAIG THOMAS SALLING et al.) 01 July 2004 See abstract, paragraphs [0029]-[0037], [0047] and figures 1A-2B.	3-6, 9-18
A	KR 10-0718997 B1 (LG ELECTRONICS INC.) 16 May 2007 See abstract, pages 3-4 and figure 6.	1-20
A	US 2010-0290165 A1 (ANDREAS HARTBERGER) 18 November 2010 See abstract, paragraphs [0041]-[0055] and figure 1.	1-20
A	US 2007-0188953 A1 (CHAO-CHENG LEE et al.) 16 August 2007 See abstract, paragraphs [0022]-[0028] and figure 3.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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Information on patent family members

International application No.

PCT/US2013/024859

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0109697 A1	17.05.2007	KR 10-0795472 B1 KR 10-2007-0052185 A US 7453676 B2	21.01.2008 21.05.2007 18.11.2008
US 2004-0125521 A1	01.07.2004	US 7187530 B2	06.03.2007
KR 10-0718997 B1	16.05.2007	None	
US 2010-0290165 A1	18.11.2010	DE 102007042103 A1 DE 112008002348 A5 US 8315025 B2 WO 2009-030639 A1	26.03.2009 29.07.2010 20.11.2012 12.03.2009
US 2007-0188953 A1	16.08.2007	TW I302374 B US 7403362 B2	21.10.2008 22.07.2008