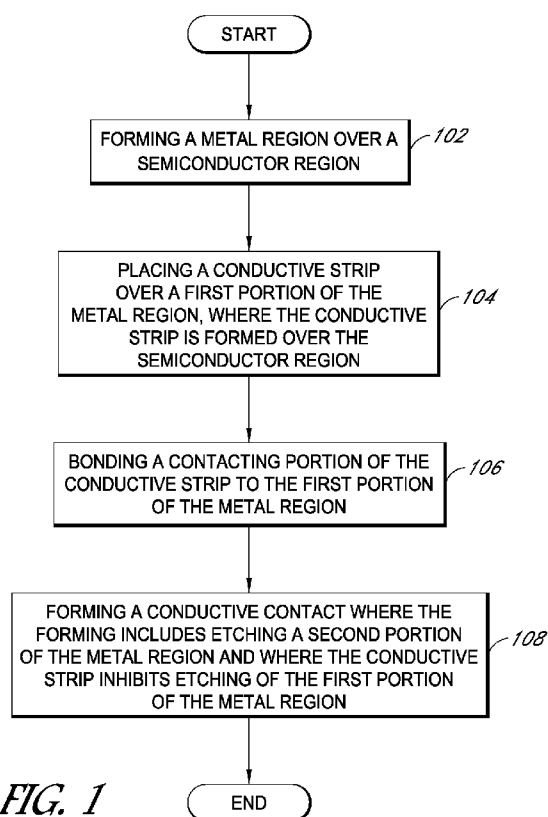




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[Continued on next page]

(54) **Title:** CONDUCTIVE STRIP BASED MASK FOR METALLIZATION OF SEMICONDUCTOR DEVICES

(57) **Abstract:** Methods of manufacturing a semiconductor device, and resulting semiconductor device are described. In an example, the method for manufacturing a semiconductor device include forming a semiconductor region and forming a metal seed region over the semiconductor region. The method can include placing a conductive strip over a first portion of the metal region, where the conductive strip is formed over the semiconductor region. The method can include bonding a contacting portion of the conductive strip to the first portion the metal region. The method can include etching a second portion of the metal region and where the conductive strip inhibits etching of the first portion of the metal region. In an example, the conductive strip can have a coating. In one example, the semiconductor device can be a solar cell.



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CONDUCTIVE STRIP BASED MASK FOR METALLIZATION OF SEMICONDUCTOR DEVICES

BACKGROUND

[0001] Semiconductor devices, for example photovoltaic (PV) cells among others, are well known electronic devices. In one example, photovoltaic (PV) cells, commonly known as solar cells, are devices for conversion of solar radiation into electrical energy. Generally, solar radiation impinging on the surface of, and entering into, the substrate of a solar cell creates electron and hole pairs in the bulk of the substrate. The electron and hole pairs migrate to p-doped and n-doped regions in the substrate, thereby creating a voltage differential between the doped regions. The doped regions are connected to the conductive regions on the solar cell to direct an electrical current from the cell to an external circuit. When PV cells are combined in an array such as a PV module, the electrical energy collected from all of the PV cells can be combined in series and parallel arrangements to provide power with a certain voltage and current.

[0002] Efficiency in producing semiconductor devices is directly related to the cost effectiveness of such semiconductor devices. Accordingly, techniques for increasing the efficiency of semiconductor devices, or techniques for increasing the efficiency in the manufacture of semiconductor devices, are generally desirable. Some embodiments of the present disclosure allow for increased semiconductor devices manufacture efficiency by providing novel processes for fabricating semiconductor devices structures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1 illustrates a flow chart representation of an example method for manufacturing a semiconductor device, according to some embodiments.

[0004] Figures 2-5 illustrate cross-sectional views of an example semiconductor device during the method of Figure 1, according to some embodiments.

[0005] Figure 6 illustrates an example semiconductor device, according to some embodiments.

[0006] Figures 7-9 illustrate cross-sectional views of another example semiconductor device during the method of Figure 1, according to some embodiments.

[0007] Figure 10 illustrates another example semiconductor device, according to some embodiments.

[0008] Figure 11 illustrates still another example semiconductor device, according to some embodiments.

DETAILED DESCRIPTION

[0009] The following detailed description is merely illustrative in nature and is not intended to limit the embodiments of the subject matter of the application or uses of such embodiments. As used herein, the word “exemplary” means “serving as an example, instance, or illustration.” Any implementation described herein as exemplary is not necessarily to be construed as preferred or advantageous over other implementations. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.

[0010] This specification includes references to “one embodiment” or “an embodiment.” The appearances of the phrases “in one embodiment” or “in an embodiment” do not necessarily refer to the same embodiment. Particular features, structures, or characteristics may be combined in any suitable manner consistent with this disclosure.

[0011] Terminology. The following paragraphs provide definitions and/or context for terms found in this disclosure (including the appended claims):

[0012] “Comprising.” This term is open-ended. As used in the appended claims, this term does not foreclose additional structure or steps.

[0013] “Configured To.” Various units or components may be described or claimed as “configured to” perform a task or tasks. In such contexts, “configured to” is used to connote structure by indicating that the units/components include structure that performs those task or tasks during operation. As such, the unit/component can be said to be configured to perform the task even when the specified unit/component is not currently operational (e.g., is not on/active). Reciting that a unit/circuit/component is “configured to” perform one or more tasks is expressly intended not to invoke 35 U.S.C. §112, sixth paragraph, for that unit/component.

[0014] “First,” “Second,” etc. As used herein, these terms are used as labels for nouns that they precede, and do not imply any type of ordering (e.g., spatial, temporal, logical, etc.). For example, reference to a “first” conductive strip does not necessarily imply that this conductive strip is the first conductive strip in a sequence; instead the term “first” is used to differentiate this conductive strip from another conductive strip (e.g., a “second” conductive strip).

[0015] “Based On.” As used herein, this term is used to describe one or more factors that affect a determination. This term does not foreclose additional factors that may affect a determination. That is, a determination may be solely based on those factors or based, at least in part, on those factors. Consider the phrase “determine A based on B.” While B may be a factor that affects the determination of A, such a phrase does not foreclose the determination of A from also being based on C. In other instances, A may be determined based solely on B.

[0016] “Coupled” – The following description refers to elements or nodes or features being “coupled” together. As used herein, unless expressly stated otherwise, “coupled” means that one element/node/feature is directly or indirectly joined to (or directly or indirectly communicates with) another element/node/feature, and not necessarily mechanically.

[0017] “Inhibit” – As used herein, inhibit is used to describe a reducing or minimizing effect. When a component or feature is described as inhibiting an action, motion, or condition it may completely prevent the result or outcome or future state completely. Additionally, “inhibit” can also refer to a reduction or lessening of the outcome, performance, and/or effect which might otherwise occur. Accordingly, when a component, element, or feature is referred to as inhibiting a result or state, it need not completely prevent or eliminate the result or state.

[0018] In addition, certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, and “below” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, “side”, “outboard”, and “inboard” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

[0019] In the following description, numerous specific details are set forth, such as specific operations, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known techniques are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure.

[0020] This specification includes a description of an example method for manufacturing a semiconductor device, followed by example semiconductor devices formed from the described methods. In an example, the semiconductor devices can be, but are not limited to, solar cells as described in Figures 2-10 below. Various examples are provided throughout. Although many of the examples are drawn and described in the context of back-contact solar cells, the structures and techniques described herein can apply equally to front-contact solar cells.

[0021] Turning now to Figure 1, a method for manufacturing a semiconductor device is shown, according to some embodiments. In various embodiments, the method of Figure 1 can include additional (or fewer) blocks than illustrated. For example, in some embodiments prior to

forming a metal seed region, a semiconductor region can be formed in or on a front or back side of the semiconductor device.

[0022] Referring to Figure 2, and corresponding operation 102 of the flowchart of Figure 1, a metal region 220 can be formed over a surface 215 of the semiconductor device 200, according to some embodiments. In an embodiment, the semiconductor device 200 can include a substrate 202. In an embodiment, the semiconductor device 200 can have a front side 204 which faces the sun during normal operation and a back side 206 opposite the front side 204. In one example, the semiconductor device 200 is a solar cell.

[0023] In an embodiment, a dielectric region 213 can be formed over the surface 215 of the substrate 202, as shown. In an embodiment, the dielectric region 213 can include silicon oxide and/or other oxides. In an embodiment, a contact opening 216 can be formed in the dielectric region 213 as shown and, as a result, the metal region 220 can be formed on the surface 215 of the substrate 202 within the contact opening 216. In an example, the contact opening 216 can be formed by laser ablation and/or by a mask and etch process, among others.

[0024] In an embodiment, the substrate 202 can be a silicon substrate. In some embodiments, the silicon substrate can be cleaned, polished, planarized and/or thinned or otherwise processed prior to the formation of the metal region 220. In an embodiment, the silicon substrate can be single-crystalline or a multi-crystalline silicon substrate. In an embodiment, the silicon substrate can be an N-type or a P-type silicon substrate.

[0025] In an embodiment, prior to the formation of the metal region 220, a semiconductor region can be formed in or above the substrate 202. In an example, a first semiconductor region 212 can include an N-type doped region. In one example, a second semiconductor region 214 can include a P-type doped region. In an embodiment, the first and second semiconductor regions 212, 214 can be in the substrate 202. In an embodiment, the first and second semiconductor regions 212, 214 can be formed over the substrate 202. In an example, the first and second semiconductor regions 212, 214 can be doped polysilicon regions. In an embodiment, the doped polysilicon regions can be formed over the substrate. In one embodiment, a dielectric region (e.g., a tunnel oxide) can be formed between the doped polysilicon regions and the substrate. In an embodiment, the semiconductor regions 212, 214 can be formed at the back side 206 of the semiconductor device 200, as shown in Figure 2. In some embodiments, one or more semiconductor regions can be formed, instead, on the front side 204 of the semiconductor device 200. In one example, a first semiconductor region can be formed on the back side of the semiconductor device 200 and/or a second semiconductor region can be formed on the front side of the semiconductor device 200. In some embodiments, a metal region can be formed over a semiconductor region on the front side of the semiconductor device.

In an example, a first metal region can be formed over a first semiconductor region on the back side and/or a second metal region can be formed over a second semiconductor region on the front side of the solar cell. Thus, in some examples, a plurality of semiconductor and/or metal regions (e.g., 2 or more) can be used.

[0026] In an embodiment, the metal region 220 can include aluminum (e.g., an aluminum region), aluminum/Si, nickel, copper, titanium, tungsten, and/or alloys thereof, among other examples. In an embodiment, the metal region 220 can be formed by blanket deposition, sputtering, by printing techniques (e.g., screen printing, ink-jet printing and/or spin coating), among other examples. In an embodiment, the metal region 220 can have a thickness 221 in a range of 50-1000 nanometers. In one embodiment, the metal region 220 can have a thickness 221 greater than 1000 nanometers (e.g., 2000 nanometers).

[0027] In an embodiment, the front side 204 of the semiconductor device 200 can be a textured surface 203 as shown in Figure 2. In an embodiment, a hydroxide-based wet etchant can be used to form at least a portion of the textured surface 203 and/or to texturize exposed portions of the substrate 202. A textured surface may be one which has a regular or an irregular shaped surface. In an example, a regular shaped surface can be a smooth and/or planarized surface. In one example, an irregular shaped surface can be a rough, uneven, and/or a non-planar surface. In an embodiment, the textured surface 203 at the front side 204 of the solar cell 200 can be configured to scatter incoming light, where the light scattered from the front side 204 of the solar cell 200 can decrease the amount of light reflected off of the front side 204 and, thus, increase the light collected at the front side 204 of the solar cell 200.

[0028] Referring to Figure 3, and corresponding operation 104 of the flowchart of Figure 1, a conductive strip 230 can be placed over a first portion 222 of the metal region 220, according to some embodiments. In an embodiment, the conductive strip 230 can be placed over the first portion 222 of the metal region 220, where the conductive strip 230 can be located substantially parallel with the semiconductor regions 212, 214 as shown. In an example, a machine vision system can be used to align the conductive strip 230 over the first portion 222 of the metal region 220, where the placement is substantially parallel with one of the semiconductor regions 212, 214. In an embodiment, the conductive strip 230 can be a conductive wire, ribbon, pre-cut foil or a strip of foil. In an example, the conductive strip 230 can include copper, nickel, aluminum, and/or alloys thereof, among other examples. In one example, the conductive strip 230 can be a copper wire or an aluminum foil. In an embodiment, the conductive strip 230 can have a thickness 231 in a range of 50-1200 nanometers. In one embodiment, the conductive strip 230 can have a thickness 231 greater than 1200 nanometers (e.g., 2000 nanometers). In an embodiment, the ratio of the thickness 231 can be twice, ten times or 100 times, or more, to the

thickness 221. In an embodiment, a second portion 224 of the metal region 220 can be exposed, e.g., not have any conductive strip over that portion. As shown in Figure 3, a respective conductive strip 230 is aligned over each of semiconductor regions 212 and 214. In an embodiment, a plurality of conductive strips can be placed over the metal region. In an example, a first and a second conductive strip can be placed over the metal region. In one example, the first and second conductive strips can be placed over substantially the same semiconductor region (e.g., placed over semiconductor regions of the same polarity). In some examples, the second conductive strip can be placed over a second, different, semiconductor region than the first conductive strip (e.g., placed over semiconductor regions of different polarities).

[0029] In some embodiments, a first conductive strip can be placed on the front side 204 and/or back side 206 of the semiconductor device 200. In an example, a first conductive strip can be placed over a first semiconductor region located on the back side of the semiconductor device 200 and/or a second conductive strip can be placed over a second semiconductor region located on the front side 204 of the semiconductor device 200. In some embodiments, a first and second metal region can be formed between the first and second conductive strips and the first and second semiconductor regions, respectively.

[0030] Referring to Figure 4, and corresponding operation 106 of the flowchart of Figure 1, a bonding process can be performed to bond a contacting portion 232 of the conductive strip 230 to the first portion 222 of the metal region 220. In an embodiment, the bonding process includes electrically connecting the conductive strip 230 to the metal region 220. As shown, the contacting portion 232 can be a portion of the conductive strip 230 in contact, e.g., flatly contacting, the first portion 222 of the metal region 220. In an embodiment, by flatly contacting the first portion 222 of the metal region 220, the contacting portion 232 can inhibit etching at the first portion 222 of the metal region 220 (e.g., during a subsequent etching process), whereas any air pockets or gaps between the conductive strip 230 and the metal region 220 can allow for etching at those regions.

[0031] In an embodiment, the bonding process of operation 106 can include applying a force 240 to the contacting portion of the conductive strip 230 to electrically connect the conductive strip 230 to the metal region 220. In an example, as shown in Figure 4, an applicator 242 can be used to apply the force 240 to the contacting portion of the conductive strip 230. In an example, the applicator 242 can be roller or a squeegee. In one such example, using the applicator 242 allows for applying the force uniformly to the contacting portion 232 of the conductive strip 230 and the first portion 222 of the metal region 220. In an example, a thermocompression process can be performed to electrically connect the contacting portion conductive strip 230 to the metal region 220.

[0032] In an embodiment, the bonding can include heating the contacting portion 232 of the conductive strip 230 to electrically connect the conductive strip 230 to the metal region 220. In one example, heat can be applied after, during, or before applying a force 240 to the contacting portion of the conductive strip 230. In an example, a laser can be used to heat the contacting portion of the conductive strip. In one example, a laser can be used to electrically connect the conductive strip 230 to the metal region 220. In some examples, a welding process (e.g., a laser weld process) can be used to bond the contacting portion 232 of the conductive strip 230 to the first portion 222 of the metal region 220. In one embodiment, the heating can include inductive heating and/or contacting heating.

[0033] In an embodiment, the conductive strip 230 can include a conductive adhesive disposed between the contacting portion 232 of the conductive strip and the first portion 222 of the metal region 230. In an example, the conductive adhesive can be a solder paste. In an embodiment, the bonding can include heating the conductive adhesive (e.g., solder paste) to electrically connect the conductive strip 230 to the metal region 220. In one embodiment, heating the conductive adhesive can include inductive heating and/or contacting heating.

[0034] Referring to Figure 5, and corresponding operation 108 of the flowchart of Figure 1, an etching process can be performed to form conductive contacts 234, 236, according to some embodiments. In one example, the second portion 224 the metal region 220 of Figure 4 can be etched 225 to form the conductive contacts 234, 236. In an example, the etching 225 can form a first conductive contact 234 over the first semiconductor region 212 and a second conductive contact 236 over the second semiconductor region 214. In one example, the etching 225 can electrically separate the first conductive contact 234 from the second conductive contact 236. In an example, the etching 225 can include at least partially etching the conductive strip 230, as shown in Figure 5, where the conductive strip 230 can inhibit etching, at block 108, of the first portion 222 of the metal seed region 220. In one example, as shown, the first and second conductive contacts 234, 236 can be formed on the back side 206 of the semiconductor device 200. In some embodiments, the conductive strip 230 may not be etched (e.g., the coating 335 is not etched at all).

[0035] In some embodiments, one or more conductive contacts can instead be formed at the front side of the semiconductor device. In an example, a first conductive contact can be formed over a first semiconductor region located on the back side of the semiconductor device 200 and/or a second conductive contact can be formed over a second semiconductor region located on the front side of the semiconductor device 200.

[0036] In an example, the conductive strip 230 of Figure 4 can have a thickness 331 greater than a thickness 321 of the metal region 220. In the same example, the etching 225 can

include etching through the metal region 220 having the thickness 331 to electrically separate the first conductive contact 236 from second conductive contact 236. In the same example, the etching 225 can include partially etching the conductive strip 230 having the thickness 331, where the conductive strip 230 inhibits etching of the first portion 222 of the metal seed region 220.

[0037] In an embodiment, a first etchant can be used to etch through the second portion 224 of the metal region 220 of Figure 4. In an example, the first etchant can include an acid having oxidizing agents (e.g., hydrogen peroxide). In some examples, the first etchant can include a base (e.g., potassium hydroxide, sodium hydroxide). In one example, the conductive strip 230 of Figure 4 can have a first thickness greater than a second thickness of the metal seed region 220 and the conductive strip 230 can include substantially the same metal as the metal region 220. In the same embodiment, the first etchant can be configured to etch through the second thickness of the metal region 220 and partially etch the first thickness of conductive strip 230. In one embodiment, etch duration can be configured to allow etching through the second portion 224 of the metal region 220 and partially etching the conductive strip 230. In an embodiment, an etch duration can be configured to allow etching through the second portion 224 of the metal region 220 and to only partially etch the conductive strip 230. In some embodiments, multiple etchants (e.g., a first, second, etc.) can be used. In an example, the first etchant can be used to etch the metal region 220 including a first metal and a second etchant can be used to etch the conductive strip 230 including a second, different, metal. In one embodiment, the conductive strip 230 can be referred to as a partial sacrificial etching barrier. In an embodiment, the first and second etchants can be substantially the same and/or different etchant altogether (e.g., acid having oxidizing agents, etc.).

[0038] In an embodiment, the conductive contacts 234, 236 can include the conductive strip 230 and the metal region 220. In one embodiment, the conductive contacts 234, 236 can form metal contact fingers. In an embodiment, the metal contact fingers can be interdigitated.

[0039] Figure 6 illustrates an example semiconductor device formed from the methods described in Figures 2-5, according to some embodiments. As shown, the semiconductor device can be a solar cell 200, which can have a front side 204 which faces the sun during normal operation and a back side 206 opposite the front side 204.

[0040] In an embodiment, the front side 204 of the solar cell 200 can have a textured surface 203 as shown in Figure 6. A textured surface may be one which has a regular or an irregular shaped surface. In an example, a regular shaped surface can be a smooth and/or planarized surface. In one example, an irregular shaped surface can be a rough, uneven, and/or a non-planar surface. In an embodiment, the textured surface 203 at the front side 204 of the solar

cell 200 can be configured to scatter incoming light, where the light scattered from the front side 204 of the solar cell 200 can decrease the amount of light reflected off of the front side 204 and, thus, increase the light collected at the front side 204 of the solar cell 200. In an embodiment, a front dielectric region 223 can be formed over the surface 203. In some embodiments, the front dielectric region 223 can include silicon oxide, among other oxides.

[0041] In an embodiment, the solar cell 200 can include a substrate 202. In an embodiment, the substrate 202 can be a silicon substrate. In some embodiments, the silicon substrate can be single-crystalline or a multi-crystalline silicon substrate. In one embodiment, the silicon substrate can be an N-type or a P-type silicon substrate.

[0042] In an embodiment, the substrate 202 can include a semiconductor region 212, 214 on the back side 206 of the solar cell 200. In an example, a first semiconductor region 212 can include an N-type doped region. In one example, a second semiconductor region 214 can include a P-type doped region. In an embodiment, the first and second semiconductor regions 212, 214 can be in the substrate 202. In an embodiment, the first and second semiconductor regions 212, 214 can be disposed over the substrate 202. In an example, the first and second semiconductor regions 212, 214 can be doped polysilicon regions. In an embodiment, the doped polysilicon regions can be disposed over the substrate 202 at the back side 206 of the solar cell 200. In one embodiment, a dielectric region (e.g., a tunnel oxide) can be disposed between the doped polysilicon regions and the substrate.

[0043] In an embodiment, conductive contacts 234, 236 can be disposed on the semiconductor regions 212, 214 at the back side 206 of the solar cell 200. In an example, a first conductive contact 234 can be disposed over the first semiconductor region 212. In one example, a second conductive contact 236 can be disposed over the second semiconductor region 214. In an example, the conductive contacts 234, 236 can be metal contact fingers. In some examples, the metal contact fingers can be interdigitated. In an embodiment, the conductive contacts 234, 236 allow for pathways for electrical current conduction from the first and second semiconductor regions 212, 214 to an external circuit. In some embodiments, the conductive contacts 220, 221 can include a metal region 220. In an embodiment, a dielectric region 213 can be disposed between the metal region 220 and the substrate 202, as shown. In one embodiment, the dielectric region 213 can include silicon oxide, among other oxides. In an embodiment, the metal region 220 can include aluminum (e.g., an aluminum region), aluminum/Si, nickel, copper, titanium, tungsten, and/or alloys thereof. In an embodiment, the metal region 220 can have a thickness approximately in the range of 50 – 1000 nanometers.

[0044] In an embodiment, the conductive contacts 234, 236 can include a conductive strip 230. In one embodiment, the conductive strip 230 can be disposed on the metal region 220,

as shown. In an embodiment, the conductive strip 224 can include copper, nickel, aluminum, iron, and/or alloys thereof. In an embodiment, the conductive strip 230 can have a thickness approximately in the range of 60 – 1200 nanometers.

[0045] In some embodiments, the metal region 220 and the conductive strip 230 can include the same metal. In an example, the metal region 220 and the conductive strip 230 can both, respectively, include aluminum. In some examples, the metal at the first portion 222 of the metal seed region 220 and the metal of the contacting portion 232 can be substantially the same. For example, the first portion 222 of the metal region 220 and contacting portion 232 of the conductive strip 230 can be aluminum or an aluminum-containing alloy.

[0046] In one embodiment, the metal region 220 and the conductive strip 230 can be substantially different. In one example, the metal region 220 can include aluminum and the conductive strip 230 can include iron or steel. In the same example, a thermocompression process can be used to bond the conductive strip including iron or steel to the metal seed region including aluminum.

[0047] In an embodiment, another semiconductor region can be located on the front side 204 of a solar cell 200. In an example, the semiconductor region can include an N-type or P-type doped region. In an embodiment, another conductive contact can be disposed on the semiconductor region on the front side 204 of the solar cell 200. In an embodiment, the conductive contact can also include a conductive strip bonded to a metal region, where the conductive contact is located on the semiconductor region on the front side of the solar cell 200. In the same embodiment, the semiconductor device 200 can be a front contact solar cell.

[0048] With reference to Figures 7-9, a method of manufacturing a semiconductor device is shown, according to some embodiments. As shown, the methods of Figures 7-9 are substantially similar to the methods of Figures 2-5. The method of Figures 7-9 have similar reference numbers to elements of Figure 2-5, wherein like reference numbers refer to similar elements throughout the figures. In an embodiment, the structure of the semiconductor device 300 of Figures 7-9 are substantially similar to the structure of the semiconductor device 200 in Figures 2-5, respectively, except as described below. Thus, unless specifically pointed out in Figures 7-9, the description of similar structures in Figures 2-5 applies equally to the structures of Figures 7-9, respectively.

[0049] Referring to Figure 7, and corresponding operation 104 of the flowchart of Figure 1, a coated conductive strip 330 can be placed over a first portion 322 of a metal region 320, according to some embodiments. In an example, coated conductive strips 330 can be placed over a first and second semiconductor regions 312, 314. In one embodiment, the coated conductive strips 330 can be placed substantially parallel with the semiconductor regions 312,

314 as shown. In an embodiment, the coated conductive strip 330 can include a metal strip 333 having a coating 335 as shown. In one embodiment, the coating 335 can have a thickness 331 approximately in the range of 1-10 μm . In an embodiment, the thickness 331 of the coating 335 can be greater than or equal to a thickness 321 of the metal region 320. In an embodiment, the metal region 320 can have a thickness approximately in a range of 50 – 1000 nanometers. In an embodiment, the coating 335 can include aluminum (e.g., an aluminum region), aluminum/Si, nickel, copper, titanium, tungsten, and/or alloys thereof, among other examples. In an embodiment, the coating can include a solder paste. In an embodiment, the metal strip can include nickel, copper, iron and steel, among other examples. In an embodiment, the ratio of the thickness 331 can be twice, ten times or 100 times, or more, to the thickness 321. In an embodiment, the coated conductive strip 330 can be a coated conductive wire, coated ribbon, coated pre-cut foil or a coated strip of foil. In one example, the coated conductive strip 330 can be a coated copper wire or a coated aluminum foil.

[0050] In some embodiments, a first coated conductive strip can be placed on the front side 304 and/or back side 306 of the semiconductor device 300. In an example, a first conductive strip can be placed over a first semiconductor region located on the back side of the semiconductor device 300 and/or a second conductive strip can be placed over a second semiconductor region located on the front side 304 of the semiconductor device 300. In some embodiments, a first and second metal region can be formed between the first and second conductive strips and the first and second semiconductor regions, respectively. As discussed above, a plurality of conductive strips (e.g., first, second conductive strips) can be used.

[0051] Referring to Figure 8, and corresponding operation 106 of the flowchart of Figure 1, a bonding process can be performed to bond a contacting portion 332 of the coated conductive strip 330 to the first portion 322 of the metal region 320. In an embodiment, the bonding process of Figure 8 is substantially similar to the bonding process described in Figure 4. Therefore the description of corresponding portions of Figure 4 applies equally to the description of Figure 8.

[0052] Referring to Figure 9, and corresponding operation 108 of the flowchart of Figure 1, an etching process can be performed to form conductive contacts 334, 336, according to some embodiments. In an embodiment, the etching process of Figure 9 is substantially similar to the etching process described in Figure 5, except as described below. Therefore the description of corresponding portions of Figure 5 applies equally to the description of Figure 9.

[0053] In one example, as shown, the first and second conductive contacts 334, 336 can be formed on the back side 306 of the semiconductor device 300. In some embodiments, one or more conductive contacts including a coated conductive strips can instead be formed at the front side of the semiconductor device. In an example, a first conductive contact can be formed over a

first semiconductor region located on the back side of the semiconductor device 300 and/or a second conductive contact can be formed over a second semiconductor region located on the front side of the semiconductor device 300.

[0054] In an embodiment, the coated conductive strip 330 can inhibit etching of the first portion 322 of the metal region 320. In an example, the etching 325 can include etching the coating 335 of the coated conductive strip 330, where the coating 335 can inhibit etching, at block 108, of the first portion 322 of the metal region 320. In one example, the coating 335 of coated conductive strip 330 of Figure 8 can have a first thickness 331 equal to a second thickness 321 of the metal seed region 220. In the same example, the etching 325 can include etching through the metal region 320 having the second thickness 321. In the same example, the etching 325 can include etching the coating 335 of the coated conductive strip 330 having the first thickness 331, where the etching 335 at least partially exposes the metal strip 333. In one example, the metal strip 333 can be at least partially coated by the coating 335 (e.g., at the interface between the first portion 322 of the metal seed region and the contacting portion 332 of the coated conductive strip 330. In some examples, the coating 337 can include substantially the same metal as the metal region 320. In some examples, the coating 335 may not be etched (e.g., the coating 335 is not etched at all).

[0055] In one example, the etching 325 can include at least partially etching, the coating 337 of the conductive strip 330, where the coated conductive strip 330 can inhibit etching, at block 108, of the first portion 322 of the metal seed region 320. In one example, the coating 337 of coated conductive strip 330 of Figure 8 can have a thickness 331 greater than a thickness 321 of the metal region 320. In the same example, the etching 225 can include etching through the metal region 320 having a second thickness 321. In one example, as shown, the etching 225 can electrically separate the first conductive contact 236 from second conductive contact 236. In one example, as shown, the first and second conductive contacts 334, 336 can be formed on the back side 306 of the semiconductor device 300. In the same example, the etching 225 can include at least partially etching the coating 337 of the conductive strip 330 having a first thickness 331, where the coating 337 of the coated conductive strip 330 inhibits etching of the first portion 322 of the metal seed region 320 and the first thickness 331 is greater than the second thickness 321.

[0056] In an embodiment, a first etchant can be used to etch through the second portion 324 of the metal region 320 of Figure. In an example, the first etchant can include an acid having oxidizing agents (e.g., hydrogen peroxide). In some examples, the first etchant can include a base (e.g., potassium hydroxide, sodium hydroxide). In one example, the coated conductive strip 330 of Figure 8 can include a coating having a first thickness 331 greater than a second thickness 321 of the metal region 320. In an example, the coating 337 of the coated

conductive strip 330 can include substantially the same metal as the metal region 320. In one example, the first etchant can be configured to etch through the second thickness 321 of the metal seed region 220 and partially etch the coating 337 having the first thickness 331 of the conductive strip 330, as shown. In an example, the first etchant can be configured to etch through both the second portion 322 of the metal region 320 and etch through the coating 337 of the coated conductive strip 330, as shown. In one embodiment, an etch duration can be configured to allow etching through the second portion 324 of the metal region 320 and partially etching the coating 337 of the coated conductive strip 330. In some examples, the etch duration can be configured to be long enough to etch through both the second portion 324 of the metal region 320 and the coating 337 of the coated conductive strip 330. In some embodiments, multiple etchants (e.g., a first, second, etc.) can be used. In an example, the first etchant can be used to etch the metal region 320 and a second etchant can be used to etch the coating 337 of the coated conductive strip 330. In some examples, the first etchant can be configured to etch the metal region 320 including a first metal and a second etchant can be used to etch the coating 337 including a second, different, metal. In one embodiment, the coated conductive strip 330 can be referred to as a partial sacrificial etching barrier.

[0057] Figure 10 illustrates an example semiconductor device formed from the methods described in Figures 7-9, according to some embodiments. As shown, the semiconductor device can be a solar cell 300. As shown, the solar cell 300 can have a front side 304 which faces the sun during normal operation and a back side 306 opposite the front side 304. In one embodiment, the solar cell 300 is substantially similar to the solar cell 200 of Figure 6. As shown, the solar cell 300 has similar reference numbers to elements of the solar cells of Figure 6, wherein like reference numbers refer to similar elements throughout the figures. In an embodiment, the structure of the solar cell 300 is substantially similar to the structure of the solar cell 200 in Figures 6, respectively, except as described below. Therefore the description of corresponding portions of Figure 6 applies equally to the description of Figure 10.

[0058] In an embodiment, the solar cell 300 can include conductive contacts 334, 336. In one embodiment, the conductive contacts 334, 336 include a coated conductive strip disposed on a metal region 320. In an example, the conductive contacts 334, 336 can be metal contact fingers. In some examples, the metal contact fingers can be interdigitated. In an embodiment, the coated conductive strip can include a metal strip 333 having a coating 337 as shown. In an example, the coating 337 can surround the metal strip 333. In an embodiment, the metal region 320 can have a thickness approximately in the range of 50 – 1000 nanometers. In an embodiment, the coating 337 can include aluminum (e.g., an aluminum region), aluminum/Si, nickel, copper, titanium, tungsten, and/or alloys thereof, among other examples. In an

embodiment, the metal strip 333 can include nickel, copper, iron and steel, among other examples. In an embodiment, the ratio of the thickness of the coating 337 can be twice, ten times or 100 times, or more, to the thickness of the metal region 320. In one embodiment, the coating 337 can have a thickness 331 approximately in the range of 1-10 μm . In an embodiment, the coated conductive strip 330 can be a coated conductive wire, coated ribbon, coated pre-cut foil or a coated strip of foil. In one example, the coated conductive strip 330 can be a coated copper wire or a coated aluminum foil.

[0059] Figure 11 illustrates an example semiconductor device formed from the methods described in Figures 7-9, according to some embodiments. As shown, the semiconductor device can be a front contact solar cell 400. As shown, the solar cell 400 can have a front side 404 which faces the sun during normal operation and a back side 406 opposite the front side 404. In one embodiment, the solar cell 400 is substantially similar to the solar cell 200 and 300 of Figure 6 and 10. As shown, the solar cell 400 has similar reference numbers to elements of the solar cells of Figure 6 and 10, wherein like reference numbers refer to similar elements throughout the figures. In an embodiment, the structure of the solar cell 400 is substantially similar to the structure of the solar cell 200 and 300 in Figures 6 and 7, respectively, except as described below. In an example, a front dielectric region 423, similar to the front dielectric region 323 of Figure 10, can be formed over the surface 403. In some embodiments, the front dielectric region 423 can include silicon oxide, among other oxides. Therefore the description of corresponding portions of Figures 6 and 10 applies equally to the description of Figure 11.

[0060] In an embodiment, another semiconductor region 414 can be located on the front side 404 of a solar cell 400. In an example, the semiconductor region 414 can include an N-type or P-type doped region. In an embodiment, another coated conductive contact 435 can be disposed on the semiconductor region 414 on the front side 404 of the solar cell 400. In an embodiment, the coated conductive contact 435 can also include a conductive strip 433 bonded to a metal region 420, where the conductive contact 435 is located on the semiconductor region 414 on the front side 404 of the solar cell 400. In an embodiment, the coated conductive strip 433 can have a coating 437. In some embodiments, the coated conductive strip 433 can be at least partially coated.

[0061] Although specific embodiments have been described above, these embodiments are not intended to limit the scope of the present disclosure, even where only a single embodiment is described with respect to a particular feature. Examples of features provided in the disclosure are intended to be illustrative rather than restrictive unless stated otherwise. The above description is intended to cover such alternatives, modifications, and equivalents as would be apparent to a person skilled in the art having the benefit of this disclosure.

[0062] The scope of the present disclosure includes any feature or combination of features disclosed herein (either explicitly or implicitly), or any generalization thereof, whether or not it mitigates any or all of the problems addressed herein. Accordingly, new claims may be formulated during prosecution of this application (or an application claiming priority thereto) to any such combination of features. In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the appended claims.

CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor device, the method comprising:
forming a first semiconductor region;
forming a first metal region over the first semiconductor region;
placing a first conductive strip over a first portion of the first metal region,
wherein the first conductive strip is formed over the first semiconductor region;
bonding a contacting portion of the first conductive strip to the first portion the first metal region to electrically connect the first conductive strip to the first metal region;
and
forming a first conductive contact over the first semiconductor region, wherein the forming comprises etching a second portion of the first metal region and wherein the first conductive strip inhibits etching of the first portion of the first metal region.
2. The method of claim 1, wherein forming a first semiconductor region comprises forming a first semiconductor region on a back side of the semiconductor device, wherein the back side is configured to face away from the sun during normal operation.
3. The method of claim 1, further comprising:
forming a second semiconductor region on a front side of the semiconductor device, wherein the front side is configured to face the sun during normal operation;
forming a second metal region over the second semiconductor region;
placing a second conductive strip over a first portion of the second metal region, wherein the second conductive strip is formed over the second semiconductor region;
bonding a contacting portion of the second conductive strip to the first portion the second metal region to electrically connect the second conductive strip to the second metal region; and
forming a second conductive contact over the second semiconductor region, wherein the forming comprises etching a second portion of the second metal region and wherein the second conductive strip inhibits etching of the first portion of the second metal seed region.
4. The method of claim 1, further comprising:
forming a second semiconductor region on a back side of the semiconductor device, wherein the back side is configured to face away from the sun during normal operation;

forming a second metal region over the second semiconductor region;
placing a second conductive strip over a first portion of the second metal region, wherein the second conductive strip is formed over the second semiconductor region;
bonding a contacting portion of the second conductive strip to the first portion the second metal region to electrically connect the second conductive strip to the second metal region; and
forming a second conductive contact over the second semiconductor region, wherein the forming comprises etching a second portion of the second metal region and wherein the second conductive strip inhibits etching of the first portion of the second metal seed region.

5. The method of claim 1, wherein placing a first conductive strip over the first portion of the first metal seed region comprises placing a first conductive wire, ribbon, or foil strip over the first portion of the first metal region.

6. The method of claim 1, wherein bonding a contacting portion of the first conductive strip to the first portion the first metal region comprises applying a force to a contacting portion of the first conductive strip to electrically connect the first conductive strip to the first metal region.

7. The method of claim 1, wherein bonding a contacting portion of the first conductive strip to the first portion the first metal region comprises using a laser to electrically connect the first conductive strip to the first metal region.

8. The method of claim 1, wherein bonding a contacting portion of the conductive strip to the first portion the metal region comprises heating a contacting portion of the conductive strip to electrically connect the conductive strip to the metal seed region.

9. The method of claim 1, wherein bonding a contacting portion of the first conductive strip to the first portion the first metal region comprises heating a conductive adhesive disposed between the contacting portion of the first conductive strip and the first portion of the first metal region, wherein the heating electrically connects the first conductive strip to the first metal region.

10. The method of claim 9, wherein heating a conductive adhesive disposed between the contacting portion of the first conductive strip and the first portion of the first metal region

comprises heating a solder paste disposed between the contacting portion of the first conductive strip and the first portion of the first metal region.

11. The method of claim 1, wherein forming a first conductive contact on the first semiconductor region comprises least partially etching the first conductive strip.

12. The method of claim 1, wherein forming a first metal region over the first semiconductor region comprises forming aluminum over the first semiconductor region.

13. The method of claim 1, wherein placing a first conductive strip over the first portion of the first metal region comprises aligning copper wire or aluminum foil over the first portion of the first metal region.

14. The method of claim 1, wherein forming a first conductive contact on the first semiconductor device comprises:

etching a second portion of the first metal region, wherein the etching etches through the first metal region having a first thickness; and

etching the first conductive strip having a second thickness, wherein the second thickness is greater than the first thickness and wherein the first conductive strip inhibits etching of the first portion of the first metal region.

15. The method of claim 1, wherein forming a first conductive contact on the first semiconductor device comprises:

etching a second portion of the first metal region with a first etchant, wherein the first etchant is configured to etch through the second portion of the first metal region; and

etching the first conductive strip with the first etchant, wherein the first conductive strip inhibits etching of the first portion of the first metal region.

16. A method of manufacturing a semiconductor device, the method comprising:
forming first and second semiconductor regions;
forming a first metal region over the first semiconductor region;
placing a first coated conductive strip over a first portion of the first metal region,
wherein the first coated conductive strip is formed over the first semiconductor region; and

bonding a contacting portion of the first coated conductive strip to the first portion the first metal region to electrically connect the first coated conductive strip to the first metal region; and

forming a first conductive contact over the first semiconductor region, wherein the forming comprises etching a second portion of the first metal region and wherein the first coated conductive strip inhibits etching of the first portion of the first metal region.

17. The method of claim 16, wherein forming a first semiconductor region comprises forming a first semiconductor region on a back side of the semiconductor device, wherein the back side is configured to face away from the sun during normal operation.

18. The method of claim 16, further comprising:

forming a second semiconductor region on a front side of the semiconductor device, wherein the front side is configured to face the sun during normal operation;

forming a second metal region over the second semiconductor region;

placing a second coated conductive strip over a first portion of the second metal region, wherein the second coated conductive strip is formed over the second semiconductor region;

bonding a contacting portion of the second coated conductive strip to the first portion the second metal region to electrically connect the second coated conductive strip to the second metal region; and

forming a second conductive contact over the second semiconductor region, wherein the forming comprises etching a second portion of the second metal region and wherein a coating of the second coated conductive strip inhibits etching of the first portion of the second metal seed region.

19. The method of claim 16, further comprising:

forming a second semiconductor region on a back side of the semiconductor device, wherein the back side is configured to face away from the sun during normal operation;

forming a second metal region over the second semiconductor region;

placing a second coated conductive strip over a first portion of the second metal region, wherein the second coated conductive strip is formed over the second semiconductor region;

bonding a contacting portion of the second coated conductive strip to the first portion the second metal region to electrically connect the second coated conductive strip to the second metal region; and

forming a second conductive contact over the second semiconductor region, wherein the forming comprises etching a second portion of the second metal region and wherein a coating of the second coated conductive strip inhibits etching of the first portion of the second metal seed region.

20. The method of claim 16, wherein placing a first coated conductive strip over the first portion of the metal region comprises placing a coated conductive wire, coated ribbon, or a coated strip of foil over the first portion of the first metal region.

21. The method of claim 16, wherein forming a first conductive contact on the first semiconductor device comprises least partially etching a coating of the first coated conductive strip.

22. The method of claim 16, wherein forming a first conductive contact on the first semiconductor device comprises:

etching a second portion of the first metal region; and

etching a first coating of the first coated conductive strip to expose a metal strip, wherein the metal strip is electrically coupled to the first portion of the first metal region.

23. The method of claim 16, wherein forming a first conductive contact on the first semiconductor device comprises:

etching the second portion of the first metal region with a first etchant, wherein the first etchant is configured to etch through the second portion of the first metal region; and

etching a coating of the first coated conductive strip with the first etchant, wherein the coating and the first metal region comprise substantially the same metal and wherein the first etchant is configured to etch the coating and the first metal region.

24. The method of claim 16, wherein forming a first conductive contact on the first semiconductor device comprises:

etching a second portion of the first metal region; and

etching a coating of the first coated conductive strip to expose a metal strip, wherein the coating and the first metal region comprise substantially the same metal and wherein the second metal is electrically coupled to the first portion of the first metal region.

25. The method of claim 16, wherein forming a first conductive contact on the first semiconductor device comprises:

etching a second portion of the first metal region, wherein the first metal region comprises aluminum; and

etching an aluminum coating of the first coated conductive strip to expose a metal strip, wherein the metal strip is electrically coupled to the first portion of the first metal region.

26. The method of claim 16, wherein aligning the first coated conductive strip over a first portion of the first metal region comprises aligning coated copper wire or coated aluminum foil over a first portion of the first metal region.

27. The method of claim 16, wherein forming a first conductive contact on the first semiconductor device comprises:

etching the second portion of the first metal region having a first thickness; and

etching a coating having a second thickness of the first coated conductive strip, wherein the second thickness is substantially equal to the first thickness of the first metal region and wherein the etching exposes a metal strip electrically coupled to the first portion of the first metal region.

28. A solar cell, the solar cell comprising:

a first semiconductor region; and

a first metal contact finger disposed over the first semiconductor region, the first metal contact finger comprising:

a first metal region disposed over the first semiconductor region; and

a first coated conductive strip disposed over at least part of the first metal region, wherein the first coated conductive strip is formed over the first semiconductor region.

29. The solar cell of claim 28, wherein the first semiconductor region is formed on the back side of the solar cell.

30. The solar cell of claim 28, wherein the first coated conductive strip comprises substantially the same metal as the first metal region.

31. The solar cell of claim 28, wherein the first metal region comprises aluminum.

32. The solar cell of claim 28, wherein the first coated conductive strip comprises a metal strip having an aluminum coating.

33. The solar cell of claim 32, wherein the metal strip is a copper wire.

34. The solar cell of claim 28, wherein a coating of the first coated conductive strip has a first thickness approximately equal to a second thickness of the first metal region.

35. The solar cell of claim 28, wherein the first coated conductive strip is at least partially coated.

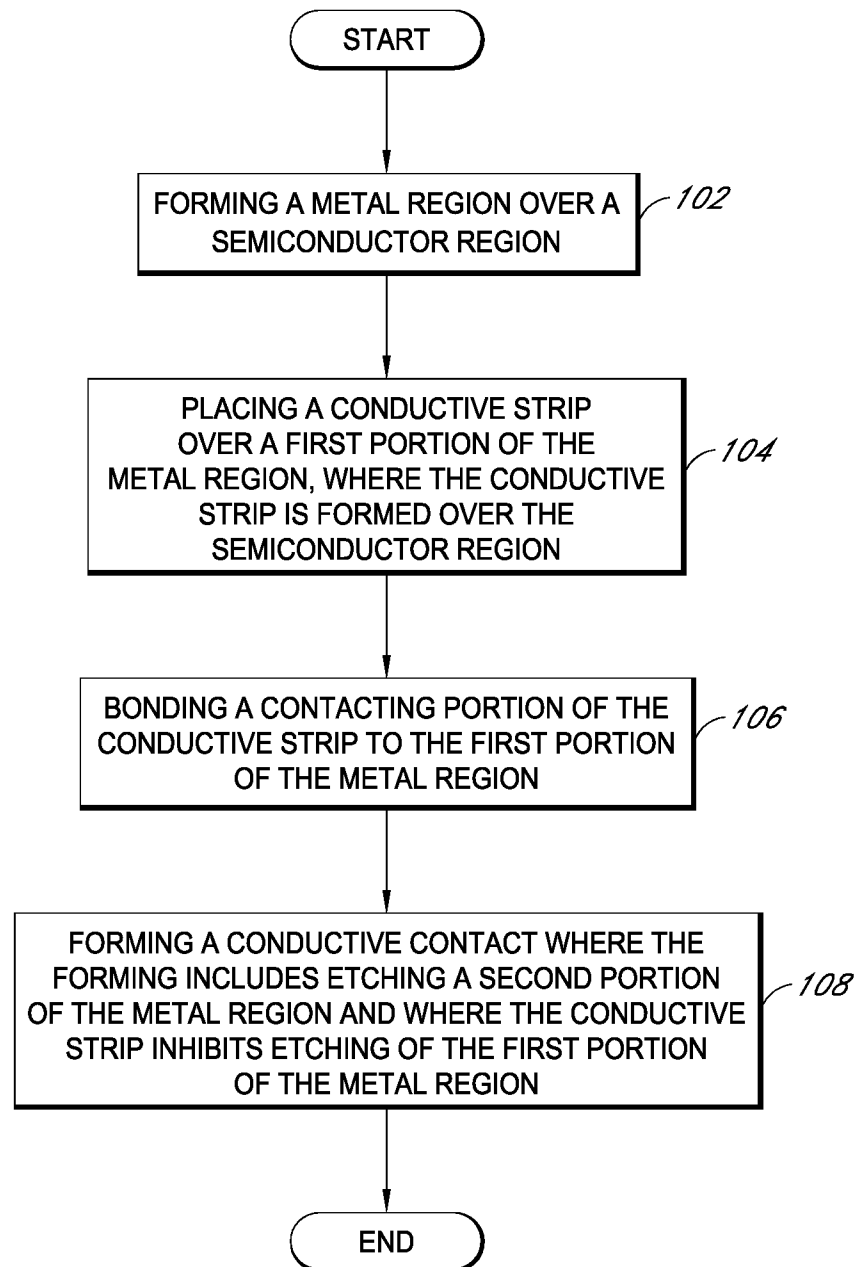
36. The solar cell of claim 28, wherein the first coated conductive strip is placed substantially parallel to the first semiconductor region.

37. The solar cell of claim 28, further comprising:
a second semiconductor region; and
a second metal contact finger disposed over the second semiconductor region, the second metal contact finger comprising:
a second metal region disposed over the second semiconductor region; and
a second coated conductive strip disposed over the second metal region, wherein the second coated conductive strip is placed over the second semiconductor region.

38. The solar cell of claim 28, wherein the first coated conductive strip is a coated wire or a coated metal foil.

39. The solar cell of claim 28, wherein the first coated conductive strip is a coated copper wire or a coated aluminum foil.

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*FIG. 1*

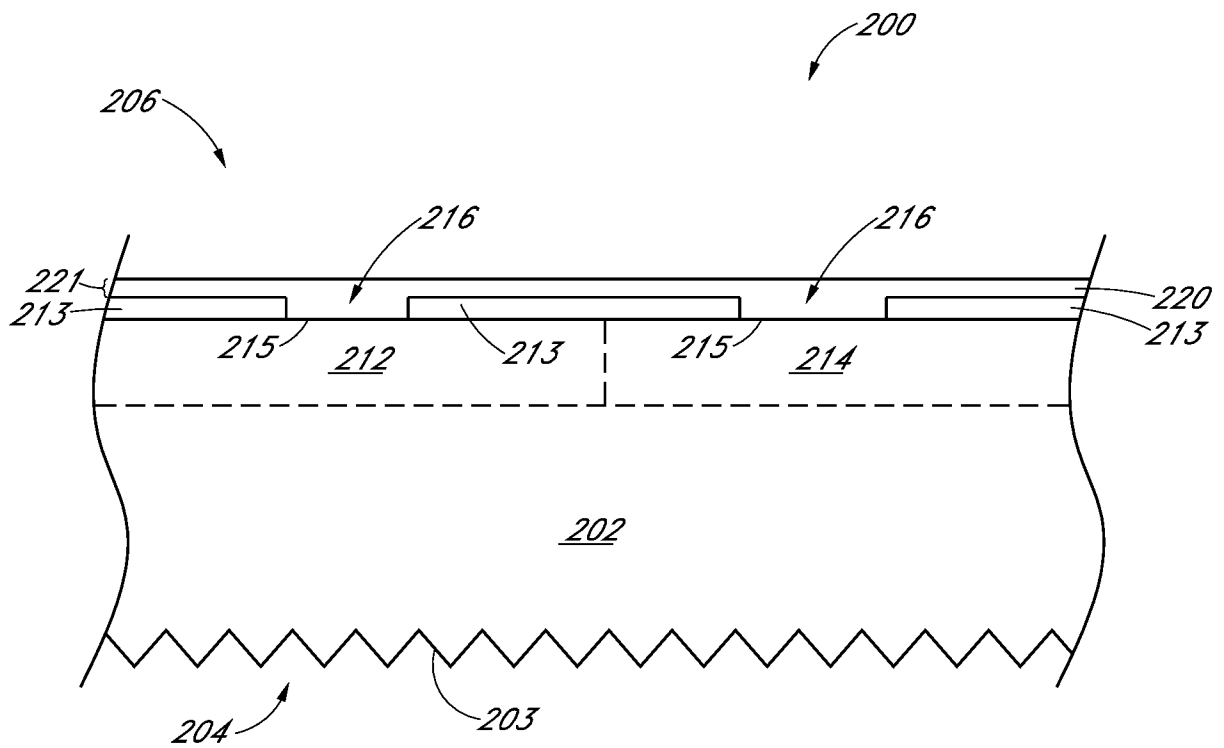


FIG. 2

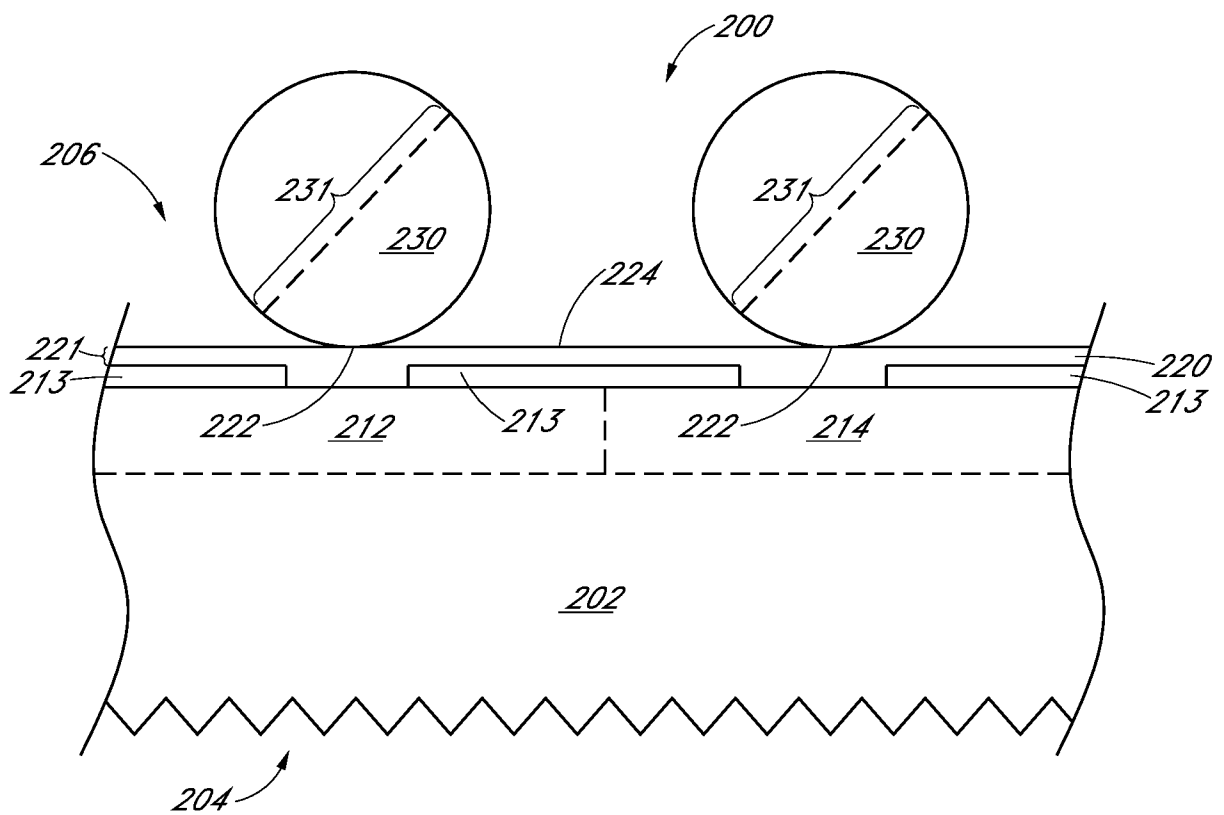


FIG. 3

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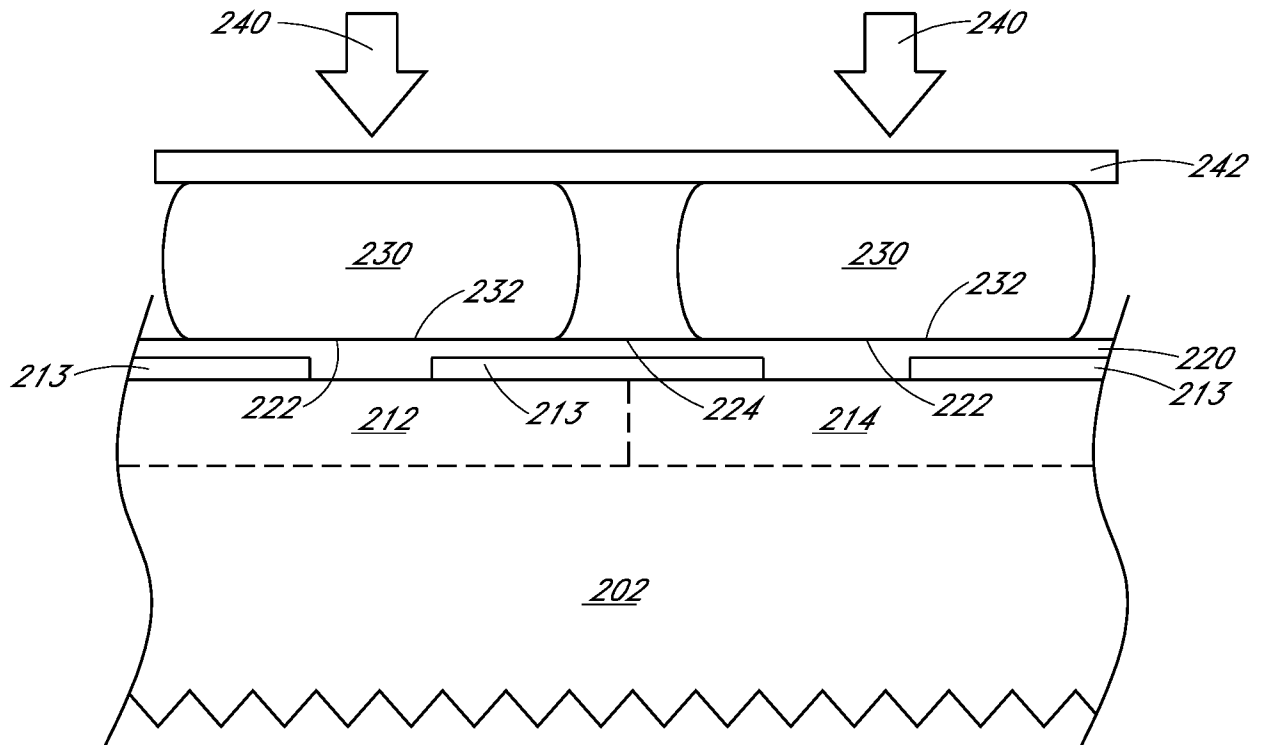


FIG. 4

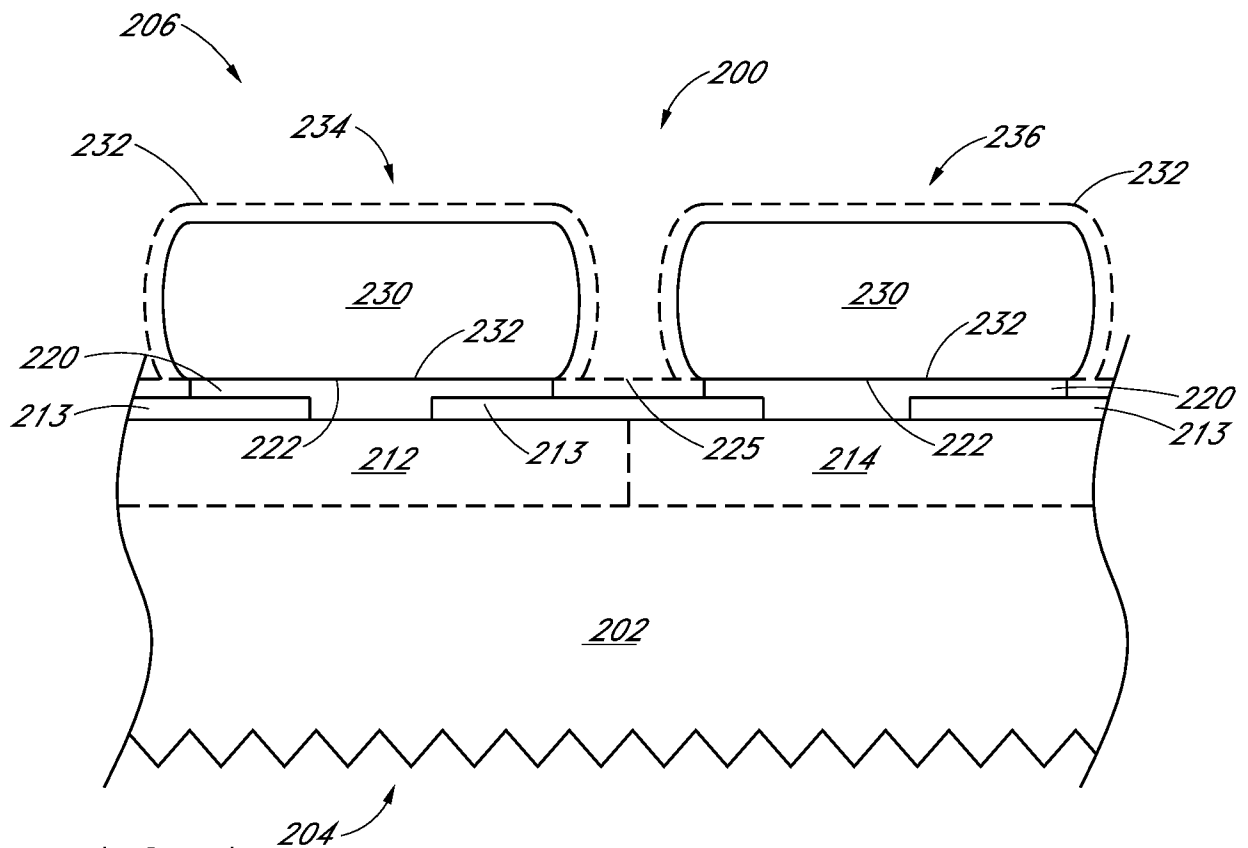
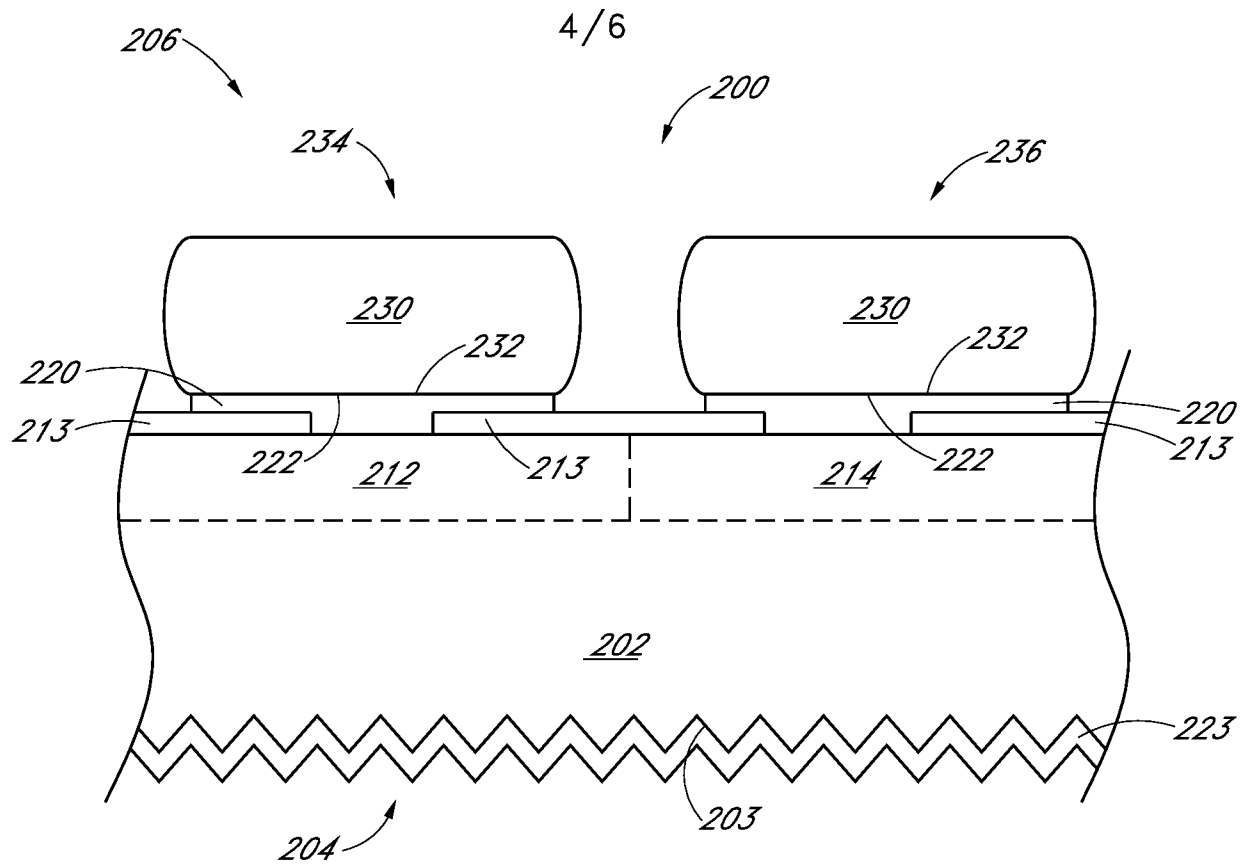
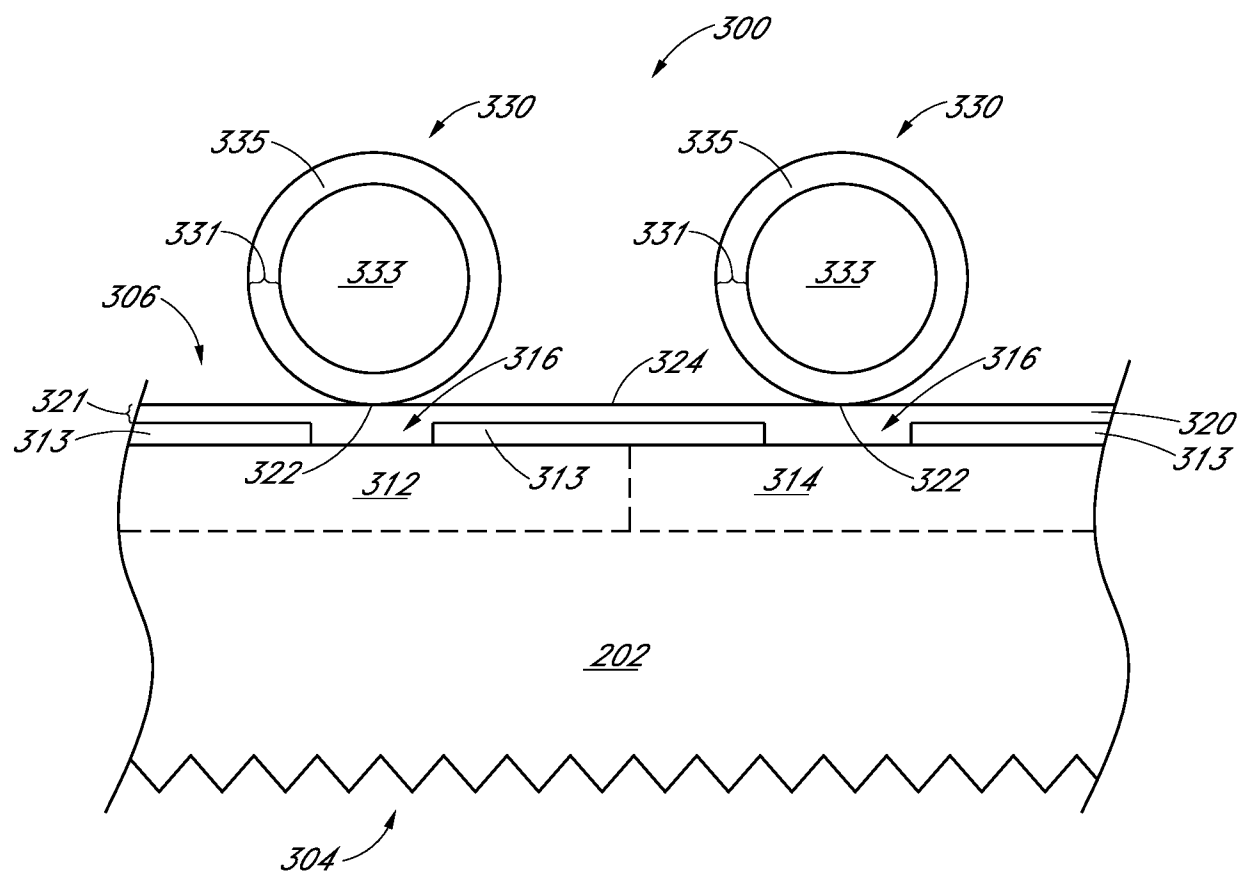


FIG. 5

**FIG. 6****FIG. 7**

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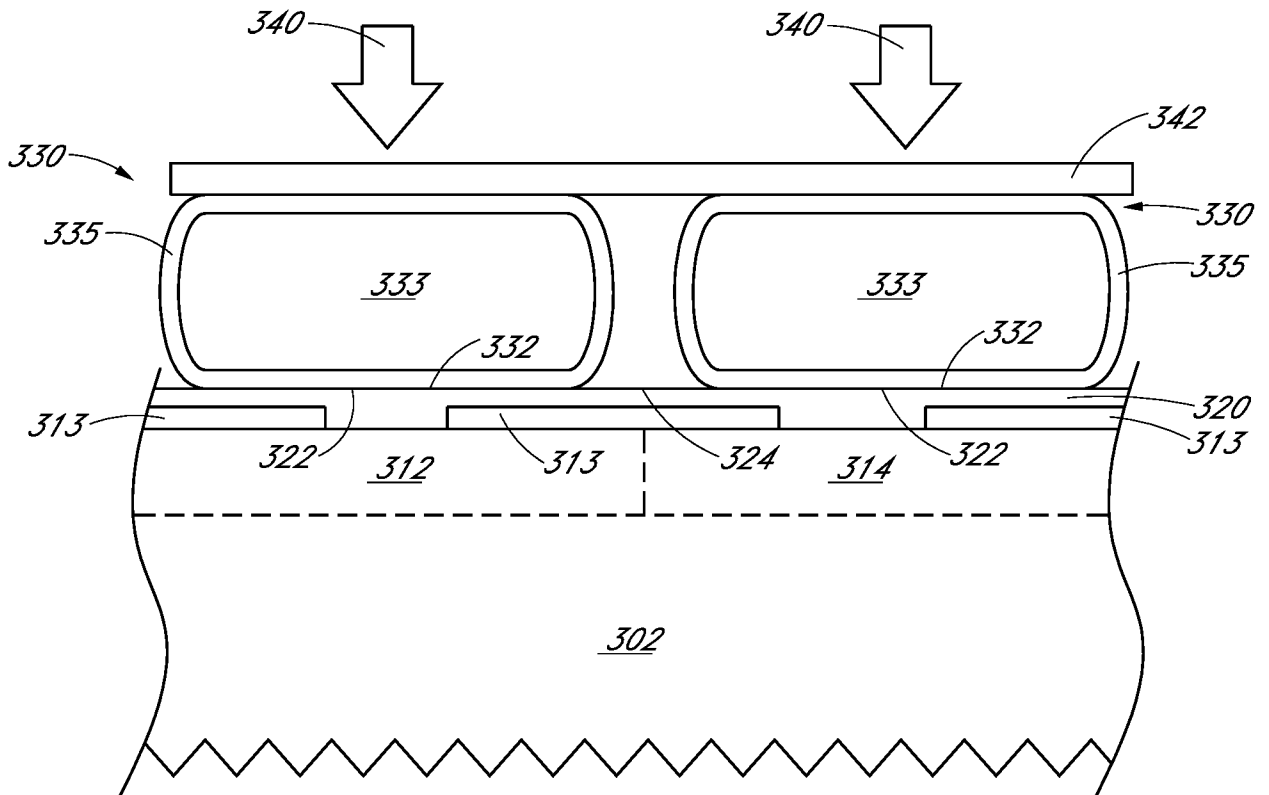


FIG. 8

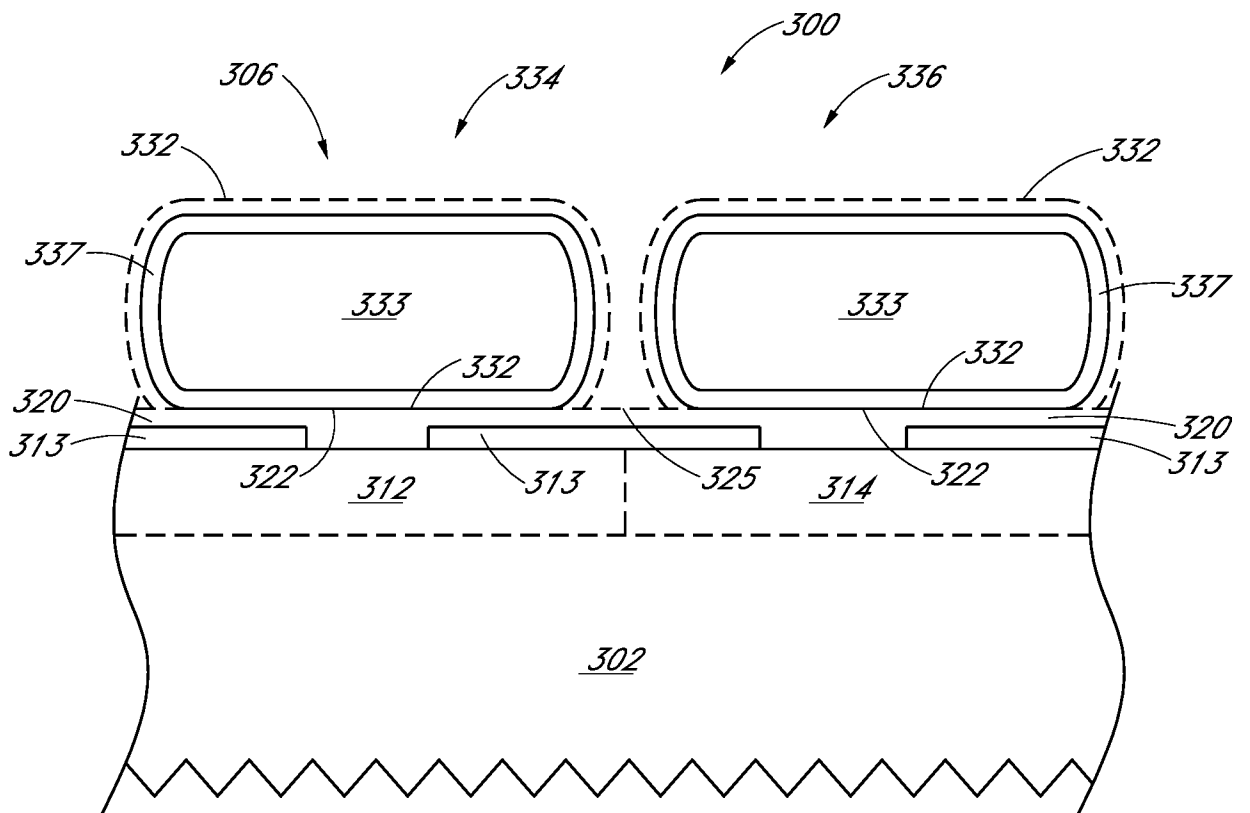


FIG. 9

304

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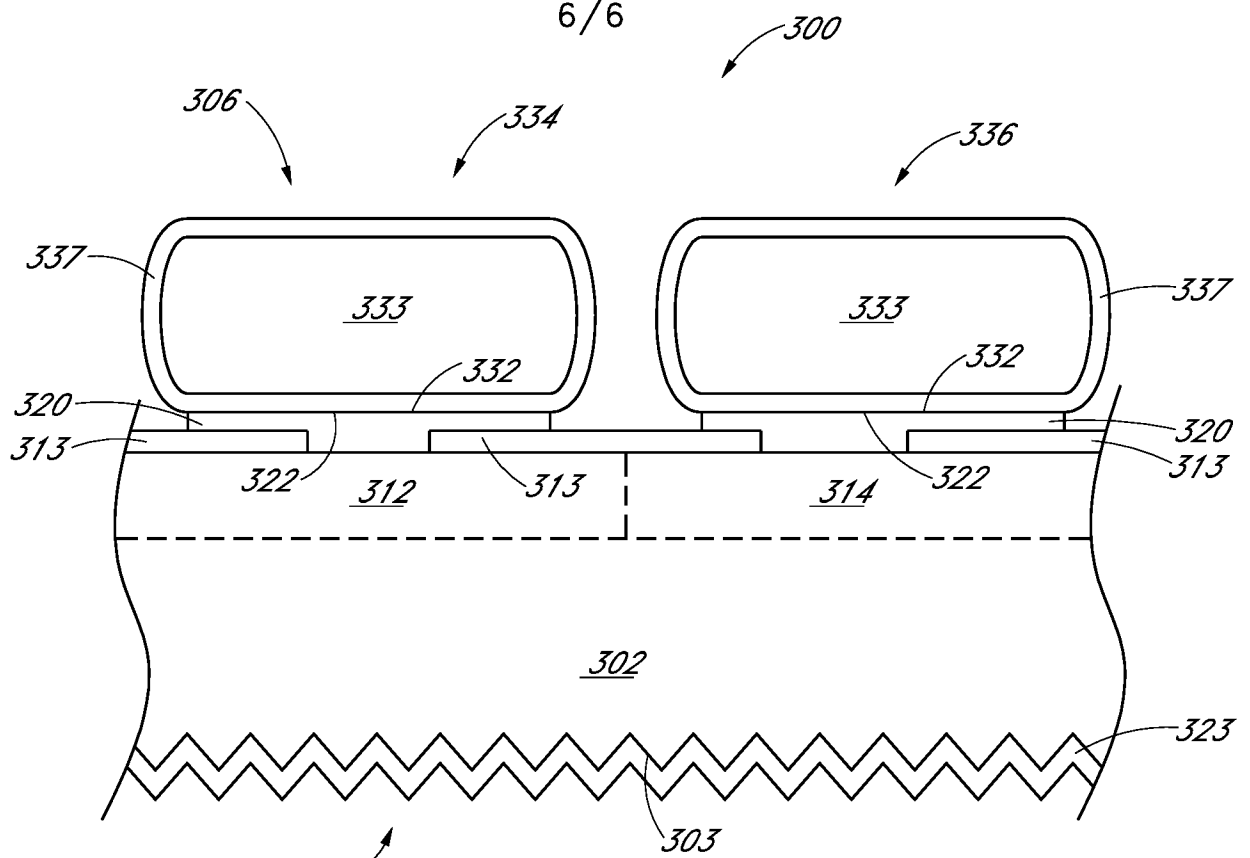


FIG. 10

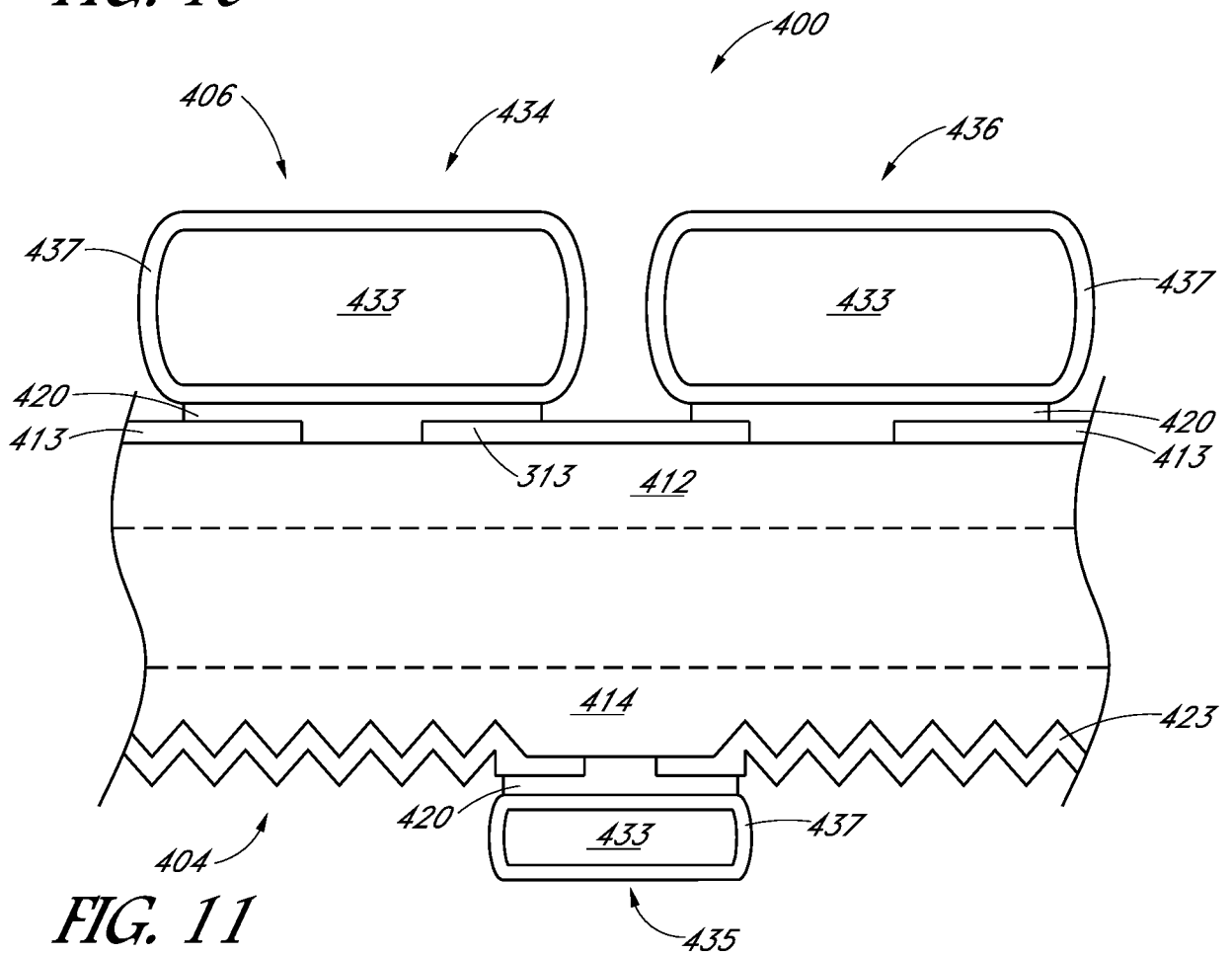


FIG. 11

A. CLASSIFICATION OF SUBJECT MATTER**H01L 31/18(2006.01)i, H01L 31/0216(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 31/18; B05D 5/12; H01L 218238; H01L 31/042; H01L 21/76; H01L 31/0216

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: solar cell, two semiconductor region, metal region, conductive strip, bonding, etching

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0051085 A1 (WEIDMAN TIMOTHY W. et al.) 04 March 2010 See paragraphs [0046]-[0055], [0076]-[0078], claims 1, 10 and figures 1A-3B, 12A-12B.	28-39
A		1-27
A	WO 2015-048197 A1 (SUNPOWER CORPORATION) 02 April 2015 See paragraphs [0032]-[0040], claims 1-2 and figures 1A-3.	1-39
A	US 6638833 B1 (OMAR VASSALLI et al.) 28 October 2003 See column 4, lines 48-54, claim 3 and figure 7.	1-39
A	US 2008-0299297 A1 (PETER JOHN COUSINS et al.) 04 December 2008 See paragraphs [0017]-[0021], [0027], claims 1-3 and figures 3A-3D.	1-39
A	US 6828187 B1 (JOYCE C. LIU et al.) 07 December 2004 See column 4, line 5 - column 5, line 57, claims 1-3 and figures 2-5.	1-39



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

14 December 2016 (14.12.2016)

Date of mailing of the international search report

15 December 2016 (15.12.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/051788

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