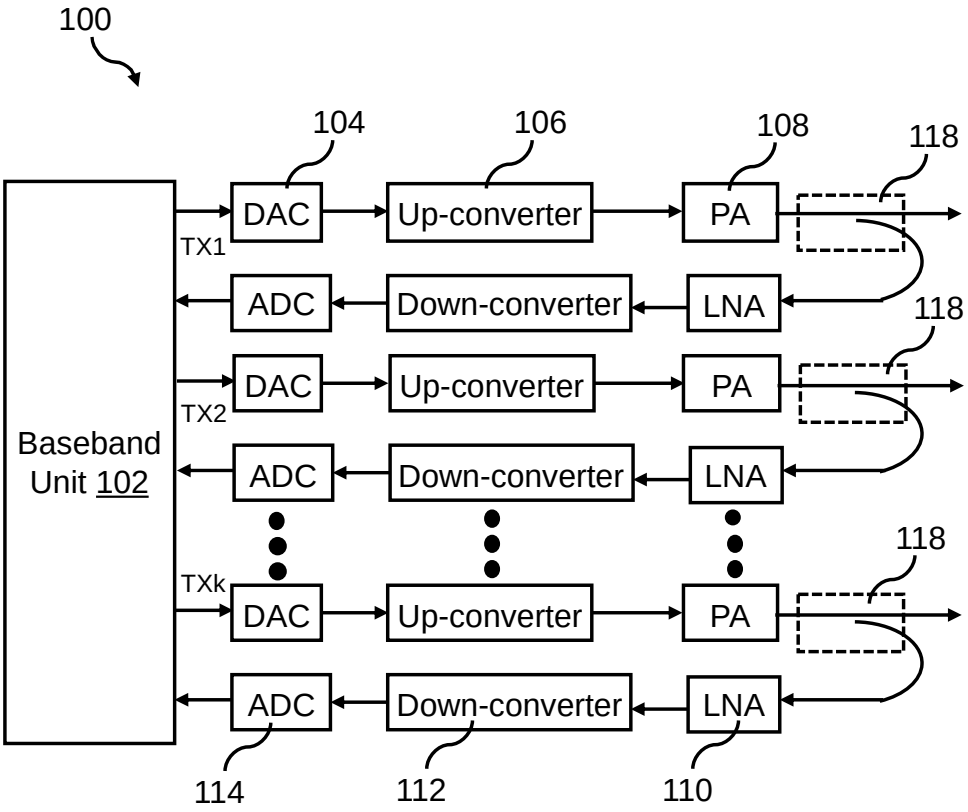

FIG. 1

Arun Kishore Narasani
Patent Agent (IN/PA 1049)

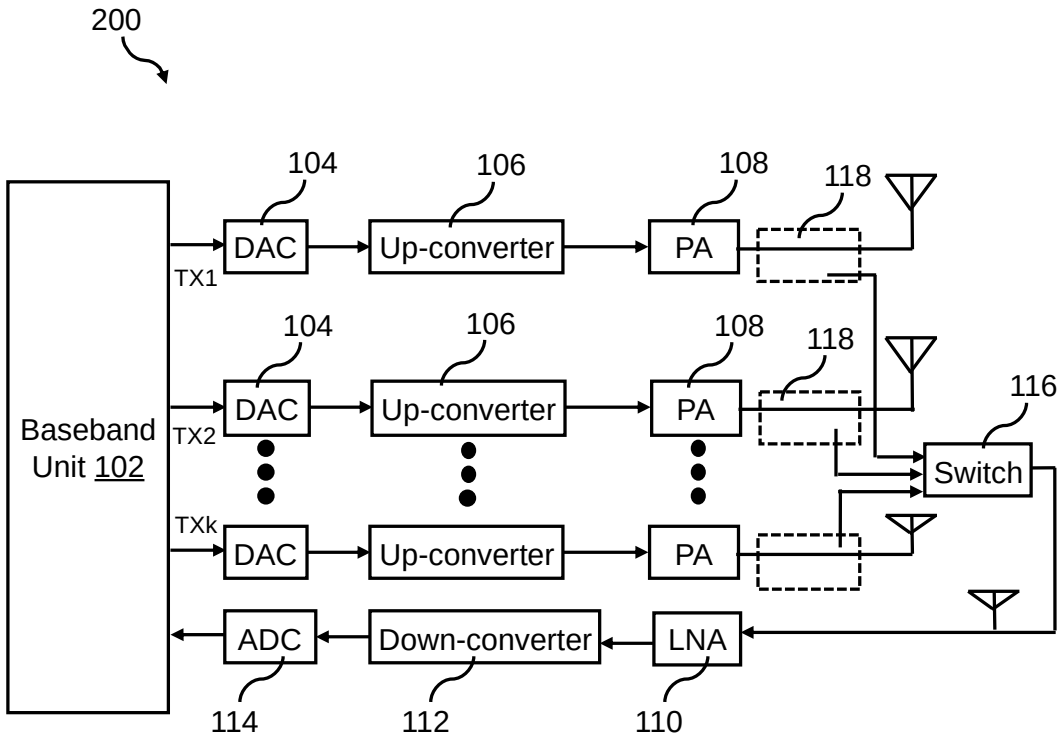

FIG. 2

Arun Kishore Narasani
Patent Agent (IN/PA 1049)

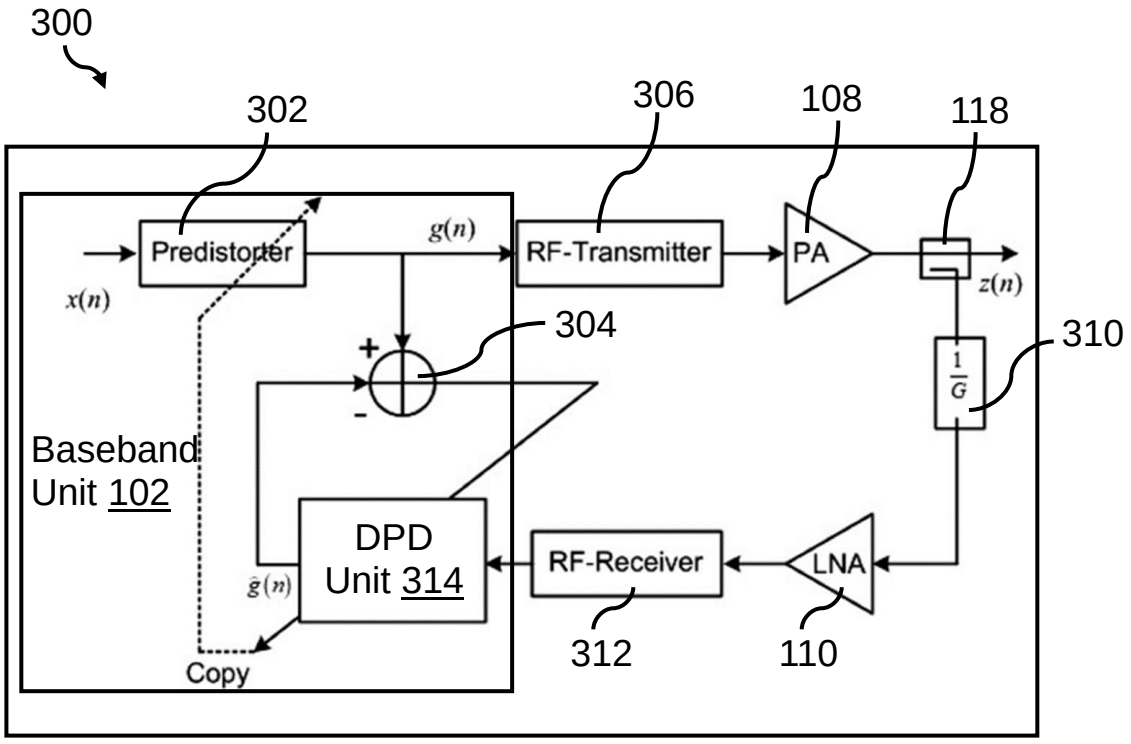

FIG. 3

Arun Kishore Narasani
Patent Agent (IN/PA 1049)

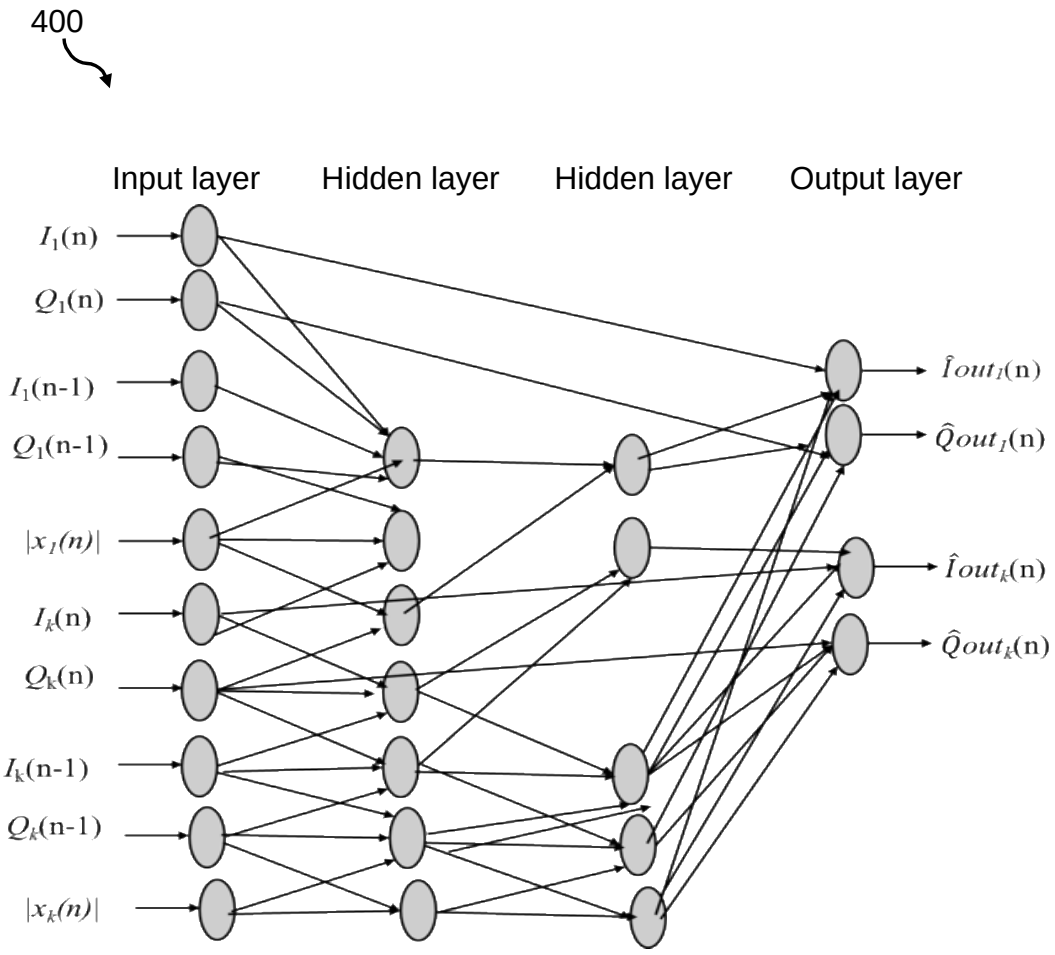

FIG. 4

Arun Kishore Narasani
Patent Agent (IN/PA 1049)

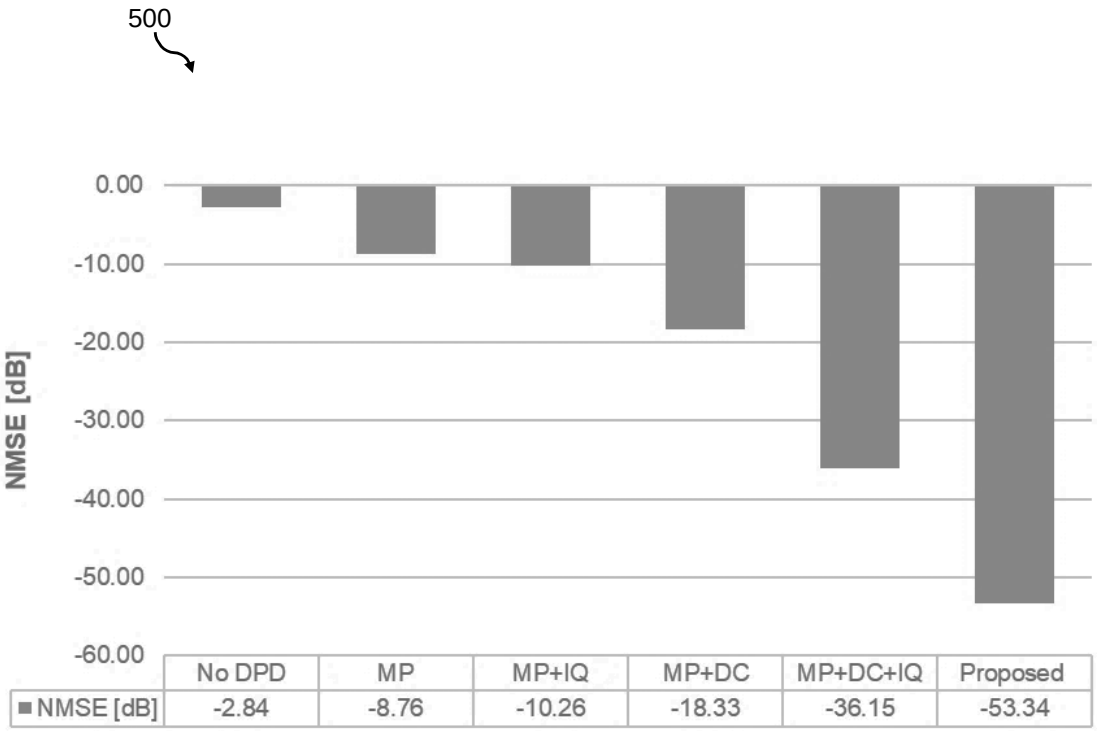

FIG. 5

Arun Kishore Narasani
Patent Agent (IN/PA 1049)

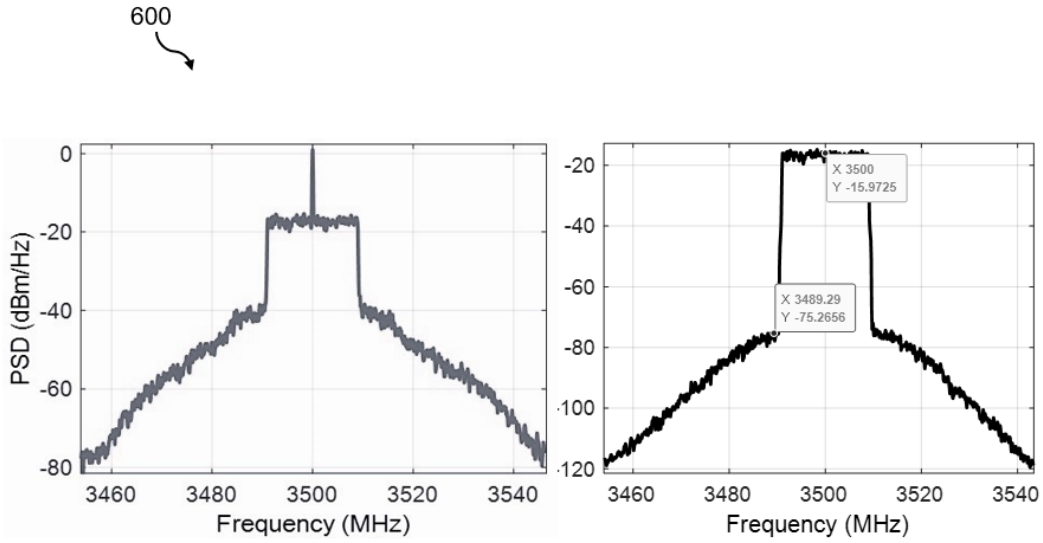

FIG. 6

Arun Kishore Narasani
Patent Agent (IN/PA 1049)

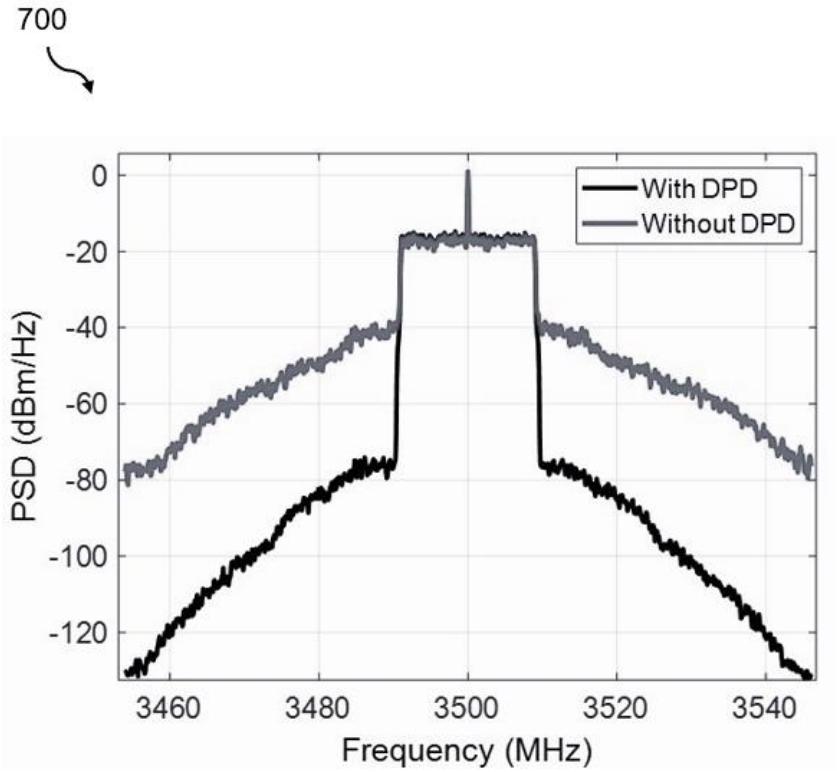

FIG. 7

Arun Kishore Narasani
Patent Agent (IN/PA 1049)

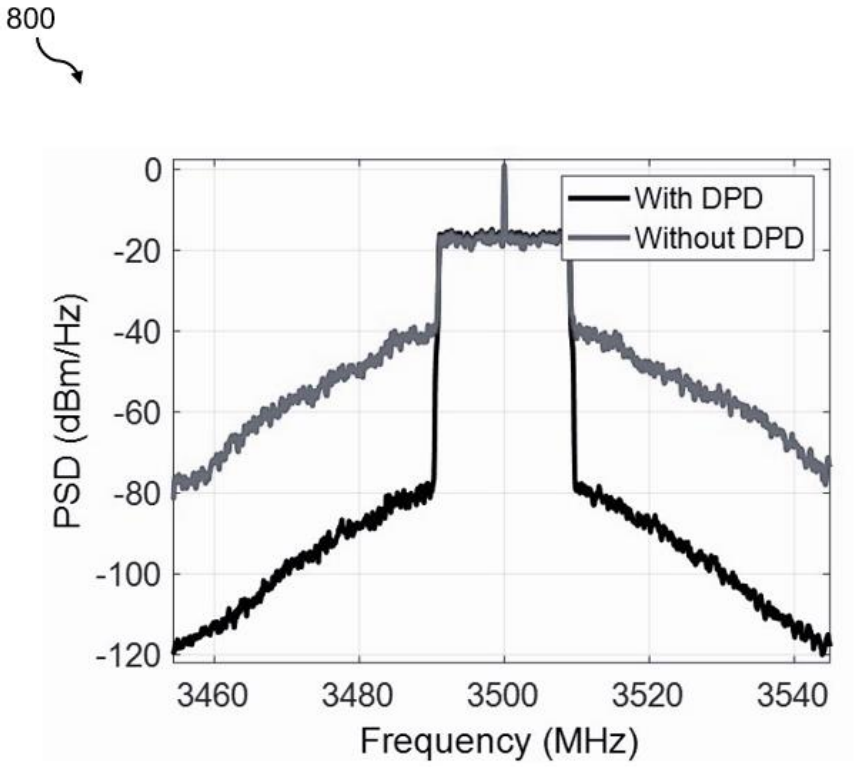

FIG. 8

Arun Kishore Narasani
Patent Agent (IN/PA 1049)

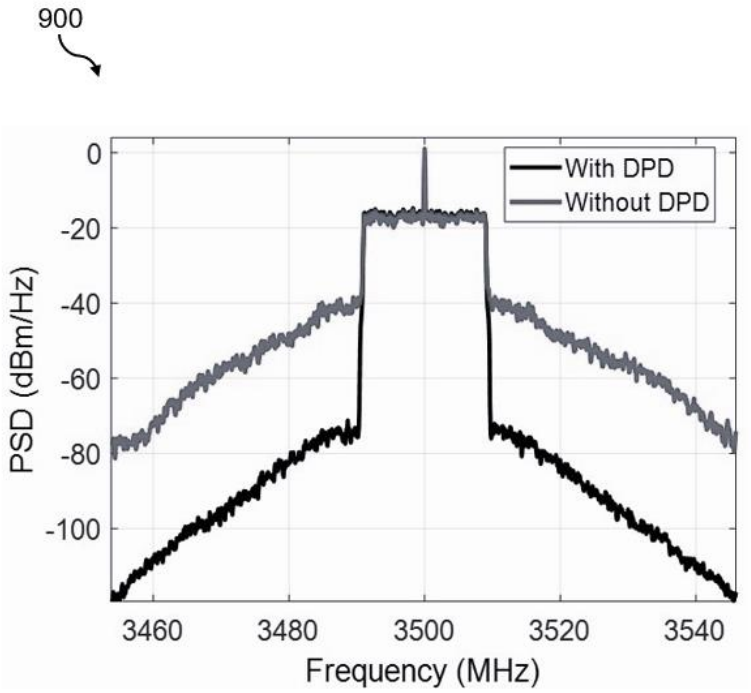

FIG. 9

Arun Kishore Narasani
Patent Agent (IN/PA 1049)

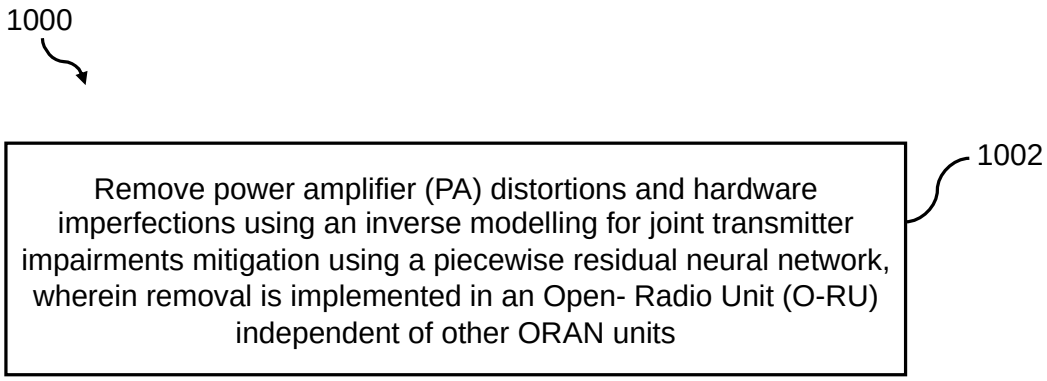

FIG. 10

Arun Kishore Narasani
Patent Agent (IN/PA 1049)

FORM 2

The Patent Act 1970

(39 of 1970)

&

The Patent Rules, 2003

COMPLETE SPECIFICATION

(SEE SECTION 10 AND RULE 13)

TITLE OF THE INVENTION

"HARDWARE IMPERFECTION MANAGEMENT FOR A RADIO UNIT IN AN OPEN RADIO ACCESS NETWORK"

APPLICANT:

Name : Sterlite Technologies Limited

Nationality : Indian

Address : 3rd Floor, Plot No. 3, IFFCO Tower,
Sector – 29, Gurugram, Haryana
122002

The following specification particularly describes the invention and the manner in which it is to be performed:

TECHNICAL FIELD

[0001] The present disclosure relates to radio units, and more specifically relates to hardware imperfection management for a radio unit in an Open Radio Access Network (O-RAN).

BACKGROUND

[0002] In radio units, power consumption can be very high due to radio-frequency power amplifiers (PAs). Moreover, a high peak-to-average power signal generated at the radio units imposes a strict linearity requirement on the radio-frequency power amplifiers (aka "power amplifiers"). PA nonlinearity is one of the major hardware impairments in the radio units, as it translates in-band errors and out-of-band emissions due to intermodulation and harmonic products. Therefore, it is required to operate the PAs in a saturation region for a higher efficiency, however, the PAs produces distortions. DC (Direct Current) offset and IQ (In-phase Quadrature) imbalance are another matter of concern in the radio units since it affects the performance of DPD. Therefore, it is essential to compensate for such distortions, DC offset, IQ imbalance or the like using signal processing techniques. An additional challenge arises in practice where there is often a large amount of missing data/signal, especially for multi-pollutant monitoring data of the radio units. Thus, a separate imputation step is required prior to dimension reduction. The PAs further exhibit memory effects during operation over large frequencies.

[0003] In order to address the aforesaid drawbacks, some of the prior art references are given below:

[0004] EP2538553A1 discloses a method and apparatus for mitigating impairments of a transmit signal due to transmitter imperfections. A neural network model is applied for mitigation of transmitter impairments of the transmit signal, such impairments being in particular the IQ imbalance due to an IQ up-conversion mixer in the transmit path of a transceiver, as well as nonlinearities due to a power amplifier (PA) in said transmit path.

[0005] US10833785B1 discloses a technique which is described with respect to 3GPP 5G-NR cellular systems. The technique uses a machine learning network approach to achieve improved performance while being able to handle hard to model impairments. The machine learning network helps in suppressing any non-linearities and distortion in the signal. The machine learning network is a neural network which uses a SWISH activation function.

[0006] US10581469B1 discloses integration of nonlinear pre-distortion machine learning model into a radio communication system for correcting radio signal distortion and interference. The nonlinear pre-distortion machine learning model may be a neural network, e.g., a deep neural network, a convolutional neural network, a recurrent neural network, or a combination of any of these types of neural networks. The radio communication system uses the nonlinear pre-distortion machine learning model to correct the radio signal distortion and interference prior to the radio signals being transmitted to the receiver.

[0007] A non-patent literature entitled “Low Complexity Joint Impairment Mitigation of I/Q Modulator and PA Using Neural Networks” discloses evaluation of the performance and complexity of impairment mitigation models for the direct conversion transceiver with multiple hardware impairments. The literature describes joint mitigation of nonlinear frequency dependent I/Q imbalance and PA nonlinearity using a shortcut real-valued time delay neural network (SVDEN) and a NN connection pruning algorithm to reduce complexity. The SVDEN compensates signal distortions caused by multiple hardware impairments, including PA nonlinearity and nonlinear frequency dependent I/Q imbalance. During the pruning process, the unimportant neural connections, i.e., those having weights with small magnitude, are gradually removed.

[0008] Another non-patent literature entitled “Swish Activation Based Deep Neural Network Predistorter for RF-PA” discloses linearization of radio frequency power amplifier using a deep neural network (DNN) for distortion compensation. The proposed DNN digital predistortion (DPD) uses Swish or Sigmoid-weighted linear unit activation function. The Swish function performs better than the ReLU in terms of linearization of the PA.

[0009] Yet another non-patent literature entitled “Augmented Iterative Learning Control for Neural-Network-Based Joint Crest Factor Reduction and Digital Predistortion of Power Amplifiers” discloses a new approach to realize a joint CFR and DPD model using neural networks (NN). The modeling accuracy is guaranteed by a new proposed augmented iterative learning control (AILC) algorithm for the NN training signals.

[0010] While the prior arts cover various approaches for hardware imperfection management for the radio units, however, the existing systems and techniques/methods are still limited by crosstalk, high power consumption, poor efficiency, large size and hardware complexity, high resource utilization or the like. Therefore, there is a scope of improvement.

OBJECT OF THE DISCLOSURE

[0011] A principal object of the present disclosure is to address the aforesaid drawbacks and to provide hardware imperfection/impairment management technique for a radio unit in an Open Radio Access Network (O-RAN) and the radio unit incorporating such hardware imperfection/impairment management technique.

[0012] Another object of the present disclosure is to remove power amplifier distortions and hardware imperfections for the radio unit (e.g., Frequency Range-1 (FR-1) radio unit and FR-2 radio unit, or the like) by using inverse modelling for joint transmitter impairments mitigation using a piecewise residual neural network.

SUMMARY

[0013] Accordingly, the present disclosure provides a hardware imperfection management method for an Open-Radio Unit (O-RU) in an Open Radio Access Network (O-RAN). The hardware imperfection management method comprises removing power amplifier (PA) distortions and hardware imperfections, wherein removal is implemented in the O-RU independent of other O-RAN units. The removing of the PA distortions and the hardware imperfections

is performed using inverse modelling for joint transmitter impairments mitigation using a piecewise residual neural network in a digital pre-distortion (DPD) unit.

[0014] The removing of the PA distortions and the hardware imperfections comprises estimating a digital pre-distortion (DPD) coefficient, by the DPD unit, from an input signal and an output signal using inverse modelling, wherein the DPD coefficient describes inverse behaviour of the PA, wherein the input signal is received at an antenna from the PA, wherein the output signal is output from the PA and eliminating the PA distortions and the hardware imperfections, by the DPD unit, based on the DPD coefficient to obtain a linear signal by using a predistortion signal, wherein the predistortion signal is generated by applying the DPD coefficient to the input signal.

[0015] The hardware imperfection management method comprises obtaining/receiving a trained network model with an optimum error, wherein the trained network model is trained by using the input signal and the output signal of the PA. The hardware imperfection management method further comprises applying the trained network model on the input signal and generating a predistorted signal, wherein the pre-distorted signal is an output of the trained network model and passing the predistorted signal through the PA by compensating for direct current (DC) offset, in-phase and quadrature-phase (IQ) imbalance, crosstalk and the power amplifier (PA) distortions.

[0016] These and other aspects herein will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following descriptions are given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the invention herein without departing from the spirit thereof.

BRIEF DESCRIPTION OF FIGURES

[0017] The invention is illustrated in the accompanying drawings, throughout which like reference letters indicate corresponding parts in the

drawings. The invention herein will be better understood from the following description with reference to the drawings, in which:

[0018] FIG. 1 illustrates a multiple receiver architecture for digital-predistortion.

[0019] FIG. 2 illustrates a single receiver architecture for digital-predistortion.

[0020] FIG. 3 represents an Open-Radio Unit (O-RU) implementing a digital-predistortion (DPD) technique for hardware imperfection management in an Open Radio Access Network (O-RAN).

[0021] FIG. 4 illustrates multiple fully connected layers of a piecewise residual neural network for digital-predistortion.

[0022] FIG. 5 is a graph depicting comparative results for inverse modelling.

[0023] FIG. 6 is an example graph depicting signal spectrum with and without DPD for a first radio frequency chain.

[0024] FIG. 7 is an example graph depicting signal spectrum with and without DPD for a second radio frequency chain.

[0025] FIG. 8 is an example graph depicting signal spectrum with and without DPD for a third radio frequency chain.

[0026] FIG. 9 is an example graph depicting signal spectrum with and without DPD for a fourth radio frequency chain.

[0027] FIG. 10 is a flow chart illustrating a method for hardware imperfection management for the O-RU in the O-RAN.

DETAILED DESCRIPTION

[0028] In the following detailed description of the invention, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be obvious to a person skilled in the art that the invention may be practiced with or without these specific details. In other instances, well known methods, procedures and components have not been described in details so as not to unnecessarily obscure aspects of the invention.

[0029] Furthermore, it will be clear that the invention is not limited to these alternatives only. Numerous modifications, changes, variations, substitutions and equivalents will be apparent to those skilled in the art, without parting from the scope of the invention.

[0030] The accompanying drawings are used to help easily understand various technical features and it should be understood that the alternatives presented herein are not limited by the accompanying drawings. As such, the present disclosure should be construed to extend to any alterations, equivalents and substitutes in addition to those which are particularly set out in the accompanying drawings. Although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are generally only used to distinguish one element from another.

[0031] Unlike existing systems and methods, the present disclosure provides a method to jointly remove power amplifier distortions and hardware imperfections/impairments of a radio unit in an open radio access network (O-RAN). The method uses a trained network model with an optimum error which is applied on an input signal to generate a pre-distorted signal. The pre-distorted signal is passed through a power amplifier for compensating hardware imperfections such as direct current (DC) offset, in-phase and quadrature-phase (IQ) imbalance, crosstalk and power amplifier (PA) distortions. That is, the method facilitates digital compensation of the hardware impairments of the radio unit.

[0032] Advantageously, the method used herein is purely a baseband method, hence can be implemented for FR-1 and FR-2 radio units and hence FR-1 radio unit can be software upgraded to FR-2 radio unit. The method used in the present disclosure is implemented in the radio unit and does not need any command from other units (like distributed unit and centralized unit) to save power of the radio unit and the O-RAN. Further, the radio unit described herein can be modified as per the need of MIMO (Multiple Input, Multiple Output), massive MIMO (mMIMO) and the O-RAN.

[0033] FIG. 1 illustrates a multiple receiver architecture (100) for digital-predistortion. The multiple receiver architecture (100) comprises a baseband unit (102), a plurality of digital to analog converters (DACs) (104), a plurality of up-converters (106), a plurality of power amplifiers (PA) (108), a plurality of low noise amplifiers (LNAs) (110), a plurality of down-converters (112), a plurality of analog to digital converters (ADCs) (114) and a plurality of couplers (118). The number of DACs, upconverters, PAs, LNAs, downconverters, ADCs and couplers depends upon the number of transmit-receive chains.

[0034] The baseband unit (102) receives an input signal coming from a frequency band to form a modulated signal. The additional details/working of the baseband unit (102) is explained below in conjunction with FIG. 3. Since the architecture is a multiple receiver architecture having multiple transmit-receive chains, the input signal is transmitted to each of the plurality of DACs (104) that converts a digital/modulated signal (i.e., the input signal) into an analog signal and the same is transmitted to respective up-converter (106). Each upconverter (106) upconverts an intermediate frequency signal (i.e., signal received from respective DAC) to a radio frequency and sends to the respective power amplifier (108). The power amplifier (108) converts a low-power radio-frequency signal into a higher-power signal and sends the same to the respective LNA (110) for further amplification through the respective coupler (118). The amplified signal from each LNA (110) is transmitted to respective downconverter (112) that down converts a beamformed antenna radio frequency signal to an intermediate frequency signal and forwards the down converted signal to the respective ADC (114) to convert the same from the analog signal to the digital signal and to further transmit the converted digital signal to the baseband unit (102).

[0035] FIG. 2 illustrates a single receiver architecture (200) for digital-predistortion. The single receiver architecture (200) comprises the baseband unit (102), the plurality of digital to analog converters (DACs) (104), the plurality of up-converters (106), the plurality of power amplifiers (PA) (108), a low noise amplifier (LNA) (110), a down-converter (112), an analog to digital converter (ADC) (114), a switch (116) and the plurality of couplers (118).

[0036] The baseband unit (102) receives the input signal coming from the frequency band to form the modulated signal. The additional details/working of the baseband unit (102) is explained below in conjunction with FIG. 3. Since the architecture is a single receiver architecture having single transmit-receive chain, the input signal is transmitted to each of the plurality of DACs (104) that converts a digital signal (i.e., the input signal) into an analog signal and the same is transmitted to respective upconverter (106). Each upconverter (106) upconverts an intermediate frequency signal (i.e., signal received from respective DAC) to a radio frequency and sends to the respective power amplifier (108). The power amplifier (108) converts a low-power radio-frequency signal into a higher-power signal and sends the same to the switch (116) through the respective coupler (118) from where the signal is transmitted to the LNA (110) for further amplification. The amplified signal from the LNA (110) is transmitted to the downconverter (112) that down converts a beamformed antenna radio frequency signal to an intermediate frequency signal and forwards the down converted signal to the ADC (114) to convert the same from analog signal to digital signal and to further transmit the converted digital signal to the baseband unit (102).

[0037] FIG. 3 represents an Open-Radio Unit (O-RU) (300) implementing a digital-predistortion (DPD) technique for hardware imperfection management in an Open Radio Access Network (O-RAN).

[0038] The O-RAN is a part of a telecommunications system which connects individual devices to other parts of a network through radio connections. The O-RAN provides a connection of user equipment (UE) such as mobile phone or computer with a core network of telecommunication systems. The O-RAN is an essential part of an access layer in the telecommunication systems which utilizes base stations (such as eNodeB, gNodeB) for establishing radio connections. The O-RAN is an evolved version of prior radio access networks, makes the prior radio access networks more open and smarter than previous generations. The O-RAN provides real-time analytics that drive embedded machine learning systems and artificial intelligence (AI) back end modules to empower network intelligence. Further, the O-RAN includes virtualized network elements with open

and standardized interfaces. Open interfaces are essential to enable smaller vendors and operators to quickly introduce their own services, or enables operators to customize the network to suit their own unique needs. Open interfaces also enable multivendor deployments, enabling a more competitive and vibrant supplier ecosystem. Similarly, open-source software and hardware reference designs enable faster, more democratic and permission-less innovation. Further, the O-RAN introduces a self-driving network by utilizing new learning-based technologies to automate operational network functions. These learning-based technologies make the O-RAN intelligent. Embedded intelligence, applied at both component and network levels, enables dynamic local radio resource allocation and optimizes network wide efficiency. In combination with O-RAN's open interfaces, Artificial intelligence (AI)-optimized closed-loop automation is a new era for network operations.

[0039] The O-RAN comprises the O-RU (300). The O-RU (300) is a logical node hosting a Low-PHY layer and RF (Radio Frequency) processing based on a lower layer functional split. This is similar to Third Generation Partnership Projects (3GPP's) "TRP (Transmission And Reception Point)" or "RRH (Remote Radio Head)" but more specific in including the Low-PHY layer (FFT/iFFT, PRACH (Physical Random Access Channel) extraction).

[0040] The O-RU (300) comprises the baseband unit (102), an RF (Radio Frequency) transmitter (306), a power amplifier (108), the coupler (118), a 1/G unit ("1/G") (310), the LNA (110), and an RF receiver (312).

[0041] The baseband unit (102) is a device that interprets baseband frequencies in the telecommunication systems including computer networks, the internet, phone networks and radio broadcasting systems. A baseband frequency is a transmission at its original frequency, before it has been altered or modulated, and it usually has a frequency range close to zero. The baseband unit (102) typically operates for frequency ranges (e.g., FR1 and FR2), where the FR1 defines bands in a sub-6 GHz spectrum (although 7125 MHz is the maximum) and the FR2 defines bands in a millimeter wave (mmWave) spectrum. Because of the

higher carrier frequencies in the FR2, it has a higher maximum bandwidth, where bandwidths include 5-100 MHz (FR1) and 50/100/200/400 MHz (FR2).

[0042] The baseband unit (102) comprises a pre-distorter (302), an adder (304) and a DPD (Digital Predistortion) unit (314).

[0043] The pre-distorter (302) receives an input signal (x(n)) to generate a pre-distorted signal (g(n)). The input signal is generated from the baseband that contains the current and past samples of cartesian I/Q components along with envelope-dependent terms.

[0044] The pre-distorter (302) performs a pre-distortion method, which aims to model an inverse of a non-linear response of the power amplifier (108). The pre-distorter (302) is placed before the power amplifier (108) such that the cascade of the pre-distorter (302) and the power amplifier (108) produces a linearly amplified signal.

[0045] The pre-distorted signal (g(n)) from the pre-distorter (302) is simultaneously transmitted to the adder (304) and the RF transmitter (306), where the RF transmitter (306) further transmits the radio frequency signal to the PA (108) to produce the linearly amplified signal. The outputs produced by the PA (108) are accurate copies of the input signal (generally at increased power levels). The linear signal is free from harmonic distortion or intermodulation distortion. Thereafter, the amplified signal from the PA (108) is transmitted to the coupler (118) and/or to an antenna (not shown). The signal z(n) from the coupler (118) is transmitted to the 1/G unit (310) to perform inverse gain to produce a low-power signal and the same is forwarded to the LNA (110) that amplifies the low-power signal without significantly degrading its signal-to-noise ratio. The amplified low-power signal from the LNA (110) is fed to the RF receiver (312) that transmits the same to the DPD unit (314).

[0046] Simultaneously, the signal from the adder (304) is also received by the DPD unit (314). The DPD unit (314) performs digital predistortion (DPD) that provides an effective way to linearize the PA (108). The DPD enables cost-efficient nonlinear PAs to run in their nonlinear regions with minimized distortions that results in higher output power and greater power efficiency. The

DPD of the signal preconditions is to correct hardware impairment(s) that the PA (108) introduces. In other words, by using the DPD, a linear signal is obtained, and the hardware imperfection(s) is eliminated. The hardware imperfection(s) comprises imperfections such as direct current (DC) offset, in-phase and quadrature-phase (IQ) imbalance, crosstalk, power amplifier (PA) nonlinearity, modulator imperfection, cross-modulation, and cross-over interference due to the multiple-frequency (multiband) and multiple-input/output transmission schemes.

[0047] Typically, the O-RU (300) suffers from the DC offset because of a local oscillator (LO) leakage, mixing of the LO signal with itself and noise from the mixers, filters, and DAC converters. The imperfections in an IQ modulator represent another important issue in the design of the baseband unit (102). The pre-distorted baseband signal is up converted to the RF using the IQ modulator. Phase and amplitude imbalances of the modulator affect the estimation of the pre-distorter coefficients. This problem motivates the joint compensation of the PA's nonlinear response and the distortion introduced in the up-conversion process. The latter distortion is due to phase and amplitude imbalances of the local oscillator (LO) and mismatch in the cascade of digital-analog converters (DAC) low-pass filters in the I and Q branches. The IQ imbalance distortions are described as static or dynamic. The static IQ imbalance introduces imaging effects to the output whereas dynamic IQ imbalance introduces phase and time misalignments. Further, in multi-antenna systems, the crosstalk is introduced between the different MIMO channels which affects severely the network performance. The crosstalk can be (a) after the transmitter antennas and (b) at the transmitter RF front-end (before PA). The crosstalk is the RF leakage that occurs due to poor isolation between the multiple transmission paths of a MIMO transmitter being implemented on the same chip-set. Furthermore, the nonlinearity in power amplifier generates spectral regrowth, which leads to adjacent channel interference and violations of the out-of-band emission requirements mandated by regulatory bodies. It also causes in-band distortion which degrades the bit error rate (BER) performance. To reduce the nonlinearity, the power amplifier can be backed off to operate within the linear portion of its operating curve.

[0048] The DPD unit (314) addresses the aforesaid hardware imperfections/impairments by removing of power amplifier (PA) distortions and hardware imperfections. The unwanted alterations generated during amplification is known as distortion. The removal of PA distortions and hardware imperfections is implemented in the O-RU (300) independent of other O-RAN units (e.g., distributed unit and centralized unit).

[0049] In order to remove the hardware imperfections and the PA distortions, the DPD unit (314) estimates a digital pre-distortion (DPD) coefficient from the input signal (x(n)) and an output signal from the PA (108) using inverse modelling, wherein the DPD coefficient describes inverse behaviour/replica of the PA (108), wherein the input signal is received at the antenna from the PA (108). Accordingly, the DPD unit (314) eliminates the PA distortions and the hardware imperfections based on the DPD coefficient to obtain a linear signal by using the predistortion signal. The predistortion signal is generated by applying the DPD coefficient to the input signal.

[0050] Further, the PA distortions and the hardware imperfections are removed by implementing inverse modelling for joint transmitter impairments mitigation using a piecewise residual neural network (400) (as shown in FIG. 4), where the DPD unit (314) obtains a trained network model with an optimum error that is trained by using the input signal and the output signal of the PA (108). The PA distortions and the hardware imperfections are removed by receiving the trained network model with the optimum error by using the input signal and the output signal. The trained network model is applied on the input signal and a pre-distorted signal is generated, wherein the pre-distorted signal is an output of the trained network model. Then, the pre-distorted signal is passed through the PA (108) by compensating for the direct current (DC) offset, the in-phase and quadrature-phase (IQ) imbalance, the crosstalk and the PA distortions.

[0051] Referring to the trained network model, the trained network model is obtained by applying one or more input signals to the piecewise residual neural network (400), without adding a memory term and/or by adding a memory term, wherein the piecewise residual neural network (400) requires feeding the input

signal and output signal to its network. The input signals, i.e. I & Q signals, can be separated and arranged for the nonlinearity of the PA (108) is given as:

$$X(n) = \begin{bmatrix} I_1(n), I_1(n-1) \ldots . I_k(n-m), I_k(n), Q_k(n) \\ Q_1(n), Q_1(n-1) \ldots . Q_k(n-m), Q_k(n)|x_k(n)| \end{bmatrix}$$

where I_k and Q_k are the I and Q components of the k_{th} transmitter, (n-m) is for memory terms, and m = memory element in the form of delay element.

[0052] The output signal is given as:

$$Y(n) = \begin{bmatrix} \hat{I}out_1(\mathrm{n}) \ldots \ldots \ldots \ldots \hat{I}out_k(\mathrm{n}) \\ \hat{Q}out_1(\mathrm{n}) \ldots \ldots \ldots . . \hat{Q}out_k(\mathrm{n}) \end{bmatrix}$$

[0053] The piecewise residual neural network (400) is trained by computation methods/procedures i.e., forward and backward propagation. In general, forward propagation means moving forward with provided input and weights (assumed in 1st run) till the output. And, backward propagation, as the name suggests, is moving from output to input. In backward propagation, the weights are reassigned based on the loss and then forward propagation runs. In terms of Neural Network, forward propagation is important as it helps to decide whether assigned weights are good to learn for the given problem statement. Similarly, the backward propagation is one of the important techniques for training the feed forward network, where after passing through forward network, output is predicted to compare with a target output.

[0054] Referring to the present disclosure, in the forward propagation, the input data is fed in forward direction through the piecewise residual neural network (400), where each hidden layer accepts the input signal (or data), processes the same as per an activation function, and passes to a successive layer. The successive layer comprises the in-phase and quadrature components (I/Q) of the complex baseband samples. The I/Q samples are also fed directly without using any memory element for direct connection to corresponding the linear region of the PA (108), and the amplitudes of the I/Q samples up to the mth power are fed as an input to account for the nonlinearity of the PA (108).

$$y(n) = f(x(n)_{DC/IQ} \ldots\ldots f(x(n)_{PA}$$

[0055] In the forward propagation (i.e., feedforward computation), the data/signal is propagated from neurons of a lower layer to an upper layer, using two layers, where a net input in layer l+1 is given as:

$$net_j^{l+1} = \sum_{i=1}^{q} w_{ji}^{l+1} o_i^l + b_j^{l+1}$$

where w_{ji}^{l+1} represents a synaptic weight between an ith input from a previous layer to a jth neuron of a present layer.

[0056] Alternatively, in the backward propagation, fine-tuning of weights of the piecewise residual neural network (400) is performed based on error rate (i.e., loss) obtained in the previous epoch (i.e., iteration), where a proper tuning of the weights ensures lower error rates, making the model reliable by increasing its generalization and where a performance index (E) for the trained network model is calculated as:

$$E = \frac{1}{2N}\sum_{n=1}^{N}\left[\left[\hat{I}out_I(\mathrm{n}) - \hat{I}out_I(\mathrm{n})\right]^2 + \left[\hat{Q}out_1(\mathrm{n}) - \hat{Q}out_I(\mathrm{n})\right]^2\right] + \cdots \frac{1}{2N}\sum_{}^{N}\left[\left[\hat{I}out_{\mathrm{k}}(\mathrm{n}) - \hat{I}out_k(\mathrm{n})\right]^2 + \left[\hat{Q}out_{\mathrm{k}}(\mathrm{n}) - \hat{Q}out_k(\mathrm{n})\right]^2\right] \quad (20)$$

$$E = \frac{1}{2N}\sum_{n=1}^{N} e_n^T\, e$$

where e is an error, $I_{outk}(n)$, and $Q_{outk}(n)$ are an actual baseband output of a kth transmitter branch of MIMO system, $\hat{I}out_k(n)$ and $\hat{Q}out_I(n)$ are the I and Q components of the outputs from output-layer neurons of the piecewise residual neural network (400).

[0057] The activation function decides whether a neuron should be activated or not by calculating weighted sum and further adding bias with it. The purpose of the activation function is to introduce non-linearity into the output of a

neuron. The activation function is called Flatten-T Swish (FTS), which is activated for hindering negative values from propagating through the piecewise residual neural network (400) and for activating the neurons. The activation function calculates a weighted sum of its input, adds a bias, and then decides whether the function should be activated or not. In other words, the FTS function is activated to calculate the weighted sum of its input, add the bias, and then decide whether it should be activated or not. A threshold value (T) is added to the FTS that is a cut-off value of the activation function (or function, i.e., FTS).

$$FTS(x) = \begin{Bmatrix} \frac{x}{1+e^{-x}} + T, \; x \geq 0 \\ T, \; x < 0 \end{Bmatrix}$$

[0058] The proposed DPD technique/method can also be implemented in a Single Input Single Output (SISO) system and multiple-input and multiple-output (MIMO) system. In the SISO system, a single antenna is used for transmission and reception. SISO is typically used in radio, satellite, Global System for Mobile communication (GSM) and Code-division multiple access (CDMA) systems. The antennas perform the activity of both transmitting and receiving the signal in order to establish the datalink. Similarly, in the MIMO system, multiple antennas are used for transmission and reception. The MIMO system achieves much higher data rates because of a technique used to transmit data simultaneously across multiple antennas. This technique is called spatial multiplexing. The use of multiple antennas in the MIMO system provides other benefits. The ability to make use of multiple antennas, each one at a slight angle, provides increased performance and resilience.

[0059] FIG. 4 illustrates multiple fully connected layers of the piecewise residual neural network (400) for the digital-predistortion in conjunction with FIG. 3. The piecewise residual neural network (400) comprises an input layer, a plurality of hidden layers and an output layer, where the input layer receives the in-phase and quadrature components (I/Q) of the complex baseband samples as an input. The I/Q samples are also fed directly without using any memory element for direct connection to correspond the linear region of the PA (108). Also, the

amplitudes of the I/Q samples up to the kth power are also fed as an input to account for the nonlinearity of the PA (108) as depicted in FIG. 4. The inputs and outputs for the piecewise residual neural network (400) are already described above, hence are not described again to avoid redundancy. Further, the piecewise residual neural network (400) acts as a universal approximator and hence the same can be used to model any DPD case.

[0060] FIG. 5 is a graph (500) depicting comparative results for inverse modelling used in the DPD unit (314). The graphs show the proposed method outperform the other methods since the NMSE is -53.34 dB.

[0061] FIG. 6 is an example graph (600) depicting signal spectrum with and without DPD for a first radio frequency chain (Chain-1). FIG. 7 is an example graph (700) depicting signal spectrum with and without DPD for a second radio frequency chain (Chain-2). FIG. 8 is an example graph (800) depicting signal spectrum with and without DPD for a third radio frequency chain (Chain-3). FIG. 9 is an example graph (900) depicting signal spectrum with and without DPD for a fourth radio frequency chain (Chain-4). The below Table 1 depicts a comparative result for all the example radio frequency chains, where an NMSE (normalized mean square error) is used to analyze the accuracy for the proposed methods by quantifying the difference between the measured and desired output and an ACPR (adjacent channel power ratio) is used to analyze the power of the measured output leaking into the adjacent channels due to the nonlinear behavior of the device under test (e.g., PA (108)).

Chain Number	**NMSE (dB)**		**ACPR (dBc)**		**Imbalance**
	Without DPD	**With DPD**	**Without DPD**	**With DPD**	**Gain [dB] /Phase [Deg.] /DC[dB]**
Chain-1	-2.84	-53.72	-23.01	-59.29	2/5/-20
Chain-2	-2.20	-54.50	-32.48	-60.69	1/5/-20
Chain-3	-3.77	52.53	-24.0126	-60.84	3/5/-20

Chain-4	-1.98	-53.9713	-22.50	-60.01	1/4/-20

Table 1

[0062] FIG. 10 is a flow chart (1000) illustrating a method for hardware imperfection management for the O-RU (300) in the O-RAN (ORAN). At step 1002, the method includes removing the power amplifier (PA) distortions and the hardware imperfections, wherein removal is implemented in the O-RU (300) independent of other O-RAN units. The power amplifier (PA) distortions and the hardware imperfections are removed by using the inverse modelling for joint transmitter impairments mitigation using the piecewise residual neural network (400).

[0063] The proposed disclosure facilitates power saving in the O-RU (300) because the O-RU (300) performs the proposed method independently and does not dependent on other O-RAN units (such as O-DU, O-CU). Due to implementation of the proposed method, the FR-1 range products can easily be software upgraded to the FR-2 range products. Further, the proposed method can be modified as per the need of MIMO and massive MIMO and can be extended to long term memory case.

[0064] The various actions, acts, blocks, steps, or the like in the flow chart (1000) may be performed in the order presented, in a different order or simultaneously. Further, in some implementations, some of the actions, acts, blocks, steps, or the like may be omitted, added, modified, skipped, or the like without departing from the scope of the invention.

[0065] The embodiments disclosed herein can be implemented using at least one software program running on at least one hardware device and performing network management functions to control the elements.

[0066] It will be apparent to those skilled in the art that other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention. While the foregoing written description of the invention enables one of ordinary skill to make and use what is considered presently to be the best mode thereof, those of

ordinary skill will understand and appreciate the existence of variations, combinations, and equivalents of the specific embodiment, method, and examples herein. The invention should therefore not be limited by the above described embodiment, method, and examples, but by all embodiments and methods within the scope of the invention. It is intended that the specification and examples be considered as exemplary, with the true scope of the invention being indicated by the claims.

[0067] The methods and processes described herein may have fewer or additional steps or states and the steps or states may be performed in a different order. Not all steps or states need to be reached. The methods and processes described herein may be embodied in, and fully or partially automated via, software code modules executed by one or more general purpose computers. The code modules may be stored in any type of computer-readable medium or other computer storage device. Some or all of the methods may alternatively be embodied in whole or in part in specialized computer hardware.

[0068] The results of the disclosed methods may be stored in any type of computer data repository, such as relational databases and flat file systems that use volatile and/or non-volatile memory (e.g., magnetic disk storage, optical storage, EEPROM and/or solid state RAM).

[0069] The various illustrative logical blocks, modules, routines, and algorithm steps described in connection with the embodiments disclosed herein can be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. The described functionality can be implemented in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the disclosure.

[0070] Moreover, the various illustrative logical blocks and modules described in connection with the embodiments disclosed herein can be implemented or performed by a machine, such as a general-purpose processor device, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components or any combination thereof designed to perform the functions described herein. A general-purpose processor device can be a microprocessor, but in the alternative, the processor device can be a controller, microcontroller, or state machine, combinations of the same, or the like. A processor device can include electrical circuitry configured to process computer-executable instructions. In another embodiment, a processor device includes an FPGA or other programmable device that performs logic operations without processing computer-executable instructions. A processor device can also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. Although described herein primarily with respect to digital technology, a processor device may also include primarily analog components. A computing environment can include any type of computer system, including, but not limited to, a computer system based on a microprocessor, a mainframe computer, a digital signal processor, a portable computing device, a device controller, or a computational engine within an appliance, to name a few.

[0071] The elements of a method, process, routine, or algorithm described in connection with the embodiments disclosed herein can be embodied directly in hardware, in a software module executed by a processor device, or in a combination of the two. A software module can reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of a non-transitory computer-readable storage medium. An exemplary storage medium can be coupled to the processor device such that the processor device can read information from, and write information to, the storage medium. In the alternative,

the storage medium can be integral to the processor device. The processor device and the storage medium can reside in an ASIC. The ASIC can reside in a user terminal. In the alternative, the processor device and the storage medium can reside as discrete components in a user terminal.

[0072] Conditional language used herein, such as, among others, "can", "may", "might", "may", “e.g.”, and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain alternatives include, while other alternatives do not include, certain features, elements and/or steps. Thus, such conditional language is not generally intended to imply that features, elements and/or steps are in any way required for one or more alternatives or that one or more alternatives necessarily include logic for deciding, with or without other input or prompting, whether these features, elements and/or steps are included or are to be performed in any particular alternative. The terms “comprising,” “including,” “having,” and the like are synonymous and are used inclusively, in an open-ended fashion, and do not exclude additional elements, features, acts, operations, and so forth. Also, the term “or” is used in its inclusive sense (and not in its exclusive sense) so that when used, for example, to connect a list of elements, the term “or” means one, some, or all of the elements in the list.

[0073] Disjunctive language such as the phrase “at least one of X, Y, Z,” unless specifically stated otherwise, is otherwise understood with the context as used in general to present that an item, term, etc., may be either X, Y, or Z, or any combination thereof (e.g., X, Y, and/or Z). Thus, such disjunctive language is not generally intended to, and should not, imply that certain alternatives require at least one of X, at least one of Y, or at least one of Z to each be present.

[0074] While the detailed description has shown, described, and pointed out novel features as applied to various alternatives, it can be understood that various omissions, substitutions, and changes in the form and details of the devices or algorithms illustrated can be made without departing from the scope of the disclosure. As can be recognized, certain alternatives described herein can be

embodied within a form that does not provide all of the features and benefits set forth herein, as some features can be used or practiced separately from others.

CLAIMS

We Claim:

1. A hardware imperfection management method for an Open-Radio Unit (O-RU) (300) in an Open Radio Access Network (O-RAN), the hardware imperfection management method comprising:

removing power amplifier (PA) distortions and hardware imperfections, wherein removal is implemented in the O-RU (300) independent of other O-RAN units.

2. The hardware imperfection management method as claimed in claim 1, wherein removing of the PA distortions and the hardware imperfections is performed using inverse modelling for joint transmitter impairments mitigation using a piecewise residual neural network (400) in a digital pre-distortion (DPD) unit (314).

3. The hardware imperfection management method as claimed in claim 1, wherein the O-RU (300) belongs to at least one of a Frequency Range-1 (FR-1) and a Frequency Range-2 (FR-2).

4. The hardware imperfection management method as claimed in claim 1, wherein removing of the PA distortions and the hardware imperfections comprises:

estimating a digital pre-distortion (DPD) coefficient, by the DPD unit (314), from an input signal and an output signal using inverse modelling, wherein the DPD coefficient describes inverse behaviour of a PA (108), wherein the input signal is received at an antenna from the PA (108), wherein the output signal is output from the PA (108); and

eliminating the PA distortions and the hardware imperfections, by the DPD unit (314), based on the DPD coefficient to obtain a linear signal by using a

predistortion signal, wherein the predistortion signal is generated by applying the DPD coefficient to the input signal.

5. The hardware imperfection management method as claimed in claim 1, wherein the hardware imperfection management method comprises:

obtaining a trained network model with an optimum error, wherein the trained network model is trained by using an input signal of a PA (108) and an output signal of the PA (108).

6. The hardware imperfection management method as claimed in claim 5, wherein obtaining the trained network model comprises:

applying one or more input signals to a piecewise residual neural network (400) by at least one of without adding a memory term and adding the memory term, wherein the piecewise residual neural network (400) requires feeding the input signal and the output signal to its network,

wherein the input signal is an I and Q (in-phase and quadrature) signal that is separated and arranged for nonlinearity of the PA (108), the input signal is given as:

$$X(n) = \begin{bmatrix} I_1(n), I_1(n-1) \ldots . I_k(n-m), I_k(n), Q_k(n) \\ Q_1(n), Q_1(n-1) \ldots . Q_k(n-m), Q_k(n)|x_k(n)| \end{bmatrix}$$

where I_k and Q_k are I and Q components of k_{th} transmitter, (n-m) is for memory terms, and m is a memory element in the form of delay element.

wherein the output signal is given as:

$$Y(n) = \begin{bmatrix} \hat{I}out_1(\mathrm{n}) \ldots \ldots \ldots \ldots \hat{I}out_k(\mathrm{n}) \\ \hat{Q}out_1(\mathrm{n}) \ldots \ldots \ldots \ldots \hat{Q}out_k(\mathrm{n}) \end{bmatrix}$$

7. The hardware imperfection management method as claimed in claim 6, wherein applying the one or more input signals to the piecewise residual neural network (400) comprises:

training the piecewise residual neural network (400) by at least one of a forward propagation and a backward propagation, wherein in the forward propagation, the input signal is fed in a forward direction through the piecewise residual neural network (400), wherein each hidden layer accepts the input signal, processes the input signal as per an activation function, and passes the input signal to a successive layer, wherein in the backward propagation, fine-tuning of weights of the piecewise residual neural network (400) is performed based on an error rate obtained in a previous epoch;

activating a Flatten-T Swish (FTS) function for hindering negative values from propagating through the piecewise residual neural network (400), wherein the activation function calculates a weighted sum of its input, adds a bias, and determines whether to be activated or not; and

adding a threshold value to the FTS, wherein the threshold value is a cut-off value of the activation function.

8. The hardware imperfection management method as claimed in claim 7, wherein the successive layer comprises in-phase and quadrature samples, wherein the in-phase and quadrature samples are fed directly without using a memory element for direct connection to corresponding linear region of the PA (108), and amplitudes of the in-phase and quadrature samples up to m^{th} power are fed as an input to account for the nonlinearity of the PA (108):

$$y(n) = f(x(n)_{DC/IQ} \ldots\ldots f(x(n)_{PA}$$

9. The hardware imperfection management method as claimed in claim 7, wherein the forward propagation comprises:

propagating the input signal from neurons of a lower layer to an upper layer, using two layers, where a net input in layer l+1 is given as:

$$net_j^{l+1} = \sum_{i=1}^{q} w_{ji}^{l+1} o_i^l + b_j^{l+1}$$

where w_{ji}^{l+1} represents a synaptic weight between an ith input from a previous layer to a jth neuron of a present layer.

10. The hardware imperfection management method as claimed in claim 7, wherein the backward propagation comprises:

fine-tuning the weights of the piecewise residual neural network (400) based on the previously obtained error rate, where a performance index for the trained network model is calculated as:

$$E = \frac{1}{2N}\sum_{n=1}^{N}\left[\left[\hat{I}out_{I}(\mathrm{n}) - \hat{I}out_{I}(\mathrm{n})\right]^{2} + \left[\hat{Q}out_{1}(\mathrm{n}) - \hat{Q}out_{I}(\mathrm{n})\right]^{2}\right] + \cdots 10$$
$$\frac{1}{2N}\sum_{}^{N}\left[\left[\hat{I}out_{\mathrm{k}}(\mathrm{n}) - \hat{I}out_{k}(\mathrm{n})\right]^{2} + \left[\hat{Q}out_{\mathrm{k}}(\mathrm{n}) - \hat{Q}out_{k}(\mathrm{n})\right]^{2}\right]$$

$$E = \frac{1}{2N}\sum_{n=1}^{N} e_n^T\, e$$

where e is an error, $I_{outk}(n)$, and $Q_{outk}(n)$ are an actual baseband output of kth transmitter branch of a MIMO (multiple-input and multiple-output) system, $\hat{I}out_k(n)$ and $\widehat{Q}out_1(n)$ are the I and Q components of outputs from output-layer neurons of the piecewise residual neural network (400).

11. The hardware imperfection management method as claimed in claim 7, wherein activating the Flatten-T Swish (FTS) function comprises activating neurons and adding threshold value (T) to the FTS as given below:

$$FTS(x) = \begin{cases} \dfrac{x}{1+e^{-x}} + T, & x \geq 0 \\ T, & x < 0 \end{cases}$$

12. The hardware imperfection management method as claimed in claim 1, wherein the hardware imperfection management method comprises:

receiving a trained network model with an optimum error by using an input signal and an output signal;

applying the trained network model on the input signal and generating a predistorted signal, wherein the pre-distorted signal is an output of the trained network model; and

passing the predistorted signal through a PA (108) by compensating for direct current (DC) offset, in-phase and quadrature-phase (IQ) imbalance, crosstalk and the power amplifier (PA) distortions.

13. An Open-Radio Unit (O-RU) (300), comprising:

a digital pre-distortion (DPD) unit (314) configured to:

remove power amplifier (PA) distortions and hardware imperfections, wherein removal of the PA distortions and the hardware imperfections is performed using inverse modelling for joint transmitter impairments mitigation using a piecewise residual neural network (400) in the DPD unit (314).

14. The O-RU) (300) as claimed in claim 13, wherein removal of the PA distortions and the hardware imperfections comprises:

estimate a digital pre-distortion (DPD) coefficient, by the DPD unit (314), from an input signal and an output signal using inverse modelling, wherein the DPD coefficient describes inverse behaviour of a PA (108), wherein the input signal is received at an antenna from the PA (108), wherein the output signal is output from the PA (108); and

eliminate the PA distortions and the hardware imperfections, by the DPD unit (314), based on the DPD coefficient to obtain a linear signal by using a predistortion signal, wherein the predistortion signal is generated by applying the DPD coefficient to the input signal.

Dated this 3rd day of October 2022



Signature:

Name: Arun Kishore Narasani
Patent Agent (IN/PA 1049)

ABSTRACT

HARDWARE IMPERFECTION MANAGEMENT FOR A RADIO UNIT IN AN OPEN RADIO ACCESS NETWORK

[0001] The present disclosure provides a hardware imperfection management method for an Open-Radio Unit (O-RU) (300) in an Open Radio Access Network (O-RAN). The method comprises removing power amplifier distortions and hardware imperfections, wherein removal is implemented in the O-RU independent of other O-RAN units. The removing of the PA distortions and the hardware imperfections is performed using inverse modelling for joint transmitter impairments mitigation using a piecewise residual neural network (400) in a digital pre-distortion (DPD) unit (314). The DPD unit (314) estimates a digital pre-distortion (DPD) coefficient from an input signal and an output signal using inverse modelling and eliminates the hardware imperfections based on the DPD coefficient to obtain a linear signal by using a predistortion signal, wherein the predistortion signal is generated by applying the DPD coefficient to the input signal.

FIG. 10