



(11) (21) (C) **2,019,373**
(22) 1990/06/20
(43) 1991/01/25
(45) 2000/10/10

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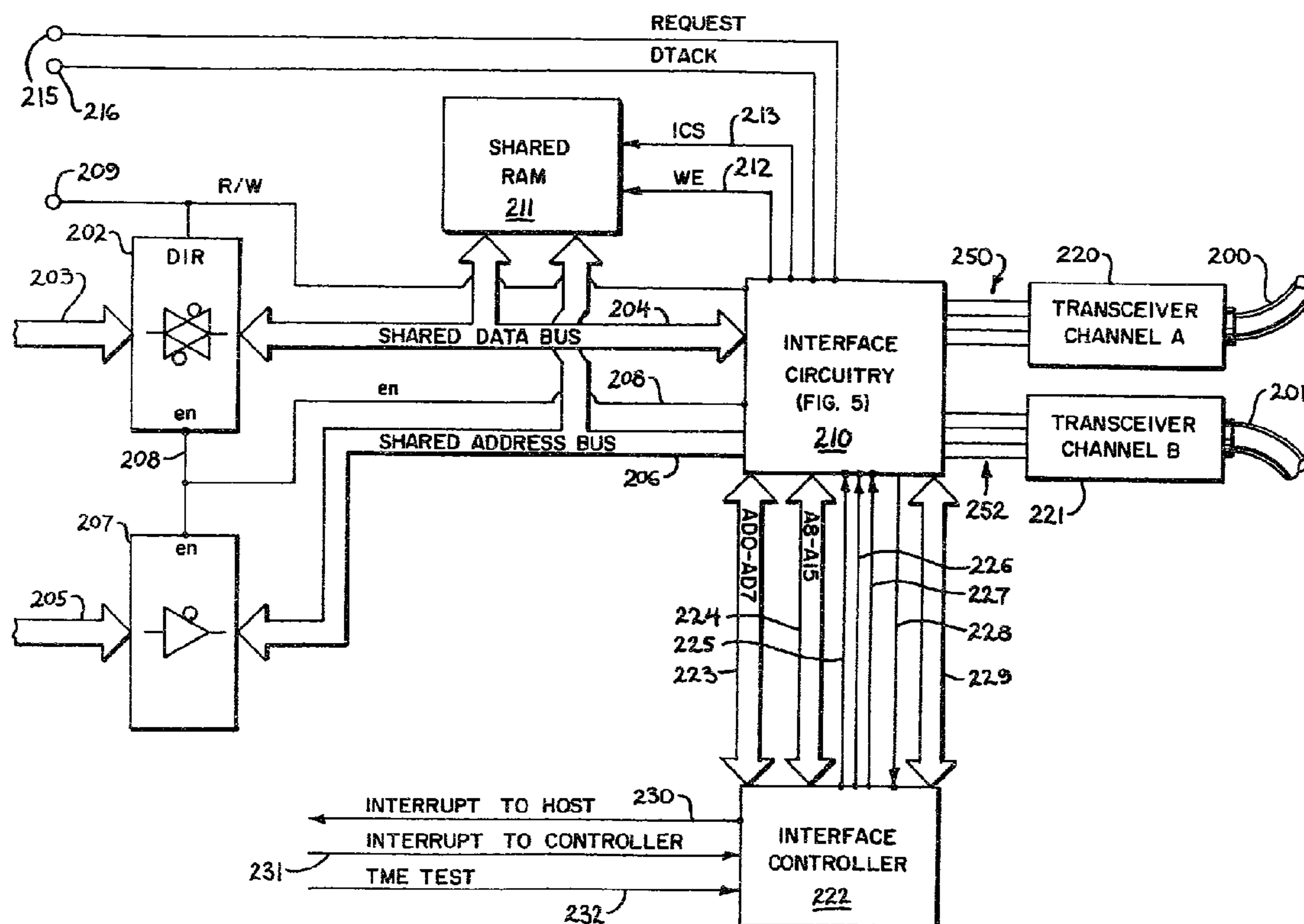
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(51) Int.Cl.⁵ G06F 13/42

(30) 1989/07/25 (384,614) US

(54) **STRUCTURE D'INTERRUPTION POUR CIRCUIT
D'INTERFACE DE RESEAU**

(54) **INTERRUPT STRUCTURE FOR NETWORK INTERFACE
CIRCUIT**



(57) A communications interface circuit couples a host processor to a pair of serial communications links. A shared memory is employed to pass message data and network management data between the host and the interface circuit, and each can interrupt the other through interrupt control lines. The shared memory stores a handshake segment that includes interrupt flags and acknowledge flags which enable a large number of different interrupt events to be efficiently serviced.



Abstract of the Disclosure

A communications interface circuit couples a host processor to a pair of serial communications links. A shared memory is employed to pass message data and network management data between the host and the interface circuit, and each can
5 interrupt the other through interrupt control lines. The shared memory stores a handshake segment that includes interrupt flags and acknowledge flags which enable a large number of different interrupt events to be efficiently serviced.

INTERRUPT STRUCTURE FOR NETWORK INTERFACE CIRCUIT

Background of the Invention

The field of the invention is serial communications networks and, particularly, interface circuits for connecting digital processors to serial communications networks.

There are numerous serial communications networks found
5 in businesses and in factories. In the business environment, for example, local area networks sold under the trademark "Ethernet" link personal computers, display terminals, minicomputers, mainframe computers, printers and disk drives together into a system in which data may be transferred rapidly
10 between its components. Similarly in the factory environment, local area networks sold under the trademark "MAP" link together cell controllers with display terminals, minicomputers, mainframe computers, computer aided design systems, computer aided manufacturing systems, computer aided
15 engineering stations and disk drives. The types of serial communications networks have proliferated, and while efforts have been made to standardize communications in certain environments, there currently are hundreds of different networks in use and the number continues to grow.

20 When designing digital processors for use in a commercial environment, one must select a strategy for connecting that processor to serial communications networks. For example, where the processor has a backplane, such as "VME BUS" or "MULTIBUS", a circuit board for that backplane may be designed
25 for each communications network. A variety of processor circuit boards and communications interface boards can be designed for the backplane and used together in any combination. On the other hand, where the digital processor does not employ a backplane, the interface to the

communications network may be constructed as an integral part of the digital processor. In such case, each digital processor must be designed and constructed to operate on a particular communications network, and if many networks are encountered, a
5 processor with integral interface circuit must be offered for each network. In other words, if a manufacturer offers a series of three digital processors of varying power and capability, and those processors must operate on three different communications networks found in their environment,
10 then six circuit board products must be offered if a common backplane architecture is used, or nine different products must be offered if the communications interface is an integral part of the processor.

Where the manufacturer offers a wide variety of digital
15 processor products of varying architectures and numerous communications networks are encountered in the environment in which those processors are used, difficult choices must be made. For example, the Allen-Bradley Company, assignee of the present application, manufactures small, inexpensive
20 programmable controllers such as those disclosed in U.S. Patent No. 4,504,927, and programming terminals such as that disclosed in U.S. Patent No. 4,527,250, which do not employ a backplane. They also offer medium sized programmable controllers such as those disclosed in U.S. Patent No. 4,443,865 that employ one
25 backplane, large programmable controllers such as that disclosed in U.S. Patent No. 4,442,504 that employ another backplane, numerical controllers such as that disclosed in U.S. Patent No. 4,228,495 that employs yet other backplanes, and cell controllers such as that disclosed in co-pending U.S.
30 patent application serial no. 928,529 filed on November 7, 1986, which employs still another backplane. Obviously, it is not commercially feasible to provide communications interface

modules or circuits for each of these processor products and for each of the communications networks that may be encountered by them in the factory.

Summary of the Invention

5 The present invention relates to an intelligent communications interface circuit which enables a serial communications network to be connected to a wide variety of digital processor-based products. More specifically, the present invention includes network access means which connects
10 to a communications network and which communicates thereon to receive and transmit message data, a shared memory for storing message data to be transmitted by the network access means, for storing message data received by the network access means, for storing a set of host interrupt flags and a corresponding set
15 of acknowledge flags, and for storing a set of interface interrupt flags and a corresponding set of acknowledge flags, a shared data bus and a shared address bus for coupling the shared memory to the network access means and to a host processor, and an interface controller coupled to the host
20 processor, the shared memory and the network access means; the interface controller being operable to toggle a host interrupt flag when message data is received by the network access means and produce an interrupt to the host, and being responsive to an interrupt from the host processor to examine the set of
25 interface interrupt flags and determine which has been toggled and to toggle its corresponding acknowledge flag.

A general object of the invention is to multiplex a set of interrupt driven events through a very simple interrupt structure. Only a single interrupt line is available to the
30 host processor and the interface controller, but by employing a set of host interrupt flags and a set of interface controller

interrupt flags in the shared memory, many different events can be indicated.

Another general object of the invention is to multiplex a set of interrupts without the need for expensive memory protection circuitry or "semaphore" schemes. An interrupt is indicated when the interrupt flag and its acknowledge flag are in the opposite logic state. The interface controller acknowledges the service of a requested interrupt by toggling the corresponding acknowledge flag and placing it in the same state as its corresponding interrupt flag. It can write to the host interrupt flags, but by software convention it will not write to the interface controller interrupt flags. Conversely, the host can write to the interface controller interrupt flags, but not the host interrupt flags. Either the interface controller or the host can read all the flags to determine if an interrupt request is pending (i.e. interrupt flag and acknowledge flag in opposite logic states) or if it has been serviced (both interrupt flag and acknowledge flag in same state).

A more specific object of the invention is to provide a means for passing message data between a host processor and a communications interface circuit. A shared memory stores data structures for incoming messages, outgoing messages and network management data, as well as an interrupt flag for each of these data structures. When either the host processor or communications interface circuit is interrupted, these interrupt flags are examined to determine which data structure should be serviced and the priority of such service. Efficient coupling of messages and their acknowledgment is thus achieved.

Yet another object of the invention is to avoid locking either processor out of the shared memory. Other systems employ a "bus lock" signal which enables one processor to lock

the other processor out of the shared memory while it performs functions. This can substantially slow the operation of the communications interface and preclude its use at higher baud rates.

5 The foregoing and other objects and advantages of the invention will appear from the following description. In the description, reference is made to the accompanying drawings which form a part hereof, and in which there is shown by way of illustration a
10 preferred embodiment of the invention. Such embodiment does not necessarily represent the full scope of the invention, however, and reference is made therefore to the claims herein for interpreting the scope of the invention.

15 In accordance with an embodiment of the invention, a control system having a host processor which carries out control functions and a communications link connected to the control system, a communications interface circuit is comprised of a protocol machine
20 coupled to the communications link, said machine including means to transmit and receive message data on said communications link; an interface controller coupled to the protocol machine and including means for generating an interrupt to the host processor; means
25 connected to the host processor for generating an interrupt to the interface controller; a shared memory coupled to the host processor and the interface controller for storing message data received by the protocol machine for reading by the host processor, for
30 storing message data from the host processor for transmission by the protocol machine, and for storing a handshake segment which contains a set of host interrupt flags and a corresponding set of acknowledge flags, and a set of interface interrupt flags and a

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corresponding set of acknowledge flags; and the interface controller includes first means for toggling one of said host interrupt flags and producing an interrupt to the host processor, and second means which is responsive to an interrupt to the interface controller generated by the host processor to examine the set of interface interrupt flags for one which has been toggled and to toggle its corresponding acknowledge flag.

10 Brief Description of the Drawings

Fig. 1 is a pictorial drawing of a programmable controller system which employs the present invention;

Fig. 2 is a block diagram of the system controller module which forms a part of the system of Fig. 1;

15 Fig. 3 is a block diagram of the remote I/O scanner module which also forms part of the system of Fig. 1;

20 Fig. 4 is a block diagram of the intelligent communications interface circuit which is used in the modules of Figs. 2 and 3;

Fig. 5 is a circuit diagram of the network access circuit which forms part of the circuit of Fig. 4;

Fig. 6 is a map of the shared RAM which forms part of the circuit of Fig. 4;

25 Fig. 7 is a map of the negotiation segment which forms part of the memory map of Fig. 6;

Fig. 8 is a flowchart of the program executed by the interface controller of Fig. 4;

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Fig. 9 is a map of the handshake segment which forms part of the memory map of Fig. 6;

Fig. 10 is a pictorial representation of the data structures stored in the channel A and channel B segments which
5 form part of the memory map of Fig. 6; and

Fig. 11 is a flow chart of the interrupt service routine executed by the interface controller of Fig. 4.

Description of the Preferred Embodiment

Referring to Fig. 1, a programmable controller 10 is
10 housed in a rack 12 which includes a series of slots that receive a plurality of printed circuit board modules. These functional modules connect to a mother board which extends along the back surface of the rack 12 to provide a backplane 11. The backplane 11 has a plurality of module connectors
15 which are interconnected by a conductive pattern on the backplane. The backplane 11 provides a series of signal buses to which the modules connect. The rack 12 contains a power supply module 14, a system controller 16, a number of program execution processor modules 18 and a plurality of remote
20 input/output (I/O) scanner modules 20.

Up to four remote I/O scanner modules 20 interface the controller 10 to external remote I/O racks 17 via serial I/O data links, such as link 15. Each remote I/O rack 17 has a plurality of local I/O modules 19 which are coupled to
25 individual sensors and actuators on the controlled equipment. The local I/O modules 19 may take many forms and may include, for example, DC inputs or outputs, AC inputs or outputs, analog inputs or outputs, and open or closed loop positioning modules.

The remote I/O rack 17 also contains an adapter module 19'; such as the one described in U.S. Patent No. 4,413,319, which connects to the serial communications network 15 and couples message data between the I/O modules 19 and the network 15.

5 The system controller 16 is connected through cable 22 to a programming terminal 24, which is used to load the user programs into the programmable controller and configure its operation, as well as monitor its performance. The terminal 24 is a personal computer programmed to enable the user to develop
10 the system's control programs. The control programs are downloaded into the programmable controller and the terminal 24 may be disconnected from the system controller 16 if further monitoring is not required. The system controller 16 may also be connected via a cable 26 to a local area network 28 over
15 which it may receive data and programming instructions, as well as issue status information and report data to a central computer. This enables a central computer or central terminal to program and control the operation of a plurality of programmable controllers on a factory floor.

20 Referring particularly to Fig. 2, the system controller module 16 provides a communication interface for the programmable controller to external terminals and local area networks. The system controller 16 also performs system housekeeping functions, such as providing an indication of the
25 system status and supervising access to the backplane 11. During normal operation of the programmable controller, the system controller 16 takes care of communication with the external devices that are connected to it, such as network 28 and the programming terminal 24. One of the significant tasks
30 is communicating with the terminal 24 to provide information allowing the operator to monitor the system performance and to detect faulty sensors or actuators. Another task supervised by

the system controller 16 is the exchange of data with a central computer or a peer programmable controller via the local area network 28. This enables the central computer to collect statistics from one or a number of programmable controllers
5 regarding their operation.

The system controller module 16 connects to the backplane buses 21-23 and is divided into three sections: the backplane interface section; the processor section; and the communications section. The backplane interface section
10 supervises the backplane access for all the rack modules and interfaces the controller module 16 itself to the backplane 11. The processor section executes a supervisory program for the controller 10. The communication section is primarily responsible for communicating with external terminal 24 through
15 serial communications line 25 and with the local area network 28 through line 26.

Referring still to Fig. 2, the processor section is linked together by a set of buses that comprise control lines 61, a sixteen bit data bus 62 and a twenty-three bit address
20 bus 63. Access to these buses is controlled by an arbitration circuit 64. The processor section is built around a sixteen-bit microprocessor 66, such as a model 68010 manufactured by Motorola, Inc., which executes program code stored in read only memory 68. The 68010 microprocessor is essentially a memory
25 mapped device and does not have any input/output lines directly connected to it. Therefore, its access to other components on the processor bus must be accomplished through issuing addresses on bus 63. The address sent from the microprocessor 66 is decoded in an address decode circuit 70 to produce the
30 proper control signals for the accessed component. The processor section also contains an interrupt processor 72 which

controls interrupts to the microprocessor 66 and provides the proper instruction address vectors.

A data transfer acknowledge and bus error (DTACK/BERR) circuit 74 is also connected to the processor control bus 61. 5 Circuit 74 responds to signals from the various components in the processor section to acknowledge the completion of a data transfer and to issue bus error signals in the event of improper addressing or failure of data transfer. These signals are acted on by the microprocessor 66 which takes corrective 10 action. The processor section also includes clock circuit 89 that contains the main system clock and a real time clock. A system status circuit 88 receives input signals related to the status of the entire system 10 and provides an indication of that status.

15 The main random access memory (RAM) 69 for the system controller 16 is also connected to the processor buses 61-63. The RAM 69 is a static memory which serves as the system memory for the entire controller 10. The main memory 69 can be directly accessed via the backplane 11 by other modules in the 20 system without the intervention of the microprocessor 66.

Referring still to Fig. 2, the processor section of the system controller 16 interfaces with the backplane buses of rack 12 via a plurality of components that are coupled to both sets of buses. Specifically, the backplane data bus 22 is 25 connected to the processor data bus 62 by a set of bi-directional data transmission gates 78 and the backplane address bus 23 is connected to the processor address bus 63 by another set of bi-directional gates 76. When the system controller 16 seeks to exercise control over the backplane 11 30 of the programmable controller 10, a master mode control circuit 81 responds to signals on the control lines of the processor bus 61 and issues the proper control signals over the

backplane control bus 21 to access other modules within the rack 12.

When another module within the rack 12 seeks access to the system controller 16 in order to read the contents of main RAM 69, for example, the system controller becomes subordinate to the control of the backplane 11 by this other module. In this circumstance, a slave mode control circuit 82 within the system controller 16 responds to the address of the system controller that appears on the backplane address bus 23 and to control signals on the control lines of the backplane bus 21 which lead from the other module. In response, the slave mode control 82 issues signals to transmission gates 76 and 78 enabling the other backplane module to access the system controller 16. In this latter instance, the master mode control circuit 81 is in a dormant state. The two bus gates 76 and 78 receive enabling control signals from the master or slave mode control circuits 81 and 82 via the lines of control bus 61 depending upon the mode of backplane communication.

A backplane arbitration circuit 84 supervises access to the backplane 11 and resolves conflicting requests for access from the modules in the system. The backplane arbitration circuit 84 employs a rotating priority system for determining which of several modules simultaneously seeking access to the backplane will be granted such access. With the rotating priority system, each time that a module relinquishes control of the backplane 11, the order of priority shifts.

The I/O scanner modules 20 gather input sensor data for use by the program execution processor modules 18. Referring to Figs. 1 and 3, a remote I/O scanner module 20 couples the programmable controller 10 to one or more remote input/output racks 17 containing individual I/O modules 19 which interface the input devices or output devices to the programmable

2019373

controller 10. Each scanner module 20 periodically requests input data pertaining to the status of the input devices connected to the remote I/O racks 17 and stores it in the module's input image table for reading by other controller
5 modules, such as the processor modules 18. The scanner module 20 also contains an image table of output data that it receives from other controller modules, such as the processor modules 18. At regular intervals the updated output data in the scanner module's output image table is transferred to the
10 respective remote input/output racks 17 to control the various actuators connected to these racks.

Each remote I/O scanner module 20 connects to the three backplane buses 21-23. The I/O scanner 20 contains two sets of internal buses: memory access buses 121-123 and microprocessor
15 buses 131-133 are connected to the backplane 11 by a set of address bus gates 124 and a set of data bus gates 126. Both of these transmission gates are controlled by an inter-bus control circuit 128 which sends signals to the gates 124 and 126 via the memory control bus 121. A local random access memory,
20 referred to as main RAM 134, is coupled to the three memory buses 121-123. It stores the input image table for the sensor information being input to the I/O scanner 20 from the remote I/O racks 17 and it also stores the output image table for the output data being output to the remote I/O racks 17.

25 The inter-bus control circuit 128 also sends control signals to an I/O data arbitration circuit 130 which resolves conflicting requests for access to the memory buses 121-123 from the backplane 11 and the microprocessor buses 131-133. Two sets of transmission gates, address gates 136 and bi-
30 directional gates 138, interconnect the memory buses 121-123 to the microprocessor buses 131-133 and receive control signals

from the I/O data arbitration circuit 130 via the memory control bus 121.

The operation of the remote I/O scanner 20 is controlled by an eight-bit microprocessor 140 which is connected to the three microprocessor buses 131-133. Microprocessor 140 is commercially available from Zilog, Inc. as the Z80 and it operates in response to a stored program to send message data to a communications section 141 from the main RAM 134 and to receive message data from the communications section 141. The communications section 141 couples message data between the microprocessor 140 and each of the serial links 15.

The above-described modules are typical of the environment in which the present invention is used. A host processor (such as microprocessor 66 or 140) which performs a number of functions must also communicate through one or more serial communication links or networks. The host processor exchanges message data with the communication network through a communications section which is responsible for executing the particular network protocol necessary to send or receive message data. The host processor is capable of reading data, including message data, from a memory which is shared with the communications section and it can write data to that shared memory.

Referring particularly to Fig. 4, the preferred embodiment of the communications interface circuit is designed to couple a host processor with either of two serial communications links 200 and 201. The host processor (not shown in Fig. 4) connects to the communications interface circuit through a set of bi-directional gates 202 which link the host's data bus 203 to a shared data bus 204. The host's address bus 205 is coupled to a 15-bit shared address bus 206 by a set of fifteen gates 207 that are enabled along with the

data gates 202 when a logic low signal is received through a
"en" control line 208. The host initiates a read or write
cycle by asserting a "request" control line 215, and the
interface circuit 210 acknowledges the request by asserting a
5 DTACK control line 216 when access to the shared buses 204 and
205 is granted. The host's read/write control line 209
determines the direction of data transfer through the data
gates 202.

The shared buses 204 and 206 connect to a shared random
10 access memory (RAM) 211 which is controlled by the interface
circuitry 210 through a WE control line 212 and an ICS control
line 213. The interface circuitry 210 also connects to the
shared buses 204 and 206 and it operates the en control line
208 to enable access to the shared RAM 211 by the host
15 processor.

As will be explained in more detail below, the shared RAM
211 serves as a means for exchanging information, including
message data, between the host processor and the communications
interface. Message data may be written to the shared RAM 211
20 by either the host processor or the interface circuitry 210 and
the other device can read that message data after being
notified of its presence. Also, as will be described in detail
below, data required by the communications interface circuit to
operate properly with the host processor is stored in the
25 shared RAM 211, as is data which configures the communications
interface circuit to the particular application.

Referring still to Fig. 4, the interface circuitry 210 is
an application specific integrated circuit (ASIC) which
performs a number of functions. First, it arbitrates access to
30 the shared RAM 211 and controls read and write cycles to the
shared RAM 211. It also passes message data from the shared
RAM 211 to either an A channel transceiver 220 or a B channel

transceiver 221 and it passes message data from the transceivers 220 or 221 back to the shared RAM 211. It also permits an interface controller 222 to read data from the shared RAM 211 and write data to it.

5 The operation of the interface circuitry 210 is controlled by the interface controller 222 which is a programmed microcomputer, model "Super 8" manufactured by Zilog, Inc. The interface controller 222 connects to the interface circuitry 210 through an 8-bit data/address bus 223,
10 and an 8-bit address bus 224 and a set of control lines. When a 16-bit address is applied to the buses 223 and 224, a signal is asserted on AS control line 225, and when 8-bits of data is applied to bus 223, a signal is asserted on DS control line 226. The direction of data transfer on bus 223 is determined
15 by the logic state of a R/W control line 227. The above buses and control lines are driven by the interface controller 222, however, a number of control lines are driven by the interface circuitry 210. These include a WAIT control line 228 which places the interface controller 222 in a wait state, and a
20 series of interrupt lines and flag lines which are indicated collectively at 229.

 The interface controller 222 is also linked to the host processor by a set of control lines. These include an
25 INTERRUPT TO HOST control line 230 which is asserted by the interface controller 222 and which signals the host processor that it should read certain data structures in the shared RAM 211. Likewise, the host processor can interrupt the interface controller 222 through an INTERRUPT TO CONTROLLER control line 231, which signals the interface controller 222 to read the
30 shared RAM 211 for information from the host processor. Finally, a TME control line 232 may be asserted by the host

processor to signal the interface controller 222 that it should enter into its test mode of operation.

Referring particularly to Figs. 4 and 5, the interface circuitry 210 links the transceivers 220 and 221 to the shared RAM 211 and the interface controller 222 to the shared RAM 211. The channel A transceiver 220 is connected through lines 250 to a channel A serial protocol machine 251, and the channel B transceiver 221 is connected through lines 252 to a channel B serial protocol machine outlined by dashed line 253. The serial protocol machines 251 and 253 are identical in construction and operation.

Message data to and from the serial protocol machines 251 and 253 is coupled to the shared RAM 211 through an 8-bit data bus 255 and a set of eight bi-directional data gates 256. A DMA control 257 actually carries out the transfer of message data to and from the shared RAM 211 by generating addresses on its shared address bus 206 through a set of fifteen address gates 258. Control of the shared buses 204 and 206 is determined by an arbitration and control circuit 260 which arbitrates requests from the host processor, from the interface controller 222 and from both the A and B channels of the DMA control 257.

Referring still to Figs. 4 and 5, the interface controller buses 223 and 224 connect to the interface circuitry 210 through a set of eight bi-directional gates 262 and a set of eight address gates 263. When data is present on the bus 223 as signaled by the DS control line 226, the bi-directional gates 262 are enabled and the data is conveyed therethrough in the direction indicated by R/W control line 227. This data is applied to an 8-bit data bus 263, which in turn is coupled to the 8-bit data bus 255 by another set of eight bi-directional data gates 264. In this manner, data may be coupled to or from

the shared RAM 211 to the data bus 263 and through gates 262 to the interface controller 222. Data on the bus 263 may also be conveyed to the DMA control 257 to enable the interface controller 222 to set the memory address which the DMA control will generate. It also couples to a set of timers 266 and processor status registers 268. The interface controller 222 may thus write data to the timers 266 which configure the serial protocol machines 251 and 253 to the particular timing requirements of the local area networks. The interface controller 222 may also write data to the registers 268 which control the operation of the interface circuitry 210 while the interface controller 222 is performing other functions. The interface controller 222 may also read from the processor status registers 268 to determine the state of the interface circuitry 210 at any moment in time. The contents of the processor status register 268 is provided in Table A.

Table AProcessor Status Registers

4 bits	tells manchester encoder how many valid bits it is
20	to receive before indicating "valid manchester"
1 bit	valid manchester signal available
1 bit	carrier detected
1 bit	Fault detect
8 bit	station address
25	4 bit state of receive FIFO fullness
3 bit	number of preamble flags sent before a packet
8 bit	number of bit times to hold transmitter after command to transmit
1 bit	transmitter is busy
30	1 bit receiver busy

Receiver syndrome register - cause of a "bad packet" interrupt to microprocessor.

- receive FIFO overflow
- manchester code lost
- 5 packet too short
- packet too long
- abort message received
- CRC bad
- read from empty receive FIFO

10 Transmit syndrome register -

- transmit FIFO underflow (empty)
- too many opening flags
- write to full transmit FIFO

When the interface controller 222 asserts an address on
 15 its bus 223, as indicated by its AS control line 225, that
 address is latched at address latch 270. Subsequently, when
 the upper eight bits of the address are asserted on bus 224,
 the complete 16-bit address is applied to an address bus 271.
 This address is decoded by decoder 272 to enable one of the
 20 devices connected to the data bus 263. In addition, if the
 shared RAM 211 is addressed, the decoder 272 generates a
 request to the arbitration and control circuit 260 and a wait
 signal is produced for the interface controller 222 by a
 processor interface control 267 through control line 228. When
 25 access is granted, this wait signal is removed and a set of
 address gates 273 are enabled to allow the address produced by
 interface controller 222 to be coupled to the shared address
 bus 206 through gates 258.

Through the above described buses and gates, the
 30 interface controller 222 has full access to the shared RAM 211
 where it can exchange information with the host processor. In

addition, the interface controller 222 can configure the operation of the serial protocol machines 251 and 253, control their operation, and monitor their operation.

Referring still to Fig. 5, the serial protocol machines 251 and 253 handle the bit oriented protocol structure used by the local area networks to which they connect. They are sometimes referred to as an HDLC engine which transmit and receive the packeted information in the serial format of the local area network protocol. Each provides the flags, zero insertion and deletion, and CRC checking and generation. Each serial protocol machine 251 and 253 is divided into a receive section which transfers all data bytes received at a manchester decoder 300 to the receive FIFO memory 280, and a transmit section which transmits all data bytes loaded into the transmit FIFO memory 281 through to a manchester encoder 301.

The receive section is operated by a receive control 302 that connects to each of its functional elements. As a data packet is received through the manchester decoder 300, the address field therein is checked by circuit 303 as it is transferred serially to a serial-to-parallel converter 304. If the address does not correspond to the local address of this station, the data packet is ignored. Otherwise, the data packet is converted to 8-bit bytes of data by the serial-to-parallel converter 304 and the bytes of data are stored in the receive FIFO memory 280. The last two bytes prior to the packet's closing flag is a cycle redundancy checking (CRC) number which is compared with the number produced by a CRC checker 305. If the numbers are the same, accurate transmission of the data packet has occurred and it is passed onto the receive FIFO memory 280. An interrupt of the interface controller 222 (Fig. 4) is produced to indicate that a data packet has been received. If the CRC bytes indicate an

error in transmission, the CRC checker 305 generates an interrupt to the interface controller 222 and error bits are set in the receive syndrome register to inform the interface controller 222 of the problem.

5 The transmit section is operated by a transmit control 306 that connects to each of its functional elements. The transmit section is commanded by the interface controller 222 to send a data message stored in the transmit FIFO memory 281. The transmitter automatically begins sending the preamble bits
10 of the data packet through the manchester encoder 301 and data bytes are then read from the transmit FIFO memory and applied to a parallel-to-serial converter 307. The data is converted to a serial bit stream which is fed to the manchester encoder 301 for transmission. A CRC generator 308 monitors all bits in
15 the transmitted data packet and when the last data bit has been sent, the CRC generator 308 produces a 16-bit CRC number which is used as described above to check the integrity of the data packet when it is received at another station.

 There are many architectures which may be employed to
20 implement the serial protocol machines 251 and 253, and their precise design is not the subject of the present invention. For example, many of their functions may be performed by universal asynchronous receiver/transmitters (UARTs) which are commercially available in integrated circuit form. The same is
25 true of the manchester encoders and decoders and the FIFO memories. As indicated above, however, these functional elements of the serial protocol machines 251 and 253 are implemented in the preferred embodiment as part of an ASIC which also includes the other functional elements shown in Fig.
30 5. Indeed, it is one of the objects of the present invention to enable this ASIC to be used in a wide variety of

communications applications so that its design, development and tooling costs can be economically justified.

As indicated above, the shared RAM 211 stores data structures which enable the communications interface circuit to adapt to the particular host processor to which it connects and to exchange message data with that host processor. These stored data structures are illustrated generally in Fig. 6 and will now be discussed in more detail.

Referring particularly to Fig. 6, the shared RAM 211 stores data in segments. The first segment 350 is a negotiation segment which contains 32 bytes of data that is used at power-up to negotiate the characteristics of the communications between the host and the communications interface circuit. This segment 350 will be described in more detail below.

The second segment is an identification segment 352 which contains information that indicates the series and revisions number of the communications interface circuit.

The third segment 351 is a segment directory that contains an array of segment descriptors that include the starting address of each segment in the shared RAM 211, the size of each segment, the type of segment, and the instance of the segment. The segment directory 351 is an index to the other segments in the shared RAM 211. The types of segments include:

- 0 - negotiation segment
- 1 - segment directory
- 2 - identification segment
- 3 - channel segment
- 4 - interprocessor handshake flags
- 5 - selection segment

The instance indicates the number of the segment of a particular type. For example, there are two channel segments 355 and 356 in the preferred embodiment and these are distinguished by their instance number "0" and "1".

5 Following the directory segment 351 is a handshake segment 354 which occupies eight 8-bit words per channel in the shared RAM 211. As shown in Fig. 9, the handshake segment 354 includes four words 370-373 which store flags that relate to interrupts from the host to the interface controller 222, and
10 four words 374-377 which store flags related to interrupts from the interface controller 222 to the host. More specifically, a flag is toggled in word 370 by the host processor when it interrupts the interface controller 222. The interface controller 222 services the interrupt by reading these flags
15 and determining which has been toggled. The first flag (bit 0) indicates that channel A is to be reset, the next flag (bit 7) indicates that diagnostic counters are to be reset, the next four flags (bits 8-11) indicate that the respective four channel A access FIFO registers require service, and the next
20 four flags (bits 12-15) indicate that the respective four channel A management FIFO registers require service. The interface controller 222 acknowledges the interrupt by toggling the corresponding flag in the word 371 and executing the routine required to service the interrupt. Words 372 and 373
25 in the handshake segment 354 are identical to the words 370 and 371, however, they relate to channel B.

The last four words 374-377 in the handshake segment 354 are organized in the same manner, however, the interrupt flags in words 374 and 376 are toggled by the interface controller
30 222 and the interrupts are serviced by the host. The host acknowledges the interrupt by toggling the corresponding flag

in word 375 or 377 and it executes the appropriate interrupt service routine.

In summary, the handshake segment 354 operates as a means for multiplexing many interrupts from either the host or the interface controller 222 through a pair of interrupt lines. An interrupt is signaled when the corresponding bits in word pairs 370-371, 372-373, 374-375 and 376-377 are in the opposite state. The host can only toggle its own flags and the interface controller 222 can only toggle its flags. Both can read all of the flags, however, and either can determine if an interrupt has been requested and if a requested interrupt has been serviced. Using this technique, neither processor need be locked out of the shared RAM 211 at any time. The operation of this interrupt multiplexing technique will be described in more detail below.

Referring still to Fig. 5, the next two segments in the shared RAM 211 store data associated with messages that are conveyed through the A channel and the B channel of the interface circuitry 210 (Fig. 5). More specifically, segment 355 stores the FIFOs, message headers, buffer headers and buffers associated with communications through channel A, and segment 356 stores similar data structures for communications through channel B. Since the two segments 355 and 356 are similar, only one will be described in detail.

Referring particularly to Fig. 10, each message which is conveyed between the host and the interface controller 222 through the shared RAM 211 is comprised of a message header, zero or more buffer headers, and one data buffer associated with each buffer header. The message headers are illustrated at 378 as a linked set of data structures, and each message header stores the following information:

	NEXT	- pointer to the next buffer header associated with this message;
	SERVICE	- the service performed by this message;
5	PRIORITY	- the priority level of this message where the protocol supports different priorities;
10	STATUS	- the result of the transmission 0 = confirmed delivery 1 = confirmed nondelivery 2 = unconfirmed delivery 3 = unconfirmed nondelivery;
	REASON	- error code which indicates the cause of a failure;
15	DESTINATION ADDRESS COUNT	- number of bytes required by destination address;
	DESTINATION NETWORK ADDRESS	- the destination of this message;
20	SOURCE ADDRESS COUNT	- the number of bytes needed to define source address;
	SOURCE NETWORK ADDRESS	- the source of this message;
25	SAP TYPE	- the type of service access point being used in this message;
	DSAP	- destination service access point number;
	SSAP	- source service access point number;
30	BUFFER HEADER POINTER	- address of the first buffer header associate with this message; and
	TAG	- user defined field.

The buffer headers are indicated in Fig. 10 at 379 as a set of linked data structures. Each buffer header stores the following information:

35	NEXT	- pointer to the next buffer header associated with this message;
	DATA	- pointer to the buffer associated with this buffer header; and
40	SIZE	- the number of data bytes in the associated buffer.

The buffers are indicated at 380 and each is a consecutive sequence of bytes associated with one of the buffer headers 379. Either the host or the interface controller 222 may form a message which is comprised of one or more of these data buffers 380 by storing the message data therein and then linking them together by their associated buffer headers 379. A message header 378 is then formed which identifies the first buffer header in this linked list of buffer headers 379.

Referring still to Fig. 10, if the host creates a message it stores a pointer to the header for that message in a REQUEST FIFO 381 as indicated by arrow 382. The REQUEST FIFO 381 is an array of such pointers preceded by the following stored information:

- 15 NEXT IN - host index to the next available location in the FIFO where a message header pointer can be stored;
- NEXT OUT - interface controller index to the next message pointer to be read and processed;
- WRAP MASK - the two indexes wrap using this field; and
- 20 IFLAG NUMBER - interrupt flag bit number used by this FIFO.

When the interface controller 222 is interrupted, it reads the next message pointer out of the REQUEST FIFO 381 as indicated by arrow 383, and it reads the indicated message header 378 and the associated data 380 indicated by the buffer headers 379 to form a message. It confirms that the message has been received and processed by writing the pointer for the same message header into a CONFIRM FIFO 384 as indicated by arrow 385. The FIFO 384 is similar in structure to the FIFO 381, and when the host is interrupted, it reads the next message header pointer from the confirm FIFO 384 as indicated by arrow 386. The host then reads the indicated message header

from the shared RAM 211 to confirm that the message which it initiated has been processed.

Similar data structures exist for messages initiated by the interface controller 222. Referring still to Fig. 10, when the interface controller 222 receives a message on the network, it stores the message data in the shared RAM 211 in available buffers 380 and the message header in an available message header 378. It then stores a pointer to the message header 378 in an indicate FIFO 387, as indicated by arrow 388, and interrupts the host. The host processor reads the next pointer in the indicate FIFO 387, as indicated by arrow 389, and the header and message data are read from the shared RAM 211. The host processor then writes a pointer to an accept FIFO 390, as indicated by arrow 391, and it interrupts the interface controller 222. The interface controller 222 reads the pointer from the accept FIFO 390 to confirm that the message has been accepted by the host as indicated by arrow 392.

Referring again to Fig. 9, the handshake segment includes interrupt flags for each of the four FIFOs 381, 384, 387 and 390. More specifically, the host interrupt in the word 370 includes four access flags which correspond to the four channel A FIFOs and word 372 includes four channel B FIFOs. Similarly, the interface controller word 374 includes four access flags which correspond to the four A channel FIFOs and the interface controller word 376 includes four access flags which correspond to the four B channel FIFOs. These flags enable the interrupted processor to promptly read the appropriate FIFO when it is interrupted by the other processor.

The channel segments 355 and 356 in the shared RAM 211 (Fig. 7) also store data structures associated with network management functions. These include four management FIFOs and associated message headers, buffer headers and buffers (not

shown in the drawings) which operate as described above. In addition, there are four management interrupt flags in each of the words 370-377 of the handshake segment 354 (Fig. 9) which enable the host and interface controller 222 to promptly
5 service the management FIFOs.

As indicated above, the primary function of the interface controller 222 is to relay messages between the shared RAM 211 and the interface circuitry 210 (Fig. 4). It performs this function and its other functions under the direction of
10 programs which are stored in its internal read-only memory (not shown in the drawings). A number of these programs are interrupt driven and include a service routine which is executed when an interrupt is received from the host through line 231, and service routines which are executed when an
15 interrupt is received from the A channel or the B channel of the interface circuitry 210. The main program which is executed by the interface controller 222, however, is illustrated in Fig. 8, and will now be described in more detail.

20 Referring particularly to Fig. 8, when the interface controller 222 is powered up, or physically reset, a set of instructions indicated by process block 400 are executed to perform diagnostic functions. For example, the integrity of the shared RAM 211 is thoroughly checked. Following this, a
25 set of instructions indicated by process block 401 are executed to negotiate a set of parameters which determine how the interface controller 222 and the host will communicate with each other through the shared RAM 211.

Following negotiation, each of the two channels is
30 configured as indicated by process block 402. Each physical channel defaults to a set of predefined access and protocol selections although other selections can also be made. More

specifically, within each channel segment 355 and 356 of the shared RAM 211 (Fig. 6) are select segments (not shown) which can be read by the host and used to select operating parameters which are different than the default values. For example, each
5 channel can be set for any one of four "access" types: (1) an active node on a local area network; (2) an inactive node on a local area network; (3) a scanner or an adaptor on a serial I/O link; or (4) a bridge between two local area networks. With each of these access types there is a menu which defines the
10 various protocols that can be selected by the host, and each selectable protocol may have values of operating parameters for the protocol (i.e. baud rate, parity, etc.). When the configuration of each channel has been completed, the channel becomes operational, or "on line".

15 Referring still to Fig. 8, after configuration is completed, each physical channel is then alternately serviced. This is accomplished by calling a subroutine indicated at 403 which switches the channel context. This context switch involves saving the values of microcomputer registers and
20 loading the register values for the other channel. A check is then made at decision block 404 to determine if the channel is operational, and a check is then made at decision block 405 to determine if any incoming messages are available in the channel's receive FIFO 280 (Fig. 5). If so, the message is
25 read from the receive FIFO 280 and written to an unused buffer 380 in the shared RAM 211 as indicated at process block 406. The corresponding buffer headers 379 and message header 378 are created and a pointer to the message header 378 is stored in the next entry of the indicate FIFO 387 (Fig. 13). As
30 indicated at process block 407, the proper flag in the handshake segment is then toggled and the host is interrupted to service the incoming message.

If no incoming message is present as determined at decision block 405, a check is made of an internal flag register at decision block 408 to determine if messages have been posted for transmission in the shared RAM 211 by the host.

5 If so, the pointer in the request FIFO 381 is read and the indicated message header 378, buffer headers 379 and buffers 380 (Fig. 10) are transferred from the shared RAM 211 to the channel's transmit FIFO 281 (Fig. 5) as indicated at process block 409. The same message header pointer is then written to
10 the confirm FIFO in the shared RAM 211 and the host is interrupted at process block 410 to indicate that the message has been processed.

The interface controller 222 continuously cycles through this program with the context being switched between the two
15 channels. Consequently, messages received at either channel are passed through to the host, and messages received from the host are passed through for transmission on the proper serial link.

When the interface controller 222 interrupts the host as
20 described above, it must first toggle the appropriate interrupt flag in the handshake segment 354. For example, as shown in Figs. 9 and 10, there is an interrupt flag in each of the channel A and channel B host interrupt words 370 and 372 which corresponds to the indicate FIFO 387 and the confirm FIFO 384.
25 Any of these may be toggled by reading the word 370 and 372 from the shared RAM 211, changing the state of the proper flag, and writing the word 370 or 372 back to the RAM 211. The INTERRUPT TO HOST control line 230 is then asserted to signal the host. Of course, if the interrupt flag is already
30 different than its acknowledge flag, then an interrupt has already been requested and the interrupt flag is not toggled again.

The host operates in the same manner when it loads message data into the request FIFO 381 or when acknowledging receipt of an incoming message by writing to the accept FIFO 390. That is, the host reads the channel A or channel B interface interrupt word 374 or 376 from the handshake segment 354, toggles the appropriate interrupt flag, and writes the word back to the handshake segment 354. The host then asserts the INTERRUPT TO CONTROLLER control line 231 to alert the interface controller 222.

When an interrupt is requested on the INTERRUPT TO CONTROLLER control line 231, the interface controller 222 responds by executing an interrupt service routine which is shown in Fig. 11. This routine determines which interrupt flag has been toggled and sets the corresponding bit in a flag register that is stored in the interface controller 222. More particularly, when the interrupt service routine is entered it enters a loop in which the channel A and then the channel B interrupt flags are checked. The interface interrupt word 374 or 376 is first read from the handshake section (Fig. 9) of the shared RAM 211, as indicated at process block 400, and then the corresponding acknowledge word 375 or 377 is read as indicated at process block 401. The respective bits in the two words are then exclusive ORed as indicated at process block 402 to determine which interrupt flag(s) has been toggled to a different state than its acknowledge flag(s). The resulting bit pattern (R) is ORed with the interface controller flag register so that the newly detected interrupt(s) is added thereto, as indicated by process block 403.

As indicated by process block 404, the next step is to toggle the state of the acknowledge flag(s) which corresponds to the newly detected interrupt(s). This is accomplished by exclusive ORing the acknowledge flag word 375 or 377 with the

result bit pattern (R) and then writing the altered acknowledge
flag word back to its location in the shared RAM 211, as
indicated by process block 405. A check is made at decision
block 406 to determine if the interrupt flags for both channels
5 have been checked, and if so, the interrupt service routine
ends by returning the interface controller 222 to resume its
interrupted functions.

As indicated above, the state of the flag register is
periodically checked to determine if any of the FIFOs require
10 service. When a flag is set indicating that a particular FIFO
requires service, all of the messages in that FIFO are
processed. This takes care of the situation in which a second
or more interrupts occur before the first interrupt can be
serviced.

It should be apparent to those skilled in the art that an
interrupt service routine similar to that just described is
also executed by the host processor when it is interrupted by
the interface controller 222. It should also be apparent that
other functions may be performed during the interrupt service.

We Claim:

1. In a control system having a host processor which carries out control functions and a communications link connected to the control system, a communications interface circuit which comprises:

5 a protocol machine coupled to the communications link, said machine including means to transmit and receive message data on said communications link;

10 an interface controller coupled to the protocol machine and including means for generating an interrupt to the host processor;

means connected to the host processor for generating an interrupt to the interface controller;

15 a shared memory coupled to the host processor and the interface controller for storing message data received by the protocol machine for reading by the host processor, for storing message data from the host processor for transmission by the protocol machine, and for storing a handshake segment which contains a set of host interrupt flags and a corresponding set of
20 acknowledge flags, and a set of interface interrupt flags and a corresponding set of acknowledge flags; and

25 the interface controller includes first means for toggling one of said host interrupt flags and producing an interrupt to the host processor, and second means which is responsive to an interrupt to the interface controller generated by the host processor to examine the set of interface interrupt flags for one which has been toggled and to toggle its corresponding
30 acknowledge flag.

2. The control system as recited in claim 1 in which the host processor includes third means for toggling one of said interface interrupt flags and producing an interrupt to the interface controller, and fourth means which is responsive
5 to an interrupt to the host processor generated by the interface controller to examine the set of host interrupt flags for one which has been toggled and to toggle its corresponding acknowledge flag.

3. The communications interface circuit as recited in claim 1 in which the message data received by the protocol machine is stored in an indicate FIFO within the shared memory and one of said host interrupt flags is associated with the
5 indicate FIFO, in which the message data from the host processor is stored in a request FIFO within the shared memory and one of said interface interrupt flags is associated with the request FIFO, and

wherein the interface controller is operable in response
10 to the toggling of said one interface interrupt flag to read the message data from the request FIFO and couple it to the protocol machine for transmission on said communications link.

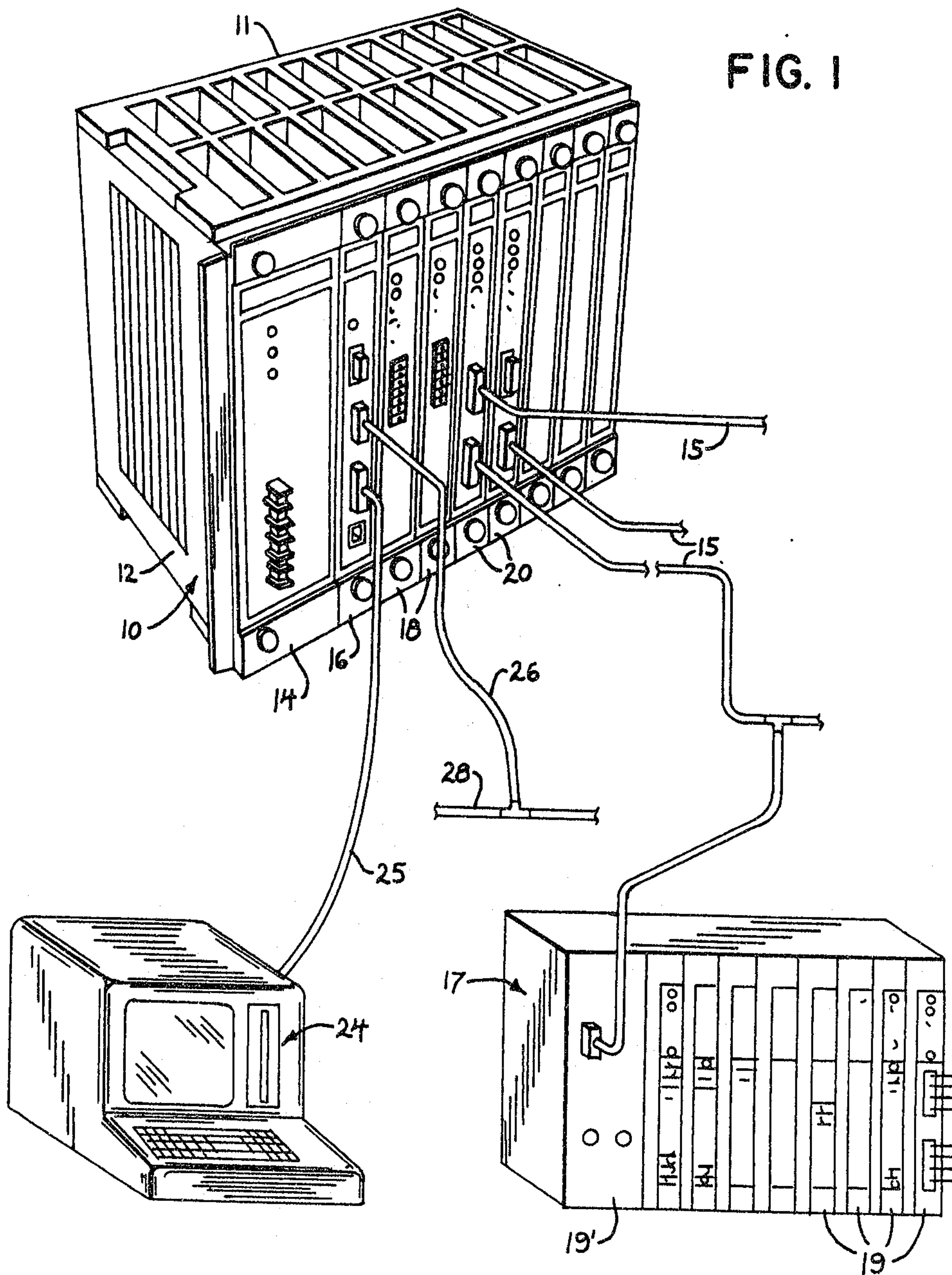
4. The communications interface circuit as recited in claim 3 in which a confirm FIFO is stored in the shared memory and a second one of the host interrupt flags is associated with the confirm FIFO, and

5 wherein the interface controller is operable after coupling message data from the request FIFO to write confirmation message data into the confirm FIFO, to toggle the second one of the host interrupt flags, and to generate an interrupt to the host processor.

5. The communications interface circuit as recited in claim 4 wherein the host processor is operable in response to the toggling of said one host interrupt flag to read the message data from the indicate FIFO.

6. The communications interface circuit as recited in claim 5 in which an accept FIFO is stored in the shared memory and a second one of the interface interrupt flags is associated with the accept FIFO, and

5 wherein the host processor is operable after reading message data from the indicate FIFO to write data into the accept FIFO, to toggle the second one of the interface interrupt flags, and to generate an interrupt to the interface controller.



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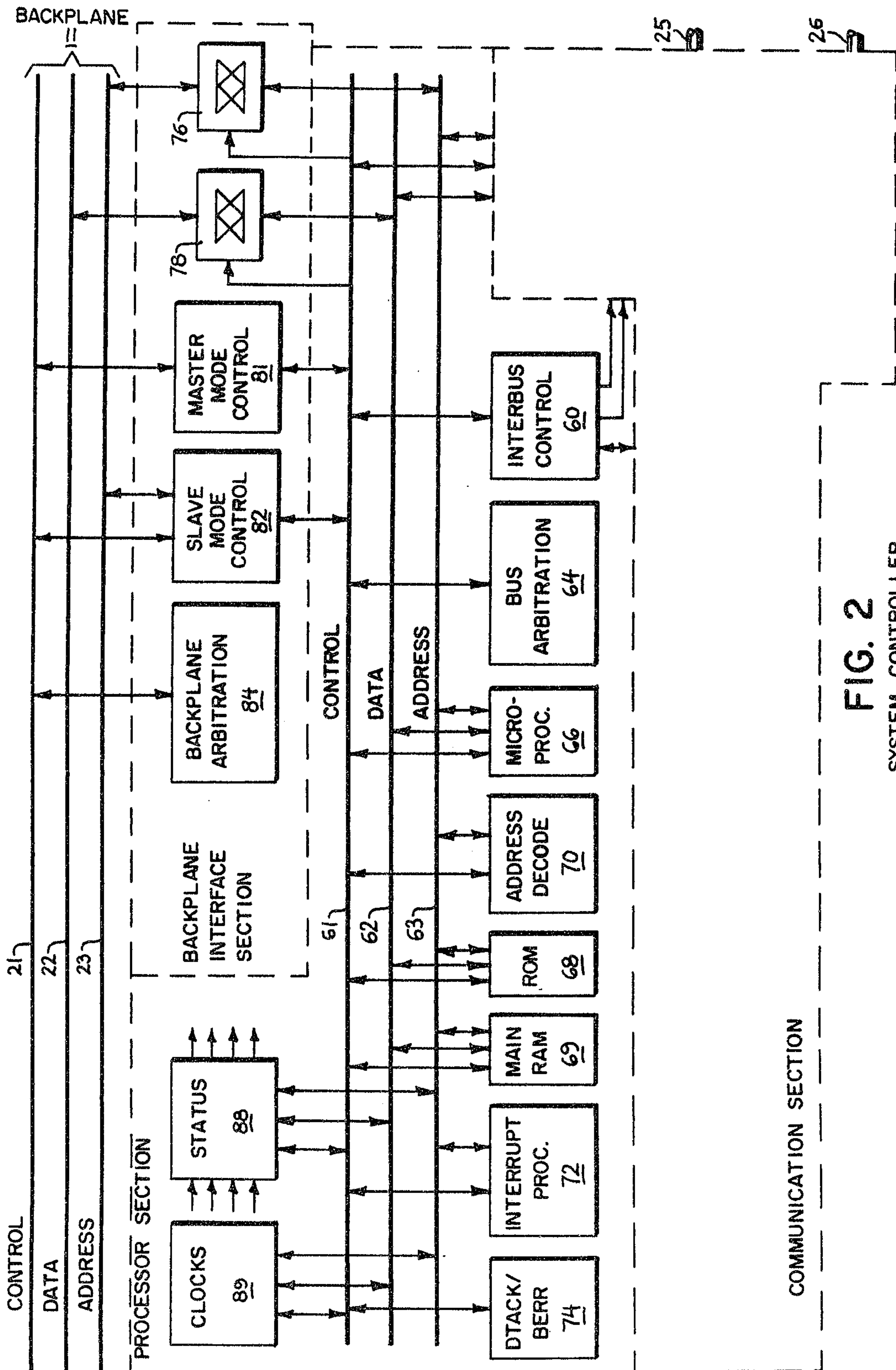
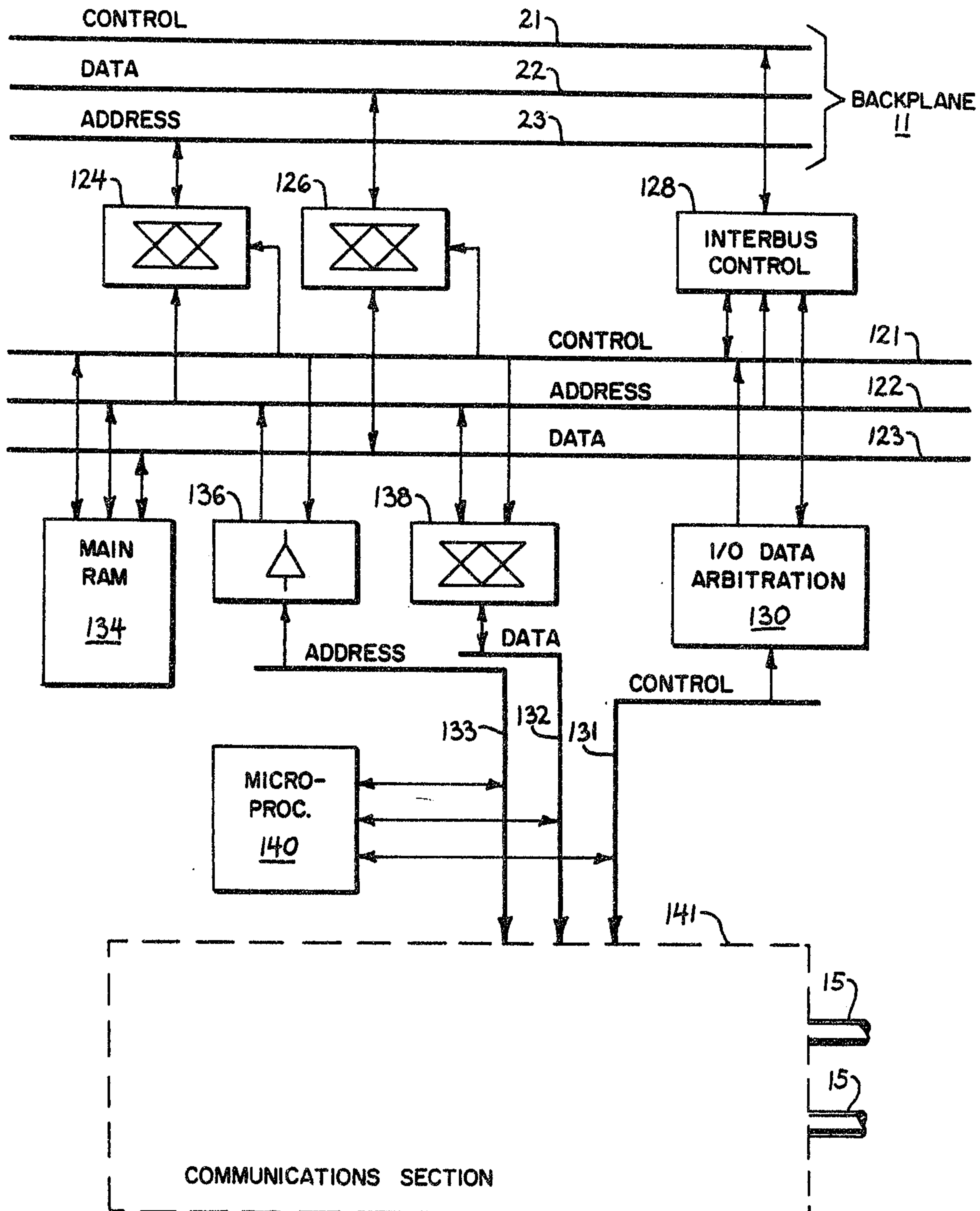


FIG. 2
SYSTEM CONTROLLER

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**FIG. 3**REMOTE I/O
SCANNER MODULE*Pascal & Associates*
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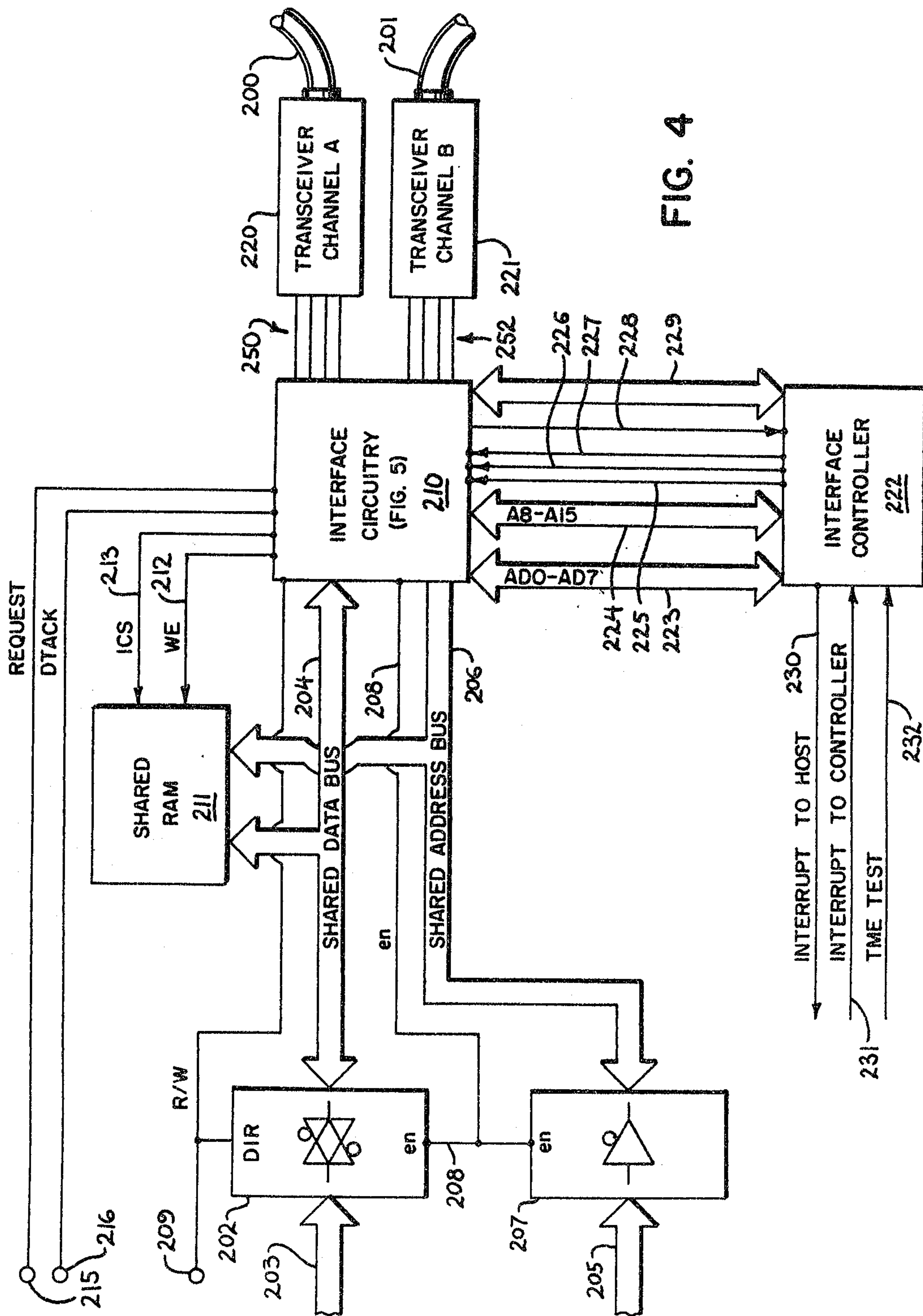


FIG. 4

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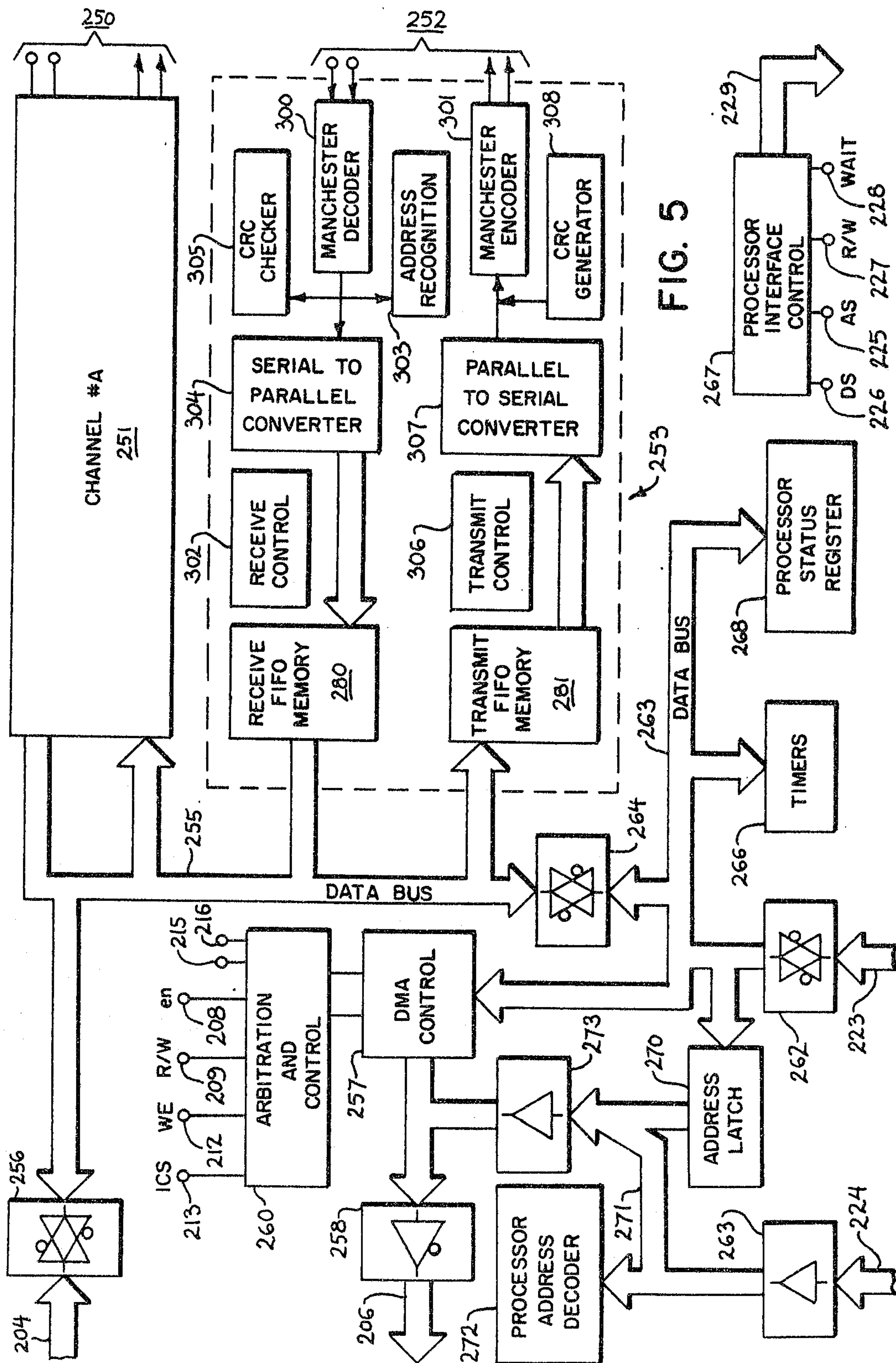


FIG. 5

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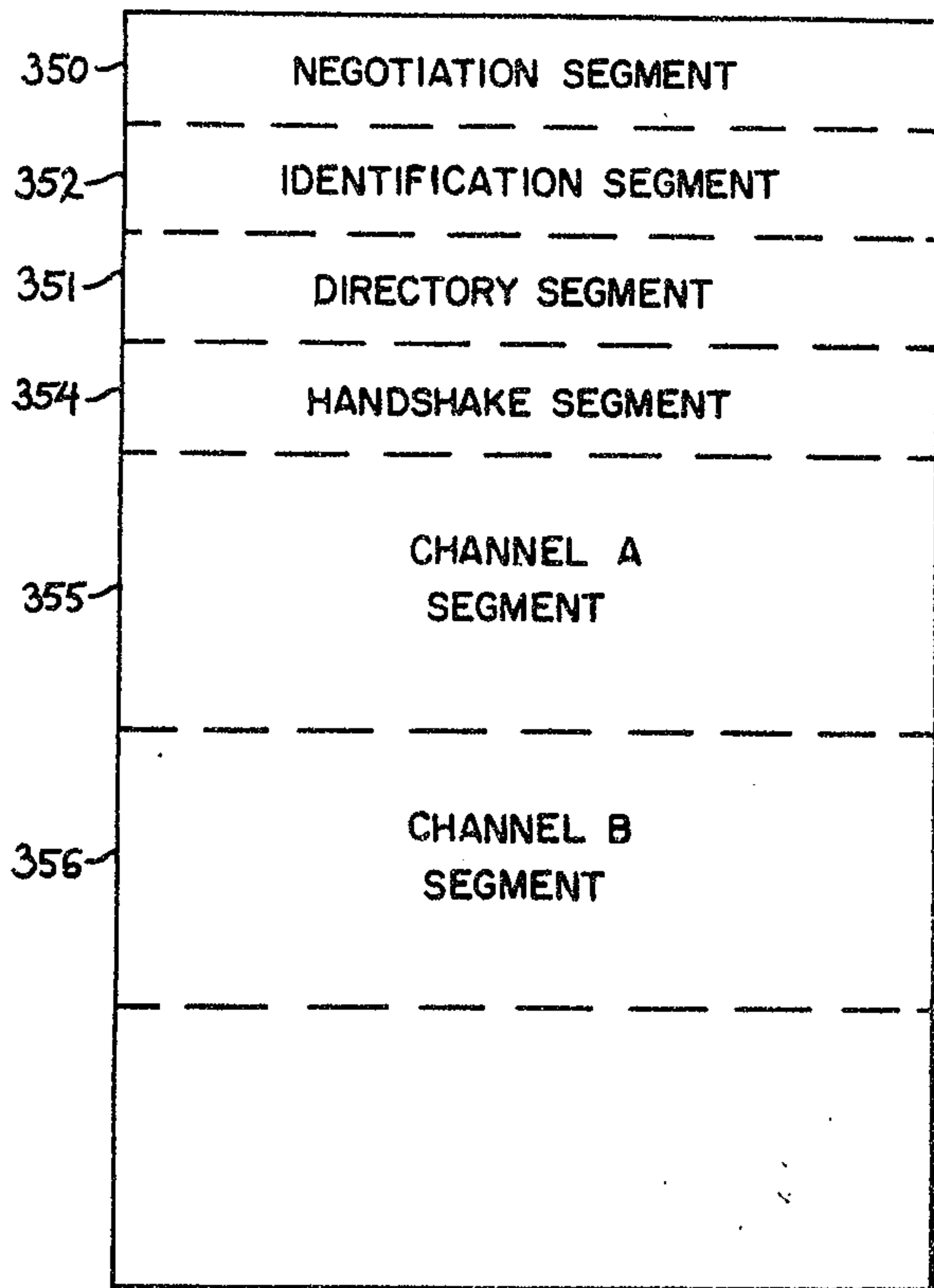


FIG. 6

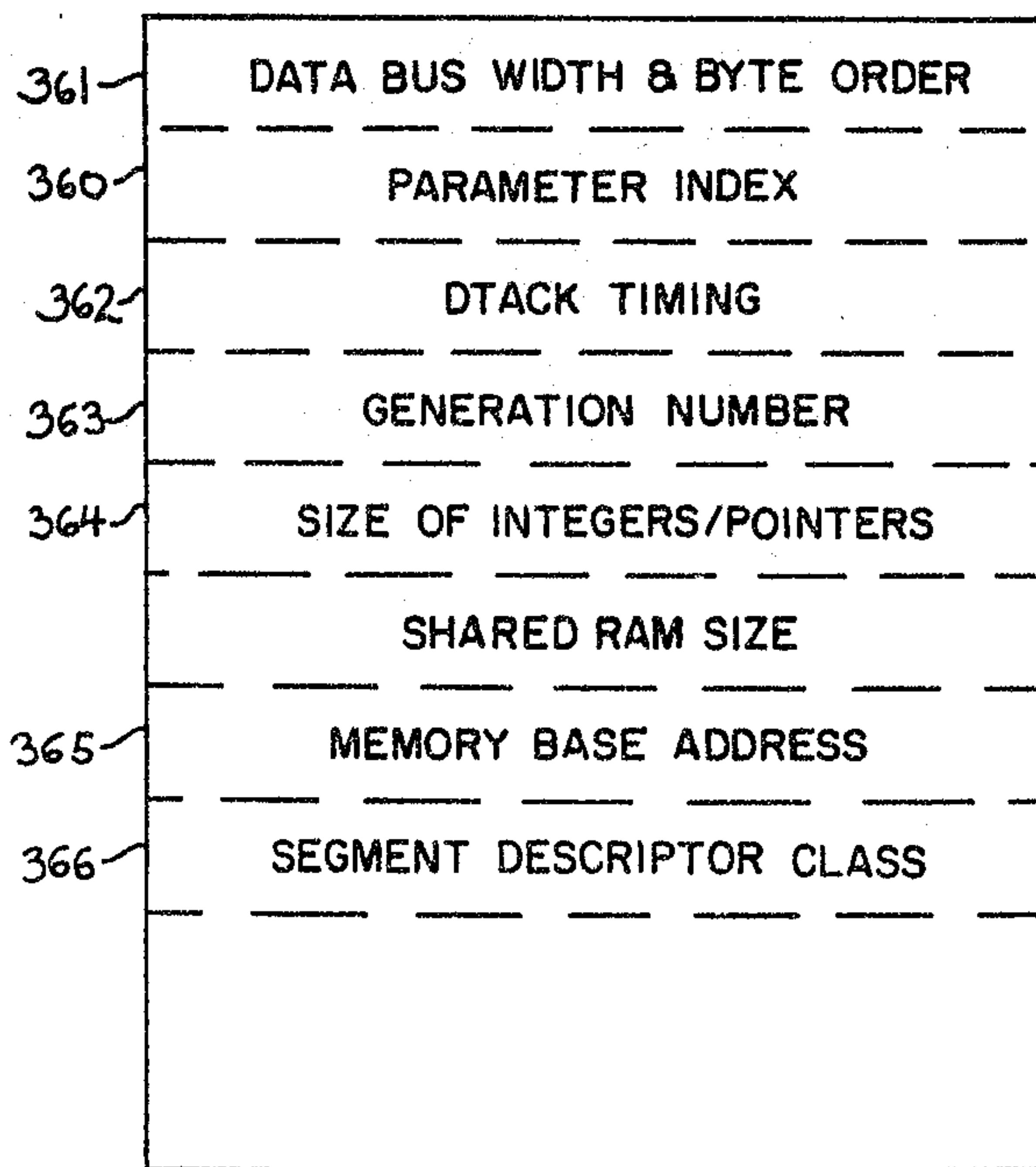


FIG. 7

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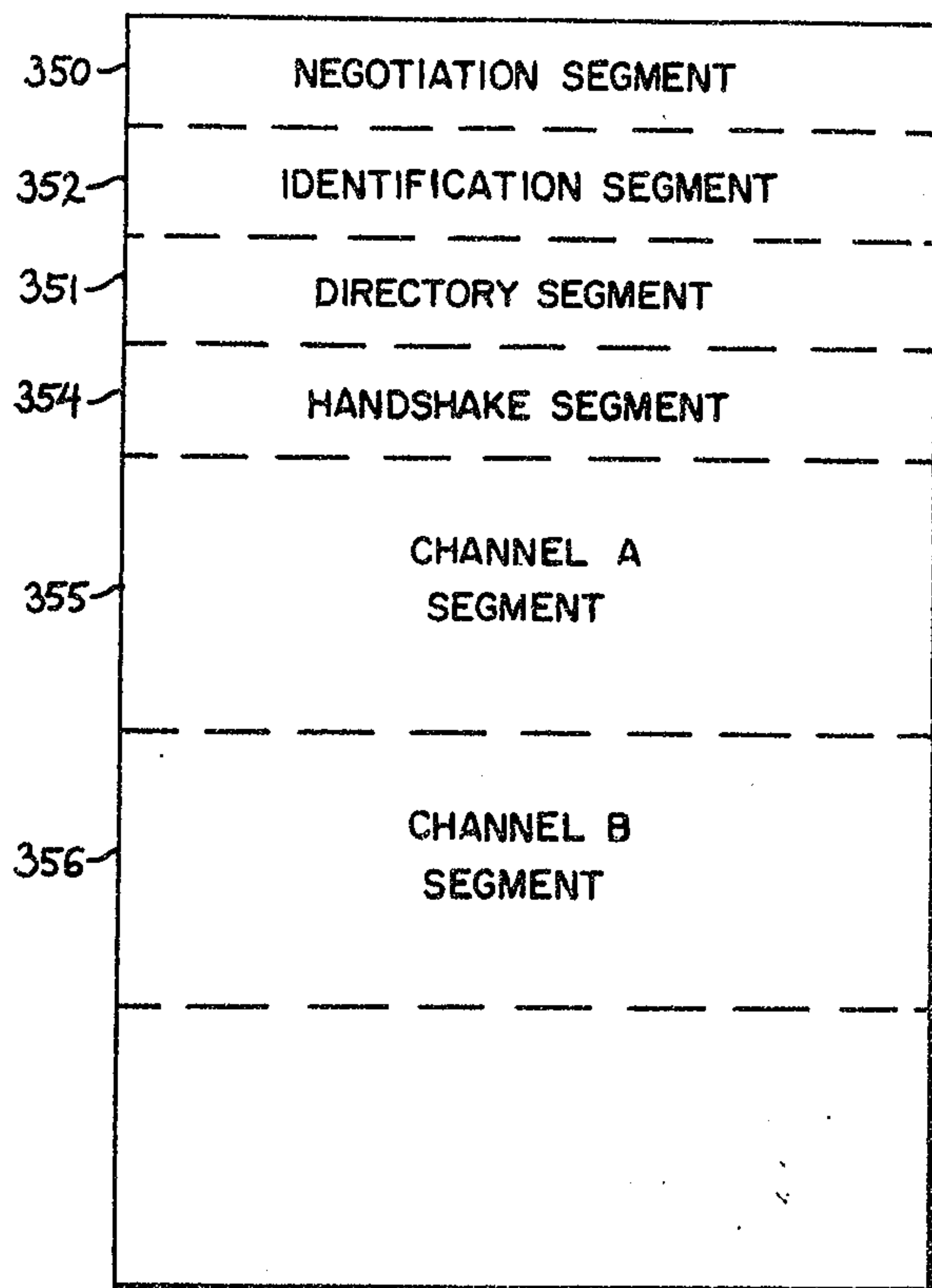


FIG. 6

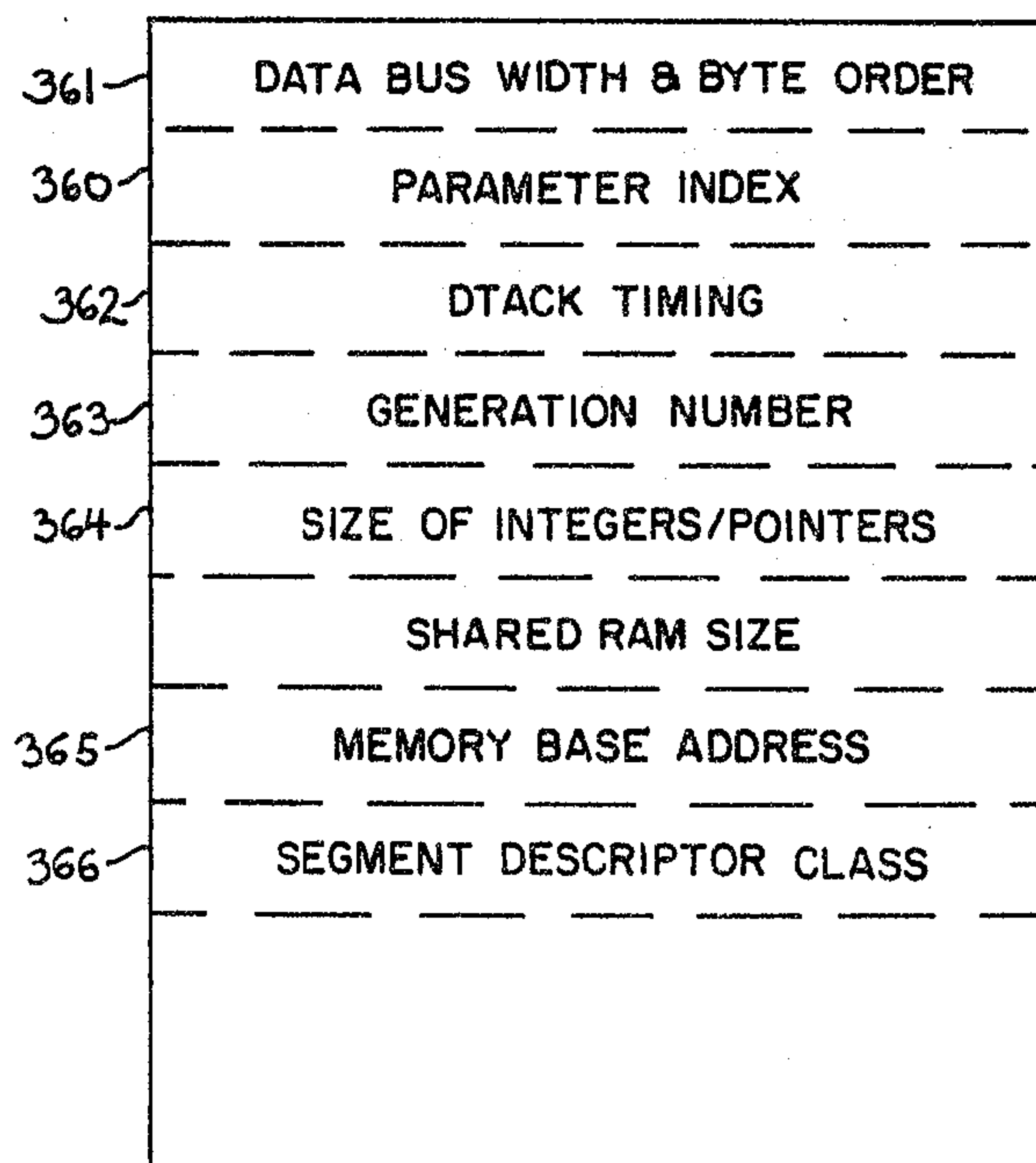
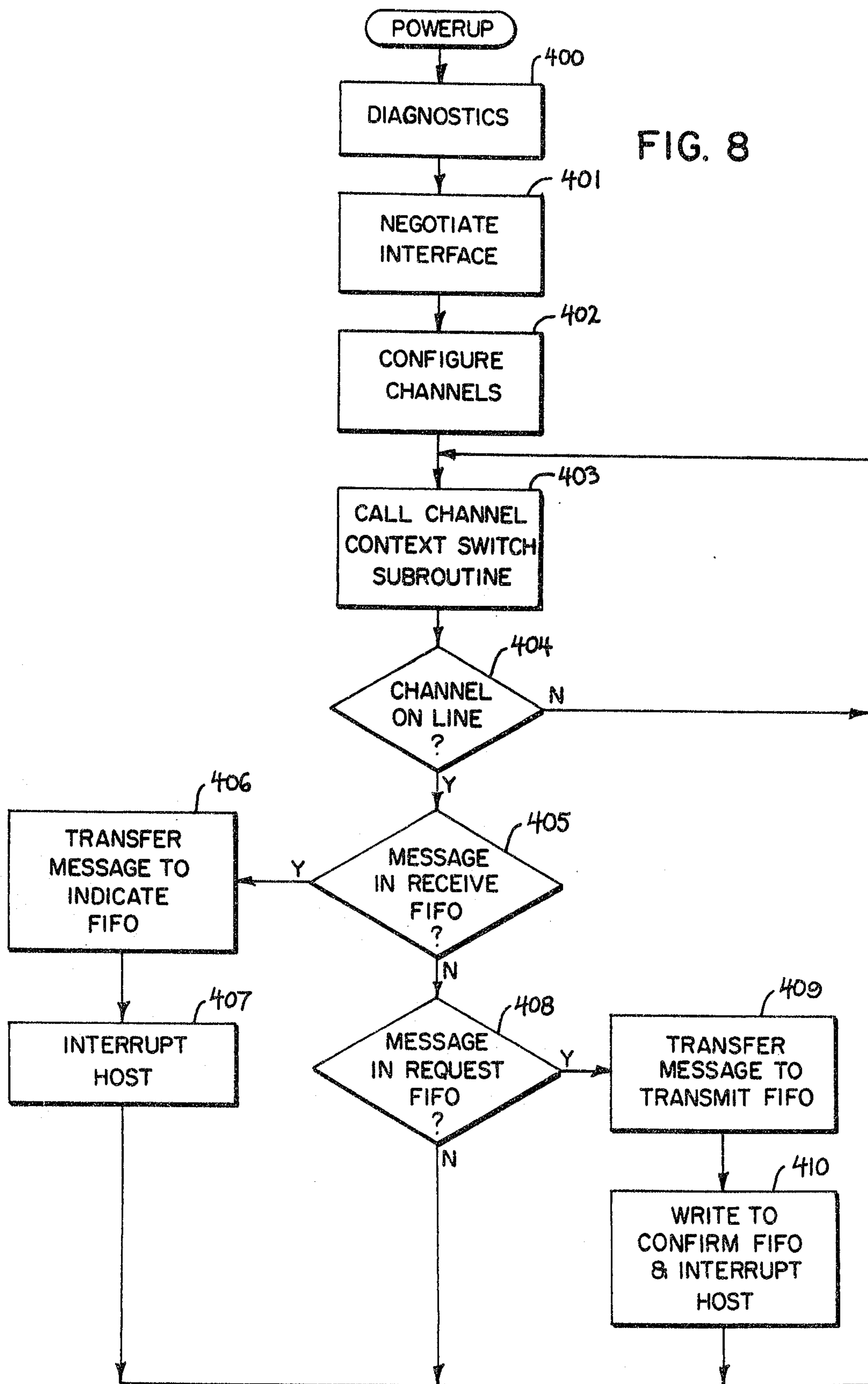


FIG. 7

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FIG. 8



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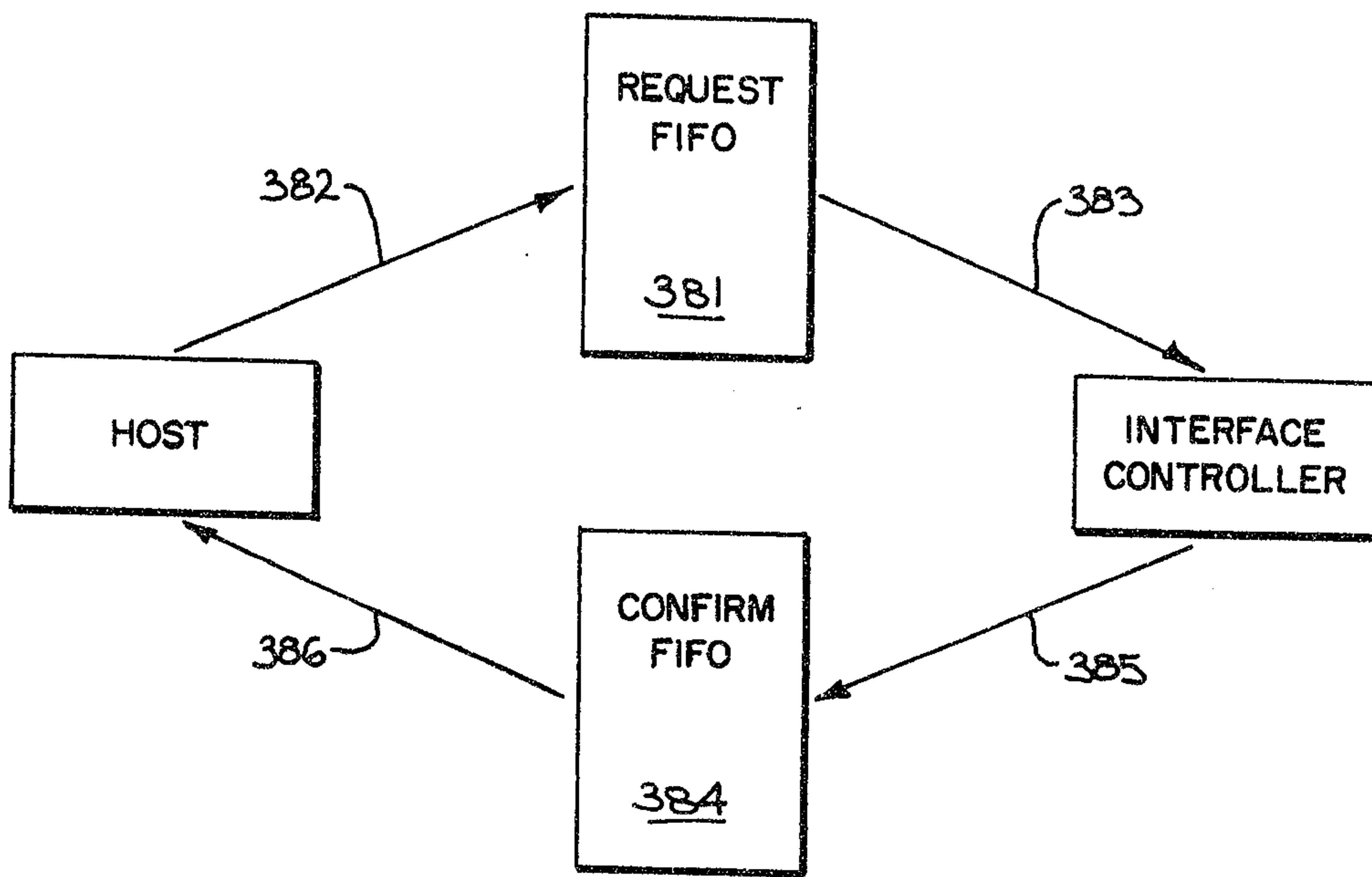
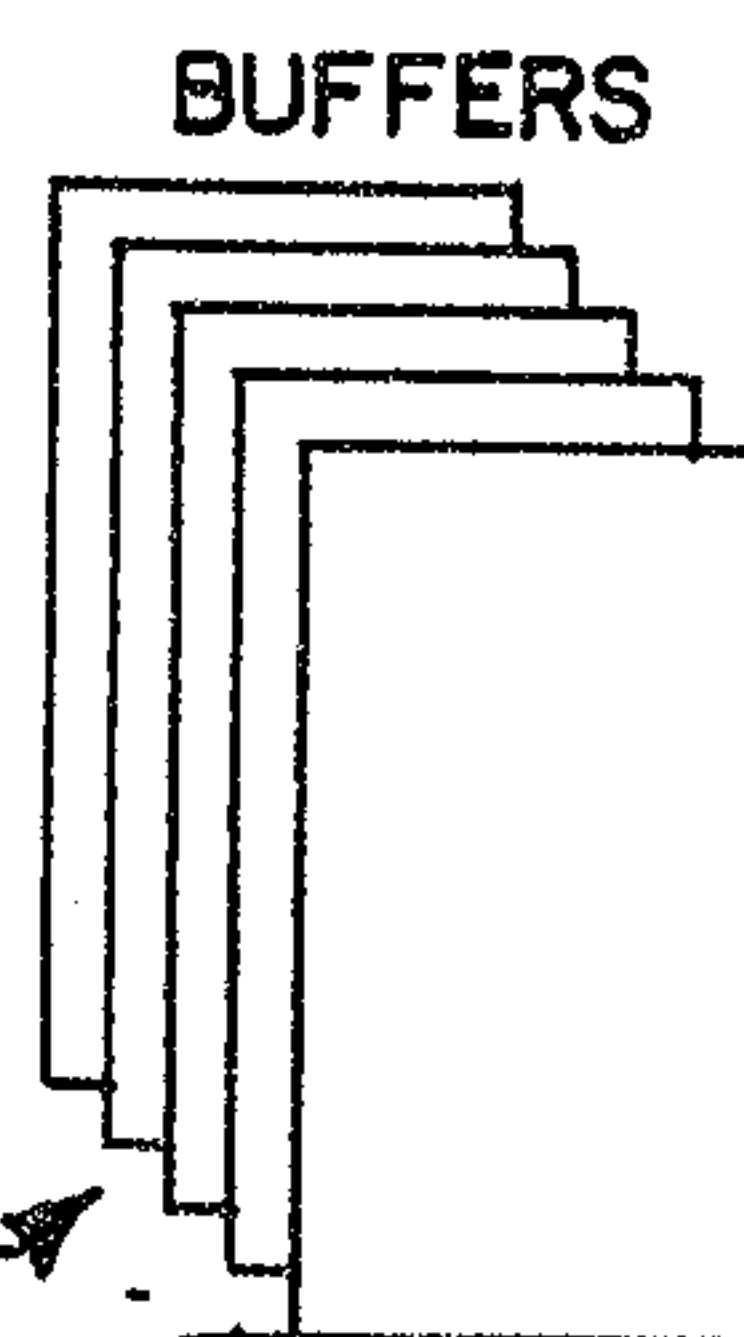
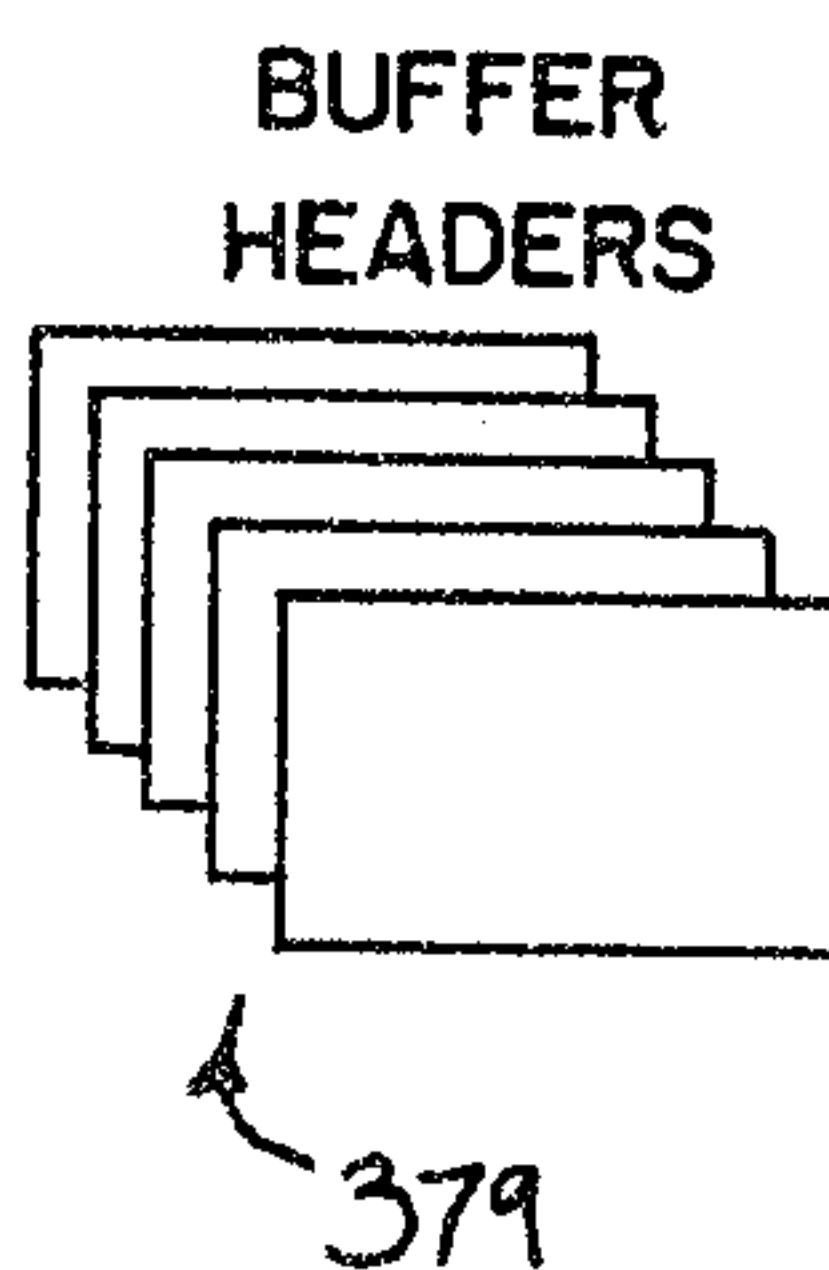
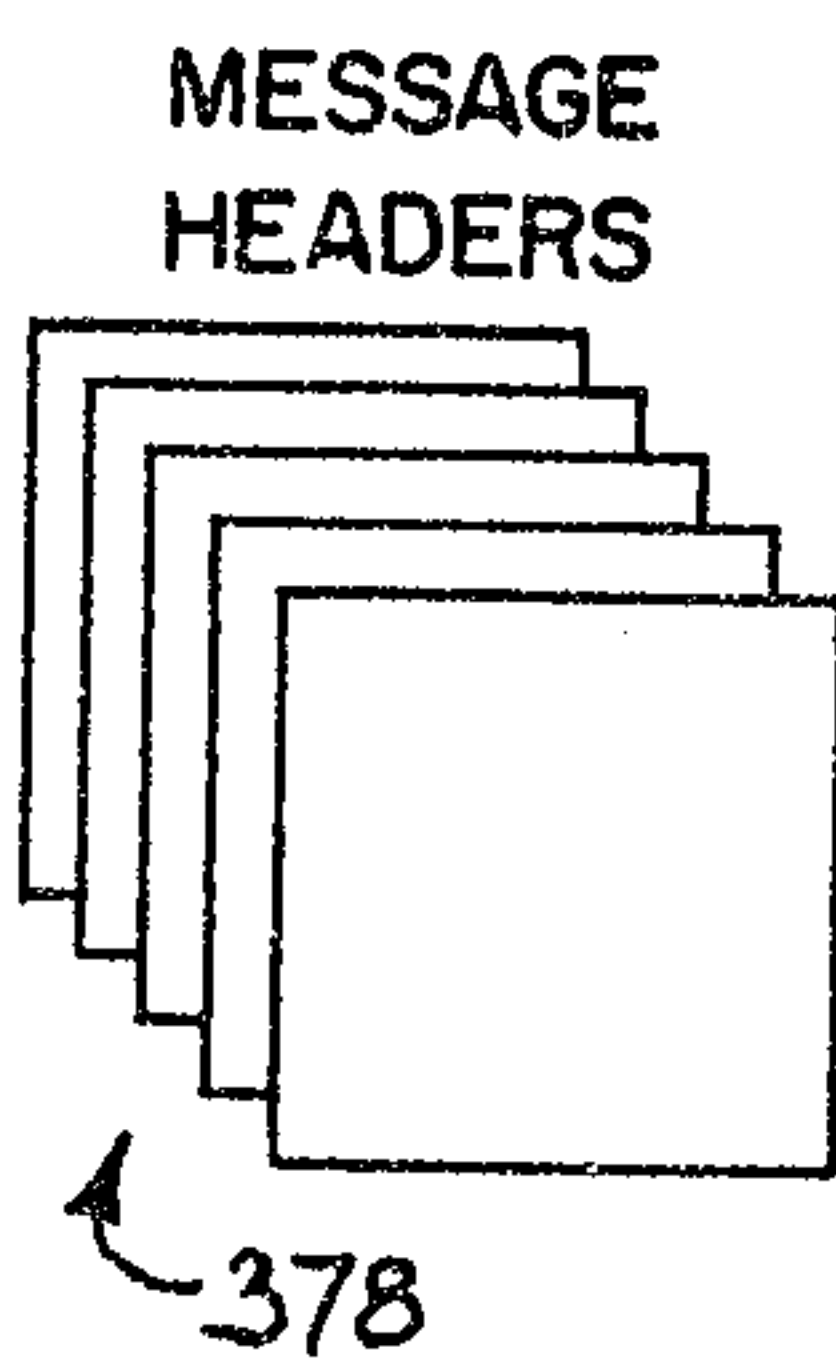
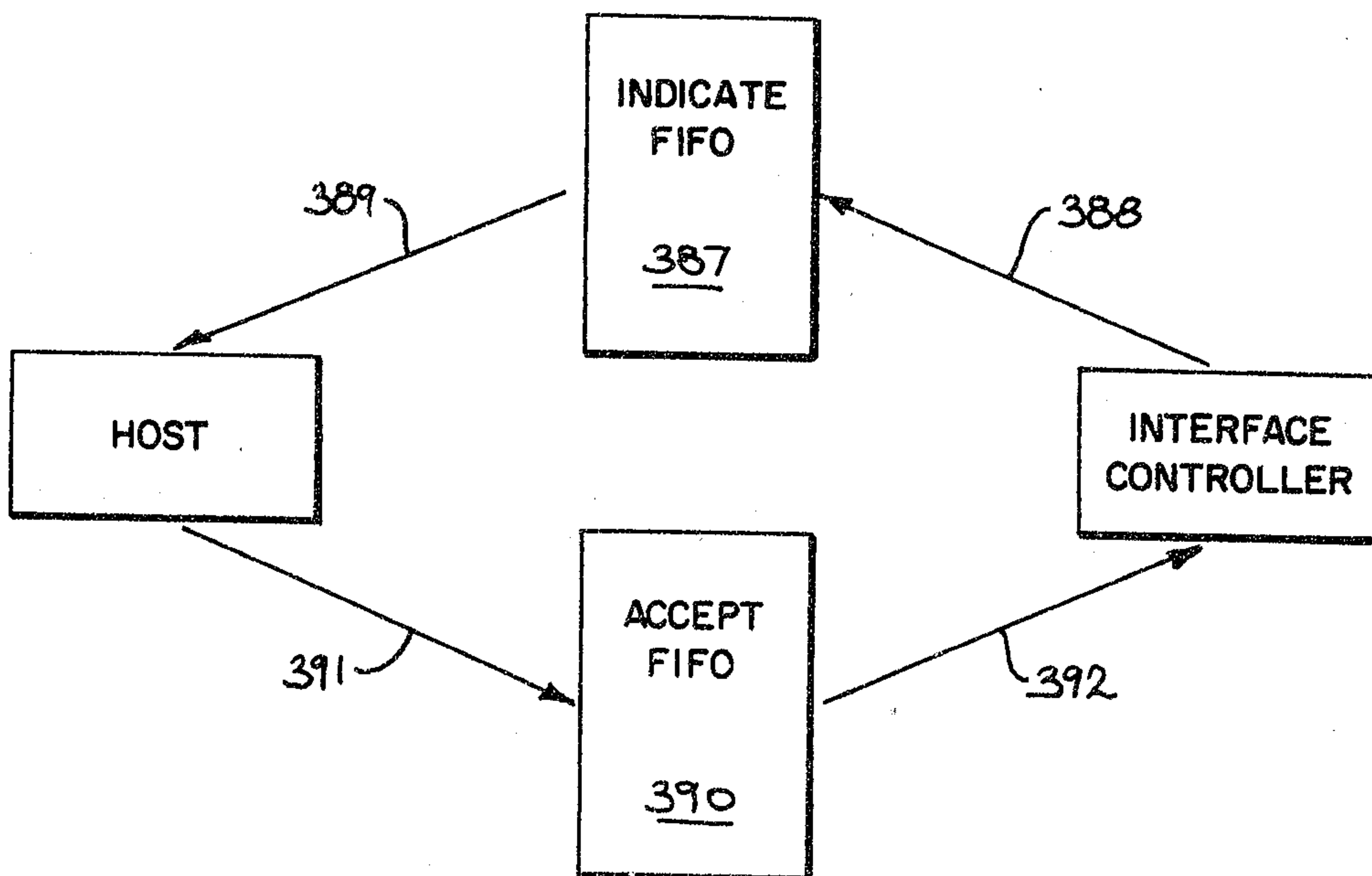


FIG. 10



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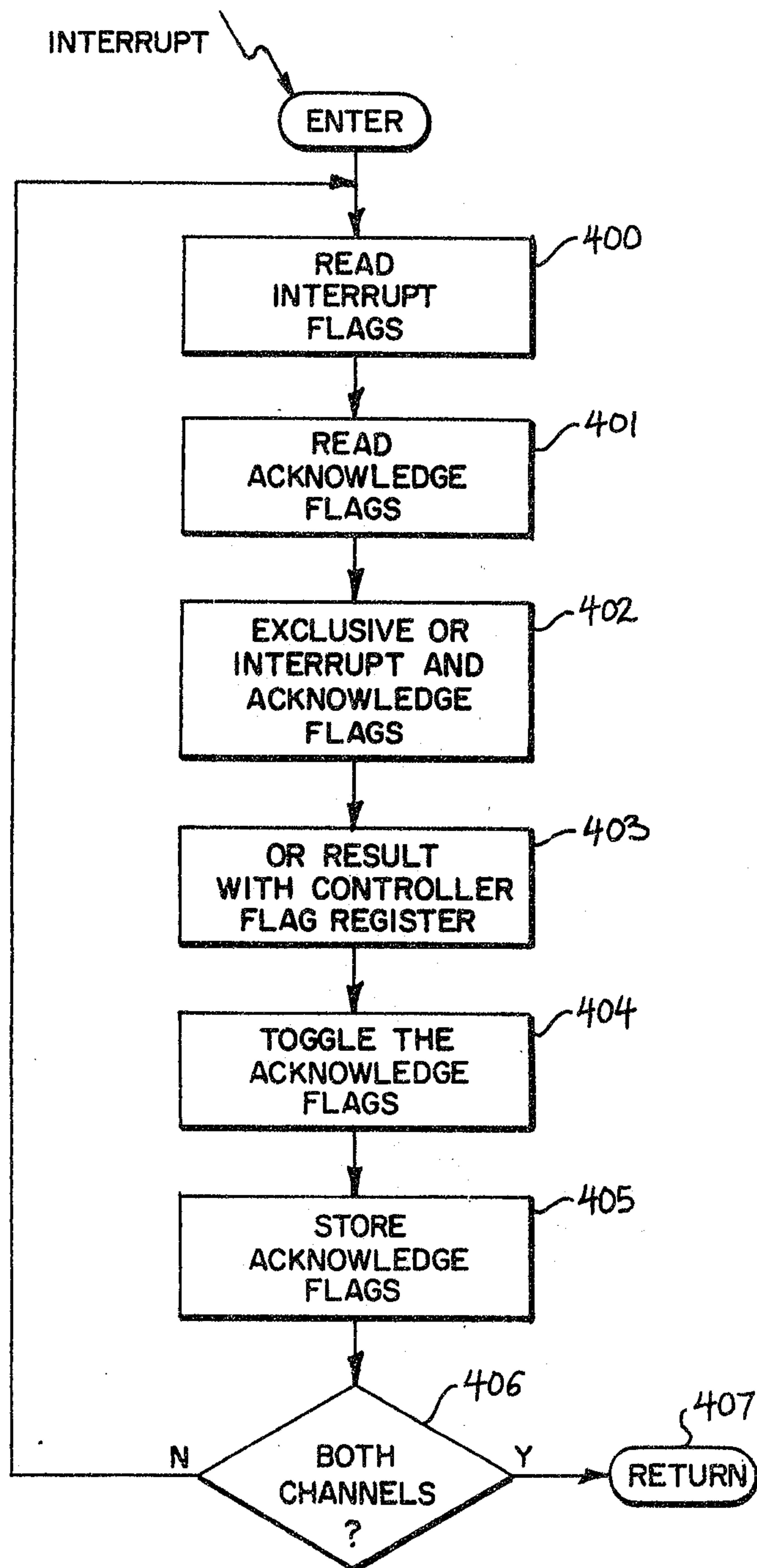


FIG. II

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