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Balise control apparatus

The application relates to a balise control apparatus for controlling at least one balise, comprising a first processing unit configured to generate a first data signal based on a provided first signal term, and a second processing unit configured to generate a further
5 first data signal based on the provided first signal term. Furthermore, the application relates to a system comprising a balise control apparatus and a method for operating a balise control apparatus.

It is known to use balises to influence vehicles, in particular, rail-based vehicles.
10 According to the application, a balise is to be understood as a transmitter that sends data to a vehicle passing the balise. In particular, a balise can be a transmitter arranged in or on a track bed that sends data to rail vehicles passing over or by it.

In the concept of the European Train Control System (ETCS), it is provided that a balise
15 at least partially takes over the influencing of a rail vehicle. The data emitted by a balise can be at least partially displayed to the driver by at least one display device of the rail vehicle and/or at least partially automatically processed by a control device of the rail vehicle and used to control the rail vehicle (e.g. for automatic braking, accelerating, etc.).

20 Basically, a distinction can be made between two different types of balises: Fixed data balises and transparent data balises.

A fixed data balise (also called static balise) is to be understood to be a balise with unchanged data content. The unchanged data content is stored in the fixed data balise.
25 To read the data, the fixed-data balise can be supplied with power, in particular, by the rail vehicle respectively by a reading device arranged on the rail vehicle. The mode of operation of a fixed-data balise is therefore similar to a contactless transponder card. Such a balise has no connection to a data network and does not have its own power supply. In particular, the distance to the next balise can be stored as data content. A rail

vehicle that receives this information from the balise will initiate an emergency stop if it does not detect the next balise within the obtained distance (possibly with a specific tolerance). Exemplary and non-exhaustive further data of a fixed-data balise can be location information, information on the track characteristics of the following track
5 section and speed setpoints and/or limits.

According to the application, a transparent data balise is to be understood to be a balise with variable data content. In other words, such a balise is configured to transmit variable data, for example, variable operating situations (information on the current
10 track conditions of the subsequent track section and/or current speed setpoints and/or speed limits) to a rail-based vehicle. In order to receive variable data, a transparent data balise is therefore connected to a data network.

The variable data content is transmitted in the form of a so-called balise telegram from a
15 (trackside) balise control apparatus (also called balise control unit (BCU)) to the balise. The balise control apparatus in turn receives the data content in the form of a signal term from a (remotely located) data source. For example, the signal term can be transmitted from an electronic interlocking to the balise control apparatus via a data network (e.g. CAN bus network). This allows variable and, in particular, always up-to-
20 date data to be transmitted to the balise in order to transmit these to the vehicles passing the balise.

The power supply of the transparent data balise is usually cable-based. In particular, a sinusoidal voltage (e.g. 22V, 8.82 kHz) can be transmitted from the balise control
25 apparatus via a cable. This sinusoidal voltage is preferably used simultaneously as a carrier signal for the data to be transmitted to the balise. In particular, a Manchester-coded data signal (e.g., 16 V at 564.48 kbit/s) may be added and modulated, respectively, onto the sinusoidal voltage. In other words, the balise control apparatus supplies the balise with power (sine signal) and data (Manchester signal) in the form of
30 a balise telegram.

Since a balise is used, in particular, for controlling a rail vehicle, high safety requirements are demanded on such a system. For example, it must be ensured that the correct data is always transmitted from the balise control apparatus to a balise. For this purpose, a balise control apparatus is designed with two channels so that the data
5 processing in the balise control apparatus corresponds to the so-called safety level 4 (Safety-Integrity-Level SIL 4).

A two-channel design is understood to mean that two separate processing units are provided, each of which comprises suitable computing means, memory means, etc. In
10 the prior art, it is known, in particular, that the two-channel design is implemented by calculating the balise telegram, in particular, the data signal of the balise telegram, on two (separate) hardware platforms. Only if the result of the calculation on the two platforms is the same, the balise telegram is transmitted as a valid signal to the balise. If
15 the two calculations of the data signals from the same signal term do not lead to the same result, the balise control apparatus interrupts the voltage supply to the balise and the balise is set to a safe operating state.

In the following, a conventional system 100 comprising a balise control apparatus 102 known in the prior art is described in more detail with reference to Figure 1.

20

The system 100 comprises a data source 106, a balise control apparatus 102, and a balise 104 fixedly associated with the balise control apparatus 102. The balise control apparatus 102 comprises two processing units 108, 110 in the form of microprocessors 108, 110, two comparators 112, 114, a disabling unit 116, an AND gate 124, a control
25 signal generating unit 126 in the form of an adder 126, an amplifier 128, and a sinusoidal signal generator 130.

The data source 106 provides the data to be sent to the balise 104 in the form of a signal term 132 (shown schematically). The same signal term 132 is provided to the first
30 processing unit 108 and the second processing unit 110. Based on the provided signal term 132, the respective processing unit 108, 110 each generates a data signal 136 and a

data stream 136, respectively. In particular, the data signal 136 may be a Manchester-encoded data signal 136.

In order to ensure that the correct data is generated for the balise 104, each
5 microprocessor 108, 110 is configured to pass the respective generated data signal 136 to both the first comparator 112 and the second comparator 114. A comparator 112, 114 and a comparison logic circuit 112, 114, respectively, compares the two received data signals 136 with each other. The comparison result (yes = data signals are identical; no (not shown) = data signals are not identical) is forwarded by each comparator 112,
10 114 respectively to the AND gate 118 of the disabling unit 116. Only when both comparison results are positive (i.e., yes is output) the switches 120 and 122 of the shutdown device 116 are closed. By closing the switches 120, 122, the respective data signals 136 can be forwarded to the AND element 124.

15 The resulting data signal 136 is output to the control signal generating unit 126. The control signal generating unit 126 generates the balise telegram 138 from the data signal 136 and the provided sine signal 140 by adding and modulating, respectively, the data signal 136 onto the sine signal 140. Before the balise telegram 138 is transmitted, this signal 138 can still be amplified by an amplifier 128. Then, the balise telegram 138 is
20 transmitted to the balise 104 via a data line.

As can be seen from the foregoing, the structure and operation of a known balise control apparatus 102 is elaborate and complex.

25 For example, in order to meet the requirements of two-channel design, the disabling unit 116 comprises two switches 120, 122 to ensure that at least one switch 120, 122 is open in the event of a negative comparison result. In addition, such disabling units 116 require that a functional test has to be performed periodically to verify that the disabling unit 116 is operating correctly. For example, it is not certain that a switch 120, 122
30 which is actuated with the command "open" actually opens. Thus, in the present disabling unit 116, the desired disconnection may have been effected by only one of the

two switches 120, 122, while the other switch 120, 122 may be defective and therefore closed.

In order to detect this condition, it is necessary to regularly perform a function test of
5 both switches 120, 122. For this purpose, with the first switch 120 closed, the other switch 122 is opened and it is verified that no signal arrives at its output. The test is repeated with switch 122 closed and switch 120 open. These tests require that two meters (not shown) has to be used.

10 Thus, the design and operation of a known balise control apparatus are costly and complex.

Furthermore, a method for transmitting use data dA, dB in parallel via at least two transmitters, two channels and two receivers from a message source to a message sink
15 is known from EP 0 738 973 A1, wherein the use data dA, dB to be transmitted are supplied to the transmitters and to at least one reference data generator which outputs reference data a; b which are selected as a function of an event which has occurred when the associated user data dA, dB arrive, the reference data a; b being transmitted by the transmitter via the associated channel and via the adjacent transmitter and the adjacent
20 channel, and the transmitted reference data a, a' or b, b' are transmitted by the receivers to at least one comparator which compares the reference data a and a' or b and b' with one another or checks them for correctness.

Further, CN 102 857 366 A discloses a trackside electronic device comprising a
25 responder interface module and a main control module, wherein the main control module is used for receiving message data of a responder from a train control station, for buffering the message data of the responder, and for respectively converting the message data into first channel serial data and second channel serial data from parallel data; the serial data of the first channel and the serial data of the second channel are
30 respectively converted into parallel data of the first channel and parallel data of the second channel; if the parallel data of the first channel and the parallel data of the second channel are identical to the cached message data of the responder, and the serial

data of the first channel is identical to the serial data of the second channel, either the serial data of the first channel or the serial data of the second channel is transmitted to the responder interface module and the responder interface module is used to convert the received first channel serial data or second channel serial data from the main control
5 module into analog signals matched with the responder and to output the analog signals to the responder.

The object of the application is to provide a balise control apparatus which meets the so-called safety level 4 and comprises a less complex structure and, in particular, can be
10 operated in a simpler manner.

According to a first aspect of the application, the objection is solved by a balise control apparatus for controlling at least one balise according to claim 1.

15 In contrast to the prior art, according to the application a balise control apparatus is provided which meets the safety level 4 requirement and has a less complex structure and, in particular, can be operated in a simpler manner. This is achieved by the fact that one of the two processing units is additionally configured to perform the at least one comparison operation and to output a carrier signal depending on the comparison
20 result. This enables a two-channel operation of a balise control apparatus without a complex disabling device.

The balise control apparatus according to the application comprises a first processing unit and a second processing unit for a two-channel operation. In operation of the balise
25 control apparatus, at least a first signal term is provided to each processing unit. A first signal term is associated with a data content to be transmitted by a first balise as a balise telegram. The balise to be controlled is, in particular, a transparent data balise which is, in particular, permanently assigned to the balise control apparatus.

30 The first processing unit and the second processing unit each comprise suitable computing means for generating a first data signal and a first data stream, respectively, based on the provided first (digital) signal term. In particular, the first data signal is

formed such that it can be transmitted to the first balise by means of a second carrier signal. Preferably, the first data signal can be a Manchester-coded data signal (e.g. 16 V with 564.48 kbit/s). For the generating, in particular, for the calculating, of the first data signal and the further first data signal, (identical) generation rules (e.g. at least one
5 conversion table or look-up table or the like) can be stored in each case in the first processing unit and in the second processing unit.

At least the second processing unit comprises a second comparator and a second comparison logic, respectively. The second comparator is configured to compare the two
10 generated first data signals with each other. In particular, the first processing unit provides the first data signal generated by the first processing unit to the second processing unit via a communication link between the processing units. In a second comparison step, the second comparator performs a comparison between this provided first data signal and the further first data signal generated by the second processing unit.

15

The first processing unit is further configured to output respectively forward the first data signal generated by the first processing unit to a first control signal generating unit. The second processing unit is configured to output respectively forward a second carrier signal to the first control signal generating unit. A carrier signal may, in particular, be a
20 sinusoidal signal, such as a sinusoidal voltage (e.g. 22V; 8.82 kHz). A control signal generating unit according to the application (e.g. an adder) is, in particular, configured to add and modulate, respectively, a received data signal onto a received carrier signal.

According to the application, it is provided that the second carrier signal is output to the
25 first control signal generating unit depending on the comparison result of the second comparison step. According to the present application, this means, in particular, that the second carrier signal is only output if the second comparison result is positive.

If the comparison result is negative, the second processing unit can prevent the second
30 carrier signal from being output. As a result, the balise is not activated and is set to a safe operating state, for example.

A positive comparison result means, in particular, that a data signal generated by the first processing unit based on a specific signal term is equal to a data signal generated by the second processing unit based on the same specific signal term. In this way, two-channel operation can be ensured.

5

According to a first and particularly preferred embodiment of a balise control apparatus according to the application, the second processing unit may be configured to generate a second data signal based on a provided second signal term. The first processing unit may be configured to generate a further second data signal, based on the provided
10 second signal term. The first processing unit may comprise a first comparator. The first comparator may be configured to compare the further second data signal generated by the first processing unit and the second data signal generated by the second processing unit in a first comparison step. The second processing unit may be configured to output the generated second data signal to a second control signal generating unit. The first
15 processing unit may be configured to output a first carrier signal to the second control signal generating unit. The output of the first carrier signal may depend on the comparison result of the first comparison step.

According to the application, it has been recognized, in particular, that a particularly
20 efficient operation of a balise control apparatus can be achieved if the hardware components required for two-channel operation, in particular, the two processing units, are used to control two balises.

Preferably, the balise control apparatus can be configured for (at least partial) parallel
25 processing of a first signal term and a second signal term for a first balise to be controlled and a second balise to be controlled. Each processing unit can, e.g. based on stored generation rules, (at least partially) generate a first data signal from a first signal term and a second data signal from a second signal term in parallel. Likewise, each processing unit may have a comparator, respectively, to perform the first and second
30 comparison step described above. Depending on the comparison result, each processing unit may output (or not output) a carrier signal. As has already been described, this

means, in particular, that a carrier signal is only output if the comparison result is positive (i.e. if the respective data signals are the same).

According to this preferred embodiment, the balise control apparatus may be formed as follows: The balise control apparatus comprises a first processing unit. The first processing unit is configured to generate a first data signal based on a provided first signal term, and to generate a further second data signal based on a provided second signal term. The balise control apparatus comprises a second processing unit. The second processing unit is configured to generate a second data signal based on the provided second signal term, and to generate a further first data signal based on the provided first signal term. The first processing unit comprises a first comparator. The first comparator is configured to compare the further second data signal generated by the first processing unit and the second data signal generated by the second processing unit in a first comparison step. The second processing unit comprises a second comparator. The second comparator is configured to compare the further first data signal generated by the second processing unit and the first data signal generated by the first processing unit in a second comparing step. The first processing unit is configured to output the generated first data signal to a first control signal generating unit and to output a first carrier signal to a second control signal generating unit. The output of the first carrier signal depends on the comparison result of the first comparison step. The second processing unit is configured to output the generated second data signal to the second control signal generating unit and to output a second carrier signal to the first control signal generating unit. The output of the second carrier signal depends on the comparison result of the second comparison step.

As has already been described, a control signal generating unit may be configured to generate a balise telegram by adding and modulating, respectively, a received data signal onto a received carrier signal. For example, an adder circuit may be provided as a control signal generating unit. Preferably, the balise control apparatus may comprise the first control signal generating unit. In particular, the first control signal generating unit may be integrated into the balise control apparatus. The first control signal generating unit may be configured to generate a first balise telegram based on the first data signal

and the second carrier signal. Alternatively or (preferably) additionally, the balise control apparatus may comprise the second control signal generating unit. In particular, the second control signal generating unit may be integrated in the balise control apparatus. The second control signal generating unit may be arranged to generate a
5 second balise telegram based on the second data signal and the first carrier signal. By preferably integrating both control signal generating unit in the balise control apparatus, a compact balise control circuit can be provided.

In order to obtain a particularly reliable comparison result, according to a further
10 embodiment of the balise control apparatus according to the application, the first comparator can be configured to compare bit by bit the further second data signal generated by the first processing unit and the second data signal generated by the second processing unit. Alternatively or (preferably) additionally, the second
15 comparator may be configured to compare bit by bit the further first data signal generated by the second processing unit and the first data signal generated by the first processing unit. By comparing the respective bits of two data signals, even a deviation in only one bit can be reliably detected. In particular, a comparison step can be performed sequentially (bit-by-bit) and in real time. This allows the output of a carrier signal to be
20 immediately interrupted as soon as a deviation between two bits is detected, i.e., a negative comparison result is present. In other words, the carrier signal can be output by a processing unit (only) as long as the comparison result is/remains positive.

According to a preferred embodiment of the balise control apparatus according to the application, the first processing unit may comprise a first carrier signal generator. The
25 first carrier signal generator may be configured to generate the first carrier signal. In particular, the first carrier signal generator may be a sinusoidal generator for generating a sinusoidal signal, in particular, a sinusoidal voltage, as the first carrier signal.

Alternatively or (preferably) additionally, the second processing unit may comprise a second carrier signal generator. The second carrier signal generator may be configured
30 to generate the second carrier signal. In particular, the second carrier signal generator may be a sinusoidal generator for generating a sinusoidal signal, in particular, a

sinusoidal voltage, as the second carrier signal. Such a carrier signal can additionally be used to supply power to the corresponding balise.

5 Preferably, the first carrier signal generator may be configured to output the first carrier signal only in case of a positive comparison result (i.e. the compared second data signals are equal) of the first comparison step. Alternatively or (preferably) additionally, the second carrier signal generator may be configured to output the second carrier signal only in case of a positive comparison result (i.e. the compared first data signals are equal) of the second comparison step. In particular, the respective carrier signal
10 generator can be communicatively connected to the respective comparator such that, at least upon a detecting of a negative comparison result, the generating and/or outputting of the respective carrier signal is (immediately) interrupted and stopped, respectively.

15 Since the comparison of the data signals is preferably bit-by-bit, a negative comparison result can also be caused by the processing units not operating synchronously or by the synchronicity of the processing units being lost due to a malfunction. According to an embodiment according to the application, therefore, in the case of a negative comparison result, the handshake method described further below may be performed for synchronization, and then a new comparison step described previously may be
20 performed. In case of a positive comparison result, the output of the carrier signal can be restarted. Preferably, the balise control apparatus can be taken out of operation if, in particular after several, e.g. 10, synchronization attempts, no positive comparison result has been obtained.

25 According to a particularly preferred embodiment of the balise control apparatus, the first processing unit and the second processing unit can be synchronized with each other. By synchronizing the processing units with respect to time, it can be ensured that the bits of the data signals corresponding to each other are compared in a comparison step. For synchronization, a first request signal of the first processing unit can be
30 transmitted from the first processing unit to the second processing unit, in particular, when the balise control apparatus is initialized and/or when the signal term changes and/or when a negative comparison result is obtained. In addition, a second

acknowledgement signal of the second processing unit can, in particular, be transmitted from the second processing unit to the first processing unit for synchronization.

Alternatively or additionally, a second request signal of the second processing unit can be transmitted from the second processing unit to the first processing unit. In addition, a
5 first acknowledgement signal of the first processing unit can, in particular, be transmitted from the first processing unit to the second processing unit for synchronization.

It has been further recognized that, for example, due to a systematic error in a
10 generation rule, both the first and the second processing units may generate the same incorrect data signal. In order to further increase reliability and safety, according to a further embodiment of the balise control apparatus according to the application, it is proposed that the first processing unit may comprise a first verifier. The first verifier may be configured to check the plausibility and/or decode the second data signal
15 generated by the second processing unit. Alternatively or (preferably) additionally, the second processing unit may comprise a second verifier. The second verifier may be configured to check the plausibility and/or decode the first data signal generated by the first processing unit. In a plausibility check, the verifier can, in particular, check a generated data signal to see whether its structure (e.g., header, checksums, certain bit
20 sequences or the like) corresponds to the structure of a (standard) balise telegram. For this purpose, the verifier can divide the data signal to be checked by a check polynomial, in particular, and if the polynomial division yields the result "zero", the structure of the checked data signal corresponds to the expected structure of a balise telegram. Alternatively or additionally, the verifier may decode a generated data signal, in
25 particular, by means of decoding rules (e.g., at least one conversion table or look-up table or the like), which may be stored in a processing unit. In particular, the decoding may determine the signal term or a data set corresponding to the signal term that was used to generate the data signal. This decoding can enable a check to be made as to whether a correct generating of a data signal by a processing unit has been made.

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Particularly preferably, the first processing unit may comprise a first evaluation module. The first evaluation module can be configured to check whether the data checked by the

first verifier based on the second data signal correspond to the structure of a balise telegram and/or whether the data correspond to the second signal term provided. Alternatively or (preferably) additionally, the second processing unit may comprise a second evaluation module. The second evaluation module may be configured to check
5 whether the data checked by the second verifier from the first data signal correspond to the structure of a balise telegram and/or whether the data correspond to the provided first signal term. For example, the first verifier may be configured to check the second data signal received from the second processing unit by polynomial division to determine whether it corresponds to the structure of a (standard) balise telegram. In
10 addition, the first verifier may be configured to decode the second data signal and to transmit the decoded data to the first evaluation module for comparison with the second signal term. Alternatively or (preferably), the second verifier may be configured to check the first data signal received from the first processing unit by polynomial division to determine whether it corresponds to the structure of a (standard) balise telegram. In
15 addition, the second verifier may be configured to decode the first data signal and to transmit the decoded data to the second evaluation module for comparison with the first signal term. In a comparison, it may be determined whether the signal term provided for generating a data signal is identical to the signal term determined by decoding the data signal. If intermediate data is generated in an intermediate step during the generation of
20 a data signal from a signal term, this data can also be used for the check, in particular, the comparison.

In case of a positive comparison result, i.e. if for example the polynomial division provides the value "zero" or/and if the respective signal terms (or intermediate data)
25 are equal, a correct generation of the data signal by a processing unit can be assumed. In the case of a negative comparison result, i.e., when a deviation between the respective signal terms (or intermediate data) is detected, a faulty operation of the balise control apparatus can be derived. In response to a negative comparison result, output of a carrier signal by a processing unit may be interrupted. Preferably, the outputting of the
30 first carrier signal and of the second carrier signal may be stopped. According to an embodiment according to the application, in the case of a negative comparison result, the handshake method described further below may be performed for synchronization,

and then a new comparison step may be performed. In case of a positive comparison result, the outputting of the first and the second carrier signals may be restarted. Preferably, the balise control apparatus can be taken out of operation if, in particular, after several, e.g. 10, synchronization attempts no positive comparison result has been
5 obtained.

As has already been described, a processing unit may comprise at least one computing means to perform the generation step and/or the comparison step. Particularly preferably, a processing unit may comprise at least one microprocessor and a Field
10 Programmable Gate Array (FPGA) coupled thereto. According to one embodiment, at least the first comparator may be formed by a first Field Programmable Gate Array. Alternatively or (preferably) additionally, at least the second comparator may be formed by a second Field Programmable Gate Array. Furthermore, the computation of the first data signal may be performed by a first generation module formed at least in part by the
15 first Field Programmable Gate Array. Alternatively or (preferably) additionally, the computation of the second data signal may be performed by a second generation module which is at least partially formed by the second Field Programmable Gate Array. It shall be understood that the first FPGA may comprise a further second generation module configured to at least partially generate the further second data signal, and that the
20 second FPGA may comprise a further first generation module configured to at least partially generate the further first data signal.

In particular, a processing unit and a computer module, respectively, may be divided into two parts. A processing unit can preferably comprise a microprocessor with its own
25 operating system and file system. Preferably, (intermediate) data corresponding to the various signal terms can be stored here. I.e., for a signal term A, a microprocessor can, for example, read (intermediate) data (A) which corresponds to the data content of a data signal and a data stream (A), respectively, which must be generated for the associated balise A.

30

The (intermediate) data can be forwarded by the microprocessor to an FPGA. In particular, the FPGA can be configured to generate a data signal, in particular, a Manchester-modulated data signal, from this (intermediate) data.

- 5 The implementation of an FPGA has several advantages. For example, the bus width of a microprocessor is typically 32 or 64 bits. Therefore, transmitting a Manchester-encoded data signal of 1024 bit length would take 16 or 32 processor steps. Preferably, the bus width of the FPGA can be programmed to allow this in 2 or 4 steps. This allows the FPGA to generate a data signal of, for example, 564 kbit/s faster and easier than a
10 microprocessor. In particular, this allows a data signal to be generated in real time.

A generated data signal can be fed from the respective FPGA into the respective other FPGA and checked by the latter. In particular, an FPGA may comprise a comparator to compare two data signals, preferably on a bit-by-bit basis. Further, an FPGA may
15 comprise the carrier signal generator. If the comparison of the two data signals results in a difference, the generation of the carrier signal may be stopped as previously described.

A carrier signal generated digitally in an FPGA, e.g. a sinusoidal signal, can preferably be
20 converted into an analog carrier signal by a digital-to-analog converter. The analog carrier signal can subsequently be low-pass filtered, in particular, to filter disturbance variables. It shall be understood that a generated data signal can also be low-pass filtered to filter disturbance variables.

- 25 The two FPGAs are initially, in particular, two independently operating units, so that two first or two second data signals could not easily be generated or encoded and compared synchronously.

Therefore, for synchronization between both FPGAs, according to a preferred
30 embodiment, the following handshake method is proposed: When the balise control apparatus is initialized (e.g. switched on) and/or when a new first signal term is to be transmitted to the first balise, then the first FPGA must generate a new first data signal.

Likewise, the second FPGA must then generate a new further first data signal and perform the second comparison step (bit-by-bit). The first FPGA sends a (first) request message to the second FPGA, with the content that a new first data signal is to be generated. As soon as the second FPGA is ready to generate a further new first data
5 signal and to receive the new first data signal (for comparison) from the first FPGA, it sends a (second) acknowledgement message to the first FPGA. Upon receiving the acknowledgement message, the first FPGA sends a start signal cyclically followed by the new first data signal; at the same time, the first FPGA cyclically sends the first clock signal. At the same time, the second FPGA also generates an identical further start signal,
10 followed by the new further first data signal, in time with the first clock signal. The second FPGA feeds these two data streams bit-synchronously to the second comparator, which now compares both data streams bit-by-bit in real time. Preferably, a defined sequence of bits can be used as start signal, in particular preferably, for example, a sequence of a specific number of zeros, e.g. 75 zeros. In other words, the handshake
15 method enables the balise control apparatus to ensure bit-by-bit verification of the (new) first data signal in the second comparator even in the event of an initialization and/or a change of the first signal term.

It shall be understood that the handshake method can be performed in an analog and
20 mirror image manner when a new second signal term is to be transmitted to the second balise.

A further aspect of the application is a system, in particular, a balise control system. The system comprises at least one balise control apparatus previously described. The system
25 comprises a first balise connected to the balise control apparatus, in particular, to the first control signal generating unit.

Preferably, the system may comprise a second balise connected to the balise control apparatus, in particular, to the second control signal generating unit.

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According to an embodiment of the system according to the application, the system may comprise a data source, in particular, an electronic interlocking and/or a light source

and an optical detection unit. The data source may be configured to generate (and provide) the first signal term and/or the second signal term. A (digital) signal term may be generated by an electronic interlocking and transmitted to the balise control apparatus via a data network. Also, a (digital) signal term can be generated from an analog light signal with subsequent digitization in a lineside electronic unit (LEU) forming the optical detection device.

In particular, the balise control apparatus may be arranged close to the rails and thus close to the first balise and/or second balise preferably arranged on the rails (e.g. in the track bed), while the data source may be arranged remote therefrom.

A still further aspect of the application is a method of operating a balise control apparatus, in particular a previously described balise control apparatus. The method comprises:

- 15 - generating, by a first processing unit, a first data signal based on a provided first signal term,
- generating, by a second processing unit, a further first data signal based on the provided first signal term,
- comparing, by a second comparator of the second processing unit, the further first data signal generated by the second processing unit and the first data signal generated by the first processing unit in a second comparing step,
- 20 - outputting, by the first processing unit, the generated first data signal to a first control signal generating unit, and
- outputting, by the second processing unit, a second carrier signal to the first control signal generating unit, wherein the outputting of the second carrier signal depends on the comparison result of the second comparison step.

According to a preferred embodiment of the method according to the application, the method may comprise:

- 30 - generating, by a first processing unit, a first data signal based on a provided first signal term and a second data signal based on a provided second signal term,

- generating, by a second processing unit, a second data signal based on the provided second signal term, and generating a first data signal based on the provided first signal term,
- comparing, by a first comparator of the first processing unit, the second data
5 signal generated by the first processing unit and the second data signal generated by the second processing unit in a first comparing step,
- comparing, by a second comparator of the second processing unit, the first data
10 signal generated by the second processing unit and the first data signal generated by the first processing unit in a second comparing step,
- outputting, by the first processing unit, the generated first data signal to a first
control signal generating unit and outputting, by the first processing unit, a first
carrier signal to a second control signal generating unit, wherein the outputting
of the first carrier signal depends on the comparison result of the first
comparison step, and
- 15 - outputting, by the second processing unit, the generated second data signal to the
second control signal generating unit, and outputting, by the second processing
unit, a second carrier signal to the first control signal generating unit, wherein the
outputting of the second carrier signal depends on the comparison result of the
second comparison step.

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There are now a multitude of possibilities to design and further develop the balise control apparatus according to the application, the system according to the application and the method according to the application. For this purpose, reference is made on the one hand to the claims subordinate to the independent claims, and on the other hand to
25 the description of embodiments in connection with the drawing. In the drawing shows:

- Fig. 1 a schematic view of a system with a balise control apparatus according to the prior art,
- 30 Fig. 2 a schematic view of an embodiment of a balise control apparatus according to the present application,

- Fig. 3 a schematic view of a further embodiment of a balise control apparatus according to the present application,
- Fig. 4 a schematic view of an embodiment of a system according to the present application,
- Fig. 5 a schematic view of an embodiment of a processing unit of a balise control apparatus according to the present application, and
- Fig. 6 a diagram of an embodiment of a method according to the present application.

In the following, the similar reference signs are used for the similar elements.

Figure 2 shows a schematic view of an embodiment of a balise control apparatus 202 according to the present application. The balise control apparatus 202 comprises a first processing unit 250 and a second processing unit 252. Furthermore, the balise control apparatus 202 in the present embodiment comprises a first control signal generating unit 266.

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The first processing unit 250 comprises at least a first generation module 254. The first generation module 254 is configured to generate respectively encode a first data signal 236 based on a provided first (digital) signal term 232. The second processing unit 252 comprises a further first generation module 260. The further first generation module 260 is configured to generate respectively encode a further first data signal based on the provided first (digital) signal term 232.

In addition, the further processing unit 252 comprises a second comparator 264. The second comparator 264 is configured to compare the first data signal 236 generated by the first processing unit 250 with the further first data signal in a second comparison step.

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Furthermore, the second processing unit 252 is configured to output a second carrier signal 240, in particular, a sinusoidal signal 240. In particular, the carrier signal 240 can be forwarded to the first control signal generating unit 266. As can be seen, the first processing unit 250 is configured to output the first data signal 236 to the first control signal generating unit 266. The first control signal generating unit 266 is configured to apply the provided first data signal 236 to the provided second carrier signal 240 to generate a first balise telegram 238 for a first (not shown) balise.

In order to ensure that a balise telegram 238 is generated and transmitted only if the first data signal 236 is generated correctly, it is provided according to the application that the second processing unit 252 is configured to output the second carrier signal 240 as a function of the comparison result of the second comparison step. By this is to be understood, in particular, that the second carrier signal 240 is only output by the second processing unit 252 in the case of a positive comparison result. In case of a negative comparison result, the output of the second carrier signal 240 is, in particular, stopped. Here, a positive comparison result is, in particular, present if the first data signal 236 is equal to the further first data signal. A negative comparison result is, in particular, present if a deviation between the first data signal 236 and the further first data signal is detected. Further, in case of a negative comparison result, the described handshake method may be performed for synchronization and thereafter a new comparison step may be performed. In case of a positive comparison result, the outputting of the carrier signal 240 may be restarted. Preferably, the balise control apparatus 202 may be taken out of operation if no positive comparison result has been obtained after several, for example 10, synchronization attempts.

Figure 3 shows a schematic view of a further embodiment of a balise control apparatus 302 according to the present application. To avoid repetitions, essentially only the differences from the embodiment according to Figure 2 are described below. For the other components of the balise control apparatus 302, reference is made, in particular, to the above explanations.

In the present embodiment, the balise control apparatus 302 comprises a second control signal generating unit 368. The first processing unit 350 comprises a further second generation module 356 and a first comparator 358 in addition to the first generation module 354. The second processing unit 352 comprises a second generation module 362 in addition to the further first generation module 360 and the second comparator 364. The advantage of the balise control apparatus 302 of the present embodiment is that two balises (not shown) can be controlled by the balise control apparatus 302 without having to duplicate the hardware used for this purpose.

10 The illustrated balise control apparatus 302 is configured to receive a first signal term 332 for a first balise and a second signal term 334 for a second balise and to process them, in particular, in parallel. Preferably, the further second generation module 356 can generate a further second data signal, for example, in parallel with the generation of the first data signal 336, based on the provided second signal term 334. The second
15 generation module 362 of the second processing unit 352 may generate a second data signal 337, based on the provided second signal term 334.

In order to ensure that a second balise telegram 344 is generated and transmitted only if the second data signal 337 is generated correctly, it is provided in the present case that
20 the first processing unit 350 is configured to output the first carrier signal 342 as a function of the comparison result of a first comparison step. In the first comparison step, the first comparator 358 can, in particular, compare the second data signal 337 with the further second data signal. In particular, the first carrier signal 342 may be output by the first processing unit 350 only when the comparison result is positive. In case of a
25 negative comparison result, the outputting of the first carrier signal 342 may be stopped. Further, in the case of a negative comparison result, the described handshake method for synchronization may be performed, and then a new comparison step may be performed. If the comparison result is positive, the outputting of the first carrier signal 342 may be restarted. Preferably, the balise control apparatus 302 may be taken out of
30 operation if no positive comparison result has been obtained after several, for example 10, synchronization attempts.

Figure 4 shows a schematic view of an embodiment of a system 400 according to the present application. The system 400 comprises an embodiment of a balise control apparatus 402 according to the present application. To avoid repetitions, essentially only the differences from the embodiments shown in Figures 2 and 3 are described
5 below. For the other components of the balise control apparatus 402, reference is made, in particular, to the above explanations.

The system 400 further comprises a data source 406. It shall be understood that two or more data sources may be provided. For example, the data source 406 is an electronic
10 interlocking 406 or a lineside electronic unit (LEU). In particular, the data source 406 is presently configured to generate at least a first digital signal term 432 for a first balise 404 and a second digital signal term 434 for a second balise 405. Via a data network (e.g., CAN bus network), the first and/or the second signal term(s) 432, 434 can be transmitted to the at least one balise control apparatus 402 of the system 400.

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As has already been described above, the system 400 presently comprises a first balise 404, in particular a transparent data balise 404, and a second balise 405, in particular a transparent data balise 405. Each balise 404, 405 is connected to the balise control apparatus 402 via a data line.

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Furthermore, it can be seen from Figure 4 that a processing unit 450, 452 is formed, in particular, by two components, namely a microprocessor 470, 474 and an FPGA 472, 476. Each FPGA 472, 476 can be supplied with its own clock signal 482, 484. The operation of the processing units 450, 452 is described in more detail below.

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Based on a first signal term 432, the first microprocessor 470 generates first (intermediate) data 478. In particular, in the first microprocessor 470, e.g., in its file system, first (intermediate) data can be stored corresponding to first signal terms (e.g., in the form of a conversion table). The first (intermediate) data 478 is forwarded to the
30 first FPGA. The FPGA generates a first data signal 436 from the first (intermediate) data 478. In particular, the first data signal 436 may be a Manchester-encoded data signal

436. In particular, a first data signal 436 may be generated with a data stream of 564 kbit/s in real time.

5 The first data signal 436 is output, by the first processing unit 450, to a first control signal generating unit 466 in the form of an adder 466 via a first low-pass filter 492. The first low-pass filter 492 preferably has a cut-off frequency of about 50 MHz.

Further, the first data signal 436 is output to the second FPGA 476 of the second processing unit 452.

10

Based on the first signal term, the second microprocessor 474 generates first (intermediate) data 478 and forwards it to the second FPGA 476. The second FPGA 476 is configured to generate a further first data signal from the first (intermediate) data 478 and to compare this with the first data signal 436 of the first processing unit 450. In particular, the second FPGA 476 is configured to perform a bit-by-bit comparison of the two first data signals.

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In order to synchronously perform the second comparison step, i.e., the bit-by-bit comparison of the two first data signals in the second FPGA 476, a handshake method is proposed in the present embodiment, which may be performed when the balise control apparatus 400 is initialized and/or when the first signal term 432 is changed and/or when the comparison result is negative: The first FPGA 472 sends a first request message 494 to the second FPGA 476, indicating that a new first data signal 436 is to be generated. Once the second FPGA 476 is ready to generate in turn a new further first data signal and to receive from the first FPGA 472 the new first data signal 436 (for comparison), it sends a second acknowledgement message 495 to the first FPGA 472. After receiving the second acknowledgement message 495, the first FPGA 472 first sends a start signal and then cyclically sends the new first data signal 436 and cyclically sends the first clock signal 486. At the same time, the second FPGA 476 also generates the start signal, cyclically followed by the new further first data signal, and this in time with the first clock signal 486. The second FPGA 476 thereby feeds these two data streams bit-synchronously to the second comparator, which now compares both data

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streams bit-by-bit in real time. Preferably, a defined sequence of bits can be used as the start signal, particularly preferably, for example, a sequence of 75 zeros.

Depending on the comparison result of the second comparison step, a digital second
5 carrier signal 440 is output by the second processing unit 452. In particular, the second carrier signal 440 is output only when the comparison result is positive. As can be seen, the second carrier signal 440 is output to a digital analog converter 490. The analog second carrier signal generated by the digital analog converter 490 is passed to the first control signal generating unit 466 via a second low-pass filter 493.

10

The first control signal generating unit 466 generates a first balise telegram 438 by adding the first data signal 436 to the second analog carrier signal 440. Optionally, the balise telegram 438 may be amplified by an amplifier 428.

15 Preferably in parallel with the processing of the first signal term 432, the processing of the second signal term 434 may be performed by the present balise control apparatus 402. In accordance with the previous embodiments, the second processing unit 452 generates second (intermediate) data 480 and, therefrom, a second data signal 437, which is output to the second control signal generating unit 468 and, together with a
20 second clock signal 488, to the first processing unit 450 to compare the second data signal 437 with the further second data signal in a first comparison step. Only if the comparison result of the first comparison step is positive, a first carrier signal 442 may be output to the second control signal generating unit 468 to generate a second balise telegram 444 in the manner previously described. For synchronization of the first
25 comparison step, the same handshake method described above for synchronization of the second comparison step may be used in a mirror image manner.

The respective balise telegram 438, 444 is transmitted to the respective balise 404, 405 via a data line. If a negative comparison result is detected, the transmitting of the
30 corresponding carrier signal 440, 442 is stopped. As a result, the transmitting of the corresponding balise telegram 438, 444 is also stopped. Further, in the event of a negative comparison result, the described handshake method can be performed for

synchronization and then a new comparison step can be performed. In case of a positive comparison result, the outputting of the corresponding carrier signals 440, 442 can be restarted. As a result, the transmitting of the corresponding balise telegram 438, 444 is also restarted. Preferably, the balise control apparatus 402 can be taken out of operation
5 if no positive comparison result has been obtained after several, for example 10, synchronization attempts.

Figure 5 shows a schematic view of a further embodiment of a first processing unit 550, which can be used as processing units 250, 350, 450 in Figures 2 to 4. A second
10 processing unit (corresponding to the processing units 252, 352, 452 of Figures 2 to 4) can be of the same design and is not shown for the sake of a better overview. Also at this point, to avoid repetitions, essentially only the differences from the previous embodiments are described below and otherwise reference is made to the previous
15 embodiments.

In the present embodiment, the first FPGA 572 is connected to the first microprocessor 570 and controller 570, respectively, via an interface 593 (e.g., a CPU interface). Among other things, the first FPGA 572 is configured to receive from the first microcontroller 570 first (intermediate) data 578 and second (intermediate) data 580 corresponding to
20 a first signal term and a second signal term, respectively. These data 578, 580 are to be used to control a first (not shown) balise and a second (not shown) balise, respectively. The data contents of the data 578, 580 may be stored in a memory area 594 (e.g., telegram memory).

25 A first generation module 554 and a first encoder 554, respectively, may read the first data 578 from the memory 594 and the generation rules stored in a further memory area 595 to generate the first data signal 536 therefrom. In a previously described manner, the first data signal 536 may be transmitted to a first balise depending on the comparison result of the second comparison step.

30 At the same time, this first data stream 536, preferably together with the first clock signal 586, may be sent to the second FPGA of the second processing unit to be checked

in the previously described manner. If the verification in the second FPGA reveals an error in the first data signal 536, the outputting of the second carrier signal generated in the second FPGA may be stopped in real time.

5 Furthermore, the present first FPGA 572 is configured to receive a second data signal 537 from the second processing unit, i.e. in particular from the second FPGA, preferably together with a second clock signal 588 from the second processing unit. With the second clock signal 588, a further second generation module 556 and a further second encoder 556, respectively, can generate, in particular, calculate, a further second data
10 signal from second (intermediate) data 580 and the generation rules stored in a further memory area 596.

In a first comparison step, in a first comparator 558, presently the second data signal 537 and the further second data signal are compared bit-by-bit and, in particular, in real
15 time. If this comparison shows a deviation, i.e. a negative comparison result is detected, the carrier signal generator 598, in particular, a sine wave generator 598, which generates the first carrier signal 542, can be switched off. Further, if a negative comparison result is detected, the described handshake method may be performed for synchronization, and then a new first comparison step may be performed. In case of a
20 positive comparison result, the output of the corresponding carrier signals 542 may be restarted.

In other words, the output of the first carrier signal 542 can be stopped, in particular, in real time, if an error has occurred in the first comparison step. In this way, it can be
25 achieved that the power supply of the second balise is switched off. If the second balise is then passed by a rail vehicle, it transmits, in particular, a preset signal to the rail vehicle. This can detect the fault and initiate a correspondingly safe reaction.

Furthermore, it is possible that a (first or second) data signal was generated incorrectly
30 (equally) in both processing units. The bitwise comparison of the two generated data signals would then show no deviation. To detect such an error, a first verifier 597 may

optionally be provided, preferably in the first FPGA 572. Similarly, a second verifier may be provided in the second processing unit.

As can be seen from Figure 5, in the first FPGA 572 not only two generated second data
5 streams can be compared with each other, but preferably the second data stream 537,
which can be received by the first FPGA from the second FPGA, can be checked for
plausibility or decoded or back-calculated by the first verifier 597. In particular, the first
verifier 597 may presently check the second data signal 537 by polynomial division to
10 determine whether this corresponds to the structure of a (standard) balise telegram,
and/or the first verifier 597 may determine the second (intermediate) data of the
second signal term 534 from the second data signal. If the plausibility check and/or a
comparison of the determined second (intermediate) data and the second
(intermediate) data generated by the first microprocessor 570 shows an error, the
outputting of the first carrier signal 542 may be stopped.

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Figure 6 shows a diagram of an example of a method according to the present
application. In particular, a preferred embodiment is shown in which two balises can be
controlled in parallel with the method. It shall be understood that in other variants of
the application only one balise can be controlled.

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In step 601, a first data signal based on a first signal term is computed by a first
processing unit. In this step, a further second data signal, based on a second signal term,
can also be computed by the first processing unit, as described above.

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For example, in parallel thereto, a second data signal based on the second signal term
may be computed by a second processing unit in step 602. In addition, the second
processing unit can generate a further first data signal in this step, based on the first
signal term.

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In steps 603 and 604, the first comparison step and the second comparison step are
performed, respectively. In particular, in a first comparison step, the first processing
unit can compare the second data signal with the further second data signal. In a second

comparison step, the second processing units compares the first data signal with the further first data signal.

5 In step 605, the first processing unit outputs the first data signal to the first control signal generating unit and the first carrier signal to the second control signal generating unit. Here, the first carrier signal is output depending on the comparison result of the first comparison step. When the comparison result is positive, the first carrier signal is output, while when the comparison result is negative, the output is interrupted. Further, in the case of a negative comparison result, the described handshake method can be
10 performed for synchronization and then a new first comparison step can be performed. In case of a positive comparison result, the outputting of the first carrier signal can be restarted. Preferably, the balise control apparatus can be taken out of operation if no positive comparison result has been obtained after several, e.g. 10, synchronization attempts.

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Accordingly, in step 606, the second processing unit may output the second data signal to the second control signal generating unit and the second carrier signal to the first control signal generating unit. The second carrier signal is output depending on the comparison result of the second comparison step. When the comparison result is
20 positive, the second carrier signal is output, while when the comparison result is negative, the output is interrupted. Further, in the case of a negative comparison result, the described handshake method can be performed for synchronization, and then a new second comparison step can be performed. In case of a positive comparison result, the outputting of the second carrier signal can be restarted. Preferably, the balise control
25 apparatus can be taken out of operation if no positive comparison result has been obtained after several, e.g. 10, synchronization attempts.

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Only if a carrier signal is output, the corresponding balise telegram can also be output to the corresponding balise as described before.

According to the application, it is provided, in particular, that a first data signal and a second data signal are generated in each of the two processing units, the two data

signals mapping the respective signal term for the first balise and the second balise.

Both data signals can be compared in one of the two processing units, preferably in real time and bit by bit. If the comparison shows a deviation, the corresponding carrier signal respectively power supply signal for the corresponding balise can be switched off and a
5 signal safe state can be established. This comparison and, if necessary, the switching-off can be performed, in particular, in real time during the generation of the data signals.

Patentkrav

1. Balisestyreindretning (202, 302, 402) til at styre mindst en balise (404, 405), hvor balisestyreindretningen (202, 302, 402) omfatter:

- 5 - en første bearbejdningsindretning (250, 350, 450, 550), der er indrettet således, at et første datasignal (236, 336, 436, 536) genereres, baseret på et tilvejebragt første signalbegreb (232, 332, 432, 532),
- en anden bearbejdningsindretning (252, 352, 452), der er indrettet således, at et yderligere datasignal genereres, baseret på det tilvejebragte første signalbegreb (232, 332, 432, 532),
- 10 - hvor den anden bearbejdningsindretning (252, 352, 452) omfatter en anden komparator (264, 364, 464), der er indrettet således, at det yderligere første datasignal, der genereres af den anden bearbejdningsindretning (252, 352, 452), og det første datasignal (236, 336, 436, 536), der genereres af den første bearbejdningsindretning (250, 350, 450, 550), sammenlignes i et andet sammenligningstrin, og
- 15 - hvor den første bearbejdningsindretning (250, 350, 450, 550) er indrettet således, at det genererede første datasignal (236, 336, 436, 536) udlæses til en første styresignalgenereringsindretning (266, 366, 466),
- 20 - **kendetegnet ved**, at den anden bearbejdningsindretning (252, 352, 452) er indrettet således, at et andet bærsignal (240, 340, 440) udlæses til den første styresignalgenereringsindretning (266, 366, 466), hvor udlæsningen af det andet bærsignal (240, 340, 440) afhænger af sammenligningsresultatet fra det andet sammenligningstrin.

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2. Balisestyreindretning (202, 302, 402) ifølge krav 1, hvor

- den anden bearbejdningsindretning (252, 352, 452) er indrettet således, at et andet datasignal (337, 437, 537) genereres, baseret på et tilvejebragt andet signalbegreb (334, 434),
- 30 - den første bearbejdningsindretning (250, 350, 450, 550) er indrettet således, at et yderligere andet datasignal genereres, baseret på et tilvejebragt andet signalbegreb (334, 434),
- hvor den første bearbejdningsindretning (250, 350, 450, 550) omfatter en første komparator (358, 458, 558), der er indrettet således, at det yderligere

andet datasignal, der genereres af den første bearbejdningsindretning (250, 350, 450, 550), og det andet datasignal (337, 437, 537), der genereres af den anden bearbejdningsindretning (252, 352, 452), sammenlignes i et første sammenligningstrin,

- 5 - hvor den anden bearbejdningsindretning (252, 352, 452) er indrettet således, at det genererede andet datasignal (337, 437, 537) udlæses til en anden styresignalgenereringsindretning (368, 468), og hvor den første bearbejdningsindretning (250, 350, 450, 550) er indrettet således, at et første bærersignal (342, 442, 542) udlæses til den anden styresignalgenereringsindretning (368, 468), hvor udlæsningen af det første bærersignal (342, 442, 542) afhænger af
10 sammenligningsresultatet fra det første sammenligningstrin.

3. Balisestyreindretning (202, 302, 402) ifølge krav 1 eller 2, hvor

- 15 - balisestyreindretningen (202, 302, 402) omfatter den første styresignalgenereringsindretning (266, 366, 466), der er indrettet således, at et første balisetelegram (238, 338, 438) genereres, baseret på det første datasignal (236, 336, 436, 536) og det andet bærersignal (240, 340, 440),
og/eller

- 20 - balisestyreindretningen (202, 302, 402) omfatter den anden styresignalgenereringsindretning (348, 468), der er indrettet således, at et andet balisetelegram (344, 444) genereres, baseret på det andet datasignal (337, 437, 537) og det første bærersignal (342, 442, 542).

4. Balisestyreindretning (202, 302, 402) ifølge et af de foregående krav, hvor

- 25 - den første komparator (358, 458, 558) er indrettet således, at det yderligere andet datasignal, der genereres af den første bearbejdningsindretning (250, 350, 450, 550), og det andet datasignal (337, 437, 537), der genereres af den anden bearbejdningsindretning (252, 352, 452), sammenlignes bitvist, og/eller
30 - den anden komparator (264, 364, 464) er indrettet således, at det yderligere første datasignal, der genereres af den anden bearbejdningsindretning (252, 352, 452), og det første datasignal (236, 336, 436, 536), der genereres af den første bearbejdningsindretning (250, 350, 450, 550), sammenlignes bitvist.

5. Balisestyreindretning (202, 302, 402) ifølge et af de foregående krav, hvor

- den første bearbejdningsindretning (250, 350, 450, 550) omfatter en første bærersignalgenerator (598), der er indrettet på en sådan måde, at det første bærersignal (342, 442, 542) genereres,
og/eller
- 5 - den anden bearbejdningsindretning (252, 352, 452) omfatter en anden bærersignalgenerator, der er indrettet på en sådan måde, at det andet bærersignal (240, 340, 440) genereres.

- 6. Balisestyreindretning (202, 302, 402) ifølge krav 5, hvor
- 10 - den første bærersignalgenerator (598) er indrettet således, at det første bærersignal (342, 442, 542) kun udlæses ved et positivt sammenligningsresultat fra det første sammenligningstrin,
og/eller
- 15 - den anden bærersignalgenerator er indrettet således, at det andet bærersignal (240, 340, 440) kun udlæses ved et positivt sammenligningsresultat fra det andet sammenligningstrin.

- 7. Balisestyreindretning (202, 302, 402) ifølge et af de foregående krav, hvor
- 20 - den første bearbejdningsindretning (250, 350, 450, 550) og den anden bearbejdningsindretning (252, 352, 452) er synkroniseret med hinanden,
- hvor der til synkroniseringen især sendes et første request-signal (494) af den første bearbejdningsindretning (250, 350, 450, 550) fra den første bearbejdningsindretning (250, 350, 450, 550) til den anden bearbejdningsindretning (252, 352, 452),
og/eller
- 25 - hvor der til synkroniseringen især sendes et andet acknowledgement-signal (495) af den anden bearbejdningsindretning (252, 352, 452) fra den anden bearbejdningsindretning (252, 352, 452) til den første bearbejdningsindretning (250, 350, 450, 550).

- 30 8. Balisestyreindretning (202, 302, 402) ifølge et af de foregående krav, hvor
- den første bearbejdningsindretning (250, 350, 450, 550) omfatter en første testindretning (597), der er indrettet således, at plausibiliteten testes, og/eller

det andet datasignal (337, 437, 537), der genereres af den anden bearbejdningsindretning (252, 352, 452), afkodes,

og/eller

- 5 - den anden bearbejdningsindretning (252, 352, 452) omfatter en anden testindretning, der er indrettet således, at plausibiliteten testes, og/eller det første datasignal (236, 336, 436, 536), der genereres af den første bearbejdningsindretning (250, 350, 450, 550), afkodes.

9. Balisestyreindretning (202, 302, 402) ifølge krav 8, hvor

- 10 - den første bearbejdningsindretning (250, 350, 450, 550) omfatter et første evalueringsmodul, der er indrettet således, at det testes, om dataene, der afkodes af den første testindretning (597) fra det andet datasignal (337, 437, 537), svarer til det tilvejebragte andet signalbegreb (334, 434, 534),
og/eller

- 15 - den anden bearbejdningsindretning (252, 352, 452) omfatter et andet evalueringsmodul, der er indrettet således, at det testes, om dataene, der afkodes af den anden testindretning fra det første datasignal (236, 336, 436, 536), svarer til det tilvejebragte første signalbegreb (232, 332, 432, 532).

20 10. System (400) omfattende:

- mindst en balisestyreindretning (202, 302, 402) ifølge et af de foregående krav,
- en første balise (404), der er forbundet med balisestyreindretningen (202, 302, 402), især den første styresignalgenereringsindretning (266, 366, 466).

25

11. Fremgangsmåde til drift af en balisestyreindretning (202, 302, 402), især en balisestyreindretning (202, 302, 402) ifølge et af kravene 1 til 8, hvor fremgangsmåden omfatter:

- 30 - at generere, ved hjælp af en første bearbejdningsindretning (250, 350, 450, 550), et første datasignal (236, 336, 436, 536), baseret på et tilvejebragt første signalbegreb (232, 332, 432, 532),
- at generere, ved hjælp af en anden bearbejdningsindretning (252, 352, 452), et yderligere første datasignal, baseret på et tilvejebragt første signalbegreb (232, 332, 432, 532),

- 5 - at sammenligne, ved hjælp af en anden komparator (264, 364, 464) af den anden bearbejdningsindretning (252, 352, 452), det yderligere første datasignal, der genereres af den anden bearbejdningsindretning (252, 352, 452), og det første datasignal (236, 336, 436, 536), der genereres af den første bearbejdningsindretning (250, 350, 450, 550), i et andet sammenligningstrin, og
- at udlæse, ved hjælp af den første bearbejdningsindretning (250, 350, 450, 550), det genererede første datasignal (236, 336, 436, 536) til en første styresignalgenereringsindretning (266, 366, 466), **kendetegnet ved, at fremgangsmåden omfatter:**
- 10 - at udlæse, ved hjælp af den anden bearbejdningsindretning (252, 352, 452), et andet bæresignal (240, 340, 440) til den første styresignalgenereringsindretning (266, 366, 466), hvor udlæsningen af det andet bæresignal (240, 340, 440) afhænger af sammenligningsresultatet fra det andet sammenligningstrin.

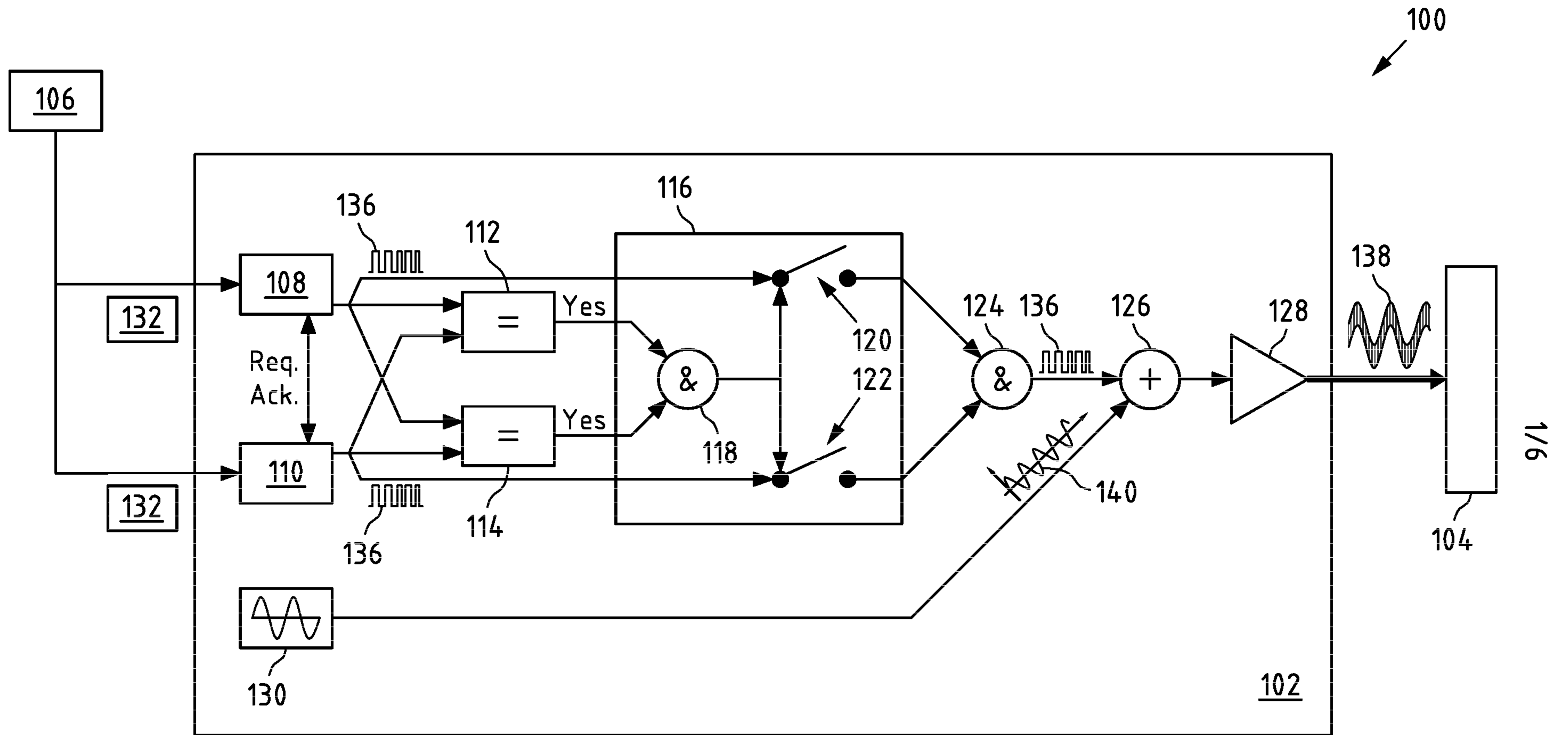


Fig.1 Prior Art

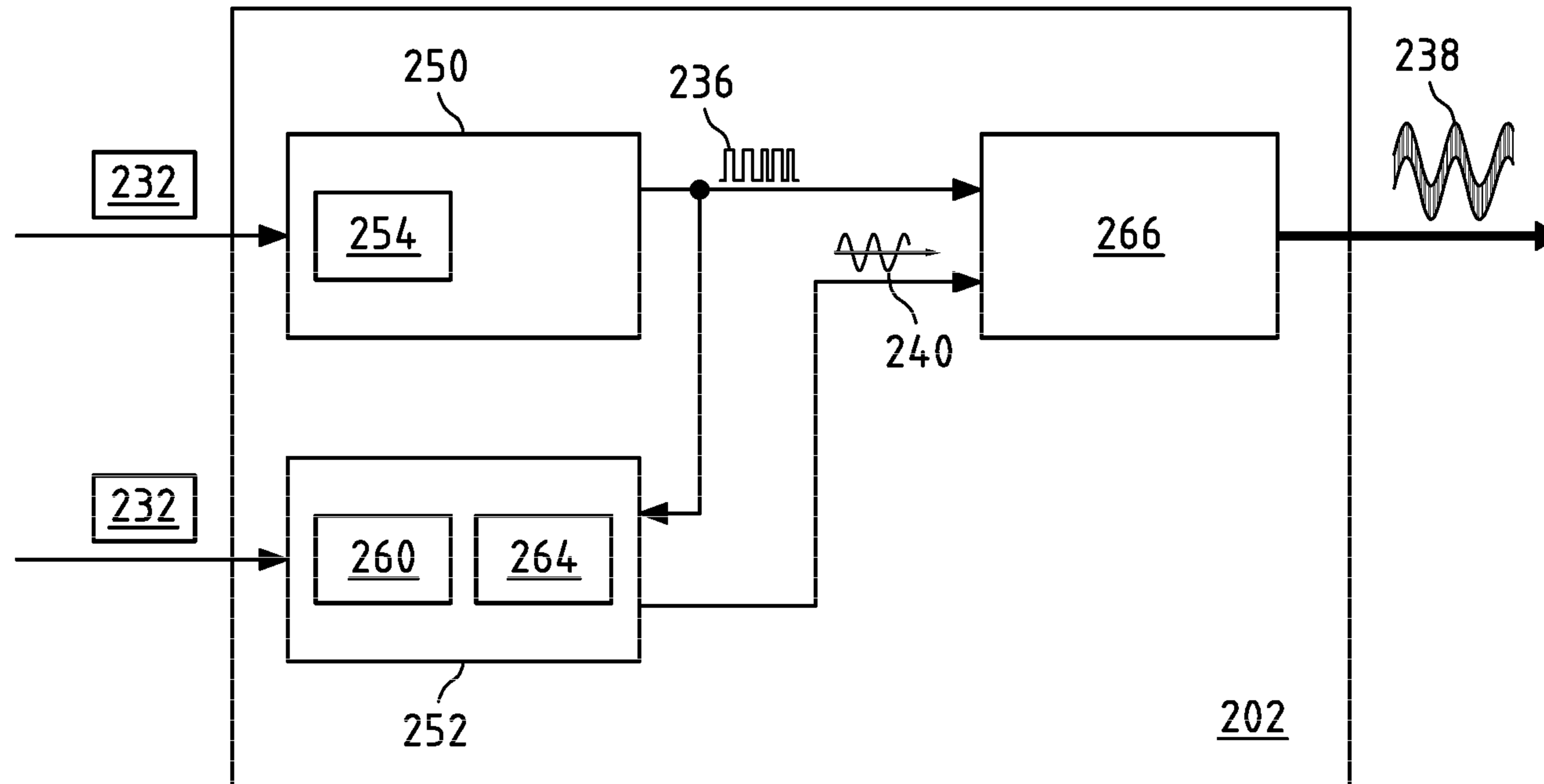


Fig.2

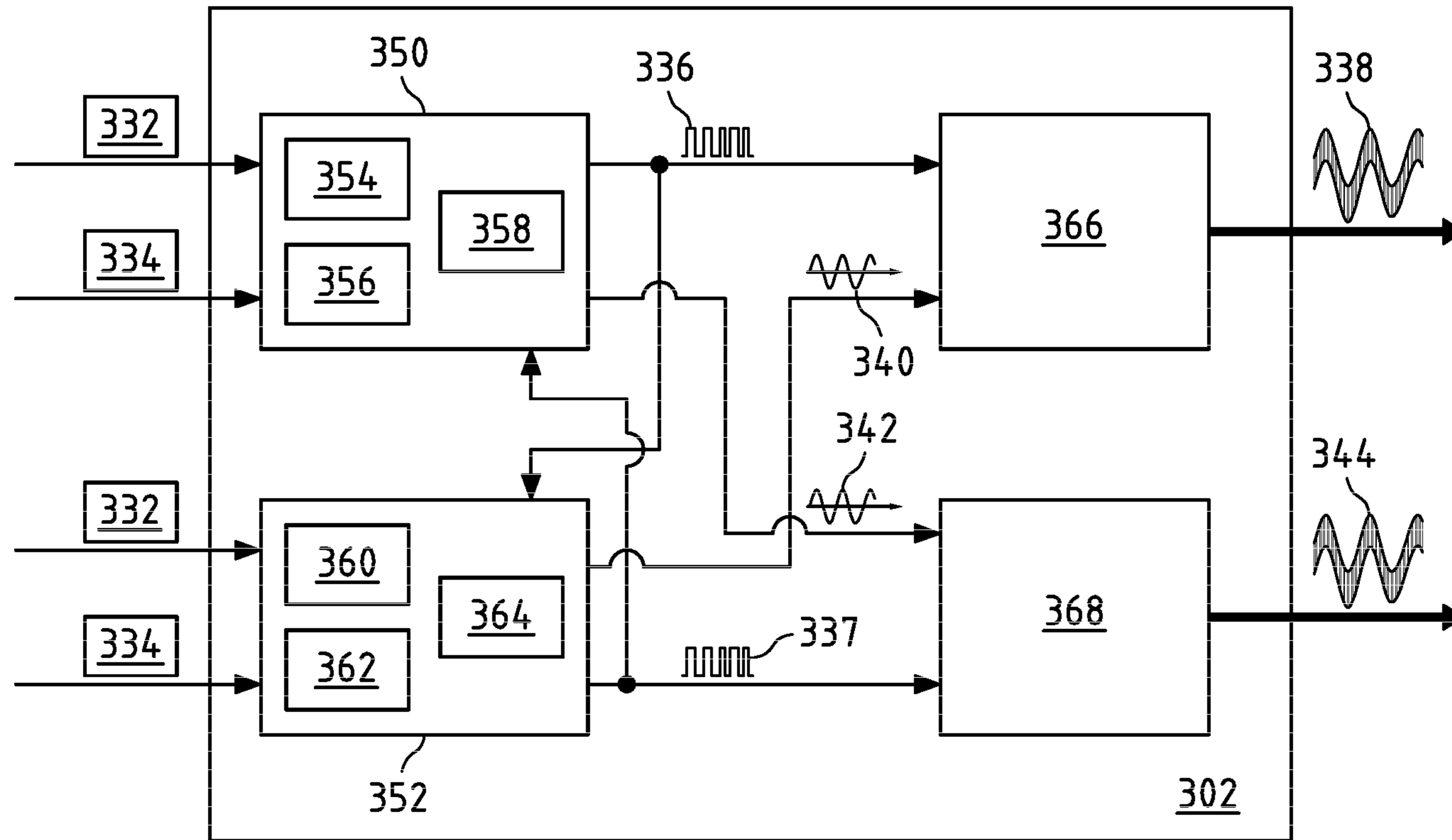


Fig.3

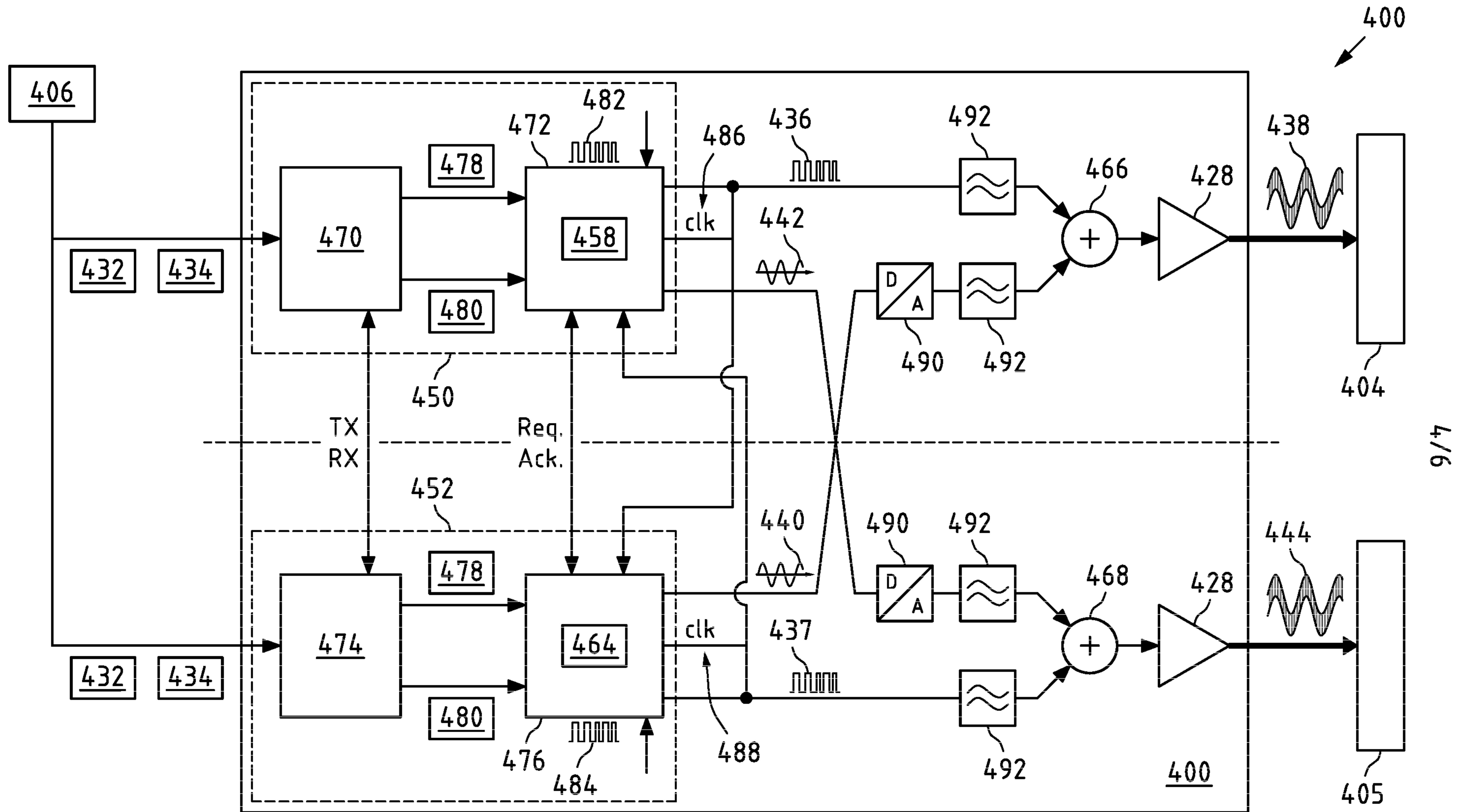


Fig.4

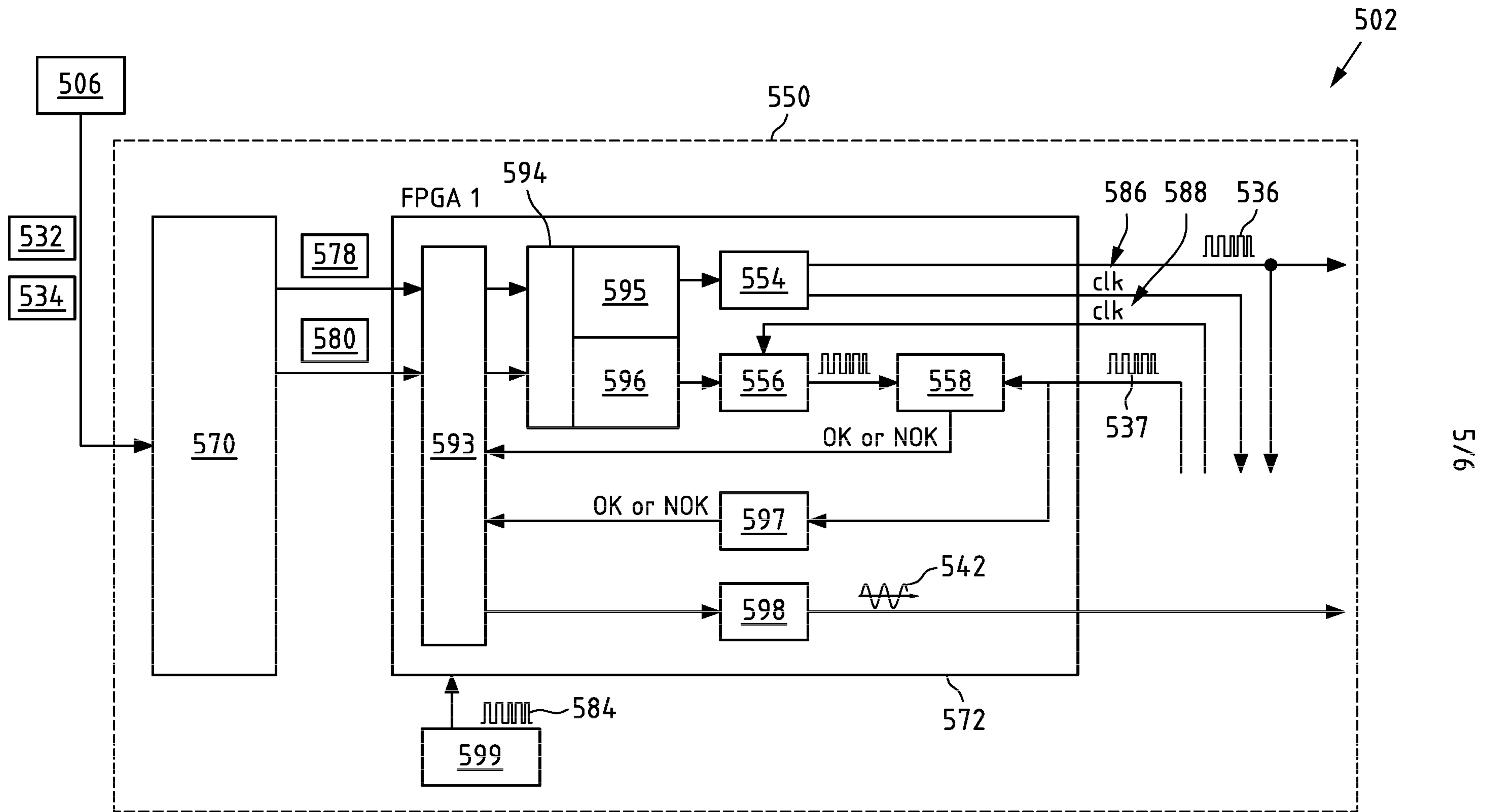


Fig.5

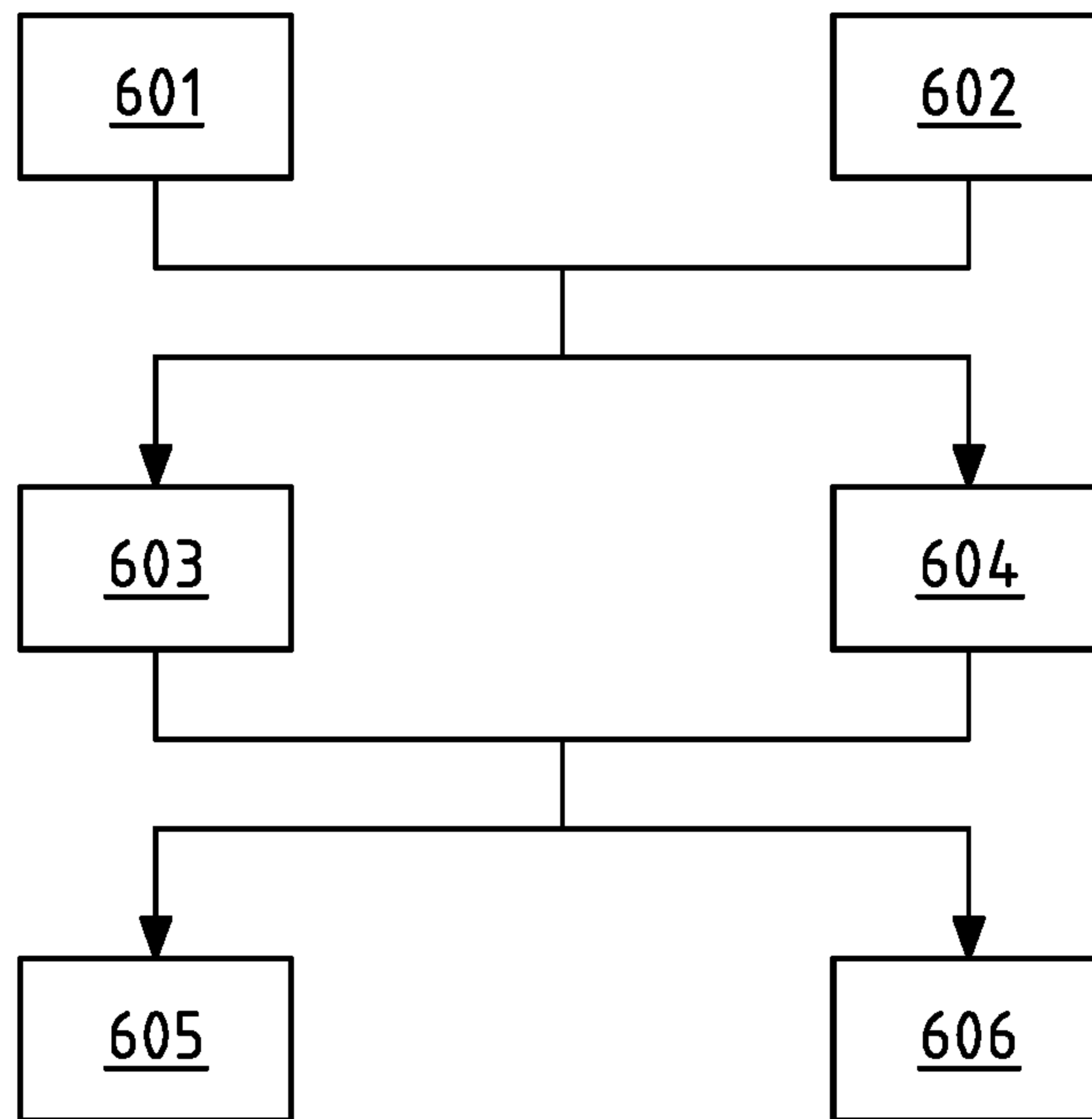


Fig.6