US 20100098111A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2010/0098111 A1**

(43) **Pub. Date: Apr. 22, 2010**

**SUN et al.**

(54) **METHOD AND SYSTEM FOR PRECISE-CLOCK SYNCHRONIZATION, AND DEVICE FOR PRECISE-CLOCK FREQUENCY/TIME SYNCHRONIZATION**

(75) Inventors: **Wenhua SUN**, Shenzhen (CN); **Xiaobo WANG**, Shenzhen (CN); **Jihui WANG**, Shenzhen (CN); **Wenguang XU**, Shenzhen (CN); **Shengbing YANG**, Shenzhen (CN); **Youhao DENG**, Shenzhen (CN); **Bingbo LI**, Shenzhen (CN)

Correspondence Address:
**Leydig, Voit & Mayer, Ltd**
**(for Huawei Technologies Co., Ltd)**
**Two Prudential Plaza Suite 4900, 180 North Stetson Avenue**
**Chicago, IL 60601 (US)**

(73) Assignee: **HUAWEI TECHNOLOGIES CO., LTD.**, Shenzhen (CN)

(21) Appl. No.: **12/582,002**

(22) Filed: **Oct. 20, 2009**

(30) **Foreign Application Priority Data**

Oct. 21, 2008 (CN) ..... 200810224615.7

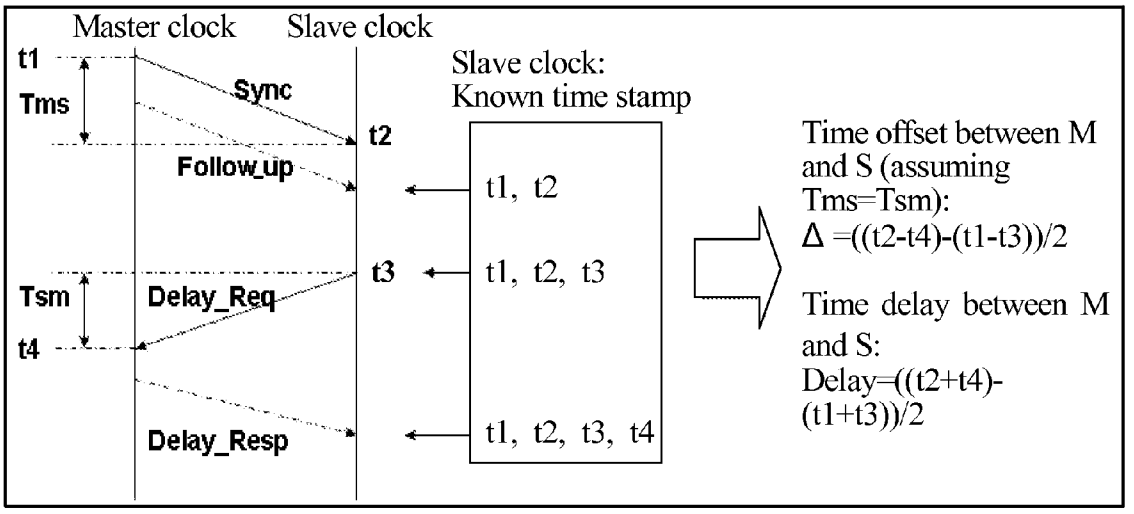
**Publication Classification**

(51) **Int. Cl.**
*H04J 3/06* (2006.01)

(52) **U.S. Cl.** ..... **370/509**

(57) **ABSTRACT**

A precise-clock synchronization method and system and a precise-clock frequency/time synchronization device are provided. In the embodiments of the present invention, two time stamp engines are provided at a slave clock side. A relative time stamp engine provides a relative arrival time stamp. An absolute time stamp engine provides an absolute arrival time stamp. The frequency/time synchronization is calculated by using different time stamps obtained from different time stamp engines, so the frequency synchronization and time synchronization of master clock and the slave clock may be separately accomplished, and one synchronization function may be enabled or disabled. Therefore, the frequency synchronization and time synchronization of the master clock and the slave clock do not interfere with each other, thus greatly reducing the occupied link bandwidth resources.



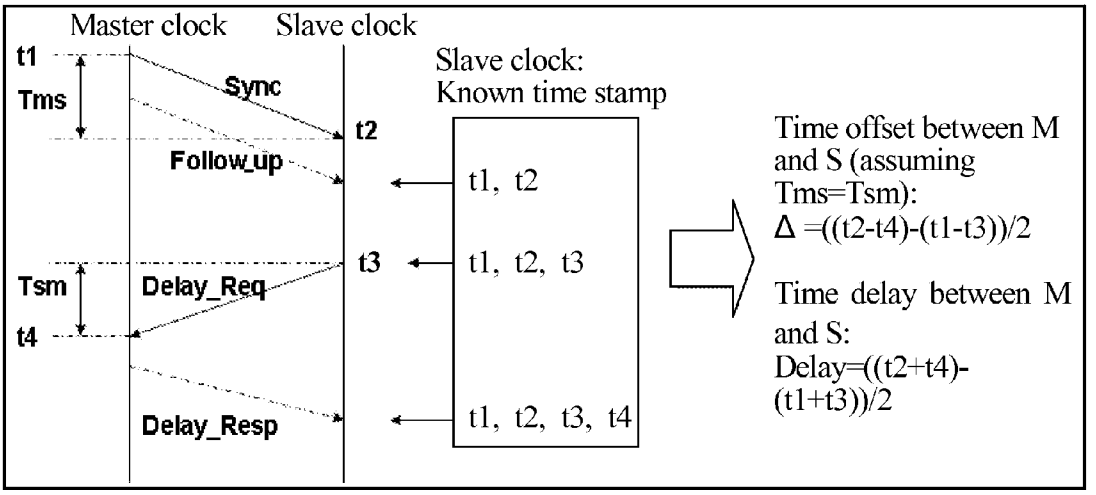

Master clock
Slave clock
t1
Tms
Sync
t2
Follow_up
Tsm
Delay_Req
t3
t4
Delay_Resp
Slave clock:
Known time stamp
t1, t2
t1, t2, t3
t1, t2, t3, t4
Time offset between M and S (assuming Tms=Tsm):
Δ =((t2-t4)-(t1-t3))/2
Time delay between M and S:
Delay=((t2+t4)-(t1+t3))/2

FIG. 1

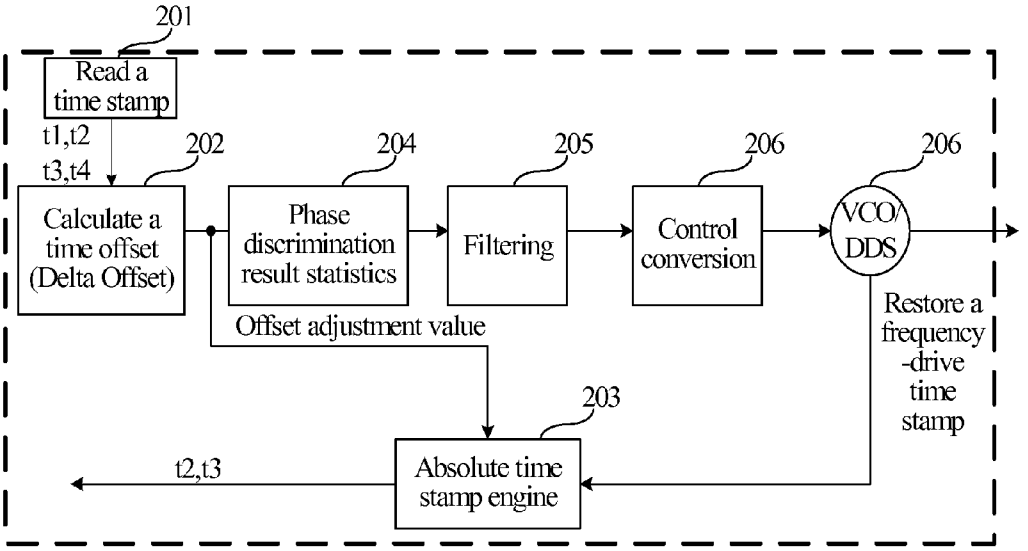

201
Read a time stamp
t1,t2
t3,t4
202
Calculate a time offset (Delta Offset)
204
Phase discrimination result statistics
205
Filtering
206
Control conversion
206
VCO/ DDS
Restore a frequency -drive time stamp
Offset adjustment value
203
Absolute time stamp engine
t2,t3

FIG. 2

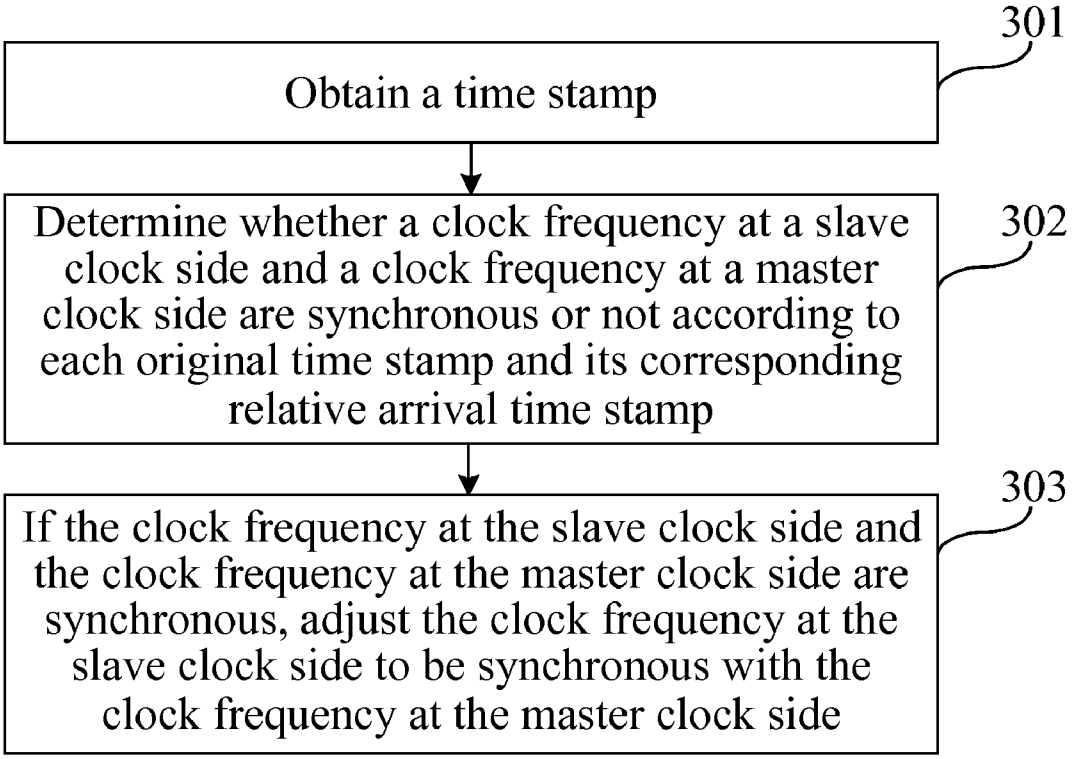

301
Obtain a time stamp
302
Determine whether a clock frequency at a slave clock side and a clock frequency at a master clock side are synchronous or not according to each original time stamp and its corresponding relative arrival time stamp
303
If the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous, adjust the clock frequency at the slave clock side to be synchronous with the clock frequency at the master clock side

FIG. 3

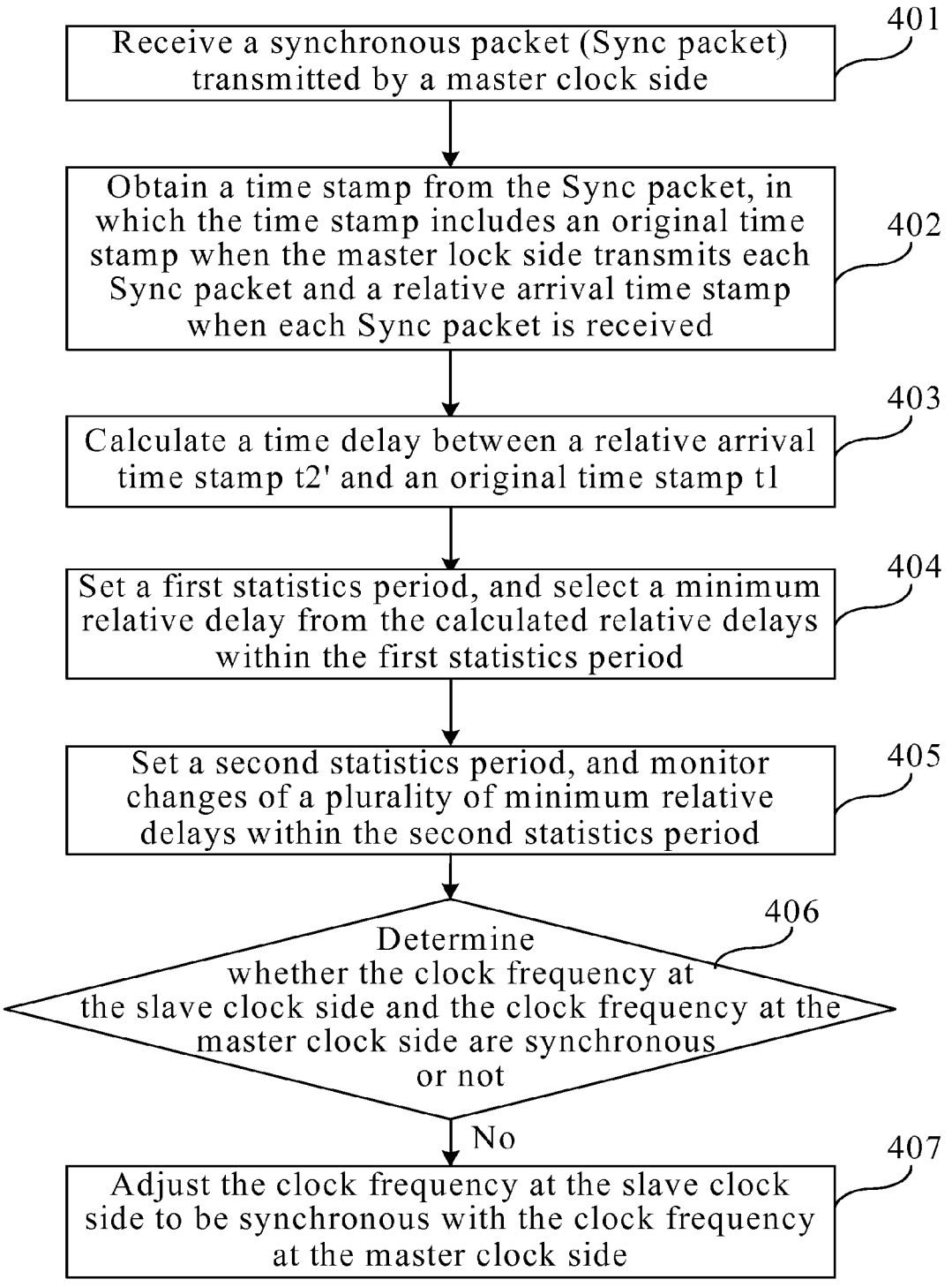

401
Receive a synchronous packet (Sync packet) transmitted by a master clock side
402
Obtain a time stamp from the Sync packet, in which the time stamp includes an original time stamp when the master lock side transmits each Sync packet and a relative arrival time stamp when each Sync packet is received
403
Calculate a time delay between a relative arrival time stamp t2' and an original time stamp t1
404
Set a first statistics period, and select a minimum relative delay from the calculated relative delays within the first statistics period
405
Set a second statistics period, and monitor changes of a plurality of minimum relative delays within the second statistics period
406
Determine whether the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous or not
No
407
Adjust the clock frequency at the slave clock side to be synchronous with the clock frequency at the master clock side

FIG. 4

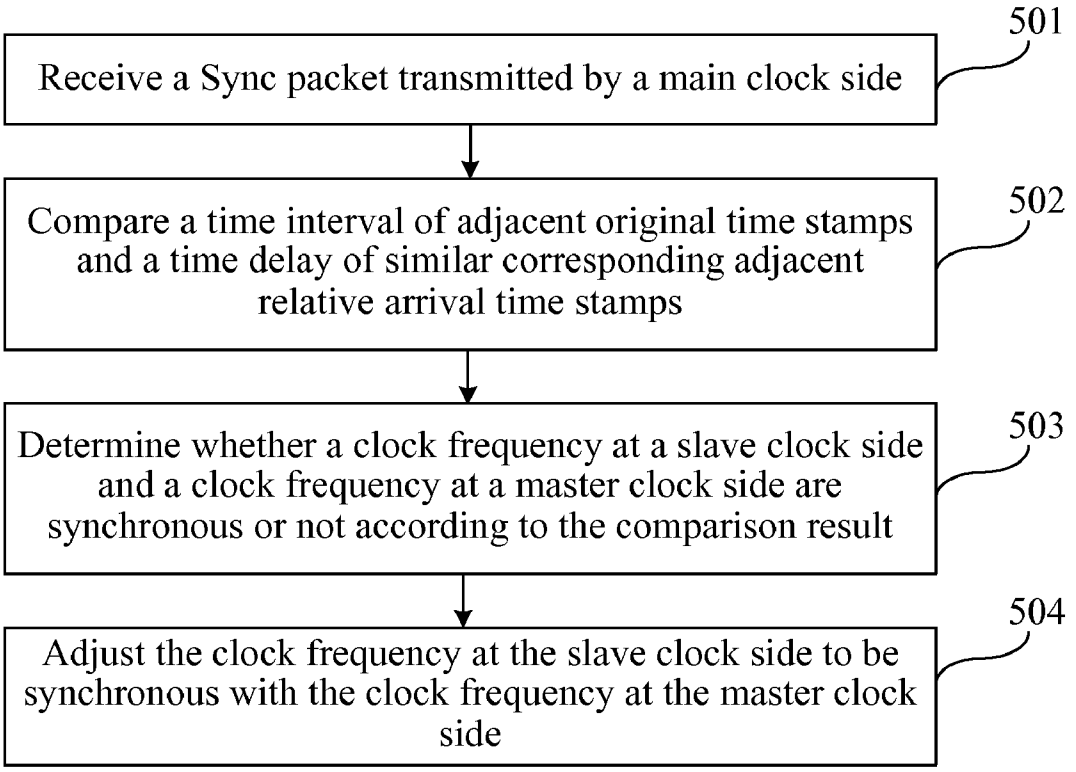

501
Receive a Sync packet transmitted by a main clock side
502
Compare a time interval of adjacent original time stamps and a time delay of similar corresponding adjacent relative arrival time stamps
503
Determine whether a clock frequency at a slave clock side and a clock frequency at a master clock side are synchronous or not according to the comparison result
504
Adjust the clock frequency at the slave clock side to be synchronous with the clock frequency at the master clock side

FIG. 5

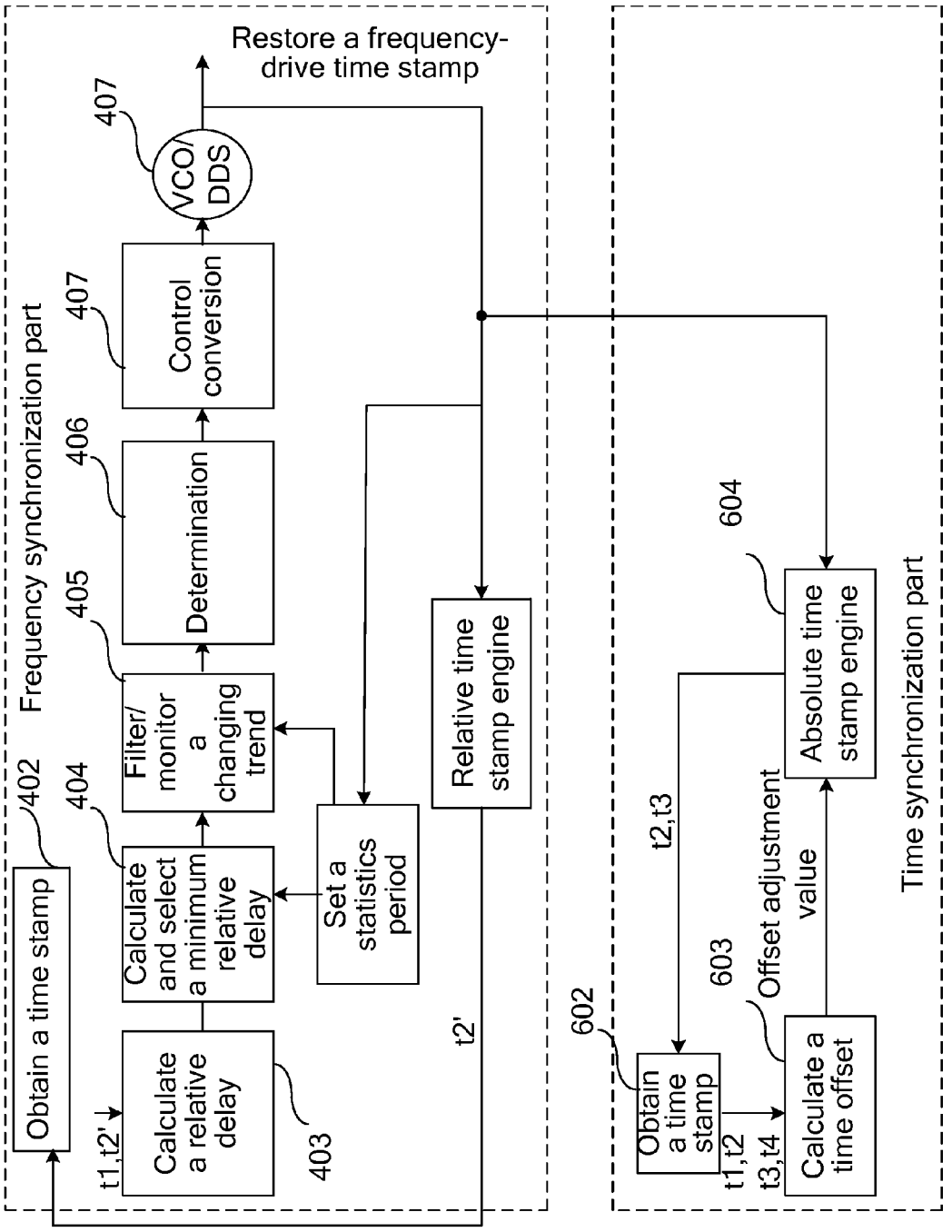

Frequency synchronization part
Time synchronization part
Restore a frequency-drive time stamp
VCO/DDS
407
Control conversion
407
406
Determination
405
Filter/monitor a changing trend
404
Calculate and select a minimum relative delay
402
Obtain a time stamp
Calculate a relative delay
403
t1,t2'
Set a statistics period
Relative time stamp engine
t2'
604
Absolute time stamp engine
t2,t3
603
Offset adjustment value
602
Obtain a time stamp
t1,t2
t3,t4
Calculate a time offset

FIG. 6

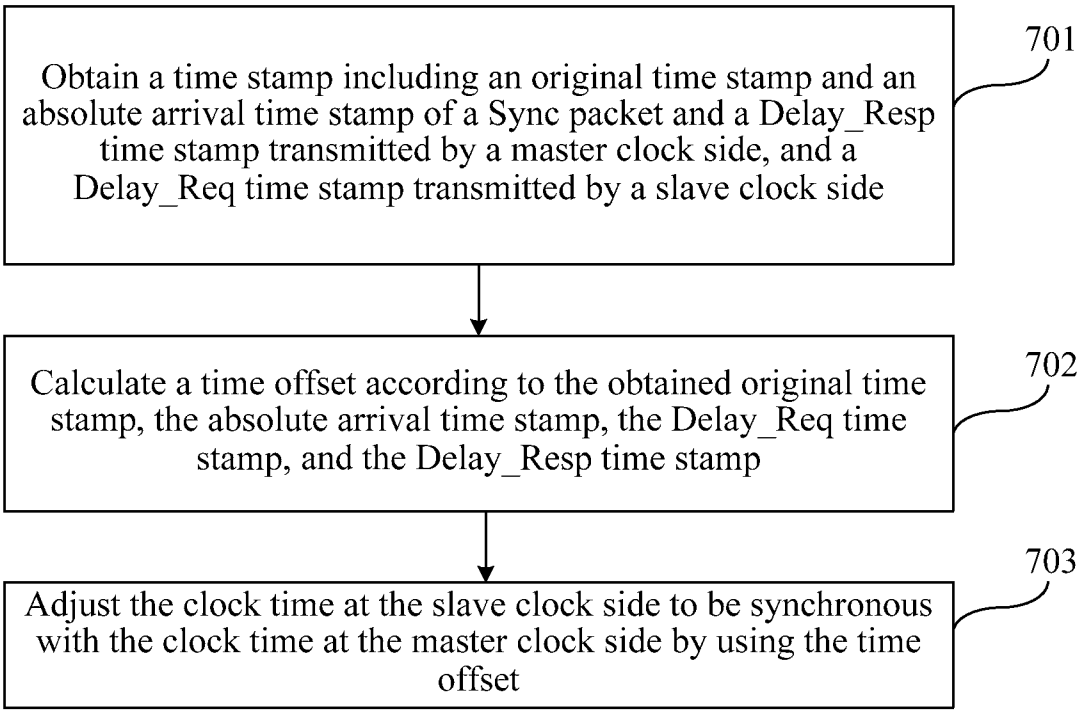

Obtain a time stamp including an original time stamp and an absolute arrival time stamp of a Sync packet and a Delay_Resp time stamp transmitted by a master clock side, and a Delay_Req time stamp transmitted by a slave clock side
701
Calculate a time offset according to the obtained original time stamp, the absolute arrival time stamp, the Delay_Req time stamp, and the Delay_Resp time stamp
702
Adjust the clock time at the slave clock side to be synchronous with the clock time at the master clock side by using the time offset
703

FIG. 7

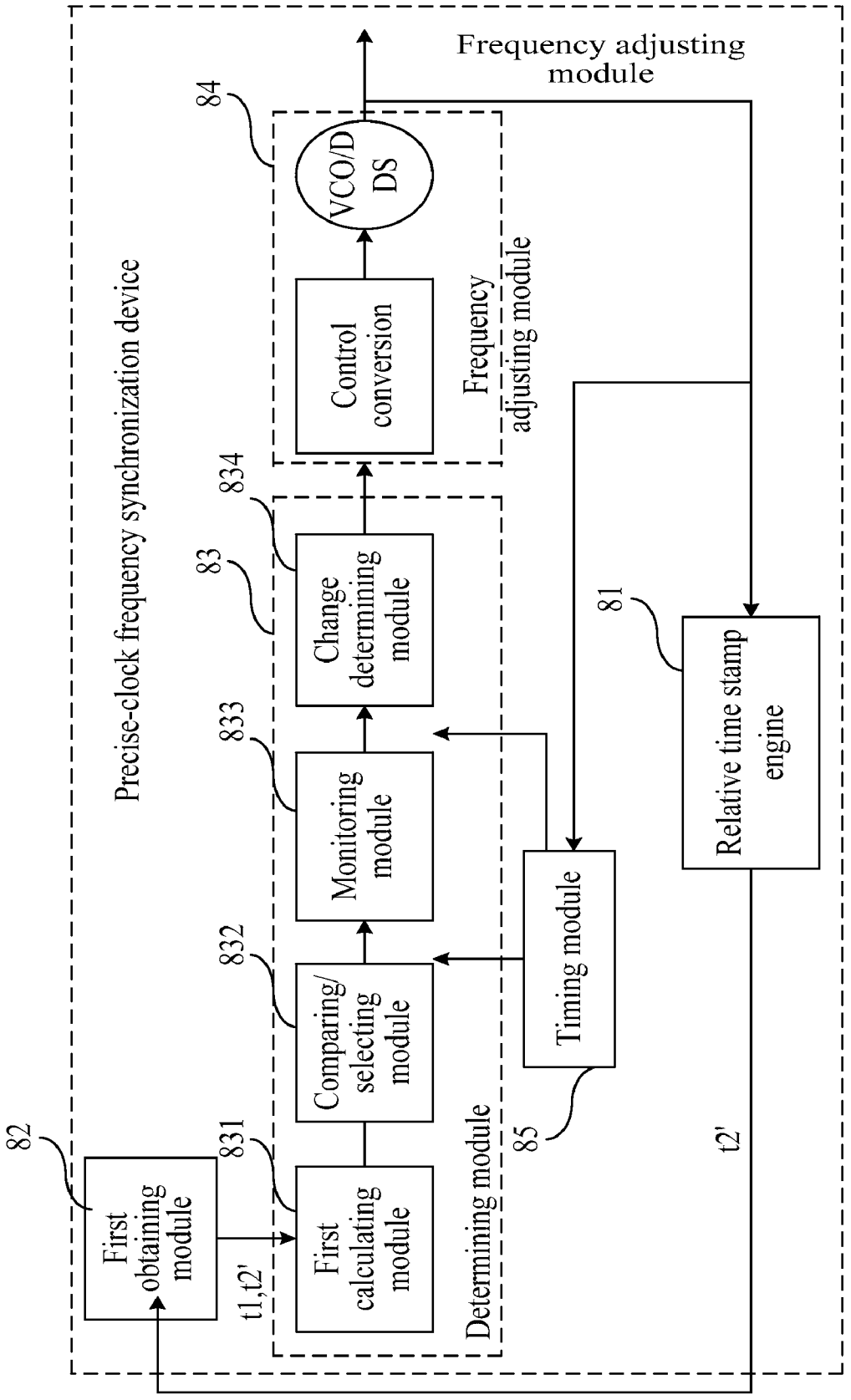

Precise-clock frequency synchronization device
Frequency adjusting module
84
VCO/DDS
Control conversion
Frequency adjusting module
834
83
Change determining module
833
Monitoring module
832
Comparing/selecting module
831
First calculating module
Determining module
82
First obtaining module
t1,t2'
85
Timing module
81
Relative time stamp engine
t2'

FIG. 8

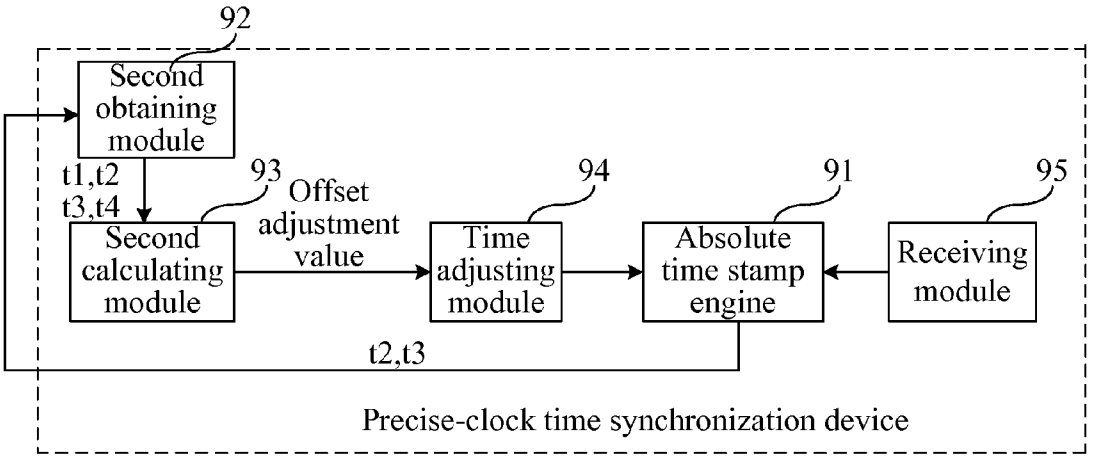

92
Second obtaining module
t1,t2
t3,t4
93
Offset adjustment value
94
91
95
Second calculating module
Time adjusting module
Absolute time stamp engine
Receiving module
t2,t3
Precise-clock time synchronization device

FIG. 9

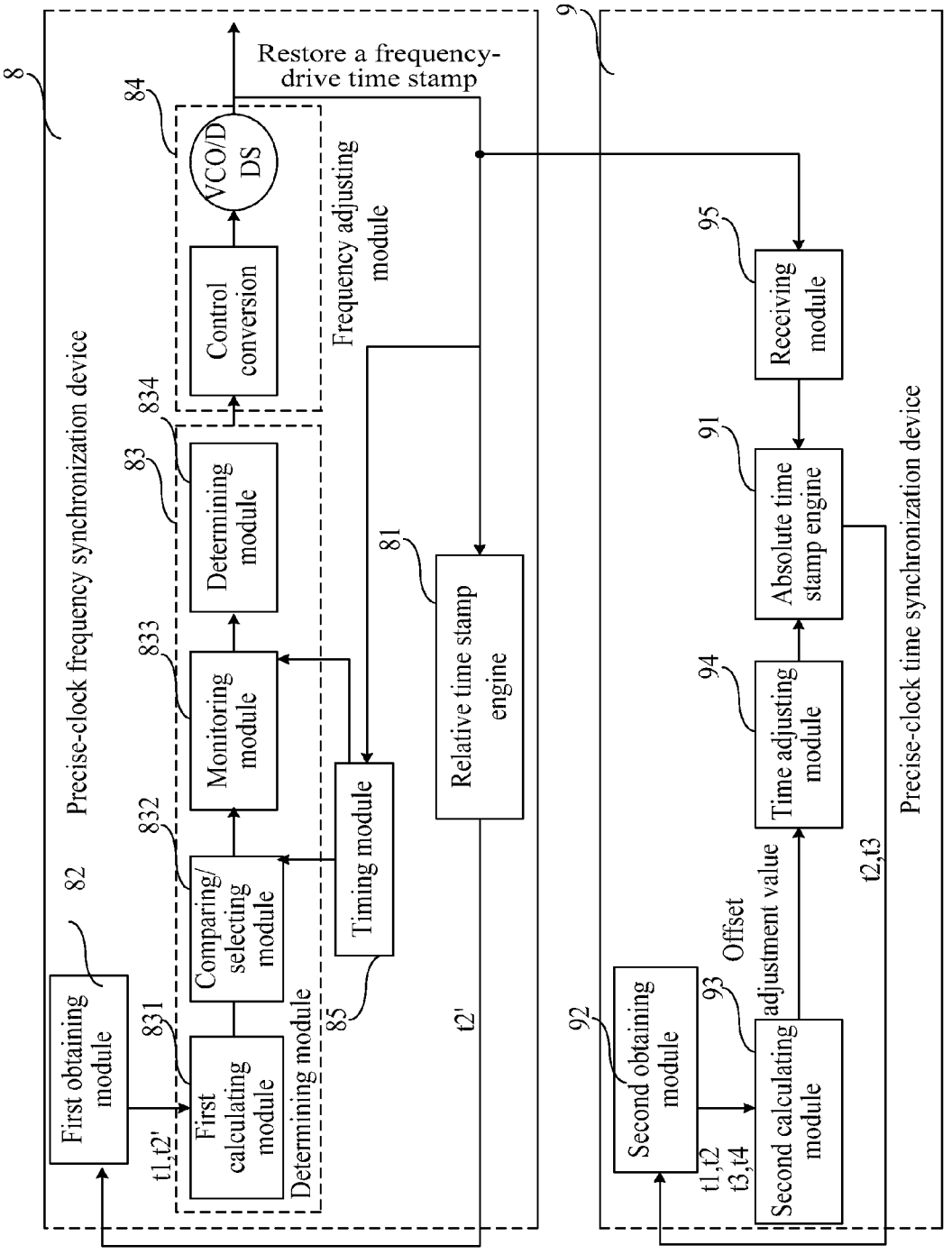

8
Precise-clock frequency synchronization device
Restore a frequency-drive time stamp
84
VCO/DDS
Frequency adjusting module
Control conversion
834
83
Determining module
833
Monitoring module
832
Comparing/selecting module
831
First calculating module
Determining module
82
First obtaining module
t1,t2'
85
Timing module
81
Relative time stamp engine
t2'
9
95
Receiving module
91
Absolute time stamp engine
94
Time adjusting module
Offset adjustment value
93
Second calculating module
t1,t2
t3,t4
92
Second obtaining module
t2,t3
Precise-clock time synchronization device

FIG. 10

# METHOD AND SYSTEM FOR PRECISE-CLOCK SYNCHRONIZATION, AND DEVICE FOR PRECISE-CLOCK FREQUENCY/TIME SYNCHRONIZATION

## CROSS-REFERENCE TO RELATED APPLICATION

**[0001]** This application claims priority to Chinese Patent Application No. 200810224615.7, filed Oct. 21, 2008, the content of which is hereby incorporated by reference in its entirety.

## FIELD OF THE TECHNOLOGY

**[0002]** The present invention relates to the field of communication technology, and more particularly, to a method and system for precise-clock synchronization and a device for precise-clock frequency/time synchronization.

## BACKGROUND OF THE INVENTION

**[0003]** IP-based communication networks have not reduced demands for clock synchronization. On the contrary, for demands of cost, safety, and services, the IP clock synchronization becomes more and more important. Among the various existing IP clock technologies, such as circuit emulation services over packet switched (CESoP), timing over packet (ToP), network time protocol (NTP), the ToP technology is a relatively new technology. For the IP clock technology, the IEEE also introduced an IEEE 1588 precision time protocol (PTP) standard. The IEEE 1588 PTP not only inherits the characteristics of performing frequency synchronization on master and slave clocks in the technology above, but also implements time synchronization, that is, phase synchronization.

**[0004]** However, in the IEEE 1588 PTP, it is necessary to collect all time stamps transmitted between the master clock and the slave clock. The time stamps are stamped by the time stamp engines located at the master clock side and the slave clock side. The time stamps mainly include transmitting time and receiving time of information such as a synchronous packet (Sync packet), follow up information (Follow_Up information), delay request packet (Delay_Req), and a delay response packet (Delay_Resp). The frequency synchronization adjustment and time synchronization adjustment of the master clock and the slave clock can be performed only after collecting sufficient information of time stamps between the master clock and the slave clock.

**[0005]** In the process of implementing the present invention, the inventor finds that there are at least the following disadvantages in the conventional art. Too much link bandwidth resources are occupied in the foresaid process. Especially, when the network transmission conditions are deteriorated and the frequency of transmitting packets needs to be increased for frequency synchronization, such a disadvantage that the clock synchronization occupies too much link bandwidth resources becomes more apparent. In addition, when only one time stamp engine exists at the slave clock side, the time of stamping a time stamp at a local position of the slave clock has to be different from the time of the local frequency synchronization; otherwise, due to the local frequency adjustment, the value of the local time stamp is influenced. Therefore, correct calculation is not able to be performed according to the obtained time stamps, and the frequency synchronization/time synchronization is thus influenced.

## SUMMARY OF THE INVENTION

**[0006]** Embodiments of the present invention provide a precise-clock synchronization method and system and a precise-clock frequency/time synchronization device, so that the frequency synchronization and time synchronization of the clocks do not interfere with each other, and the occupied link bandwidth resources are greatly reduced.

**[0007]** In an embodiment, the present invention provides a precise-clock synchronization method, which includes the following steps.

**[0008]** A time stamp is obtained. The time stamp includes at least an original time stamp about the time when a master clock side transmits each synchronous packet (Sync packet) and a relative arrival time stamp about the time that a slave clock side receives each Sync packet.

**[0009]** It is judged whether a clock frequency at the slave clock side and a clock frequency at the master clock side are synchronous or not according to each original time stamp and the corresponding relative arrival time stamp.

**[0010]** If the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous, the clock frequency at the slave clock side is adjusted to become synchronous with the clock frequency at the master clock side.

**[0011]** In another embodiment, the present invention provides a precise-clock frequency synchronization device. The precise-clock frequency synchronization device includes a relative time stamp engine, a first obtaining module, a judging module, and a frequency adjusting module.

**[0012]** The relative time stamp engine is adapted to provide a relative arrival time stamp about the time when a slave clock side receives a Sync packet.

**[0013]** The first obtaining module is adapted to obtain a time stamp. The time stamp includes at least an original time stamp about the time when the master clock side transmits each Sync packet and a relative arrival time stamp about the time when the slave clock side receives each Sync packet.

**[0014]** The judging module is adapted to judge whether a clock frequency at the slave clock side and a clock frequency at the master clock side are synchronous or not according to each original time stamp and its corresponding relative arrival time stamp.

**[0015]** The frequency adjusting module is adapted to adjust the clock frequency at the slave clock side to be synchronous with the clock frequency at the master clock side if the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous.

**[0016]** In another embodiment, the present invention provides a precise-clock time synchronization device. The precise-clock time synchronization device includes an absolute time stamp engine, a second obtaining module, a second calculating module, and a time adjusting module.

**[0017]** The absolute time stamp engine is adapted to provide an absolute arrival time stamp about the time when a slave clock side receives a Sync packet and a delay request packet (Delay_Req) time stamp about the time when the slave clock side transmits a Delay_Req.

**[0018]** The second obtaining module is adapted to obtain a time stamp including an original time stamp and an absolute arrival time stamp of the Sync packet transmitted by the

master clock side, a Delay_Resp time stamp transmitted by the master clock side, and a Delay_Req time stamp transmitted by the slave clock side.

**[0019]** The second calculating module is adapted to calculate a time offset according to the obtained original time stamp, absolute arrival time stamp, Delay_Req time stamp, and Delay_Resp time stamp.

**[0020]** The time adjusting module is adapted to adjust the clock time at the slave clock side to be synchronous with the clock time at the master clock side by using the time offset.

**[0021]** In another embodiment, the present invention provides a precise-clock synchronization system. The precise-clock synchronization system includes a precise-clock frequency synchronization device and a precise-clock time synchronization device.

**[0022]** The precise-clock frequency synchronization device is adapted to adjust a clock frequency at a slave clock side to be synchronous with a clock frequency at the master clock side according to an original time stamp about the time when the master clock side transmits a Sync packet and a relative arrival time stamp about the time when the slave clock side receives the Sync packet.

**[0023]** The precise-clock time synchronization device is adapted to calculate a time offset according to the original time stamp of the Sync packet and an absolute arrival time stamp about the time when the slave clock side receives the Sync packet, as well as a Delay_Req time stamp and Delay_Resp time stamp, and to adjust the clock time at the slave clock side to be synchronous with the clock time at the master clock side by using the time offset.

**[0024]** As can be seen from the technical solution above, in the embodiments of the present invention, the precise-clock synchronization method and system and the precise-clock frequency/time synchronization device may accomplish frequency synchronization and time synchronization of the master clock and the slave clock independently by using time stamps provided by two different time stamp engines, so that the frequency synchronization and time synchronization of the clocks do not interfere with each other, thus greatly reducing the occupied link bandwidth resources.

**[0025]** The present invention is further illustrated in detail below through specific embodiments with reference to the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0026]** To illustrate the technical solutions according to the embodiments of the present disclosure more clearly, the accompanying figures for describing the embodiments are introduced briefly in the following. Apparently, the accompanying drawings in the following description are only some embodiments of the present disclosure; persons of ordinary skill in the art can derive other drawings according to the accompanying drawings without paying any creative efforts.

**[0027]** FIG. **1** is a schematic structural view of a synchronization message exchange scheme of the IEEE 1588 PTP;

**[0028]** FIG. **2** is a schematic flow chart of a common precise-clock synchronization method;

**[0029]** FIG. **3** is a schematic flow chart of a precise-clock synchronization method according to a first embodiment of the present invention;

**[0030]** FIG. **4** is a schematic flow chart of a precise-clock synchronization method according to a second embodiment of the present invention;

**[0031]** FIG. **5** is another schematic flow chart of the precise-clock synchronization method according to the second embodiment of the present invention;

**[0032]** FIG. **6** is a schematic flow chart of a precise-clock synchronization method according to a third embodiment of the present invention;

**[0033]** FIG. **7** is a schematic flow chart of a precise-clock synchronization method according to a fourth embodiment of the present invention;

**[0034]** FIG. **8** is a schematic structural view of a precise-clock frequency synchronization device according to an embodiment of the present invention;

**[0035]** FIG. **9** is a schematic structural view of a precise-clock time synchronization device according to an embodiment of the present invention; and

**[0036]** FIG. **10** is a schematic structural view of a precise-clock synchronization system according to an embodiment of the present invention.

## DETAILED DESCRIPTION OF THE EMBODIMENTS

**[0037]** The technical solutions in the embodiments of the present invention are described clearly below with reference to the accompanying drawings in the embodiments of the present invention. Apparently, the described embodiments are only a part of embodiments of the present invention, rather than all the embodiments. On the basis of the embodiments of the present invention, all the other embodiments obtained by those of ordinary skill in the art without carrying out creative activities fall within the protection scope of the present invention.

**[0038]** FIG. **1** is a schematic structural view of a synchronization message exchange scheme of the IEEE 1588 PTP. Referring to FIG. **1**, the simple descriptions are provided as follows.

**[0039]** First, a master clock transmits a certain synchronous packet (Sync packet) periodically, usually once every two seconds. The Sync packet includes a time stamp precisely describing an estimated time of transmitting a data packet. A slave clock measures an accurate receiving time t**2** for receiving the Sync packet. As the Sync packet includes the estimated time of transmitting the data packet instead of a practical time, the master clock further transmits a piece of Follow_Up information after transmitting the Sync packet. The Follow_Up information is added with a time stamp accurately recording a practical time t**1** of transmitting the Sync packet. In such a manner, the slave clock obtains the time stamps t**1** and t**2** after receiving the Follow_Up information.

**[0040]** Subsequently, the slave clock transmits a delay request packet (Delay_Req) at a time t**3** after the Sync packet is received. After the master clock receives the Delay_Req, the master clock carries a time stamp including an accurate receiving time t**4** in a delay response packet (Delay_Resp) and transmits the Delay_Resp to the slave clock. In this way, the slave clock obtains the time stamps t**1**, t**2**, and t**3** when transmitting the Delay_Req, and obtains time stamps t**1**, t**2**, t**3**, and t**4** when receiving the Delay_Resp.

**[0041]** The slave clock calculates a time offset between the master clock and the slave clock, and a delay of the transmission link by using the collected t**1**, t**2**, t**3**, and t**4**. The time offset between the master clock and the slave clock is a value of "Δ" in FIG. **1**, and is used to modify a time difference between the master clock and the slave clock. The delay of the transmission link is a value of "Delay" in FIG. **1**, and is used

to measure a delay time caused by the network transmission. The slave clock utilizes a clock restoration algorithm through the two values, so that the master clock and the slave clock become synchronous in time and frequency.

**[0042]** It should be noted that, the Delay_Req is transmitted randomly, and has no time limits. Also, in the whole process of measurement, it is assumed that the transmission medium is uniform and symmetric.

**[0043]** FIG. **2** is a schematic flow chart of a common precise-clock synchronization method. Referring to FIG. **2**, when the exchange of synchronization messages in FIG. **1** is finished, the following steps are performed locally, that is, at the slave clock side.

**[0044]** In step **201**, a time stamp is obtained. That is, four time stamps t**1**, t**2**, t**3**, and t**4** are obtained.

**[0045]** The t**2** and t**3** are obtained from a local absolute time stamp engine. The time represented in the absolute time stamp engine is an absolute time, which has to be synchronous with the master clock.

**[0046]** In step **202**, a time offset is calculated periodically.

**[0047]** In step **203**, time adjustment is performed on the slave clock by directly using the time offset calculated each time, so as to make the time of the slave clock synchronous with the time of the master clock, and update the time of the absolute time stamp engine synchronously.

**[0048]** In step **204**, in a certain period, a statistical calculation for phase-discrimination results is performed on the multiple time offsets obtained by periodical calculation, so as to obtain an optimal time offset.

**[0049]** Step **204** and step **203** may be performed at the same time.

**[0050]** In step **205**, high frequency components in the time offset obtained in step **204** are filtered, such as a jitter value of the network, or transient value jump occurred due to occasional errors when the time stamp engine processes data, and the changing trend of the time offset is monitored.

**[0051]** Specifically, if the time offset obtained at a later time is always greater than the time offset obtained at a former time, that is, the time offset is in a forward change, it shows that a local drive frequency, that is, the drive frequency of slave-clock timing is higher than that of master-clock timing; otherwise, the drive frequency of the slave-clock timing is lower than that of the master-clock timing.

**[0052]** In step **206**, conversion of reverse control is performed according to the changing trend of the time offset, the time offset is converted into a signal that is able to be identified by a local voltage controlled oscillator (VOC) or direct digital synthesizer (DDS), so as to control the adjustment of the local oscillator such as the VCO or DDS. As a negative feedback loop is used, reverse adjustment is performed, so as to realize the frequency synchronization of the master clock and the slave clock, and the frequency synchronization result is used to update the frequency of the absolute time stamp engine synchronously.

**[0053]** After step **203** and steps **204** to **206** are performed, both the time and frequency of the absolute time stamp engine are updated. Next time a local time stamp is obtained from the absolute time stamp engine after synchronous update, and in this embodiment, it is the step of obtaining t**2** and t**3**. Steps **201** to **206** are continuously repeated, until the frequency and time locks a prime reference source, that is, the master clock.

**[0054]** The embodiment of precise-clock synchronization method is characterized in that, only one absolute time stamp engine exists, so the time of the absolute time stamp engine is changed after either time synchronization or frequency synchronization; and all synchronization messages exchanged in FIG. **1** need to be processed, so as to obtain the time offset required in both frequency restoration (frequency synchronization) and time setting (time synchronization).

**[0055]** The solution in the embodiment of the present invention utilizes two time stamp engines. One is a relative time stamp engine, which does not need time setting. The other one is an absolute time stamp engine representing an absolute time. The two time stamp engines are used to perform frequency and time synchronization for the master clock and the slave clock respectively, so that the frequency synchronization and the time synchronization of the master clock and the slave clock may be performed independently. Also, when frequency synchronization is performed for the relative time stamp engine, the synchronization message does not need to be processed.

**[0056]** FIG. **3** is a schematic flow chart of a precise-clock synchronization method according to a first embodiment of the present invention. Referring to FIG. **3**, the precise-clock synchronization method includes the following steps.

**[0057]** In step **301**, a time stamp is obtained. The time stamp includes at least an original time stamp about the time when a master clock side transmits each Sync packet and a relative arrival time stamp about the time when each Sync packet is received.

**[0058]** The original time stamp is a time of transmitting the Sync packet stamped at the master clock side, that is, the time of the master clock. The relative time stamp is a local time when the slave clock side receives the Sync packet, that is, the time of the slave clock.

**[0059]** In step **302**, it is judged whether a clock frequency at the slave clock side is synchronous with a clock frequency at the master clock side or not according to each original time stamp and its corresponding relative arrival time stamp.

**[0060]** In step **302**, several manners are available for judging whether the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous or not according to each original time stamp and its corresponding relative arrival time stamp. For example, the judgment may be formed through a changing trend of a relative delay, that is, a changing trend of a time difference between the original time stamp and the relative arrival time stamp. Alternatively, the judgment may also be formed through comparison between a time interval of adjacent original time stamps and a time interval of similar adjacent relative arrival time stamps, and the like.

**[0061]** In step **303**, if the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous, the clock frequency at the slave clock side is adjusted to become synchronous with the clock frequency at the master clock side.

**[0062]** The precise-clock synchronization method provided in this embodiment is able to be applied in a situation not requiring the time synchronization of the master clock and the slave clock or having a low requirement on the time synchronization or having good time synchronization. As the frequency synchronization of the master clock and the slave clock may be realized by using the Sync packet only, the bandwidth is greatly saved. Especially when the network is deteriorated, a packet transmission frequency needs to be increased to obtain more sampling points to ensure clock synchronization quality, the advantage becomes more apparent.

**[0063]** FIG. **4** is a schematic flow chart of a precise-clock synchronization method according to a second embodiment of the present invention. Referring to FIG. **4**, the precise-clock synchronization method includes the following steps.

**[0064]** In step **401**, a Sync packet transmitted by a master clock side is received.

**[0065]** In step **402**, a time stamp is obtained from the Sync packet. The time stamp includes an original time stamp about the time when the master clock side transmits each Sync packet and a relative arrival time stamp about the time when each Sync packet is received.

**[0066]** As shown in FIG. **1**, the original time stamp of the Sync packet is a time t**1** when the master clock side transmits the Sync packet. The relative arrival time stamp of the Sync packet is transmitted locally, that is, transmitted by the relative time stamp engine at the slave clock side. The relative time stamp engine does not need time setting and is only used for frequency synchronization. Therefore, the relative arrival time stamp obtained from the relative time stamp engine is indicated by t**2'**, denoting a relative arrival time, rather than an absolute arrival time.

**[0067]** In step **403**, a relative delay between the relative arrival time stamp t**2'** and the original time stamp t**1** is calculated.

**[0068]** The relative delay=the relative arrival time stamp t**2'**—the original time stamp t**1**. Alternatively, the relative delay=the original time stamp t**1**—the relative arrival time stamp t**2'**. In the embodiment of the present invention, the equation that the relative delay=the relative arrival time stamp t**2'**—the original time stamp t**1** is used.

**[0069]** In step **404**, a first statistics period is set. Within the first statistics period, a minimum relative delay is selected from a plurality of calculated relative delays.

**[0070]** Within a certain statistics period, one minimum relative delay is selected from the plurality of relative delays calculated by using step **403** many times. The minimum relative delay represents the best network transmission performance, which is able to show the transmission delay characteristic of the physical layer more practically. It is equivalent to that the jittering of the network is filtered once.

**[0071]** In step **405**, a second statistics period is set, and a changing trend of the minimum relative delay within the second statistics period is monitored.

**[0072]** The second statistics period in step **405** is a time period including a plurality of continuous first statistics periods. Within this time period of the second statistics period, the changing trend of the obtained minimum relative delay is monitored. The changing trend may include that the value of the minimum relative delay gradually increases or decreases.

**[0073]** In addition, before step **405**, the method further includes filtering the selected minimum relative delay, so as to filter high frequency components. The first statistics period and second statistics period may be set by a timer respectively.

**[0074]** In step **406**, it is judged whether the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous or not according to the changing trend of the minimum relative delay monitored in step **405**.

**[0075]** Specifically, if the values of two adjacent minimum relative delays gradually increase or decrease, it indicates that the clock frequency at the slave clock side and the clock frequency at the master clock side are not synchronous, so step **407** is performed. If the value of the minimum relative delay is constant, it indicates that the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous.

**[0076]** In step **407**, the clock frequency at the slave clock side is adjusted to become synchronous with the clock frequency at the master clock side.

**[0077]** In step **406**, if it is found that the values of two adjacent minimum relative delays gradually increase by statistics, it indicates that the local relative time stamp engine, that is, the relative time stamp engine at the slave clock side runs is faster than the time engine at the master clock side, denoting that the frequency of the slave clock is higher than the frequency of the master clock. On the contrary, it denotes that the frequency of the slave clock is lower than the frequency of the master clock. Therefore, if the frequency of the slave clock is higher than the frequency of the master clock, in step **407**, a variation of the minimum relative delay is converted into a signal value that can be identified by the oscillator. The output frequency of the local oscillator is then turned slower. The local oscillator may be a VCO or a DDS.

**[0078]** FIG. **5** is another schematic flow chart of the precise-clock synchronization method according to a second embodiment of the present invention. Referring to FIG. **5**, the precise-clock synchronization method includes the following steps.

**[0079]** In step **501**, a Sync packet transmitted by a master clock side is received.

**[0080]** In step **502**, a time interval of adjacent original time stamps and a time interval of similar corresponding adjacent relative arrival time stamps are compared.

**[0081]** In step **503**, it is judged whether a clock frequency at a slave clock side and a clock frequency at the master clock side are synchronous or not according to a comparison result.

**[0082]** It is assumed that a periodic interval that the master clock side transmits the Sync packet is ΔTT. A time interval that the slave clock side receives the corresponding Sync packet is ΔTR. If the ΔTT is not equal to the ΔTR, it indicates that the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous, and step **503** is performed. On the contrary, if the intervals are the same, it indicates that the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous.

**[0083]** In step **504**, the clock frequency at the slave clock side is adjusted to become synchronous with the clock frequency at the master clock side.

**[0084]** For the precise-clock synchronization method provided in this embodiment, the frequency synchronization of the slave clock and the master clock may be performed as long as an original time stamp and a relative arrival time stamp of the Sync packet are obtained locally, that is, at the slave clock side. The method may be applied in a situation having low requirement on the time synchronization of clock or having good time synchronization, so the bandwidth may be greatly saved. Especially, when the network is deteriorated, the packet transmission frequency needs to be increased to obtain more sampling points to ensure clock synchronization quality, the advantages becomes more apparent.

**[0085]** FIG. **6** is a schematic flow chart of a precise-clock synchronization method according to a third embodiment of the present invention. Referring to FIG. **6**, the differences between the flow in FIG. **6** and that in the second embodiment shown in FIGS. **4** and **5** are described as follows. The obtained time stamp further includes an absolute arrival time stamp, a

Delay_Req time stamp, and a Delay_Resp time stamp of the Sync packet. After the frequency synchronization is accomplished, the time of the master clock and the slave clock may be synchronized according to the calculated time offset. Taking the precise-clock synchronization method in steps **401** to **407** as an example, the time synchronization has the following two situations.

**[0086]** In the first situation, the method further includes the following steps after receiving the Sync packet transmitted by the master clock side in step **401**.

**[0087]** In step **601**, a Delay_Req packet is transmitted, and a Delay_Resp packet returned by the master clock side after it receives the Delay_Req packet is received.

**[0088]** In step **602**, a time stamp including an absolute arrival time stamp, a Delay_Req packet time stamp, and a Delay_Resp packet time stamp of the Sync packet is obtained.

**[0089]** The absolute arrival time stamp, the Delay_Req time stamp, and the Delay_Resp time stamp of the Sync packet are an accurate receiving time t**2** when the slave clock side receives the Sync packet, a time t**3** when the slave clock transmits the Delay_Req, and an accurate receiving time t**4** of the master clock introduced in the synchronization message exchange scheme in the IEEE 1588 PTP, respectively.

**[0090]** In step **603**, a time offset is calculated according to the obtained time stamp.

**[0091]** At this time, the time stamp used to calculate the time offset obtained in step **603** includes the original time stamp t**1** obtained in step **402**, the absolute arrival time stamp t**2**, the Delay_Req time stamp t**3**, and the Delay_Resp time stamp t**4** obtained in step **602**. The process of calculating the time offset according to t**1**, t**2**, t**3**, and t**4** are as shown in FIGS. **1** and **2**, and the description of which is not repeated here.

**[0092]** After the synchronization of the clock frequency at the slave clock side and the clock frequency at the master clock side in step **407** is performed, the method further includes step **604**, in which a time synchronization enable signal is received, and the clock time of the slave clock side is adjusted to be synchronous with the clock time at the master clock side by using the time offset in step **603**.

**[0093]** In FIG. **6**, steps **401** and **601** among the steps are not shown.

**[0094]** In the second situation which is not shown in FIG. **6**, after step **407** is performed so that the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous, the method further includes the following steps.

**[0095]** In step **601'**, a time synchronization enable signal is received.

**[0096]** In step **602'**, a Delay_Req is transmitted at the time when the time synchronization enable signal is received, and a Delay_Resp returned by the master clock side after it receives the Delay_Req is received.

**[0097]** In step **603'**, a time stamp including an original time stamp and an absolute arrival time stamp, a Delay_Req time stamp, and a Delay_Resp time stamp of the Sync packet is obtained.

**[0098]** In step **604'**, a time offset is calculated according to the obtained time stamp. The time stamp includes the original time stamp t**1**, the absolute arrival time stamp t**2**, the Delay_Req time stamp t**3**, and the Delay_Resp time stamp t**4**.

**[0099]** In step **605'**, the clock time at the slave clock side is adjusted to become synchronous with the clock time at the master clock side by using the time offset.

**[0100]** As can be seen from the precise-clock synchronization method provided in this embodiment, when the time and frequency of the master clock and the slave clock need to be synchronous, the relative delay time may be calculated according to the relative arrival time stamp of the Sync packet provided by the relative time stamp engine and the time offset may be calculated according to the absolute arrival time stamp of the Sync packet provided by the absolute time stamp engine at the same time. Next, after the frequencies of the master clock and the slave clock are synchronized by using the relative delay time, the time of the master clock and the slave clock are then synchronized by using the time offset according to the enable indication after the frequency synchronization is accomplished. Alternatively, the relative delay time may also be calculated first, and the time offset is then calculated to perform time synchronization on the master clock and the slave clock a relatively long time after the frequencies of the master clock and the slave clock are synchronized. In this way, the frequency synchronization and the time synchronization may be separately performed and do not interfere with each other, thus saving the bandwidth.

**[0101]** FIG. **7** is a schematic flow chart of a precise-clock synchronization method according to a fourth embodiment of the present invention. Referring to FIG. **7**, the precise-clock synchronization method includes the following steps.

**[0102]** In step **701**, a time stamp including an original time stamp, an absolute arrival time stamp, and a Delay_Resp time stamp of a Sync packet transmitted by a master clock side, as well as a Delay_Req time stamp transmitted by the slave clock side are obtained.

**[0103]** The master clock side transmits the Sync packet. The slave clock side transmits a Delay_Req after receiving the transmitted Sync packet for a set period of time. The master clock side transmits a Delay_Resp after receiving the Delay_Req. The slave clock side receives the Delay_Resp. Time stamps, i.e. the time stamps obtained in step **701** are stamped in the packets.

**[0104]** In step **702**, a time offset is calculated according to the obtained original time stamp, absolute arrival time stamp, Delay_Req time stamp, and Delay_Resp time stamp.

**[0105]** In step **703**, the clock time at the slave clock side is adjusted to become synchronous with the clock time at the master clock side by using the time offset.

**[0106]** In this embodiment, the time of the master clock and the slave clock may be synchronized independently by calculating the obtained time stamps.

**[0107]** Before the clock time at the slave clock side is adjusted by using the time offset in step **703**, or before the slave clock side transmits the Delay_Req, the method may further include receiving a time synchronization enable signal to enable the time synchronization process. The time that the time synchronization enable signal is received before the slave clock side transmits the Delay_Req is a time of the arrival set time. The time synchronization enable signal may be a completion indication for the synchronization between the clock frequency at the slave clock side and the clock frequency at the master clock side. From the descriptions of the precise-clock synchronization method in the first, second, and third embodiments, the method of realizing frequency synchronization of the master clock and the slave clock may be used in this embodiment to be combined with the time synchronization.

**[0108]** FIG. **8** is a schematic structural view of a precise-clock frequency synchronization device according to an

embodiment of the present invention. Referring to FIG. **8**, the precise-clock frequency synchronization device includes a relative time stamp engine **81**, a first obtaining module **82**, a judging module **83**, and a frequency adjusting module **84**. The relative time stamp engine **81** provides a relative arrival time stamp about the time when the slave clock side receives a Sync packet. The first obtaining module **82** obtains a time stamp, and the time stamp includes at least an original time stamp about the time when the master clock side transmits each Sync packet and a relative arrival time stamp about the time when the slave clock side receives each Sync packet. The judging module **83** judges whether the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous or not according to each original time stamp and its corresponding relative arrival time stamp. The frequency adjusting module **84** adjusts the clock frequency at the slave clock side to be synchronous with the clock frequency at the master clock side if the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous. A plurality of manners exists for the judging module **83** to judge whether the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous or not according to each original time stamp and its corresponding relative arrival time stamp. For example, the judgment may be formed through a changing trend of the relative delay, that is, a changing trend of a time difference between the original time stamp and the relative arrival time stamp. Alternatively, the judgment may be formed through the comparison between a time interval of the adjacent original time stamps and a time interval of similar corresponding adjacent relative arrival time stamps, and the like.

**[0109]** In this embodiment, the judging module **83** in the precise-clock frequency synchronization device specifically includes a first calculating module **831**, a comparing/selecting module **832**, a monitoring module **833**, and a change judging module **834**. The first calculating module **831** calculates a relative delay between the relative arrival time stamp and the original time stamp. The comparing/selecting module **832** selects a minimum relative delay from a plurality of calculated relative delays within a first statistics period. The monitoring module **833** monitors changes of the plurality of minimum relative delays within a second statistics period. The change judging module **834** judges whether the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous or not according to a changing trend of the plurality of minimum relative delay. If values of two adjacent minimum relative delays gradually increase or decrease, it indicates that the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous. If a value of the minimum relative delay is constant, it indicates that the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous. The monitoring module **833** further has a function of filtering the selected minimum relative delays to filter high frequency components.

**[0110]** In this embodiment, the precise-clock frequency synchronization device further includes a timing module **85** adapted to set the first statistics period and the second statistics period.

**[0111]** The specific process that the precise-clock frequency synchronization device provided in this embodiment performs frequency synchronization of the master clock and the slave clock is as described in the embodiments of the methods, which may be separately applied in the situation not requiring the time synchronization of the master clock and the slave clock or having low requirement on the time synchronization or having good time synchronization. As the use of the Sync packet may realize the frequency synchronization of the master clock and the slave clock, the bandwidth is greatly saved. Especially when the network is deteriorated and packet transmission frequency needs to be increased to ensure the clock quality, the advantage becomes more apparent.

**[0112]** FIG. **9** is a schematic structural view of a precise-clock time synchronization device according to an embodiment of the present invention. Referring to FIG. **9**, the precise-clock time synchronization device includes an absolute time stamp engine **91**, a second obtaining module **92**, a second calculating module **93**, and a time adjusting module **94**. The absolute time stamp engine **91** provides an absolute arrival time stamp about the time when a slave clock side receives a Sync packet and a Delay_Req time stamp about the time when the slave clock side transmits a Delay_Req. The second obtaining module **92** obtains a time stamp including an original time stamp and an absolute arrival time stamp of the Sync packet transmitted by the master clock side, a Delay_Resp time stamp transmitted by the master clock side, and a Delay_Req time stamp transmitted by the slave clock side. The second calculating module **93** calculates a time offset according to the obtained original time stamp, absolute arrival time stamp, Delay_Req time stamp, and Delay_Resp time stamp. The time adjusting module **94** adjusts the clock time at the slave clock side to be synchronous with the clock time at the master clock side by using the time offset.

**[0113]** In this embodiment, the precise-clock time synchronization device further includes a receiving module **95** adapted to receive a time synchronization enable signal.

**[0114]** The specific process that the precise-clock time synchronization device provided in this embodiment performs time synchronization of the master clock and the slave clock is as described in the methods in the embodiments. The time of the master clock and the slave clock may be synchronized separately by calculating the obtained time stamps.

**[0115]** FIG. **10** is a schematic structural view of a precise-clock synchronization system according to an embodiment of the present invention. Referring to FIG. **10**, the precise-clock synchronization system includes a precise-clock frequency synchronization device **8** and a precise-clock time synchronization device **9**. The precise-clock frequency synchronization device **8** adjusts a clock frequency at a slave clock side to be synchronous with a clock frequency at a master clock side according to an original time stamp about the time when the master clock side transmits a Sync packet and a relative arrival time stamp about the time when the slave clock side receives the Sync packet. The precise-clock time synchronization device **9** calculates a time offset according to the original time stamp of the Sync packet and an absolute arrival time stamp about the time when the slave clock side receives the Sync packet, as well as a Delay_Req time stamp and a Delay_Resp time stamp, and adjusts the clock time at the slave clock side to be synchronous with the clock time at the master clock side by using the time offset. Specific structures of the precise-clock frequency synchronization device **8** and the precise-clock time synchronization device **9** are described in the embodiment of the precise-clock frequency synchronization device shown in FIG. **8** and the embodiment of the precise-clock time synchronization device shown in FIG. **9**, and the descriptions of which are not repeated here.

**[0116]** The specific process of the precise-clock synchronization system provided in this embodiment performing frequency synchronization, time synchronization and their combination of the master clock and the slave clock is as described in the embodiments of the methods. When the time and frequency of the master clock and the slave clock need to be synchronized, the relative delay time may be calculated according to the relative arrival time stamp of the Sync packet provided by the relative time stamp engine and the time offset may be calculated according to the absolute arrival time stamp of the Sync packet provided by the absolute time stamp engine at the same time. Next, after the frequencies of the master clock and the slave clock are synchronized by using the relative delay time, the time of the master clock and the slave clock are then synchronized by using the time offset according to an enable indication after the frequency synchronization is accomplished. Alternatively, the relative delay time may be calculated first, and the time offset is then calculated to perform time synchronization of the master clock and the slave clock, after accomplishing the frequency synchronization of the master clock and the slave clock for a long time. In this way, the frequency synchronization and the time synchronization may be separately processed and do not interfere with each other, thus saving the bandwidth.

**[0117]** Those of ordinary skill in the art should understand that all or a part of processes in the method according to the embodiments may be implemented by a computer program instructing relevant hardware. The program may be stored in a computer readable storage medium. When the program is executed, the processes of the methods according to the embodiments of the present invention are performed. The storage medium may be a magnetic disk, an optical disk, a read-only memory (ROM), a random access memory (RAM), or the like.

**[0118]** Finally, it should be noted that the above embodiments are merely provided for describing the technical solutions of the present invention, but not intended to limit the present invention. It should be understood by those of ordinary skill in the art that although the present invention has been described in detail with reference to the foregoing embodiments, modifications can be made to the technical solutions described in the foregoing embodiments, or equivalent replacements can be made to some technical features in the technical solutions, and such modifications or replacements do not cause the essence of corresponding technical solutions to depart from the spirit and scope of the present invention.

What is claimed is:

**1**. A precise-clock synchronization method, comprising:

obtaining a time stamp, wherein the time stamp comprises at least an original time stamp about the time when a master clock side transmits a Sync packet and a relative arrival time stamp about the time when a slave clock side receives the Sync packet;

determining whether a clock frequency at the slave clock side is synchronous with a clock frequency at the master clock side or not according to the original time stamp and its corresponding relative arrival time stamp;

synchronizing the clock frequency at the slave clock side with the clock frequency at the master clock side, if the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous.

**2**. The precise-clock synchronization method according to claim **1**, wherein the synchronizing the clock frequency at the slave clock side with the clock frequency at the master clock side comprises:

calculating a relative delay between the relative arrival time stamp and the original time stamp;

setting a first statistics period having a minimum relative delay selected from a plurality of calculated relative delays;

setting a second statistics period, and monitoring a changing trend of the minimum relative delay within the second statistics period;

determining whether the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous or not according to the changing trend of the minimum relative delay.

**3**. The precise-clock synchronization method according to claim **2**, wherein if the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous, the method comprises:

determining that the clock frequency at the slave clock side and the clock frequency at the master clock side are not synchronous, if the values of two adjacent minimum relative delays are not substantially the same.

**4**. The precise-clock synchronization method according to claim **2**, wherein the calculating a relative delay between the relative arrival time stamp and the original time stamp comprises:

getting the relative delay through calculating the absolute value of the difference between the relative arrival time stamp and the original time stamp.

**5**. The precise-clock synchronization method according to claim **2**, wherein before setting the second statistics period, the method further comprises:

filtering the selected minimum relative delay.

**6**. The precise-clock synchronization method according to claim **1**, wherein the determining whether a clock frequency at the slave clock side is synchronous with a clock frequency at the master clock side or not according to the original time stamp and its corresponding relative arrival time stamp comprises:

comparing a time interval of adjacent original time stamps with a time interval of similar corresponding adjacent relative arrival time stamps;

determining whether a clock frequency at a slave clock side and a clock frequency at the master clock side are synchronous or not according to a comparison result.

**7**. The precise-clock synchronization method according to claim **6**, wherein if the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous, the method comprises:

determining that the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous, if the time interval of original time stamps is different from the time interval of relative arrival time stamps.

**8**. The precise-clock synchronization method according to claim **1**, wherein obtaining a time stamp comprises:

receiving the Sync packet transmitted by a master clock side;

transmitting a Delay_Req packet, and receiving a Delay_Resp packet returned by the master clock side after it receives the Delay_Req packet;

obtaining the time stamp including the original time stamp, the relative arrival time stamp and an absolute arrival time stamp of the Sync packet, a Delay_Resp time stamp, and a Delay_Req time stamp; and

calculating a time offset according to the original time stamp, the absolute arrival time stamp, the Delay_Resp time stamp, and the Delay_Req time stamp.

**9**. The precise-clock synchronization method according to claim **8**, wherein the method further comprises:

receiving a time synchronization enable signal after the synchronization between the clock frequency at the slave clock side and the clock frequency at the master clock;

synchronizing the clock time at the slave clock side with the clock time at the master clock side by using the time offset.

**10**. The precise-clock synchronization method according to claim **1**, wherein the method further comprises:

receiving a time synchronization enable signal after the synchronization between the clock frequency at the slave clock side and the clock frequency at the master clock side;

transmitting a Delay_Req at the time when the time synchronization enable signal is received, and receiving a Delay_Resp returned by the master clock side after it receives the Delay_Req;

obtaining the time stamp including the original time stamp, and an absolute arrival time stamp of the Sync packet, a Delay_Resp time stamp, and a Delay_Req time stamp;

calculating a time offset according to the original time stamp, the absolute arrival time stamp, the Delay_Resp time stamp, and the Delay_Req time stamp; and

synchronizing the clock time at the slave clock side with the clock time at the master clock side by using the time offset.

**11**. A precise-clock frequency synchronization device, comprising:

a relative time stamp engine, adapted to provide a relative arrival time stamp about the time when the slave clock side receives a Sync packet;

a first obtaining module, adapted to obtain a time stamp, wherein the time stamp comprises at least an original time stamp about the time when the master clock side transmits each Sync packet and the relative arrival time stamp about the time when the slave clock side receives the Sync packet;

a judging module, adapted to judge whether the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous or not according to the each original time stamp and its corresponding relative arrival time stamp;

a frequency adjusting module, adapted to synchronize the clock frequency at the slave clock side with the clock frequency at the master clock side, if the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous.

**12**. The precise-clock frequency synchronization device according to claim **11**, wherein the judging module comprises:

a first calculating module, adapted to calculate a relative delay between the relative arrival time stamp and the original time stamp;

a comparing/selecting module, adapted to select a minimum relative delay from a plurality of calculated relative delays within a first statistics period;

a monitoring module, adapted to monitor changes of the plurality of minimum relative delays within a second statistics period;

a change judging module, adapted to judge whether the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous or not according to a changing trend of the plurality of minimum relative delay.

**13**. The precise-clock frequency synchronization device according to claim **12**, wherein the precise-clock frequency synchronization device further comprises a timing module adapted to set the first statistics period and the second statistics period.

**14**. A precise-clock time synchronization device, comprising:

an absolute time stamp engine, adapted to provide an absolute arrival time stamp about the time when a slave clock side receives a Sync packet and a Delay_Req time stamp about the time when the slave clock side transmits a Delay_Req;

a second obtaining module, adapted to obtain an original time stamp and an absolute arrival time stamp of the Sync packet transmitted by the master clock side, a Delay_Resp time stamp transmitted by the master clock side, and a Delay_Req time stamp transmitted by the slave clock side;

a second calculating module, adapted to calculate a time offset according to the obtained original time stamp, the absolute arrival time stamp, the Delay_Req time stamp, and the Delay_Resp time stamp;

a time adjusting module, adapted to synchronize the clock time at the slave clock side with the clock time at the master clock side by using the time offset.

**15**. The precise-clock time synchronization device according to claim **14**, wherein the precise-clock time synchronization device further comprises a receiving module adapted to receive a time synchronization enable signal.

**16**. A precise-clock synchronization system, comprising:

a precise-clock frequency synchronization device, adapted to synchronize a clock frequency at a slave clock side with a clock frequency at a master clock side, according to an original time stamp about a time when the master clock side transmits a Sync packet and a relative arrival time stamp about a time when the slave clock side receives the Sync packet;

a precise-clock time synchronization device, adapted to calculate a time offset according to the original time stamp of the Sync packet and an absolute arrival time stamp about the time when the slave clock side receives the Sync packet, as well as a Delay_Req time stamp and a Delay_Resp time stamp, and adjust the clock time at the slave clock side to be synchronous with the clock time at the master clock side by using the time offset.

**17**. The precise-clock synchronization system according to claim **16**, wherein the precise-clock frequency synchronization device comprises:

a relative time stamp engine, adapted to provide a relative arrival time stamp about the time when the slave clock side receives the Sync packet;

a first obtaining module, adapted to obtain a time stamp, wherein the time stamp comprises at least the original

time stamp about the time when the master clock side transmits the Sync packet and the relative arrival time stamp about the time when the slave clock side receives the Sync packet;

a judging module, adapted to determine whether the clock frequency at the slave clock side and the clock frequency at the master clock side are synchronous or not according to the original time stamp and its corresponding relative arrival time stamp;

a frequency adjusting module, adapted to synchronize the clock frequency at the slave clock side with the clock frequency at the master clock side, if the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous.

**18**. The precise-clock synchronization system according to claim **16**, the precise-clock time synchronization device comprises:

an absolute time stamp engine, adapted to provide an absolute arrival time stamp about the time when the slave clock side receives the Sync packet and the Delay_Req time stamp about the time when the slave clock side transmits a Delay_Req;

a second obtaining module, adapted to obtain an original time stamp and an absolute arrival time stamp of the Sync packet transmitted by the master clock side, a Delay_Resp time stamp transmitted by the master clock side, and a Delay_Req time stamp transmitted by the slave clock side;

a second calculating module, adapted to calculate a time offset according to the obtained original time stamp, the absolute arrival time stamp, the Delay_Req time stamp, and the Delay_Resp time stamp;

a time adjusting module, adapted to synchronize the clock time at the slave clock side with the clock time at the master clock side by using the time offset.

**19**. A computer readable media, comprising logic encoded in the computer readable media, the logic when executed by a processor, instructing the processor to:

obtain a time stamp, wherein the time stamp comprises at least an original time stamp about a time when a master clock side transmits each Sync packet and a relative arrival time stamp about a time when a slave clock side receives each Sync packet;

judge whether a clock frequency at the slave clock side is synchronous with a clock frequency at the master clock side or not according to the original time stamp and its corresponding relative arrival time stamp; and

synchronizing the clock frequency at the slave clock side with the clock frequency at the master clock side, if the clock frequency at the slave clock side and the clock frequency at the master clock side are asynchronous.

* * * * *