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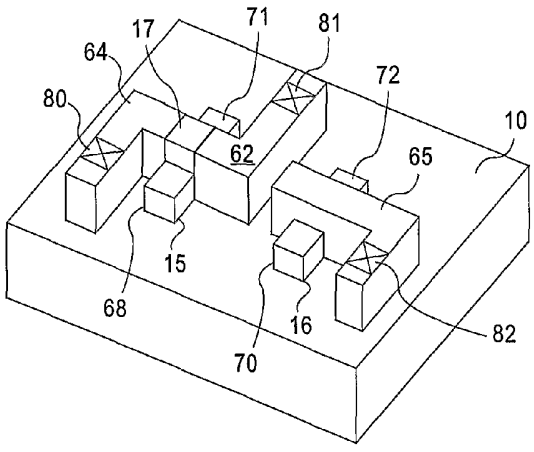
(54) **Title:** INDEPENDENTLY ACCESSED DOUBLE-GATE AND TRI-GATE TRANSISTORS IN SAME PROCESS FLOW



(57) **Abstract:** An independent access, double-gate transistor and tri-gate transistor fabricated in the same process flow is described. An insulative plug is removed from above the semiconductor body of the I-gate device, but not the tri-gate device. This allows, for instance, metalization to form on three sides of the tri-gate device, and allowing independent gates for the I-gate device.

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INDEPENDENTLY ACCESSED DOUBLE-GATE AND TRI-GATE TRANSISTORS IN SAME PROCESS FLOW

FIELD OF THE INVENTION

[0001] The invention relates to the field of semiconductor processing.

PRIOR ART AND RELATED ART

[0002] One relatively recent development in semiconductor processing is the independently-controlled double-gate (I-gate) transistor. This transistor has two gates disposed on opposite sides of a channel, each gate being independently controlled. Independent gate control provides some unique transistor characteristics and enables, for example, a single body, dynamic random-access memory (DRAM) cell.

[0003] Another relatively recent development in semiconductor processing is the tri-gate transistor. Here, a gate is formed on three sides of a channel region. This transistor, particularly when used with a high-k insulator and metal gate, provides substantial performance improvements.

[0004] Several I-gate structures have been proposed. This and other related technology is described at *C. Kuo, IEDM, Dec. 2002, following M. Chan Electron Device Letters, Jan 1994; C. Kuo, IEDM, Dec. 2002, "A Hypothetical Construction of the Double Gate Floating Body Cell;" T. Ohsawa, et al., IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002; David M. Fried, et al., "High-Performance P-Type Independent-Gate FinFETs," IEEE Electron Device Letters, Vol. 25, No.4, April 2004; and David M. Fried, et al., "Improved Independent Gate N-Type FinFET Fabrication and Characterization," IEEE Electron Device Letters, Vol. 24, No. 9, September 2003.*

[0005] Tri-gate structures are described at, for instance, publication number U.S. 2004-0036127-A1.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1A is a perspective view of a substrate which includes two silicon bodies with overlying insulative members

[0007] Figure 1B is a cross-sectional, elevation view of the structure of Figure 1 taken through section line 1B-1B of Figure 1A.

[0008] Figure 2A illustrates the structure of Figure 1 following the patterning of a sacrificial layer.

[0009] Figure 2B is a cross-sectional, elevation view of the structure of Figure 2A taken through section line 2B-2B of Figure 2A.

[0010] Figure 3 is a perspective view of the structure of Figure 2A following the deposition of an interlayer dielectric (ILD).

[0011] Figure 4A is a perspective view of the structure of Figure 3 following planarization.

[0012] Figure 4B is a cross-sectional, elevation view taken through section line 4B-4B of Figure 4A.

[0013] Figure 5 is a perspective view of the structure of Figure 4 following the covering of a section of the substrate on which an I-gate transistor is fabricated.

[0014] Figure 6A is a perspective view of the structure of Figure 5 following an etching step.

[0015] Figure 6B is a cross-sectional view of the structure of Figure 6A taken through section line 6B-6B of Figure 6A.

[0016] Figure 7A is a perspective view of the structure of Figure 6A following removal of the patterned, sacrificial layer.

[0017] Figure 7B is a cross-sectional, elevation view of the structure of Figure 7A taken through section line 7B-7B of Figure 7A.

[0018] Figure 8 is a cross-sectional, elevation view of the structure of Figure 7A and 7B following the formation of an insulative layer and a metal layer.

[0019] Figure 9A is a perspective view of the structure of Figure 8 following planarization of the metal layer.

[0020] Figure 9B is a perspective view of the structure of Figure 9A with the ILD removed.

DETAILED DESCRIPTION

[0021] In the following description, the fabricating of an independently accessed, double-gate (I-gate) transistor and a tri-gate transistor on a common substrate is described. Numerous specific details are set forth, such as specific materials, in order to provide a thorough understanding of the present invention. It will be apparent to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well known processing steps have not been described in detail, in order not to unnecessarily obscure the present invention. For example, well-known cleaning steps, and some protective layers often used in the fabrication of integrated circuits, are not described.

[0022] The method which follows describes the formation of both the I-gate transistor and a tri-gate transistor in a single process flow. While the fabrication of only a single I-gate transistor and a single tri-gate transistor are illustrated, it will be apparent to one skilled in the art, that in a typical integrated circuit, numerous such transistors are simultaneously fabricated. Moreover, the I-gate and tri-gate transistors may be fabricated wherever needed in the integrated circuit. Thus, a single circuit, such as a buffer, may have both I-gate and tri-gate transistors. In some cases, for example in a DRAM, an array of memory cells using only I-gate transistors may be fabricated and connected to peripheral circuits which use both I-gate and tri-gate transistors. A memory using I-gate

memory cells is described in "Memory with Split-Gate Devices and Method of Fabrication," Serial No. 10/816,282, filed March 31, 2004, and assigned to the assignee of the present application.

[0023] In one embodiment, the transistors are fabricated on an oxide layer 10 which is formed on a silicon substrate 12. The transistor bodies are fabricated from a monocrystalline silicon layer 14 (shown in dotted lines in Figures 1A and 1B) disposed on layer 10. This silicon-on-insulator (SOI) substrate is well-known in the semiconductor industry, where as shown, the layer 14 is disposed on the layer 10. By way of example, the SOI substrate is fabricated by bonding the oxide layer 10 and a silicon layer 14 onto the substrate 12, and then, planarizing the layer 14 so that it is relatively thin. This relatively thin, low body effect layer, is used to form the bodies of active devices, as mentioned. Other techniques are known for forming an SOI substrate including, for instance, the implantation of oxygen into a silicon substrate to form a buried oxide layer. In the subsequent cross-sectional views, the transistors are shown fabricated on the oxide layer 10, the underlying silicon substrate 12 is not shown.

[0024] The layer 14 may be selectively ion-implanted with an n-type dopant in the regions where n channel devices are to be fabricated, and with a p type dopant in those regions where p channel devices are to be fabricated. This is used to provide the relatively light doping typically found in the channel regions of MOS devices fabricated in a CMOS integrated circuit. Both the I-gate and tri-gate transistors may be fabricated with the described process as either p channel or n channel devices. (The doping of the channel regions of the transistors may be done at other points in the process flow such as the point in the process shown in Figures 1A or 7A.)

[0025] In the processing for one embodiment, a protective oxide (not shown) is disposed on the silicon layer 14 followed by the deposition of a silicon nitride layer. The

nitride layer is masked to define a plurality of insulative members, such as members 17 and 18 of Figures 1A and 1B. Then, the underlying silicon layer 14 is etched in alignment with these members resulting in the silicon bodies 15 and 16.

[0026] The width of the silicon bodies 15 and 16 may be the critical dimension in a particular process, for instance, in a 30 nanometer (nm) gate length process, these bodies may have a width of 30 nm. The thickness of the layer 14, and the silicon nitride layer from which the members 17 and 18 are formed, may each be, by way of example, in the range of 10-50 nm.

[0027] Now, a sacrificial layer is deposited over the structure of Figure 1A on the oxide layer 10. In one embodiment, this layer is a polysilicon layer 50-100 nm thick. Other materials may be used for the sacrificial layer. The material for the sacrificial layer should be able to protect the channel regions of the devices from ion implantation during the formation of the source and drain regions, as will be described. Moreover, the sacrificial layer should be able to be etched without destroying the integrity of an ILD formed around the sacrificial layer after patterning, as will be described. Additionally, the insulative members must be able to be selectively etched in the presence of the sacrificial layer.

[0028] Next, the sacrificial layer is patterned into gate-defining members shown as members 20 and 22 in Figure 2A. The member 20 occupies the region in which the two gates for the I-gate transistor is fabricated as well as "fins" for these gates to allow contact with the gates as shown later. The member 22 occupies the region in which the tri-gate is formed for the tri-gate transistor, as well as a fin, again for contact.

[0029] At this point in the processing, the silicon nitride members 17 and 18 may be etched in alignment with the member 20 and 22, thereby exposing portions of the underlying silicon bodies 15 and 16. As shown by the arrows 25, the silicon bodies, to the

extent they are not covered by the members 20 and 22, are ion implanted to form source and drain regions for both the I-gate and tri-gate transistors. As is commonly done, but not shown, separate ion implantation steps are used for the p channel and n channel devices, with protective layers being used to permit separate implantation of the source and drains for the p channel and n channel devices.

[0030] Alternatively, the silicon nitride members 17 and 18 may remain in place, and the source and drain regions implanted at an angle, so that the dopant enters the sides of the silicon bodies 15 and 16.

[0031] Additionally, spacers may be formed to allow a more lightly doped source and drain region to be implanted adjacent the channel region, and more heavily doped source and drain regions spaced apart from the channel region. This is described in the above-referenced application serial number 10/816,282.

[0032] An ILD 30 is now formed on the insulative layer 10 as shown in Figure 3. The ILD 30 surrounds the members 20 and 22, and as will be seen, allows the inlay of metal once the polysilicon is removed. The ILD 30 may be, for instance, a chemical vapor deposited (CVD) silicon dioxide layer.

[0033] The structure of Figure 3 is now planarized, for instance, if a chemical mechanical polishing (CMP) process, so as to expose the silicon nitride insulative members 17 and 18. This is illustrated in both Figures 4A and 4B. Note, the members 17 and 18 are flush with the upper surface of the ILD 30, as are the members 20 and 22.

[0034] Now, a photoresist layer is deposited over the structure of Figure 4A and 4B, and patterned so as to remain in place over the I-gate transistor region. The photoresist layer 50 covers the insulative member 17. As shown in Figure 5, the photoresist layer 50 leaves exposed insulative member 18 of the tri-gate device.

[0035] Then, as shown in Figures 6A and 6B, an etching process is used to remove the plug-shaped silicon nitride member 18. An etchant that discriminates between the silicon nitride and both the ILD 30 and sacrificial layer is used so that the ILD 30 and member 22 remains substantially intact. A dry or wet etchant may be used. Once the member 18 is removed, the underlying silicon body 16 as shown in Figure 6B is exposed.

[0036] The polysilicon sacrificial layer is next removed with, for example, a wet etch process. The resultant structure is shown in Figures 7A and 7B. The remaining ILD 30 now defines a form in which the gates for the transistors may be fabricated.

[0037] A gate dielectric layer 60 is formed on and around each semiconductor bodies 15 and 16 as seen in Figure 8. Specifically, a gate dielectric may be deposited such that it covers the top surface of the semiconductor body 16 and the insulative member 17 as well as on the opposite side-walls of each of the semiconductor bodies. This gate dielectric, ideally has a high dielectric constant, such as a metal oxide dielectric, for instance, HfO_2 or ZrO or other high-k dielectrics, such as PZT or BST. A high-k dielectric film can be formed by any well-known technique such as by chemical vapor deposition (CVD). Alternatively, the gate dielectric can be a grown dielectric. In one embodiment, the gate dielectric layer 60 is a silicon dioxide film grown with a dry/wet oxidation process. For example, the silicon dioxide film is grown to a thickness of between 5-50Å. (A conformally deposited dielectric layer is shown in Figure 8.)

[0038] Next, as shown in Figure 8, a gate electrode (metal) layer 61 is formed over the gate dielectric layer 60. The gate electrode layer 61 may be formed by blanket deposition of a suitable gate electrode material. In one embodiment, a gate electrode material comprises a metal film such as Tungsten, Tantalum, Titanium and/or nitrides and alloys thereof. For the n channel, I-gate and tri-gate transistors, a work function in the range of 4.0 to 4.6 eV may be used. For the p channel, I-gate and tri-gate transistors, a

work function of 4.6 to 5.2 eV may be used. Consequently, for substrates with both n channel and p channel transistors, two separate metal deposition processes may need to be used.

[0039] The metal layer 61 is planarized using, for example CMP, and such planarization continues until at least the upper surface of the insulative member 17 is exposed, as shown in Figure 9A. This is done in order to assure that no metal spans the member 17, since otherwise, the gates in the I-gate transistor will be shorted together. As can be seen in Figure 9, there are two independent gates 62 and 64 for the I-gate transistor, and a single gate 65 for the tri-gate device.

[0040] The gate 65 for the tri-gate transistor has a top surface opposite the bottom surface and has a pair of laterally opposite sidewalls formed adjacent the tri-gate structure best seen in Figure 9B. These sidewalls are connected on the upper surface of the silicon body. Thus, the gate surrounds the channel region of the tri-gate transistor on three sides. For the I-gate transistor, two independent gates 62 and 64 are separated by the insulative member 17, again best seen in Figure 9B where the ILD is shown removed.

[0041] Also, best seen in Figure 9B, the silicon bodies 15 and 16 are shown on the insulative layer 10. Source regions 68 and 70 are shown for each of the transistors along with drain regions 71 and 72. The independent gates 62 and 64 along with their orthogonally disposed fins are readily seen. The same is true for the gate 65. These fins allow for easier contact to be made to the gates from overlying metalization layer, as shown by contact regions 80, 81 and 82. While not shown in Figure 9B, contact is made to the source and drain regions as well as to the gates from overlying metalization layers through contacts not shown.

[0042] I-gate transistors may be used in logic circuits along with the tri-gate transistors. I-gate transistors have characteristics which make them desirable in certain

circuits. For instance, a single I-gate transistor may provide both a high current and medium current device depending on the potential applied to one or both gates. Such devices may provide a "strong off" device to reduce leakage in a sleep mode or power-down mode. I-gate transistors also provide a device for pre-charge lines by allowing a trickle current. In the above-mentioned patent application, the I-gate devices are used as DRAM cells, and the process described above, may be used in connection with such DRAM fabrication. In this case, the silicon body 15 is an elongated body formed in a plurality of parallel, spaced-apart lines and used in an array of DRAM cells.

[0043] While in the figures two separate silicon bodies are shown, it will be appreciated that a single body may be used. Then, a tri-gate and I-gate transistor may be fabricated in series with one another. In this case, the series transistors have a source/drain region.

[0044] Thus, a process has been described and a resultant structure for an integrated circuit having both an I-gate and tri-gate structure on a common substrate.

CLAIMS

What is claimed is:

1. A method comprising:

forming at least two silicon bodies having overlying insulative members;

patterning a sacrificial layer defining gate regions, intersecting the silicon bodies;

enclosing the patterned sacrificial layer in a dielectric material;

covering one of the insulative members;

removing the other of the insulative members;

removing the patterned sacrificial layer;

forming an insulative layer and metal layer within the gate regions.

2. The method of claim 1, including planarizing the dielectric material to expose the insulative members.

3. The method defined by claim 2, wherein the silicon bodies comprise a monocrystalline silicon.

4. The method defined by claim 3, wherein the insulative members comprise silicon nitride.

5. The method defined by claim 4, wherein the sacrificial layer comprises polysilicon.

6. The method defined by claim 5, wherein the planarizing comprises chemical-mechanical polishing.

7. The method defined by claim 1, including removing the insulative members to the extent that they are exposed following the patterning of the sacrificial layer.

8. The method defined by claim 1, including forming source and drain regions in the silicon bodies after the patterning of the sacrificial layer.

9. The method defined by claim 8, wherein the doping of the source and drain regions is done in two doping processes, one before formation of sidewall spaces and one after the formation of sidewall spaces.

10. The method defined by claim 1, wherein the removal of the other of the insulative members is done with an etchant that has a higher etch rate for the insulative member than the etch rate for the dielectric material.

11. A method comprising:

defining on an insulative layer, a first and a second silicon body with a first and a second insulative member, respectively;

removing at least a portion of the first insulative member while leaving in place the second insulative member;

forming a first gate structure on opposite sides of the second silicon body, the first gate structure having two independent gates; and

forming a second gate structure on three sides of the second silicon body.

12. The method defined by claim 11, wherein the first and second gate structures are metal, insulated from their respective silicon bodies by high-k insulation.

13. The method defined by claim 12, wherein the gate structures are formed by removal of a sacrificial layer surrounded by an interlayer dielectric.

14. The method defined by claim 13, wherein the sacrificial layer comprises polysilicon and the insulative members comprise silicon nitride.

15. An integrated circuit comprising:

a substrate;

a first transistor on the substrate having a first body surround on three sides by a first metal gate; and

a second transistor on the substrate having a second body having two independent metal gates on opposite sides of the second body.

16. The circuit defined by claim 15, wherein the first and second bodies comprise a monocrystalline silicon.

17. The circuit defined by claim 16, including an insulative member disposed on the second body between the independent gates.

18. The circuit defined by claim 17, wherein the insulative member comprises silicon nitride.

19. The circuit defined by claim 15, including a plurality of the first and second transistors, some of which are n channel transistors and others of which are p channel transistors.

20. The circuit defined by claim 19, wherein the bodies of the transistors comprise monocrystalline silicon.

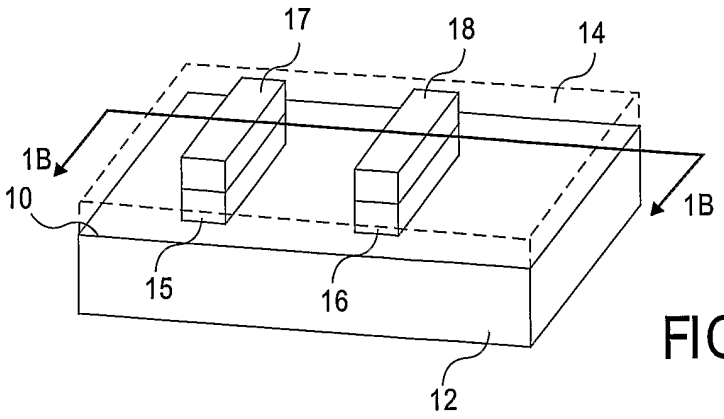

FIG. 1A

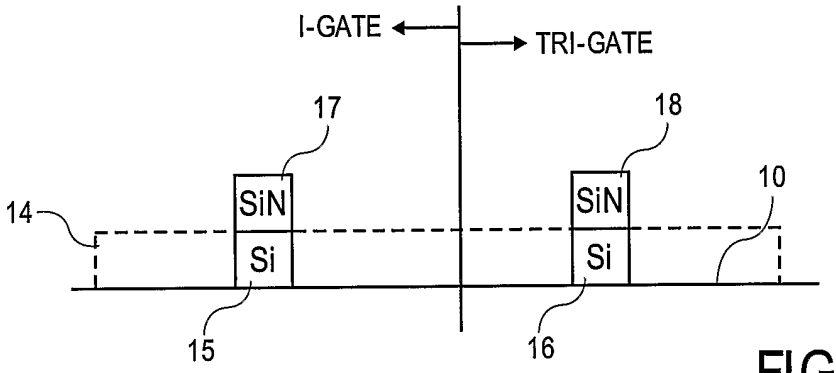

FIG. 1B

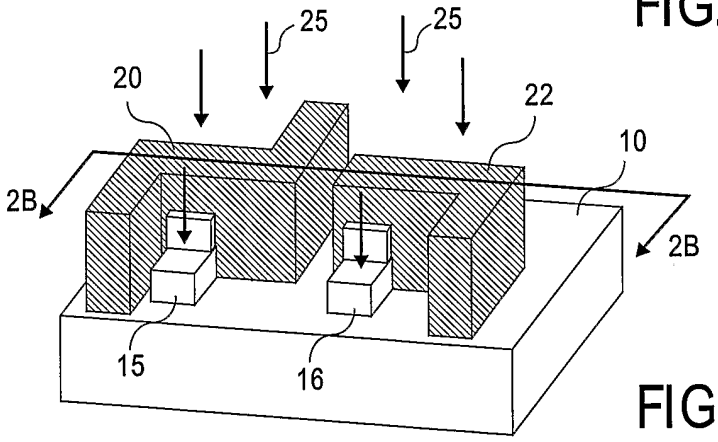

FIG. 2A

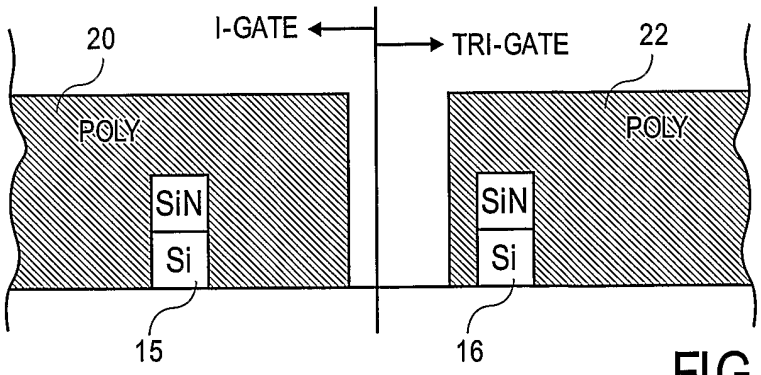

FIG. 2B

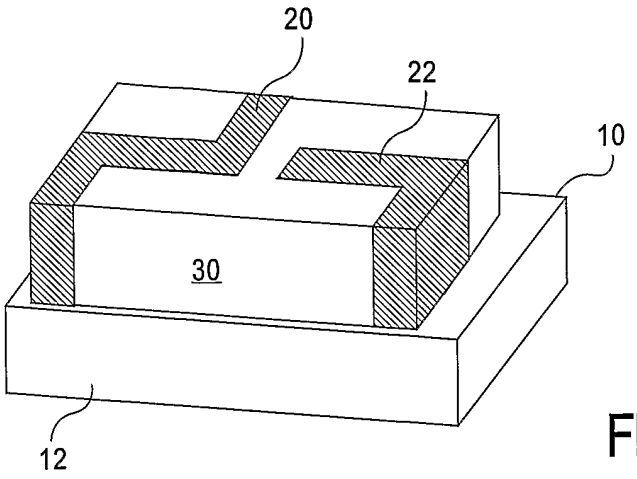

FIG. 3

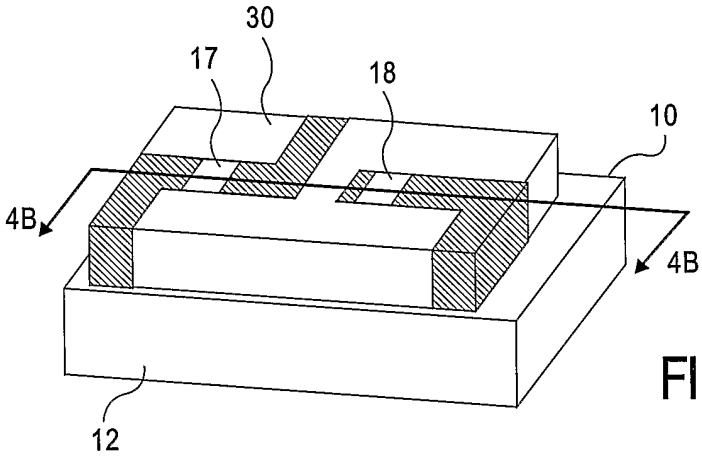

FIG. 4A

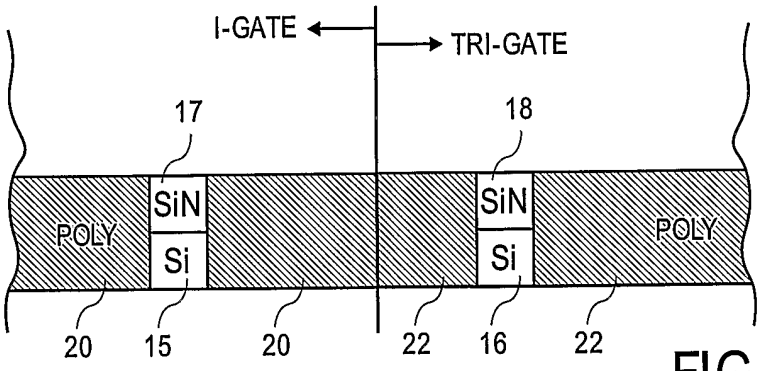

FIG. 4B

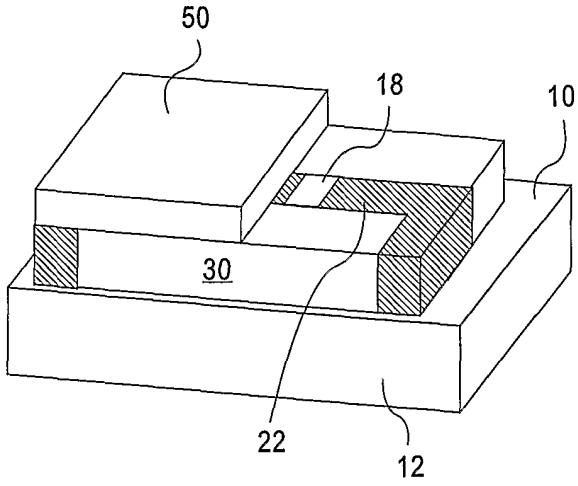

FIG. 5

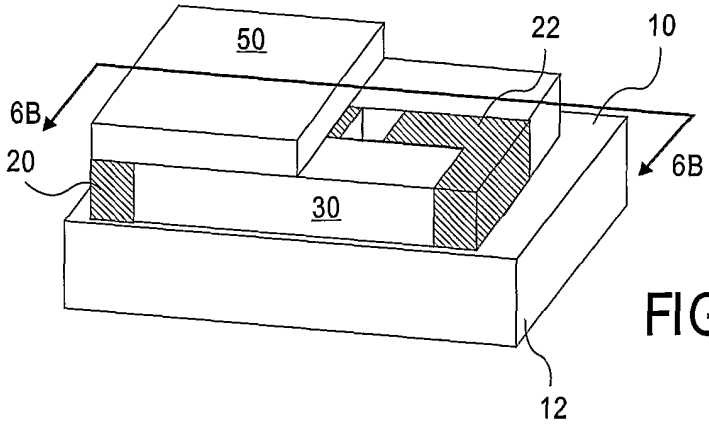

FIG. 6A

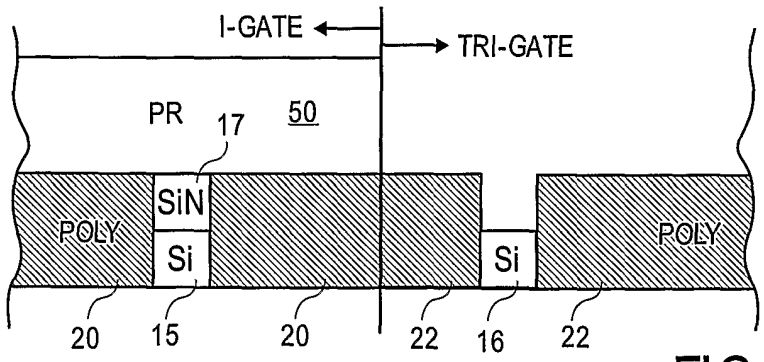

FIG. 6B

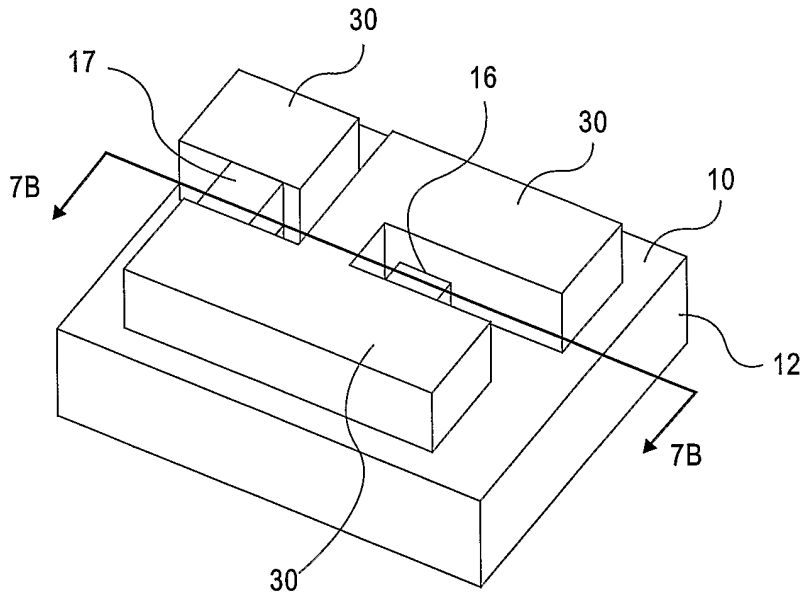

FIG. 7A

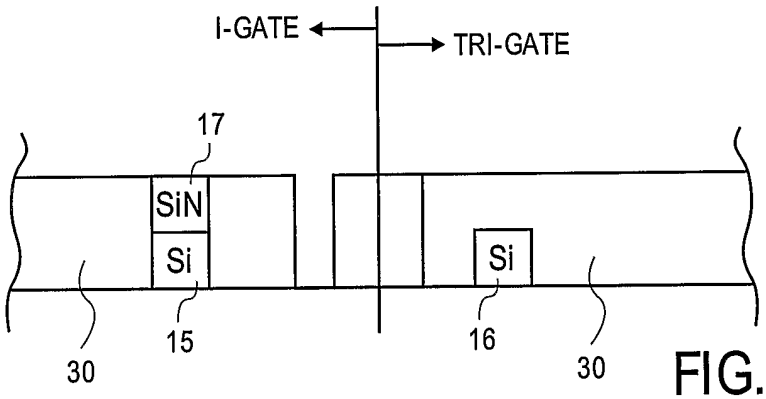

FIG. 7B

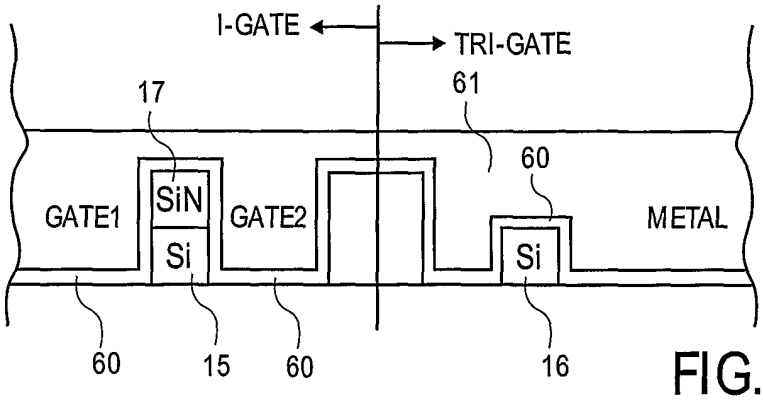

FIG. 8

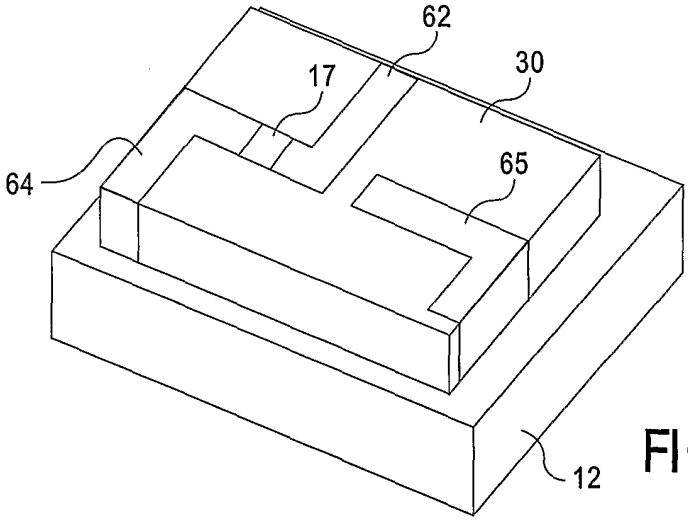

FIG. 9A

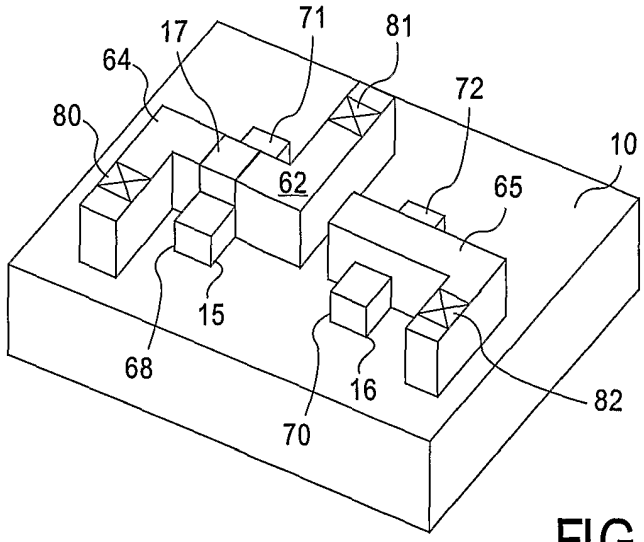

FIG. 9B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/035380

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/84 H01L27/12 H01L21/336 H01L29/786

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/036118 A1 (ABADEER WAGDI W ET AL) 26 February 2004 (2004-02-26) page 7, paragraph 92 - paragraph 97; figures 13-17	11-20
Y		1-10
Y	US 2004/092067 A1 (HANAFI HUSSEIN I ET AL) 13 May 2004 (2004-05-13) claims; figures	1-10
Y	US 2004/110097 A1 (AHMED SHIBLY S ET AL) 10 June 2004 (2004-06-10) the whole document	1-20
Y	US 6 764 884 B1 (YU BIN ET AL) 20 July 2004 (2004-07-20) the whole document	1-20

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[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
3 February 2006	13/02/2006

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INTERNATIONAL SEARCH REPORT

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PCT/US2005/035380

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2004/059726 A (INTERNATIONAL BUSINESS MACHINES CORPORATION; RANKIN, JED, H; ABADEER,) 15 July 2004 (2004-07-15) page 4, line 20 - page 6, line 10; figures 1A-1G	11-20
A	US 2003/122186 A1 (SEKIGAWA TOSHIHIRO ET AL) 3 July 2003 (2003-07-03) page 4, paragraph 69 - page 5, paragraph 71; figures 25-27	1-10
A	US 2004/092062 A1 (AHMED SHIBLY S ET AL) 13 May 2004 (2004-05-13) page 3, paragraph 39	11-20
A	US 2004/126975 A1 (AHMED SHIBLY S ET AL) 1 July 2004 (2004-07-01) page 2, paragraph 34	11-20
A	US 2003/151077 A1 (MATHEW LEO ET AL) 14 August 2003 (2003-08-14) the whole document	11-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2005/035380

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004036118 A1	26-02-2004	JP 2004088101 A	18-03-2004
US 2004092067 A1	13-05-2004	JP 2003017710 A	17-01-2003
		TW 541698 B	11-07-2003
		US 2002177263 A1	28-11-2002
US 2004110097 A1	10-06-2004	AU 2003286831 A1	30-06-2004
		WO 2004053963 A1	24-06-2004
		US 6686231 B1	03-02-2004
US 6764884 B1	20-07-2004	WO 2004093181 A1	28-10-2004
WO 2004059726 A	15-07-2004	AU 2002368525 A1	22-07-2004
		EP 1581968 A1	05-10-2005
US 2003122186 A1	03-07-2003	NONE	
US 2004092062 A1	13-05-2004	AU 2003282842 A1	03-06-2004
		EP 1559137 A1	03-08-2005
		WO 2004044973 A1	27-05-2004
US 2004126975 A1	01-07-2004	AU 2003291641 A1	03-06-2004
		DE 10393687 T5	06-10-2005
		GB 2408849 A	08-06-2005
		WO 2004044992 A1	27-05-2004
		US 6611029 B1	26-08-2003
US 2003151077 A1	14-08-2003	AU 2003217294 A1	04-09-2003
		EP 1476901 A1	17-11-2004
		JP 2005518094 T	16-06-2005
		WO 03069664 A1	21-08-2003