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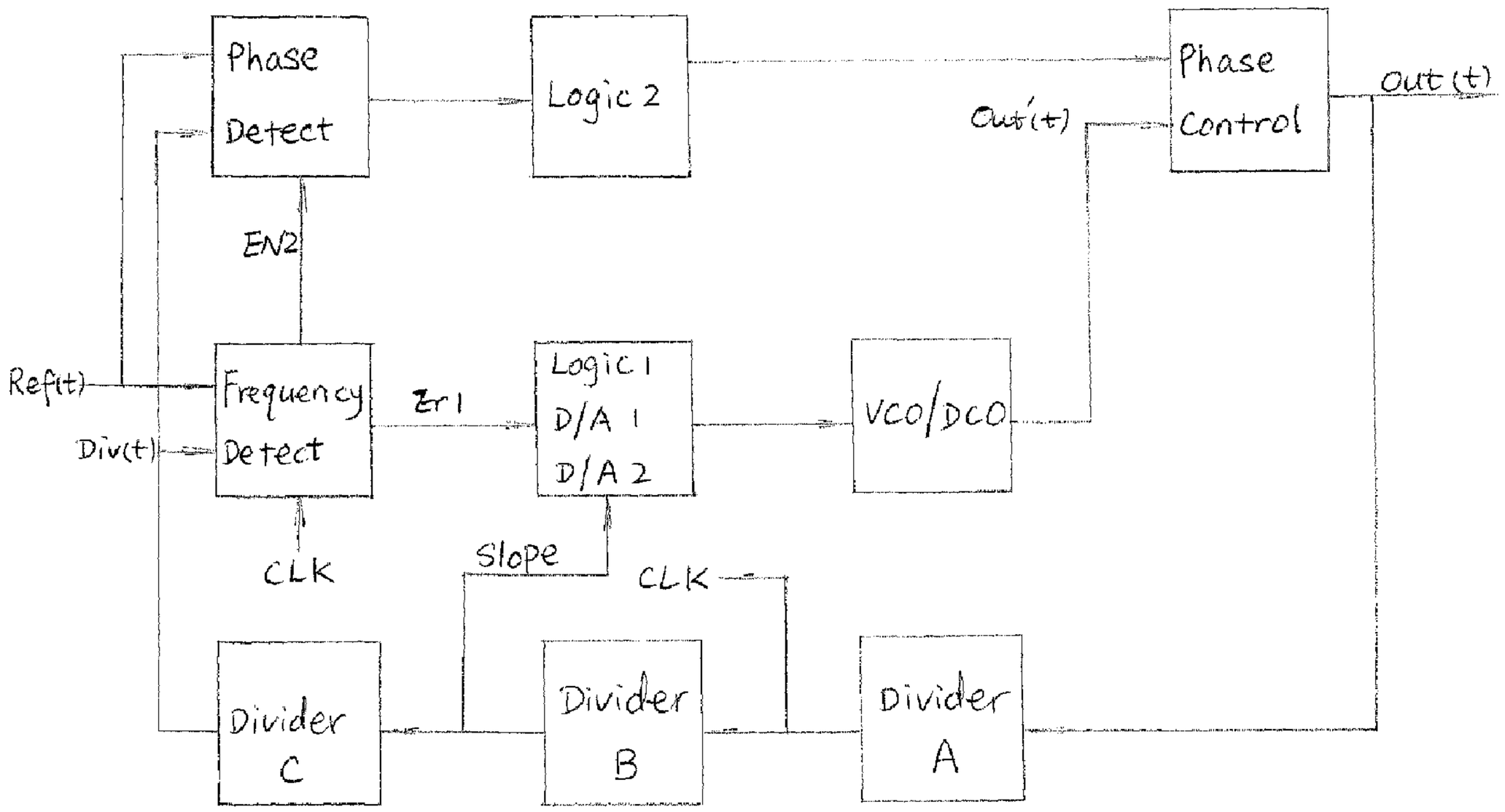
(54) **Titre : FREQUENCE ET BOUCLES A VERROUILLAGE DE PHASE**
(54) **Title: FREQUENCY AND PHASE LOCKED LOOPS**



(57) **Abrégé/Abstract:**
Frequency and Phase locked Loops for controlling the frequency and phase of an output signal in response to an input Ref(t) signal, comprising a frequency control loop for controlling the frequency of an output signal in response to an input signal Ref(t) frequency according to frequency error between its output signal and input signal, a phase control loop for controlling the phase of an output signal to match with an input signal phase according to the first static phase error between its output signal and input signal Ref(t) and to the phase error between the first static phase error and the subsequent static phase error, means for using the first static phase error of Er2 value as a reference phase error to compare with subsequent Er2 to add or subtract phase delay to output signalgenerated by the frequency control loop and output a frequency and phase locked output signal out(t).

Title: Frequency and Phase Locked Loops

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Frequency and Phase locked Loops for controlling the frequency and phase of an output signal in response to an input Ref(t) signal, comprising a frequency control loop for controlling the frequency of an output signal in response to an input signal Ref(t) frequency according to frequency error between its output signal and input signal, a phase control loop for controlling the phase of an output signal to match with an input signal phase according to the first static phase error between its output signal and input signal Ref(t) and to the phase error between the first static phase error and the subsequent static phase error, means for using the first static phase error of Er2 value as a reference phase error to compare with subsequent Er2 to add or subtract phase delay to output signalgenerated by the frequency control loop and output a frequency and phase locked output signal out(t).

Frequency and Phase Locked Loops

1.Field of the Invention

The present invention relates to Phase Locked Loops(PLL) including PLL using VCO(Voltage Controlled Oscillator) and DCO(Digital Controlled Oscillator).

2.Description of prior art

Analog PLL are generally built of a phase detector, low pass filter, voltage controlled oscillator(VCO) and frequency divider in a negative feedback configeration.

Digital PLL are generally built of a time to digital converter, Digital loop filter, digital controlled oscillator(DCO) and frequency divider in a negative feedback configeration.

VCO or DCO efficiently provides oscillation waveform with variable frequency. PLL synchronizes VCO / DCO frequency to input reference frequency through feedback.

VCO output frequency Fvco = Kvco * Vctl, Kvco is constant gain over most of usable control voltage range, Vctl is VCO control voltage.

An important part of a phase locked loop is the phase detector or time to digital converter. This compares the phase of two inputs to the detector and outputs a corrective signal to control the oscillator such that the phase between the two inputs becomes zero. The two inputs of the phase detector are usually the reference and the divided output of VCO or DCO. The purpose of PLL is to generate a frequency and phase locked output oscillation signal.

But actually, prior art can not do it as expected. Because first, said VCO and DCO are frequency variable and contrllable but not phase variable and controllable. Second, using said phase error (static phase error) to correct frequency is not directly relevant or proper. It is a conflicting control and leads to PLL output in infinite Jitter(diviation of VCO / DCO output edges from ideal placement in time) mode, neither frequency nor phase will be actually locked and PLL performance is hard to improve.

3.Summary of the invention

The present invention provides a new, different approach. First, to replace prior single loop PLL with a frequency locked loop and a phase locked loop, so that the frequency loop is controlled by frequency error and the phase locked loop is controlled by dynamic phase error(dynamic phase error is the difference between the first static phase error and each consecutive static phase error) instead of static phase error. The control target

of the frequency locked loop is a variable frequency unit like VCO and DCO. The control target of the phase locked loop is a variable phase delay unit. Second, to provide an simple, high resolution frequency error detector and an improved proportional and integral feedback control for the said frequency locked loop. Third, to provide a dynamic phase error detection and correction for the said phase locked loop.

With the present invention, several advantages are obtained,first , frequency and phase can be separately controlled and truly locked(theoretically, error to zero), resulting in significant reduction of Jitter. Second, fast output response with limited or no overshoot / undershoot. Third, simple in design and easy for manufacturing.

4.Brief description of the drawings

FIG1 provides an embodiment of block diagram for the frequency phase locked loops according to the present invention.

FIG2 provides an embodiment of block diagram for the frequency locked loop according to the present invention.

FIG3 provides an embodment of block diagram for the phase locked loop according to the present invention.

FIG4 shows signal waveform relation according to the present invention.

FIG5 is a block diagram of prior art analog / digital PLL

FIG6 is a graph of VCO gain.

FIG7 is a graph of output Jitter of prior art analog / digital PLL.

5.Description of preferred embodiment

In FIG1, a frequency locked loop is built of Frequency Detect, Logic1, D/A1, D/A2, VCO / DCO, Phase Control, Divider A, Divider B, Divider C. A phase locked loop is built of Phase Detect, Logic 2, Phase Control, Divider A, Divider B, and Divider C. A frequency phase locked loop is built of connecting above frequency and phase loops with Phase Control to output a frequency and phase locked signal out(t).

In the frequency locked loop, out(t) is first divided by Divider A to generate a signal CLK. CLK is provided to Divider B for futher division and to frequency Detect as high speed Ref(t) / Div(t) sampling clock. The output of Divider B generates a signal

Slope. Slope is provided to the Logic, D/A1, D/A2 as a clock of a counter used for frequency coarse tune and to Divider C for further division. Because the frequency of signal Slope will determine the rising speed of the counter's outputs which are converted to a frequency control voltage by D/A1 for frequency proportional control/coarse control, it is named Slope. Change Divider B can change the slope of proportional frequency control . Divider C generates signal Div(t). Div(t) is provided to Frequency Detect where its frequency is compared with and subtracted by reference signal Ref(t). Frequency Detect generates a frequency error signal Er1 and an enable signal EN2. Er1 is the frequency difference error between Ref(t) and Div(t) and is provided to Logic, D/A1, D/A2 for setting the D/A1 s output at the end of proportional / coarse control and for D/A2 s integral / fine tune control so that Er1 will equal or approximate to zero and frequency can be locked. EN2 is an enable signal which will become '1' when frequency is locked and is provided to phase Detect to enable phase error detect. The output of Logic1 , D/A1, D/A2 is a voltage control signal which is provided to VCO / DCO. The output of VCO / DCO, out'(t) is a frequency locked signal which is provided to phase control. The output of Phase Detect is provided to Logic2. Logic2 generates a phase control signal which decides whether to increase or decrease phase delay and is provided to phase control. Phase control will add or subtract delay to the VCO / DCO output signal out'(t) accordingly and output a frequency and phase locked signal out(t).

In FIG.2, TDC1 and TDC2 comprise two identical counters which will be reset at Ref(t) and Div(t) rising edges respectively, then start to count CLK and stop at Ref(t) and Div(t) falling edges respectively. Referring to FIG4, at the end, TDC1 s output is the CLK pulse number counted during D1. TDC2 s output count number is the CLK pulse number counted during D2. In this way, high resolution time to digital conversion is achieved. Digitalized D1 and D2 are provided to SUB1. SUB1 substracts D1 with D2 and output an absolute value of the difference, ER1 as a frequency error and generates an EN2 high when Er1 first time becomes zero. Er1 is provided to Digital Add and Logic. In Logic, Er1's first rising edge generates a start signal to initiate coarse tune / proportional frequency control and to start counter. Meanwhile sets D/A2 initial output value to half of its maxim value. When Er1 first time becomes zero, Logic will generate a stop signal to end coarse tune and to stop counter, meanwhile generate an EN1 high to COMP1 to initiate fine tune / integral frequency control. The counter will hold its output value for D/A1 to generate an output voltage V1 as the result of coarse tune. V1 is provided to Analog Add. When En1 becomes high, COMP1 compares D1 with D2. If D1 is greater than D2, COMP1 will generate an up signal. If D1 is smaller

than D2, COMP1 will generate a down signal. If D1 is equal to D2 , COMP1 will let both up and down signals be low. The up and down signals are provided to Digital Add. In Digital Add, the previous output value D is read back from D/A2 and then is added or substracted by current Er1 value according to the up or down signal respectively. The result will be used to update D and to generate next V2(t). This process will continue until Er1 becomes zero. The output of D/A2, V2(t) is provided to analog add. Analog Add adds V2(t) with V1(t) to generate a proportional and integral frequency control voltage V1(t) for VCO. VCO generates a frequency locked signal out'(t) when Er1 becomes zero. Because TDC1 and TDC2 are identical and have the same CLK, time to digital conversion error caused by CLK can be mostly cancelled by SUB1, no additional ring oscillator is needed to generate a clock. This significantly simplifies design while providing high resolution, small error time to digital conversion even during loop transaction time.

In FIG3, referring to FIG4, when EN2 becomes high, AND2 is first selected as inital delay selection. SUB2 will convert time difference between Reset1 /t1 and Reset2 / t2 into a digital static phase error Er2. The first static phase error / first Er2 value will be kept in SUB2 ' s register as Er0 as reference for future comparison. Er2 is provided to COMP2. The next Er2 value will be compared with Er0. If Er2 is less than Er0, COMP2 will generate an up signal high, if Er2 is greater than ER0, COMP2 will generate a down signal high and if Er2 is equal to Er0, both up and down signals will be low. Up and down signals are provided to SHIFT Reg. If up event and up is high, AND3 will be selected to add delay to out'(t). If down event and down is high, AND1 will be selected to reduce delay to out'(t). If both up and down are low, no change will happen. Only one of the three AND gates will be selected at a time. In this way, relative phase difference between Ref(t) and Div(t) is kept close to Er0 or locked. Therefor, out(t) is locked in frequency with Ref(t) and in phase with itself. Increasing the number of the delay components can increase the accuracy of the phase locked loop.

6.Claims

I claim:

1. Frequency and Phase locked Loops for controlling the frequency and phase of an output signal in response to an input Ref(t) signal, comprising

(a) A frequency feedback control loop for controlling the frequency of an output signal in response to an input Ref(t) signal frequency according to frequency error between its output signal and input signal.

(b) A phase feedback control loop for controlling the phase of an output signal in alliance to / to match with an input signal phase according to the first static phase error between its output signal and input signal Ref(t) and to the phase error between the first static phase error and the subsequent static phase error.

2. The apparatus of claim 1, where in said frequency feedback control loop comprises:
A proportional control loop and an integral control loop.

3. The apparatus of claim 2, where in said proportional control loop comprises:
Means for changing the slope and controlling the time length of proportional control establishment.

4. The apparatus of claim 3, where in said means for changing the slope comprises:
Changing slope by changing Divider B's constant divider value.

5. The apparatus of claim 3, where in said meansfor controlling the time lenth of proportional control establishment comprises:
Logic generates an EN1 high to stop counter and to enable integral control when first time, frequency error Er1 becomes zero.

6.The apparatus of claim 2, where in said integral control loop comprises:
Means for frequency error generation and integral control.

7. The apparatus of claim 6, where in said frequency error generation comprises:
Using a high frequency clock CLK from the feedback Divider A to drive two identical counters combining with logic control within TDC1 and TDC2 to achive Time to Digital conversion, to subtract the results of theTime to Digital conversion, to reduce CLK caused error impact and to generate a frequency error signal Er1 and to generate an EN2 high signal to enable phase feadback control when second time, Er1 becomes zero.

8. The apparatus of claim 6, where in said integral control comprises:
Means for adding or subtracting the next frequency error Er1 with previous result D and updating D.

9. The apparatus of claim 1, where in said phase feedback loop comprises:

Means for using the first static phase error of Er2 value as a reference phase error to compare with subsequent Er2 to add or subtract phase delay to output signal out'(t).

The diagrams depicted herein are just examples. There may be many variations to these diagrams or the steps (or operations) described herein without departing from the spirit of the invention. All of these variations are considered a part of the cliamed invention.

While the preferred embodiment to the invention has been described, it will be understood that those skilled in the art, both now and in the future, may take various improvements and enhancements which fall within the scope of the claims which follow. These claims should be construed to maintain the proper protection for the invention first described.

7. Reference:

Practical Phase-Locked Loop Design, 2004 ISSCC Tutorial, Dennis Fischette, http://www.delroy.com/pll

First time, Every Time-Practical Tips for Phase-Locked Loop Design, Dennis Fischette, 2009

Practical Phase-Locked Loop Design, Dennis Fischette, 2004

Tutorial on Digital Phase-Locked Loops, CICC 2009, Michael H. Perrott, September 2009

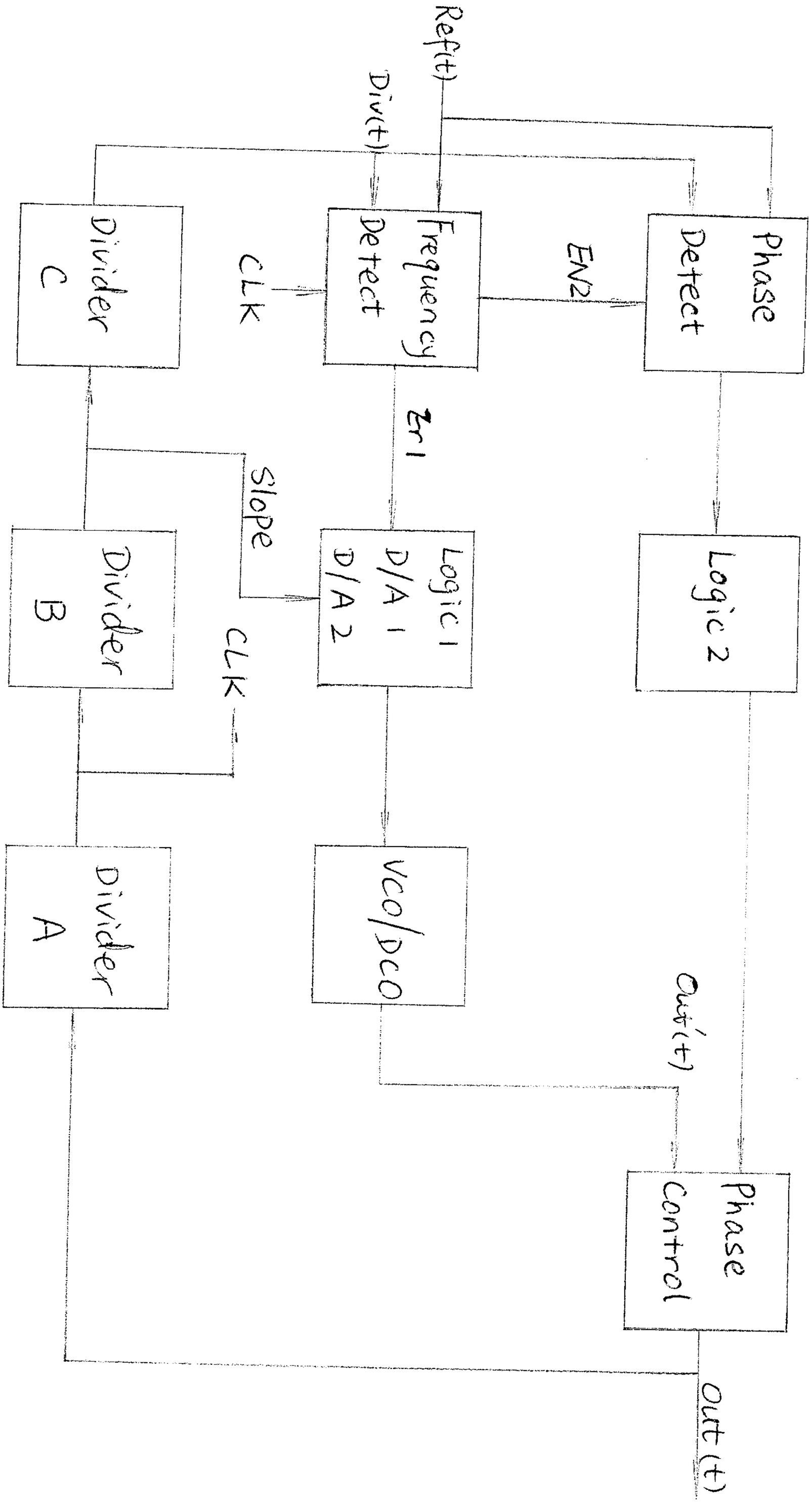

Ref(t)
Div(t)
Divider C
Frequency Detect
Phase Detect
CLK
EN2
Logic 1 D/A 1 D/A 2
Logic 2
Slope
Divider B
CLK
Divider A
VCO/DCO
Out(t)
Phase Control
Out (t)

FIG 1

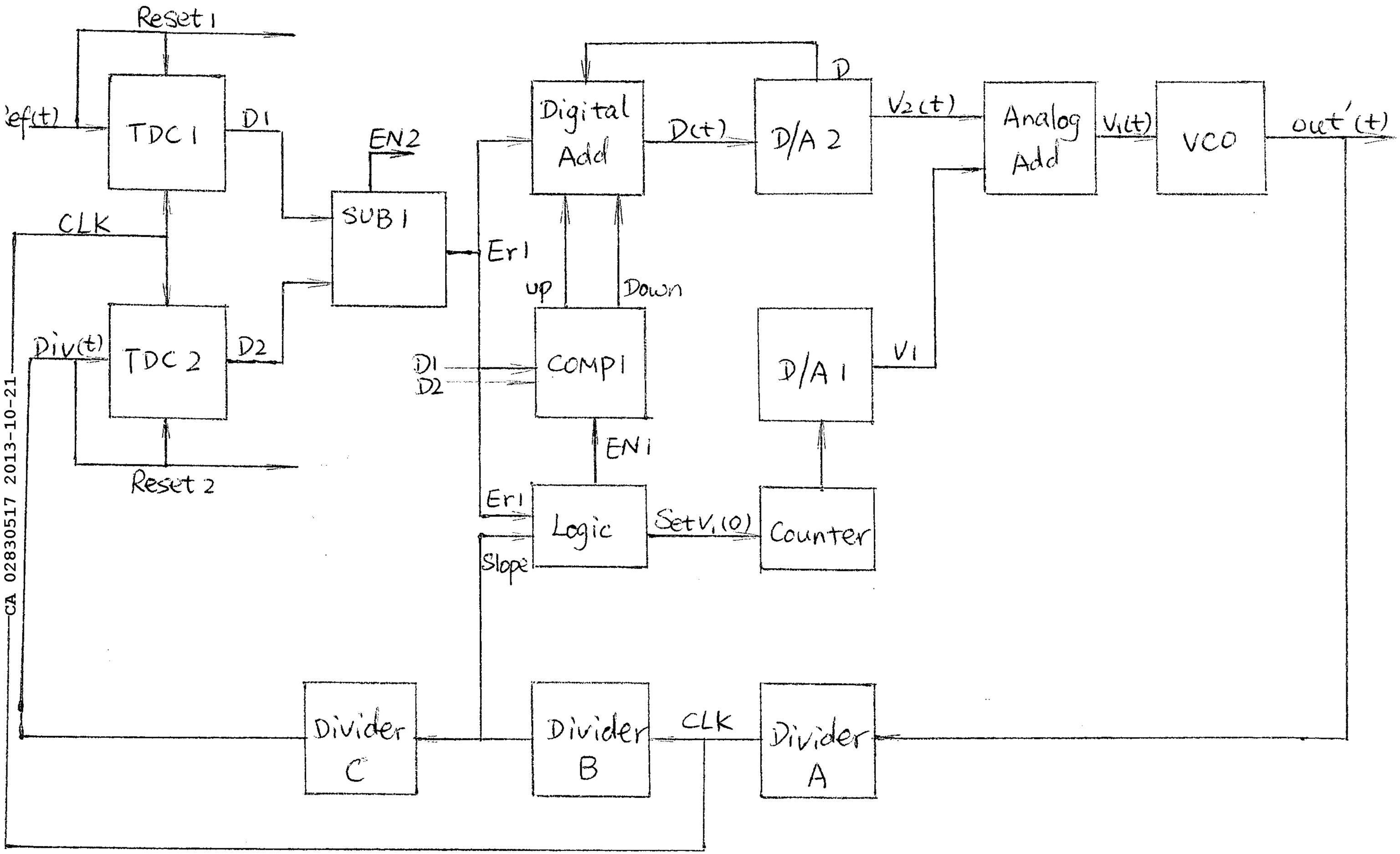


FIG 2

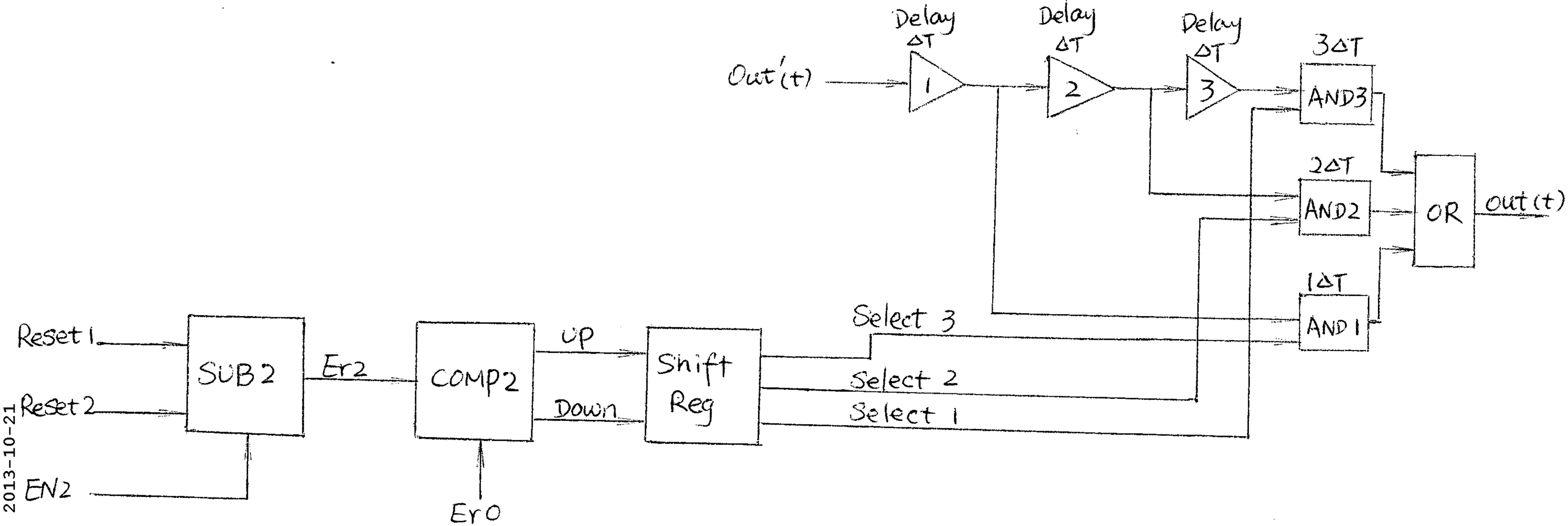


FIG 3

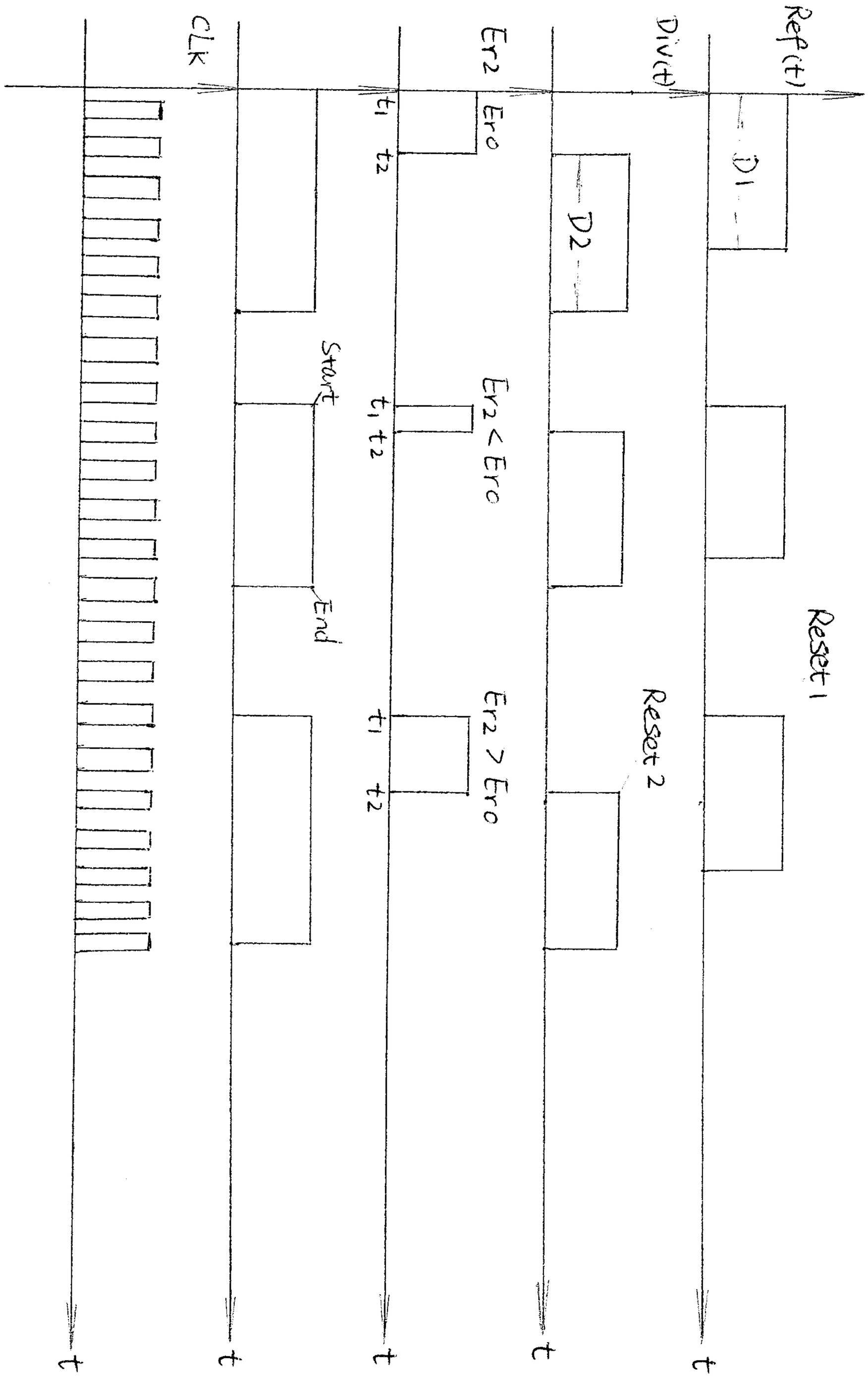
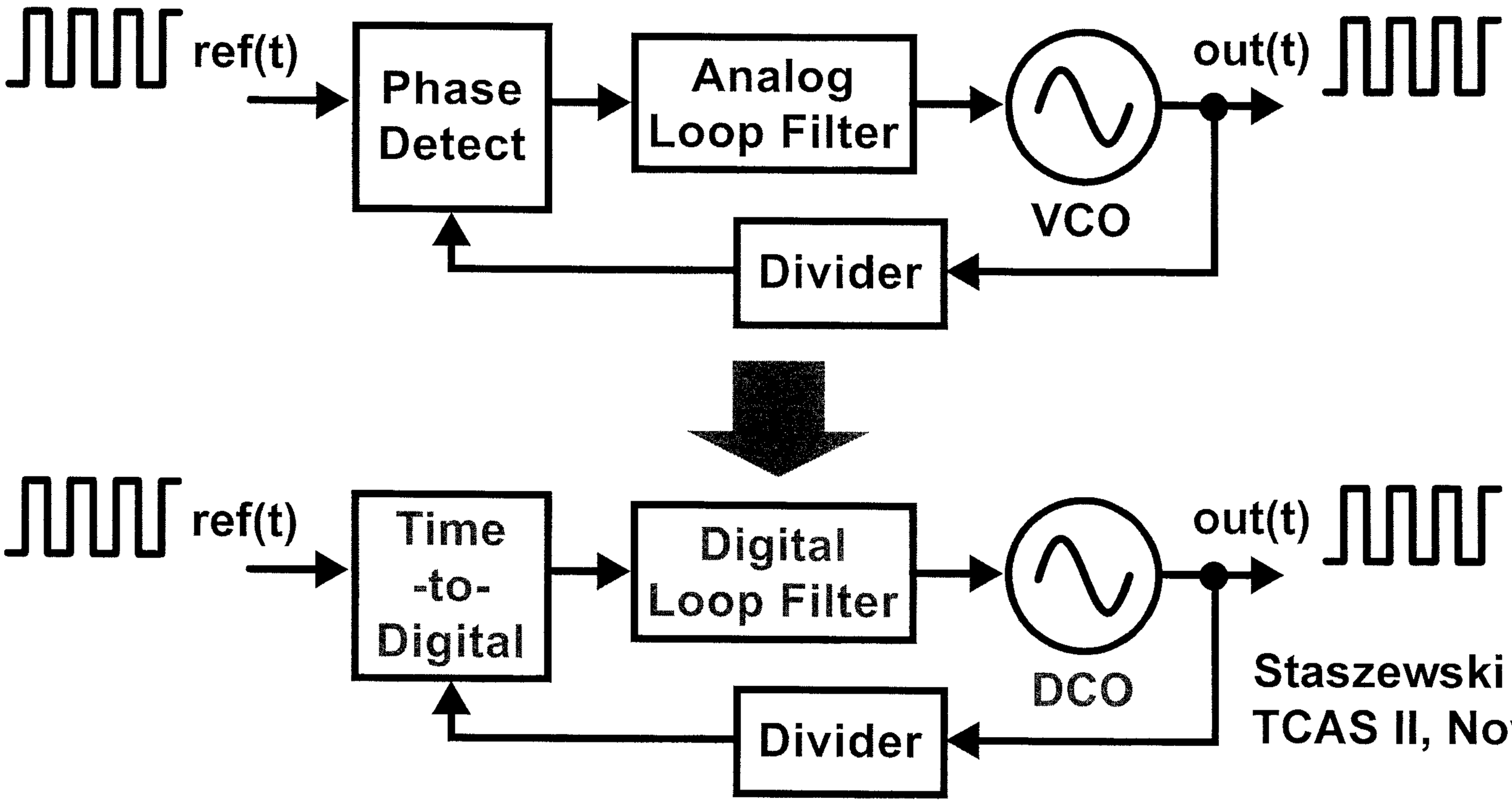

CLK
Er2
Ero
Div(t)
Ref(t)
t1
t2
D1
D2
Start
End
Reset 1
Reset 2
Er2 < Ero
Er2 > Ero
t1 t2
t1
t2
t
t
t
t
t

FIG 4

Going Digital …



- Digital loop filter: compact area, insensitive to leakage
- Challenges:
  - Time-to-Digital Converter (TDC)
  - Digitally-Controlled Oscillator (DCO)

FIG 5

RO VCO Gain

- Typical VCO gain: K_{vco} ~ 1-3× * f_{max}. May vary w/PVT by > 2×
  - need frequency range: >2× to allow for PVT
  - desire constant gain over most of usable control voltage range
  - use digital calibration to reduce : K_{vco} variation

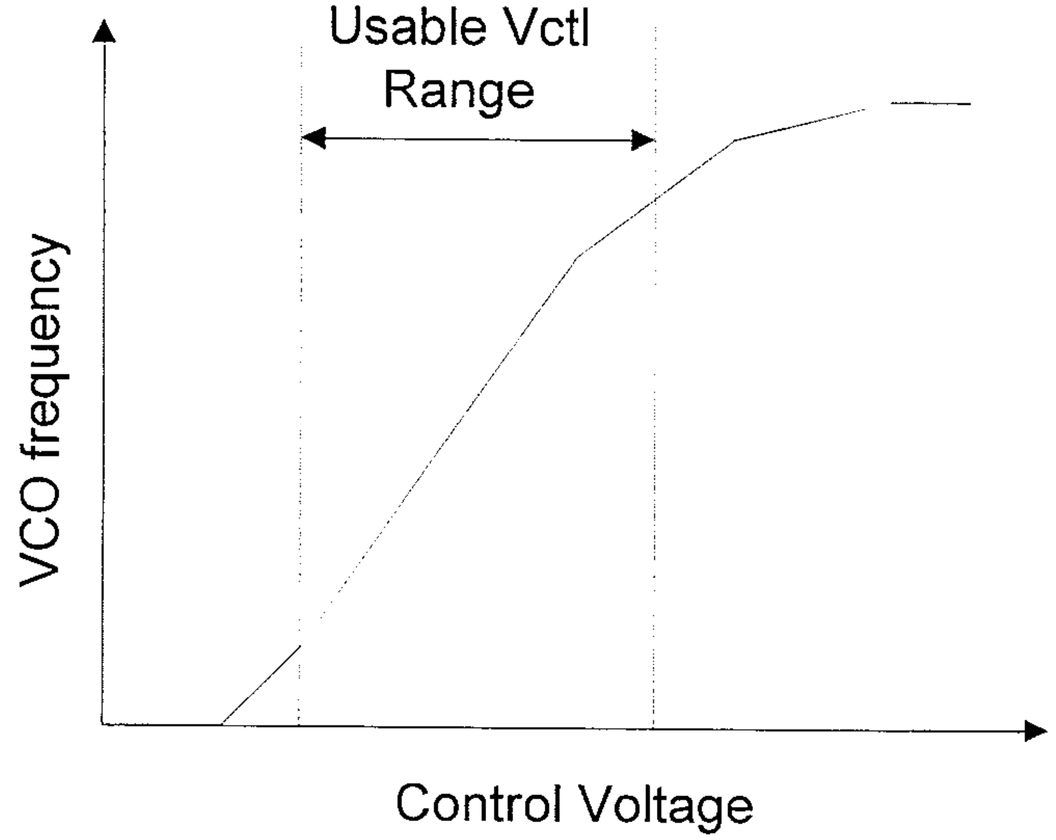


FIG 6

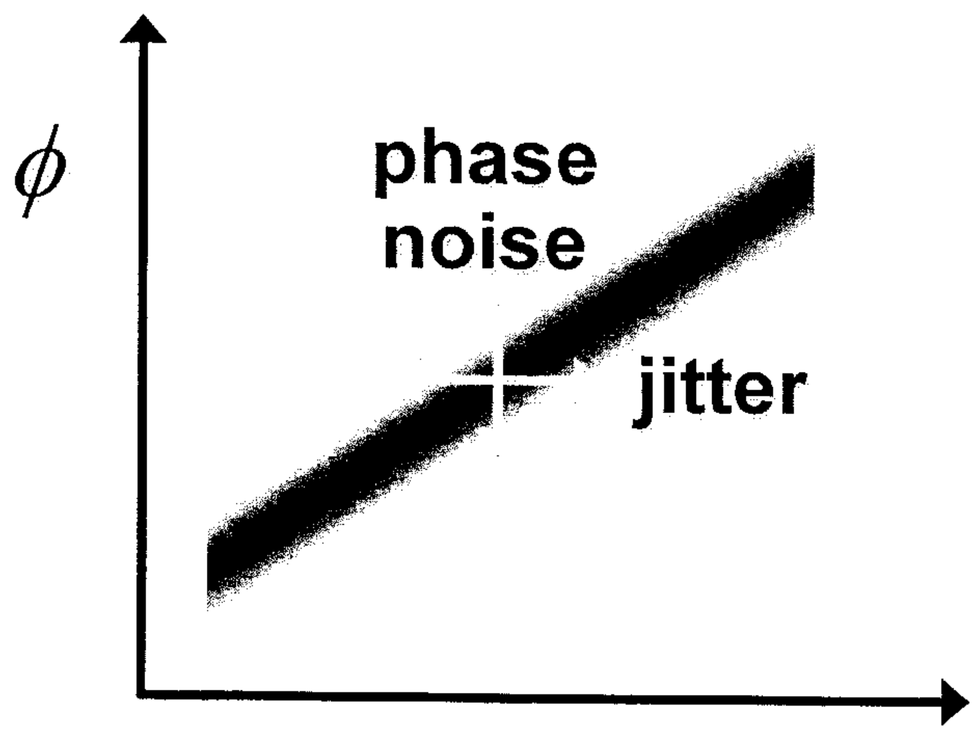
Phase Noise and Timing Jitter

- **Phase Noise (frequency domain) ↔ Jitter (time domain)**
- **Noise is frequency-dependent with random & deterministic components**

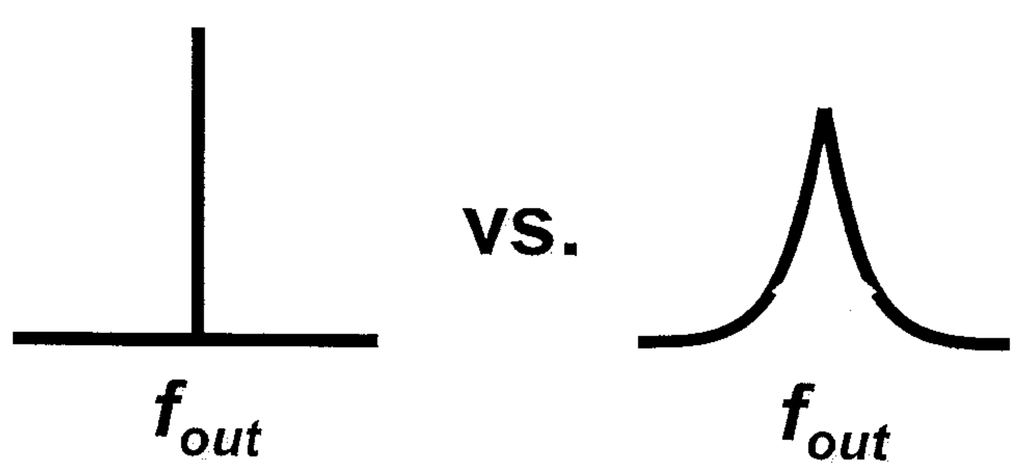
- **VCO and loop filter resistor often largest sources of noise**

PLL Output

$$V_{out}(t) \propto \sin\left(2\pi f_{out} t + \phi_n(t)\right)$$

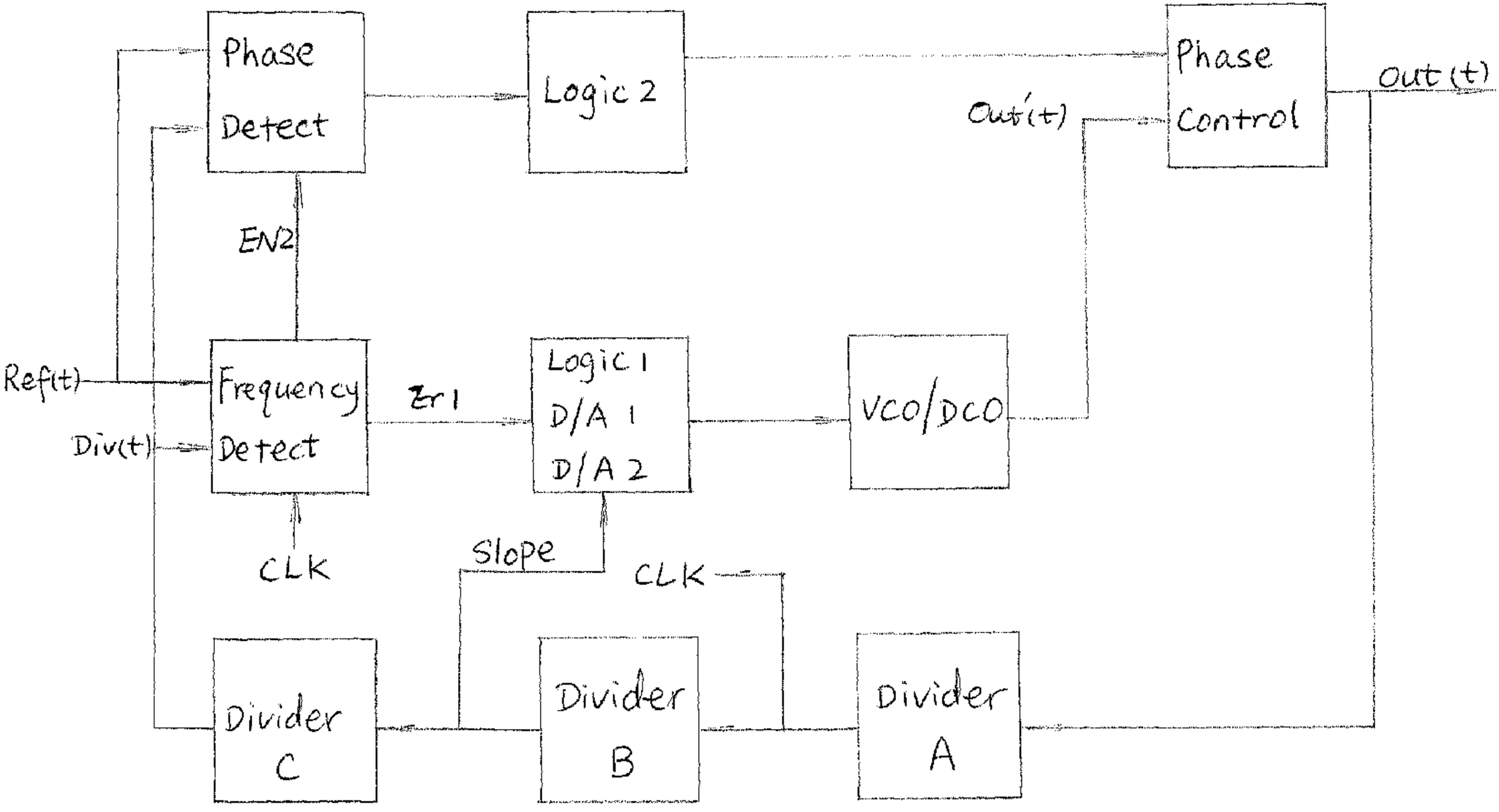


Frequency Domain



Time Domain

FIG 7


Phase
Detect
Logic 2
Phase
Control
Out(t)
Out(t)
EN2
Ref(t)
Frequency
Detect
Div(t)
Err
Logic 1
D/A 1
D/A 2
VCO/DCO
CLK
Slope
CLK
Divider
C
Divider
B
Divider
A