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(54) Title: SEMICONDUCTOR STRUCTURE AND METHOD

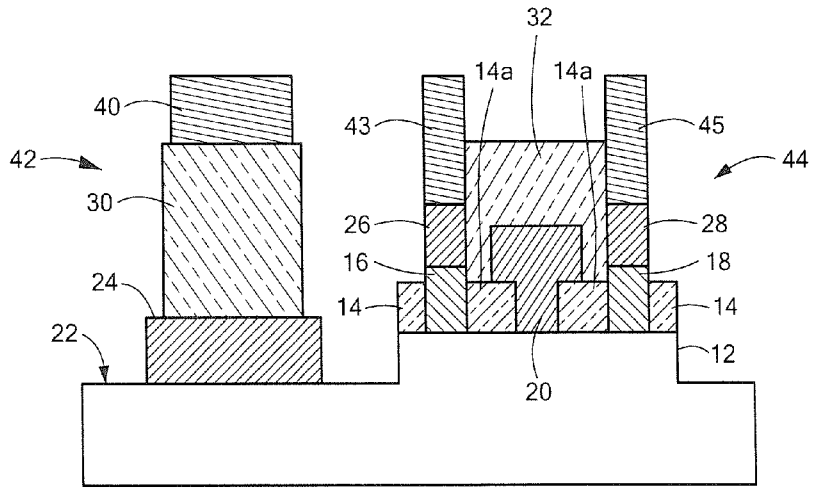


FIG. 8

(57) Abstract: A method for forming a structure on a surface of a semiconductor. The method includes: forming the material as a lower layer of the structure using a first deposition process to provide the lower layer with a first etch rate to a predetermined etchant; forming the upper layer of the structure with the material on the lower using a second deposition process to provide the upper layer with a second etch rate to the predetermined etchant higher than the first etch rate; and applying the predetermined etchant to upper layer to selectively remove the upper while leaving the lower layer.

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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SEMICONDUCTOR STRUCTURE AND METHOD

TECHNICAL FIELD

This disclosure relates generally to semiconductor structures and methods.

BACKGROUND AND SUMMARY

As is known in the art, many present Microwave (Millimeter-wave) Monolithic Integrated Circuit (MMIC) fabrication processes require two deposited layers of Plasma Enhanced Chemical Vapor Deposition (PECVD) silicon nitride (SiN): (1) thin (<100-nm) layer for surface passivation (Pass-SiN) of the transistors; and (2) a thick (>200-nm) layer for robust Metal-Insulator-Metal (MIM) capacitors (Cap-SiN). These two layers are over the active region between the source and drain contacts of the transistors. In this scenario, the latter layer or film is not essential on the transistor yet it adds unwanted parasitic capacitances between the metal contacts in the active region (e.g. source-gate, gate-drain, and source-drain) that deleteriously load the radio frequency (rf) gain performance of the device. This becomes a significant problem for millimeter-wave devices where gain becomes the limiting component to its overall performance.

This RF loading by the Cap-SiN is best exemplified on gallium nitride (GaN) based high electron mobility transistors (HEMTs), where the gain (G_{MAX}) across frequency may be lowered by up to 2.0-2.5 dB when the 200-nm Cap–SiN is added. Since the function of this film does not bring any benefit to the HEMT, the finished device inherently incurs this 2-3 dB gain reduction. Therefore, there is a need to decouple the Cap-SiN from the Pass-SiN in the transistor.

Pass-SiN films and similar ones from other groups has proven over the years to be an essential feature of the device because of its ability to dramatically reduce rf dispersion effects to tolerant levels that otherwise would be significantly deleterious to overall device power performance.

The common method to realize Pass- and Cap-SiN for MMICs is by deposition at approximately 300C with PECVD. For the latter film, this elevated temperature process eliminates the ability for selective area deposition with standard photolithography processes. Thus this film must be blanket-coated over the whole wafer and then selectively patterned to form MIM capacitors. However, because the deposition conditions for both SiN films are the same, selectively removing upper portions of the Cap-SiN layer in a reproducible manner down to the Pass-SiN to thin the dielectric for the

transistor relative to the thickness desired for the capacitor SiN layer is extremely difficult and impractical on a production level.

Another issue is that the PECVD Pass-SiN layer is deposited on the semiconductor after the semiconductor has been removed from the growth apparatus causing significant surface contamination from air exposure. High concentrations of contaminants such as carbon, oxygen, and silicon are now present on the air-exposed surface, which are very difficult to remove prior to PECVD deposition. Residual contaminants, which become buried at the semiconductor/Pass-SiN interface, are in the high electric field region between the gate and drain electrodes of the transistor, which can lead to deleterious transistor leakage currents.

SUMMARY

In accordance with the present disclosure, a method is provided for forming a structure on a surface of a semiconductor. The method includes: forming the material as a lower layer of the structure using a first deposition process to provide the lower layer with a first etch rate to a predetermined etchant; forming the upper layer of the structure with the material on the lower using a second deposition process to provide the upper layer with a second etch rate to the predetermined etchant higher than the first etch rate; and applying the predetermined etchant to upper layer to selectively remove the upper while leaving the lower layer.

In one embodiment, a method is provided for forming a pair of structures of a material having different thicknesses on a pair of different regions of a surface of a semiconductor. The method includes: forming the material as a lower layer with a first thickness extending over the pair of different regions using a first deposition process, such lower layer being formed with the first deposition process to provide the lower layer with a first etch rate to a predetermined etchant; forming the upper layer with the material on the lower layer over the pair of different regions with a second thickness different from the first thickness using a second deposition process to provide the second layer with a second etch rate higher than the first etch rate; masking a first portion of the upper layer over a first one of the pair of different regions while exposing a second portion of the upper layer over a second one of the pair of different regions; and applying the predetermined etchant to the exposed second portion of the upper layer to selectively remove the upper layer over the second one of the pair of different regions to form one of the structures while leaving the lower layer over the second one of the pair of different regions and leaving the upper

layer on the lower layer over the first one of the pair of regions to provide another one of the structures.

In one embodiment, a method is provided for forming a semiconductor device and a capacitor over different laterally spaced surface regions of a semiconductor, comprising: forming a dielectric material as a lower dielectric layer extending over the different laterally spaced regions using a first deposition process, such lower dielectric layer being formed with the first deposition process to provide the lower dielectric layer with a first etch rate to a predetermined etchant; forming the device in a first one of the regions with portions of the lower dielectric layer being disposed between a gate contact and a drain contact of the device and between the gate contact and a source contact of the device; removing portions of the lower dielectric layer over a second region to expose a capacitor region; forming the lower electrode of the capacitor on the capacitor region; forming the dielectric material as a continuous upper dielectric layer extending on the lower electrode of the capacitor and on the lower dielectric layer disposed between the gate contact and the drain contact and between the gate contact and the source contact, the upper dielectric layer being formed thicker than the lower dielectric layer using a second deposition process to provide the second dielectric layer with a second etch rate to the predetermined etchant being higher than the first etch rate; masking a portion of the upper dielectric layer on the lower electrode of the capacitor while exposing a portion of the upper dielectric layer on the lower dielectric layer over the gate contact and between the gate contact and the drain contact and between the gate contact and the source contact; applying the predetermined etchant to the exposed portion of the upper dielectric layer on the lower dielectric layer over the gate contact and between the gate contact and the drain contact and between the gate contact and the source contact to selectively remove the upper dielectric layer on the lower dielectric layer over the gate contact and between the gate contact and the drain contact and between the gate contact and the source contact while leaving unetched the masked portion of the upper dielectric layer on the lower electrode of the capacitor, and forming an upper electrode for the capacitors on the unetched portion of the upper dielectric layer on the lower electrode of the capacitor.

In one embodiment, the upper dielectric layer is formed thicker than the lower dielectric layer using a second deposition process different from the first deposition process

In one embodiment, the first deposition process is molecular beam epitaxial (MBE) growth and the second deposition process is non-MBE growth, for example Metal Organic Chemical Vapor Deposition (MOCVD), Atomic Layer Deposition (ALD) or PECVD.

In one embodiment, the second deposition process is performed in a hydrogen environment wherein the hydrogen content of the environment is at least an order of magnitude greater than the hydrogen content of the environment used in the first deposition process.

In accordance with the disclosure, a structure on a surface of a semiconductor includes a lower layer having a different hydrogen content than an upper layer of the structure.

In one embodiment, the lower layer and the upper layer are the same material.

In one embodiment, the material is a dielectric material.

In accordance with the disclosure, a structure includes: a first layer; and a second layer having a different hydrogen content than the first layer.

In one embodiment, the first layer and the second layer are the same material.

In one embodiment, the material is a dielectric material.

In one embodiment, a structure is provided having: a semiconductor; a capacitor disposed on one surface portion of the semiconductor and a transistor device disposed on a second surface portion of the semiconductor; wherein the capacitor includes a capacitor dielectric; wherein electrodes of the transistor device are separated by a device dielectric; wherein the capacitor dielectric and the device dielectric are the same material and have different thicknesses; and wherein one of the dielectrics has a different hydrogen content than the other dielectric.

The details of one or more embodiments of the disclosure are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the disclosure will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIGS. 1-8 are cross sectional diagrammatical sketches of a semiconductor structure having a transistor device and a capacitor formed in different regions of the structure at various steps in the fabrication thereof in accordance with the disclosure.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Referring now to FIG. 1, a wafer 10, here gallium nitride (GaN) for example, has a layer of semiconductor material 12, here GaN, for example, epitaxially formed *in situ* on the wafer 10 using molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD). Next, in an MBE embodiment, with the wafer 10 remaining in the MBE apparatus, not shown, the GaN layer 12, is coated *in situ* with a dielectric layer 14, here silicon nitride (SiN) to provide a passivation layer using the MBE apparatus. In an MOCVD/MBE embodiment, the substrate is coated with GaN and is then removed from the MOCVD (not shown) equipment and placed in the MBE apparatus, not shown, the GaN layer 12, is coated ex *situ* with a dielectric layer 14, here silicon nitride (SiN) to provide a passivation layer using the MBE apparatus. The passivation dielectric layer is formed in the MBE apparatus in an environment with little, e.g. much less than one percent, hydrogen at a growth temperature of 500-700°C. Next, the structure is removed from the MBE apparatus and etched to form a mesa structure as shown in FIG. 1. This etch also creates a mesa-like structure for a transistor device region 21 and an adjacent capacitor region 22 where the dielectric layer 14 is removed.

Next, as shown in FIGS. 2 and 3, source, drain and gate contacts 16, 18 and 20 are etched through openings in the dielectric layer 14 using conventional photolithographic-etching techniques. More particularly, ohmic source and drain contacts 16, 18 are formed to the GaN layer and a gate electrode 20 is formed, as shown, using conventional techniques. It is noted that portions 14a of the dielectric passivation layer 14 remain disposed between the gate contact 20 and a drain contact 18 of the device and between the gate contact 20 and the source contact 16 of the device.

Next, in the capacitor region 22 on the substrate, a conductive layer is deposited over the structure and patterned using conventional techniques to form a lower electrode 24 for a capacitor and upper contacts 26, 28 for the source and drain contacts 16, 18 as shown in FIG. 4.

Next, a second dielectric layer 30, herein also referred to as an upper dielectric layer, of the same material as dielectric layer 14, here SiN, is deposited as a continuous upper dielectric layer extending over the entire surface of the structure including over the lower electrode 24 of the capacitor and on the dielectric layer 14 including the portions 14a of the dielectric layer 14 disposed between the gate contact 20 and the drain 18 and between the gate contact 20 and the source contact 16 as well as over the gate contact 20

itself, as shown in FIG 5, the upper dielectric layer 30 being formed thicker than the lower dielectric layer 14 using a second deposition process, here for example PECVD. The thickness of the upper dielectric layer 30 is in the range of 100-300 nm and the thickness of the first dielectric layer 14 is in the range of 10-100 nm.

It is to be noted that in non-MBE SiN films such as PECVD films (*ex situ*) there is a higher hydrogen (H_2) content (~10%) and the hydrogen is actually bonded to the silicon and nitrogen. The material is sometimes considered SiNH. Hydrogen can be detected in the SiN films of the finished product. The capacitor dielectric SiN, i.e., the second dielectric layer, is, as noted above, will have a detectable higher hydrogen content than passivation SiN first dielectric layer fabricated by, here for example, in the *in situ* MBE embodiment or the *ex situ* MOCVD/MBE embodiment . In the case of PECVD SiN, the atomic concentration of hydrogen films is approximately 10% (10% of the atoms are hydrogen) compared to less than 0.1% in MBE SiN. Therefore, the MBE deposition process provides the first dielectric layer with a substantially lower etch rate to buffered hydrofluoric acid (BHF) wet etch chemistry than the etch rate of BHF wet etch chemistry to the PECVD deposited second SiN dielectric layer. The etch selectivity between PECVD SiN and, here for example, MBE SiN is as high as 14 (= 0.38/0.03) – 16 (= 0.49/0.03) to 1.

Next, the portion of the upper dielectric layer 30 on the lower electrode 24 of the capacitor is masked while exposing a portion of the upper dielectric layer 30 on the lower dielectric layer 14 including the portions 14a between the gate contact 20 and the drain contact 18 and between the gate contact 20 and the source contact 16.

Next, the unmasked structure is exposed to a BHF wet etch chemistry to selectively remove the exposed portions of the upper dielectric layer 30 on the lower dielectric layer 14 including the portions 14a between the gate contact 20 and the drain contact 18 and between the gate contact 20 and the source contact 16 while leaving unetched the masked portion of the upper dielectric layer 30 on the lower electrode of the capacitor, as shown in FIG. 6.

It is noted that the selectivity in the etching of the exposed portions of the upper SiN dielectric layer 30 and the lower SiN dielectric layer 14. More particularly, the etching of the exposed portions of the upper SiN layer 30 is self limiting because of the different etch rates of the upper SiN layer 30 and the lower SiN layer 14. Thus, while both the upper dielectric layer 30 and lower dielectric layer 14 are of the same dielectric

material, here SiN, the lower SiN dielectric layer 14 is deposited by MBE on *ex-situ* MOCVD material or *in-situ* MBE material during the GaN transistor epitaxy growth process while the upper SiN dielectric layer 30 is formed *ex-situ* using PECVD for example. This layer 14, which hereby is referred to as Pass-SiN, is deposited at the growth temperature of 500-700°C and has among a host of favorable attributes, a dramatically slower etch rate (by a factor of 14-16 in the case of PECVD SiN) compared to alternate deposited SiN dielectric layer 30 used for the capacitor SiN. This 14-16:1 etch rate ratio provides the selectivity needed for wet etch chemistry processes to effectively remove the capacitor SiN dielectric layer 30 and leave the in-situ SiN lower dielectric layer 14 intact or unaltered. Wet etch chemistries as opposed to plasma-based dry etch chemistries provides a gentler approach to completely remove the exposed capacitor SiN dielectric layer 30 in key areas surrounded by metal structures, such as the source, drain and gate contacts of varying topologies (e.g. mushroom gates and source/drain ohmic contacts) with minimal or no damage to them. In addition, because the *pass*-SiN layer 14 is part of the GaN transistor epitaxy process, its thickness can be controlled reproducibly at the sub-nm scale which allows for thinner pinhole-free films much less than 50-nm to be realized. This in turn should further minimize RF loading while still maintaining true passivation of the device.

An additional benefit the *pass*-SiN layer 14 brings because of its high density, pinhole-free quality in ultra-thin layers is the ability to realize ultra-low leakage, high quality metal-insulator-semiconductor field effect transistors (MISFETs) where the gate metal can sit directly on top of an ultra-thin in-situ dielectric layer 14 rather than through it. Adjusting the underlying Schottky AlGaN thickness to accommodate the additional ultra-thin *pass*-SiN layers for such devices provides another degree of flexibility and design towards greatly improving linearity performance without sacrificing transconductance and gain performance. This could be further extended for ultra-high frequency and gain performance at millimeter-wave frequencies, where MISFETs or HEMTs based on high Al-containing (>25%) ultra-thin AlGaN or AlN Schottky layers on GaN can be realized without the potential concern of carrier loss due to surface trapping/depletion or leakage along the semiconductor surface.

A final benefit is noted of the pass-SiN layer 14 when it is deposited in the MBE machine after MBE growth of the semiconductor, a process known as *in situ* deposition. With *in situ* deposition, the critical interface between the semiconductor and pass-SiN is

never exposed to contaminating air, which occurs with the alternate pass-SiN process. *The in situ* process eliminates the high concentration of surface contaminants such as oxygen, carbon, and silicon at the semiconductor-pass-SiN interface.

Next, a low-k dielectric layer 32, here for example, SiO_2, is deposited over the surface of the structure, here using atomic layer deposition (ALD) or PECVD, as shown in FIG. 6. Next, portions of the low-k dielectric layer 32 are selectively removed using conventional photolithograph-etching processes to form the structure shown in FIG. 7.

Next, portions of layer 32 are removed above the source and drain contacts 26, 28 using conventional photolithograph-etching processes. Next, an upper conductor is deposited over the structure and patterned to form an upper electrode 40 for the capacitor 42 on the unetched portion of the upper dielectric layer 30 and upper contacts 43, 45 for the source and drain contacts 16, 26 and 18, 28, respectively for transistor device 44, as indicated in FIG. 8.

Thus, the method selectively removes the capacitor SiN dielectric layer 30 between source and drain of the transistor during device fabrication and replaces it with an alternate low-k dielectric film without compromising the voltage capability of the MIM capacitor 42 while still maintaining good passivation and high frequency performance of the HEMT 44. For MISFETs the process flow is as described above with the etching through the lower dielectric layer 14 for the gate contact 20 step shown in FIG. 3 skipped.

A number of embodiments of the disclosure have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the disclosure. For example, while the use of two different dielectric layers having different hydrogen content has been used as described above to form a structure with a capacitor and a transistor, the use of two different dielectric layers having different hydrogen contents may be used for other structures. Further, while two different processes were used to form the SiN dielectric layers, (a MBE (or MBE/MOCVD) for the first process and non-MBE for the second process), the same process may be used to form the SiN dielectric layers with two different hydrogen concentrations such as forming the first SiN layer using a MBE with almost no hydrogen content, and later the SiN is grown with hydrogen added to the growth process. Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A method for forming a structure on a surface of a semiconductor, comprising:

forming the material as a lower layer of the structure using a first deposition process to provide the lower layer with a first etch rate to a predetermined etchant;

forming the upper layer of the structure with the material on the lower using a second deposition process to provide the upper layer with a second etch rate to the predetermined etchant higher than the first etch rate;

applying the predetermined etchant to upper layer to selectively remove the upper while leaving the lower layer.

2. A method for forming a pair of structures of a material having different thickness on a pair of different regions of a surface of a semiconductor, comprising:

forming the material as a lower layer with a first thickness extending over the pair of different regions using a first deposition process, such lower layer being formed with the first deposition process to provide the lower layer with a first etch rate to a predetermined etchant;

forming the upper layer with the material on the lower layer over the pair of different regions with a second thickness different from the first thickness using a second deposition process to provide the second layer with a second etch rate higher than the first etch rate;

masking a first portion of the upper layer over a first one of the pair of different regions while exposing a second portion of the upper layer over a second one of the pair of different regions;

applying the predetermined etchant to the exposed second portion of the upper layer to selectively remove the upper layer over the second one of the pair of different regions to form one of the structures while leaving the lower layer over the second one of the pair of different regions and leaving the upper layer on the lower layer over the first one of the pair of regions to provide another one of the structures.

3. A method for forming a semiconductor device and a capacitor over different laterally spaced surface regions of a semiconductor, comprising:

forming a dielectric material as a lower dielectric layer extending over the different laterally spaced regions using a first deposition process, such lower dielectric layer being formed with the first deposition process to provide the lower dielectric layer with a first etch rate to a predetermined etchant;

forming the device in a first one of the regions with portions of the lower dielectric layer being disposed between a gate contact and a drain contact of the device and between the gate contact and a source contact of the device;

removing portions of the lower dielectric layer over a second one of the regions to expose a capacitor region;

forming the a lower electrode of the capacitor on the capacitor region;

forming the dielectric material as a continuous upper dielectric layer extending on the lower electrode of the capacitor and on the lower dielectric layer disposed over the gate contact and between the gate contact and the drain contact and between the gate contact and the source contact, the upper dielectric layer being formed thicker than the lower dielectric layer using a second deposition process to provide the second dielectric layer with a second etch rate to the predetermined etchant being higher than the first etch rate;

masking a portion of the upper dielectric layer on the lower electrode of the capacitor while exposing a portion of the upper dielectric layer on the lower dielectric layer over the gate contact and between the gate contact and the drain contact and between the gate contact and the source contact;

applying the predetermined etchant to the exposed portion of the upper dielectric layer on the lower dielectric layer over the gate contact and between the gate contact and the drain contact and between the gate contact and the source contact to selectively remove the upper dielectric layer on the lower dielectric layer between the gate contact and the drain contact and between the gate contact and the source contact electrode while leaving unetched the masked portion of the upper dielectric layer on the lower electrode of the capacitor, and

forming an upper electrode for the capacitors on the unetched portion of the upper dielectric layer on the lower electrode of the capacitor.

4. The method recited in claim 3 wherein the first deposition process is different from the second deposition process.

5. The method recited in claim 4 wherein the second deposition process is performed in a hydrogen environment wherein the hydrogen content of the environment is at least an order of magnitude greater than hydrogen environment used in the first deposition process.

6. A structure, comprising:

a lower layer of the structure having a different hydrogen content than an upper layer of the structure.

7. The structure recited in claim 6 wherein the lower layer and the upper layer are the same material.

8. The structure recited in claim 7 wherein the material is a dielectric material.

9. A structure comprising:

a semiconductor;

a capacitor disposed on one surface portion of the semiconductor and a transistor device disposed on a second surface portion of the semiconductor;

wherein the capacitor includes a capacitor dielectric;

wherein electrodes of the transistor device are separated by a device dielectric;

wherein the capacitor dielectric and the device dielectric are the same material and have different thicknesses; and

wherein one of the dielectrics has a different hydrogen content than the other one of the dielectrics.

10. A method for forming a structure, comprising:

forming a lower layer of the structure with a different hydrogen content than an upper layer of the structure.

11. The method recited in claim 10 wherein the upper layer is formed using process different from a process used to form the lower layer.

12. The method recited in claim 11 wherein the upper dielectric layer is formed thicker than the lower dielectric layer using a second deposition process different from the first deposition process.

13. The method recited in claim 3 wherein the upper dielectric layer is formed with a process different from a process used to form the lower dielectric layer.

14. The method recited in claim 12 wherein the first deposition process is molecular beam epitaxy.

15. The method recited in claim 14 wherein the second deposition process MOCVD, ALD or PECVD.

16. The method recited in claim 13 wherein the first deposition process is molecular beam epitaxy.

17. The method recited in claim 16 wherein the second deposition process MOCVD, ALD or PECVD.

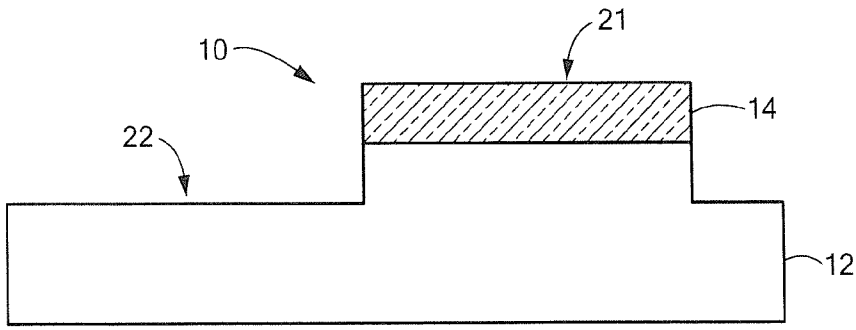


FIG. 1

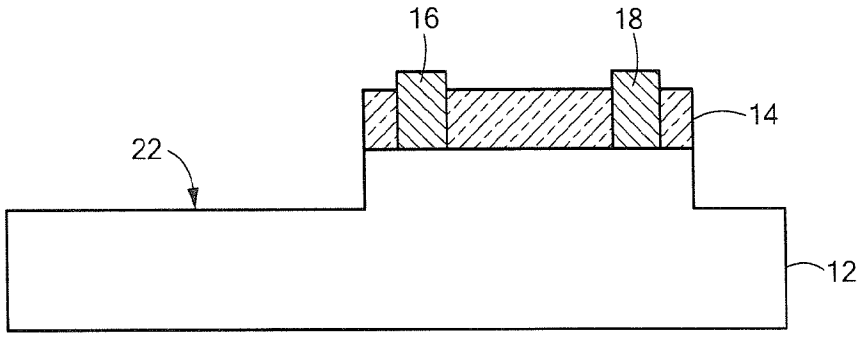


FIG. 2

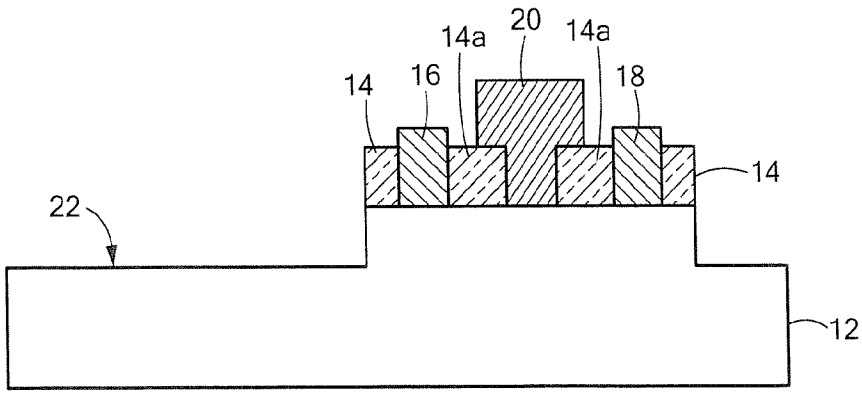


FIG. 3

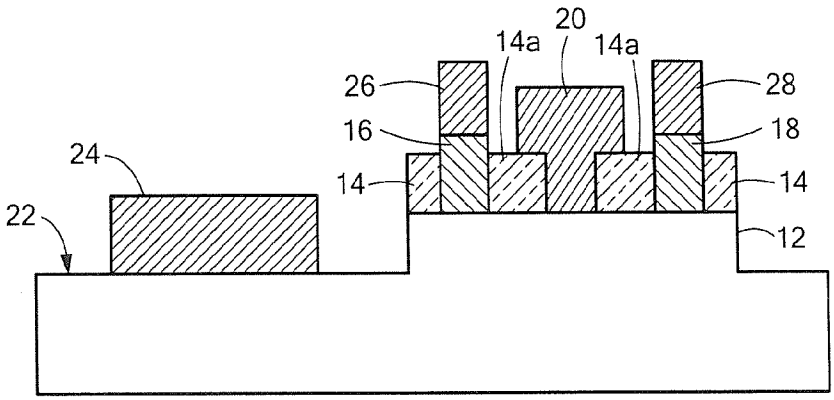

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FIG. 4

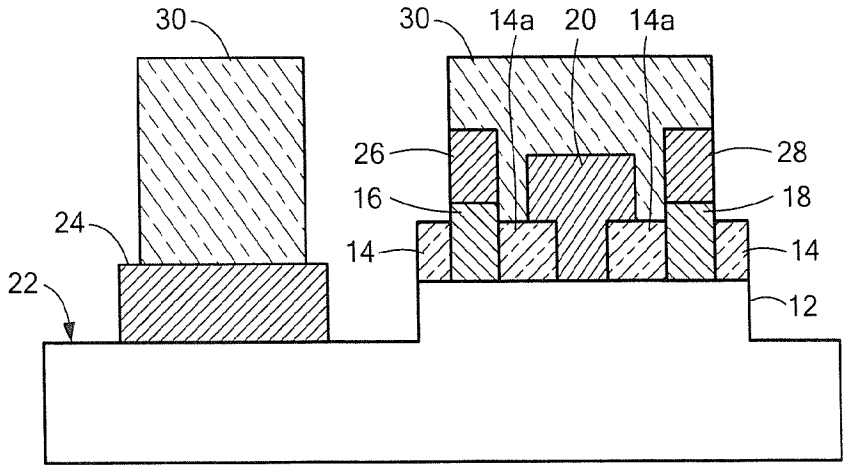

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FIG. 5

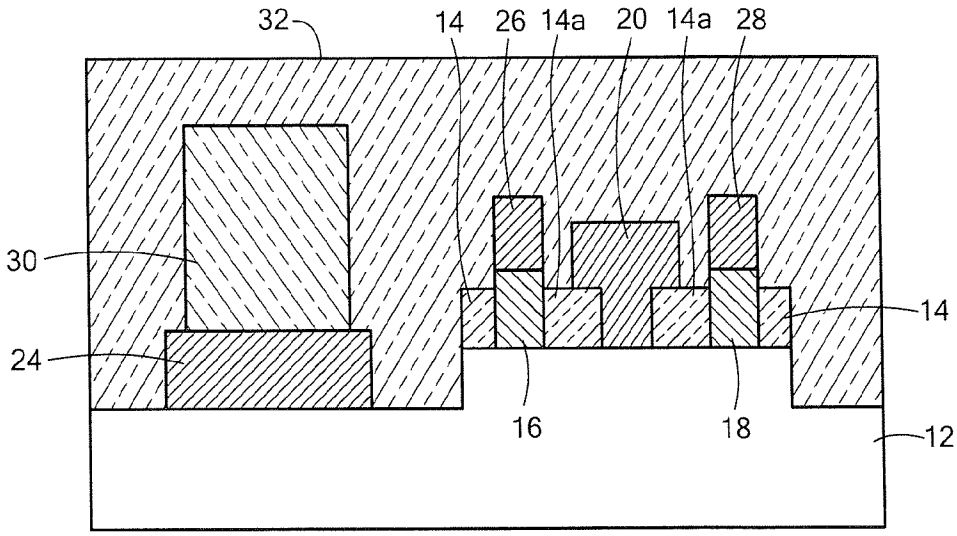

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FIG. 6

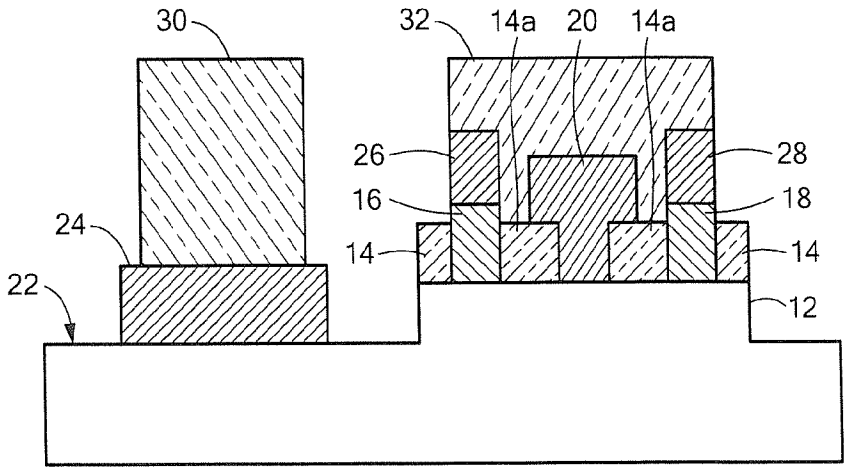

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FIG. 7

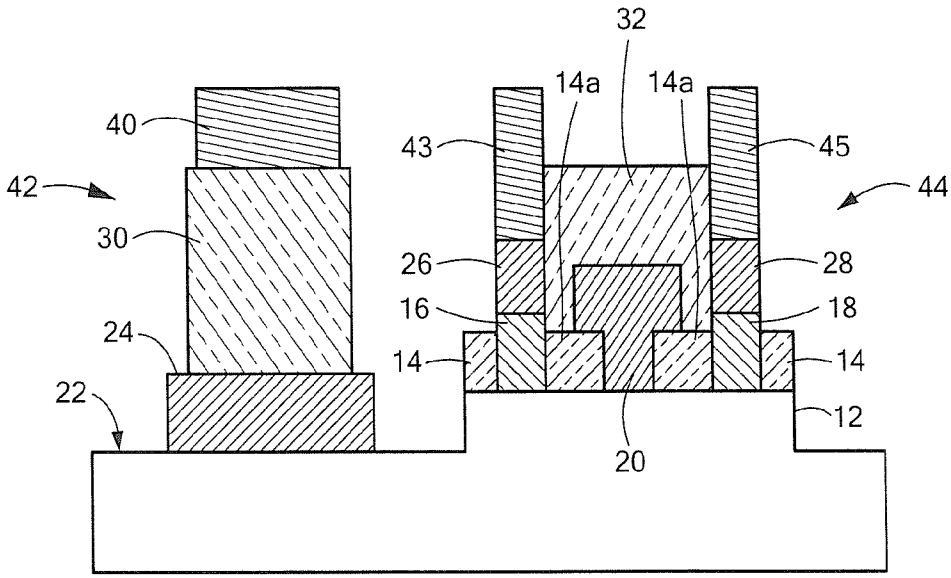


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/046283

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/8252 H01L27/06 H01L21/311
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 742 584 A2 (IBM [US]) 13 November 1996 (1996-11-13)	1,2,6-8, 10-12, 14-16
Y	* abstract; claims; figures 1,2 column 3, line 37 - line 45	4,5,9, 13,17
X	US 6 222 257 B1 (CATHEY DAVID A [US] ET AL) 24 April 2001 (2001-04-24)	1,6-8, 10-12, 14-16
Y	* abstract; claims; figures 1,2 column 7, line 27 - line 37	4,5,9, 13,17
X	US 6 229 156 B1 (MURAI HIROYUKI [JP] ET AL) 8 May 2001 (2001-05-08) * abstract; claims; figure 2(a) column 5, line 5 - line 31	1,6,10

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
5 November 2010	12/11/2010

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International application No
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	US 2001/012652 A1 (MATSUDA HAJIME [JP]) 9 August 2001 (2001-08-09) * abstract; claims; figure 6F paragraphs [0065], [0094], [0095], [0096]	9
X Y	US 2008/280400 A1 (AIHARA YASUKI [JP]) 13 November 2008 (2008-11-13) * abstract; claims; figure 7	14,16 3
X	US 2002/130389 A1 (ARIMOCHI KENJI [JP] ET AL) 19 September 2002 (2002-09-19) * abstract; claims; figure 2K paragraphs [0042], [0050]	6,10,14, 16
A	JP 10 261616 A (TOSHIBA CORP) 29 September 1998 (1998-09-29) * abstract	1-17

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