

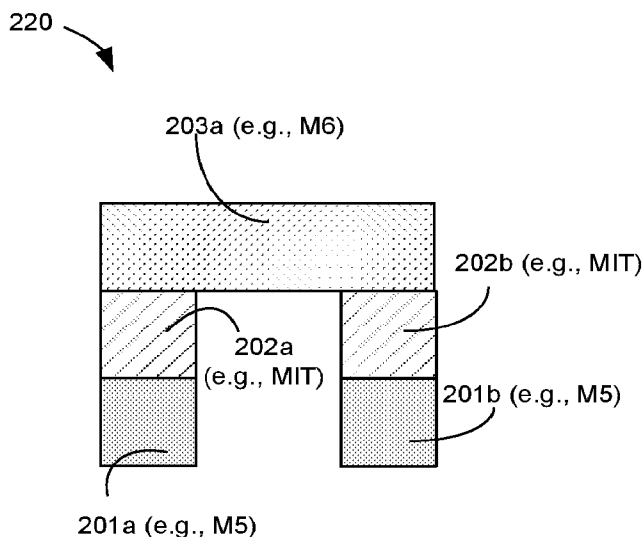


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[Continued on next page]

- (54) **Title:** CONFIGURABLE INTERCONNECT APPARATUS AND METHOD



- (57) **Abstract:** Described is an apparatus which comprises: a first interconnect; a second interconnect; a third interconnect; a first via comprising a metal-insulator-transition (MIT) material, the first via to couple the first interconnect to the third interconnect; and a second via comprising the MIT material, the second via to couple the second interconnect to the third interconnect.

Fig. 2B



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CONFIGURABLE INTERCONNECT APPARATUS AND METHOD

BACKGROUND

[0001] Today, a single product design is required to operate at different supply voltages. For example, the same processor is designed to operate at a high voltage supply (e.g., 1.2V) and a low voltage supply (e.g., 0.5V). The supply voltage (or voltage range) may be selected and fixed according to the performance and power requirements of a market segment (e.g., tablet, laptop, desktop, etc.). For example, a processor in the desktop market segment may operate at a higher voltage providing higher frequency and processing speed (i.e., higher performance) while the same processor in a tablet or laptop market segment may operate at a lower voltage and at lower frequency and processing speeds. Also, the voltage may be adjusted dynamically during operation (e.g., low power mode, turbo mode, etc.).

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0003] Fig. 1A illustrates a plot comparing performance of a logic in terms of frequency of operation with changing supply voltage for the cases using ideal interconnects, interconnects with resistive effect, and configurable interconnects of some embodiments.

[0004] Fig. 1B illustrates a plot showing a design which is optimized to achieve high turbo performance and which may not achieve as low energy as possible even when operating at low power supplies.

[0005] Fig. 2A illustrates a top view of a configurable interconnect, in accordance with some embodiments of the disclosure.

[0006] Fig. 2B illustrates a side view of the configurable interconnect of Fig. 2A, in accordance with some embodiments of the disclosure.

[0007] Fig. 3A illustrates a configurable interconnect configured to have high resistivity due to change in stimulus, in accordance with some embodiments.

[0008] Fig. 3B illustrates the configurable interconnect of Fig. 3A configured to have low resistivity due to change in stimulus, in accordance with some embodiments.

[0009] **Fig. 4** illustrates a cross-sectional view of a configurable interconnect which is configurable via application of an electric field, in accordance with some embodiments of the disclosure.

[0010] **Fig. 5** illustrates a cross-sectional view of a configurable interconnect which is configurable via an application of current flow, in accordance with some embodiments of the disclosure.

[0011] **Fig. 6A** illustrates a schematic with configurable interconnects which are configured to bypass a buffer, in accordance with some embodiments of the disclosure.

[0012] **Fig. 6B** illustrates a schematic with configurable interconnects which are configured to incorporate the buffer, in accordance with some embodiments of the disclosure.

[0013] **Fig. 7** illustrates a top view of an interconnect network having a configurable interconnect formed of a Micro-Electro-Mechanical Switch (MEMS), in accordance with some embodiments of the disclosure.

[0014] **Fig. 8A** illustrates a cross-section of part of the network of the MEMS based configurable interconnect, in accordance with some embodiments of the disclosure.

[0015] **Fig. 8B** illustrates a cross-section of part of the network of the MEMS based configurable interconnect in a first configuration, in accordance with some embodiments of the disclosure.

[0016] **Fig. 8C** illustrates a cross-section of part of the network of the MEMS based configurable interconnect in a second configuration, in accordance with some embodiments of the disclosure.

[0017] **Fig. 9** illustrates a flowchart of a method for configuring resistivity and/or capacitance of a configurable interconnect using an electric field, in accordance with some embodiments of the disclosure.

[0018] **Fig. 10** illustrates a flowchart of a method for configuring resistivity and/or capacitance of a configurable interconnect using change in temperature, in accordance with some embodiments of the disclosure.

[0019] **Fig. 11** illustrates a smart device or a computer system or a System-on-Chip (SoC) with one or more configurable interconnect, according to some embodiments.

DETAILED DESCRIPTION

[0020] The power and performance effects of resistive interconnect depend strongly on the supply voltage. As such, the designs that operate best at low voltages are less efficient operating at high voltages, and vice-versa. Applying one design for different market segments and power modes provides for design and manufacture efficiency, but compromises performance and energy. This compromise may only get more severe as interconnect resistance increases with scaling.

[0021] Current solutions to designing logic or processors with resistive interconnect are limited to two non-optimal methods. In the first method, the design of the Integrated Circuit (IC) is optimized at a given performance point (e.g., high-performance or low-power). In this case, the other performance target product will suffer significantly operating at sub-optimal power-performance. For example, an IC design optimized to operate at high performance (e.g., high frequency) may result in sub-optimal power efficiency for a product operated at a low voltage and frequency because more power would be consumed than the minimum actually needed to operate with lower performance.

[0022] Fig. 1A illustrates plot 100 comparing the performance of a logic in terms of frequency of operation with changing supply voltages for the cases with ideal interconnects, interconnects with resistive effect, and configurable interconnects of some embodiments. Here, the x-axis is supply (V_{dd}) and the y-axis is Frequency (in GHz). Plot 100 shows three curves—101, 102, and 103.

[0023] Curve 101 (dotted curve) illustrates a performance of an IC having logic dominated path not substantially comprised of interconnect (e.g., interconnect resistance is much smaller than transistor resistance). For example, logic performance mainly depends on the logic delay and not on the interconnect propagation delay. Here, the interconnect has a very low resistivity and frequency is determined by transistor current drive (e.g., inverse of transistor resistance) which is high at higher supply resulting in higher frequency and performance, and lower when the logic is operating at lower supply resulting in lower frequency and performance).

[0024] Curve 102 illustrates a performance of an IC logic using interconnects designed for a certain supply voltage and performance. In this case, as the supply voltage increases, the increase in frequency of operation is limited by the interconnect propagation delay. Curve 103 illustrates the performance of an IC logic using a configurable interconnect as described with

reference to the various embodiments. In this case, as the supply level increases (e.g., Vdd increases from 0.4V to 1.0V), the interconnect delay is reduced to lower levels than curve 102 which allows for higher frequency of operation compared to curve 102. For example, various buffers are dynamically introduced to the logic path to overcome interconnect propagation delay.

[0025] Likewise, as the supply level decreases (e.g., 1.0V to 0.4V), the interconnect delay is allowed to increase because the performance may not be the primary concern, but lowering energy with less frequent buffers is. For example, for lower power operation, the various buffers that were dynamically introduced can now be dynamically bypassed. For example, at high voltage, a buffer may decrease total delay but at low voltage the same buffer may increase the total delay compared to the delay seen during low voltage operation of the circuit with a bypassed buffer.

[0026] In the second method, IC products are redesigned at two separate performance points appropriate for separate applications (e.g., laptop or desktop). This method can improve upon performance and efficiency when a single design is used in products with different power and performance requirements, but cannot fully address when a single product needs to dynamically adjust its power and performance requirement.

[0027] Fig. 1B illustrates plot 120 showing a design (e.g., Turbo Design) which is optimized to achieve high turbo (or highest) performance, and which may not achieve as low energy as possible even when operating at low power supplies. Also this two-design approach is very expensive. Various embodiments provide a configurable interconnect that achieves the Optimal Design (e.g., lower energy per operation than the Turbo Design) at lower frequency of operation and comparable energy per operation as the Turbo Design at turbo frequency levels (i.e., higher frequencies).

[0028] Table 1 shows that it may be better to optimize to lower wire or interconnect capacitance 'C' at low voltages (e.g., 0.65V), but to optimize to lower wire or interconnect resistance 'R' at high voltages (e.g., 1.10V). In some embodiments, the configurable interconnect follows the behaviors outlined in Table 1.

Table 1

Vdd	Approximate % change in Capacitance 'C'	Approximate % change in Resistance 'R'
0.65V	10%	41%
1.10V	10%	16%

Table 1 illustrates low and high voltage cases, and percentage change in capacitance 'C' and its equivalent change in resistance 'R.' In this example, 10% change in capacitance 'C' is equivalent in delay to 41% change in resistance 'R' at 0.65V Vdd, but is 16% at 1.1V Vdd.

[0029] In some embodiments, interconnect resistance and/or capacitance is configurable dynamically (e.g., with change in temperature, by applying electric field, by introducing a temporary current, by applying external pressure, etc.) to achieve optimum interconnect design. In some embodiments, the interconnect resistance and/or capacitance is dynamically reconfigurable by metal-insulator-transition (MIT) switches. In some embodiments, the interconnect resistance and/or capacitance is dynamically reconfigurable by micro-electro-mechanical (MEMs) switches or nano-electro-mechanical (NEMs) switches.

[0030] In some embodiments, dynamic reconfiguration of the interconnect properties (e.g., resistance, capacitance, buffer spacing and sizing) is achieved by a layer of via which can be made into a conductor-like metal or an insulator-like dielectric depending on different product targets. In some embodiments, the dynamic reconfiguration is achieved by using schemes of alternate sub-circuits selected to operate depending on the supply voltage mode. For example, buffers may be added to drive interconnects during high voltage operation while during low voltage operation, buffers can be bypassed to reduce power. In some embodiments, fabrication-time configuration of the interconnect (e.g., resistance, capacitance, buffer spacing, sizing, etc.) is achieved by a layer of via which can be made conductor-like metal or insulator-like dielectric depending on different product targets.

[0031] In some embodiments, at low voltage, one or more interconnects are reconfigured to have long spacing between buffers for high performance per watt and high performance at low voltage. For example, at low voltage it may be best to size wires to minimize (e.g., reduce) wire capacitance. In some embodiments, at high-voltage, one or more interconnects are reconfigured to have short spacing between buffers for high performance at high voltage. For example, at high voltage it may be best to size wires to minimize resistance.

[0032] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block

diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0033] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0034] Throughout the specification, and in the claims, the term "connected" means a direct connection, such as electrical, mechanical, or magnetic connection between the things that are connected, without any intermediary devices. The term "coupled" means a direct or indirect connection, such as a direct electrical, mechanical, or magnetic connection between the things that are connected or an indirect connection, through one or more passive or active intermediary devices.

[0035] The term "circuit" or "module" may refer to one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" may refer to at least one current signal, voltage signal, magnetic signal, or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0036] The term "scaling" generally refers to converting a design (schematic and layout) from one process technology to another process technology and subsequently being reduced in layout area. The term "scaling" generally also refers to downsizing layout and devices within the same technology node. The term "scaling" may also refer to adjusting (e.g., slowing down or speeding up – i.e. scaling down, or scaling up respectively) of a signal frequency relative to another parameter, for example, power supply level. The term "scaling" may also refer to adjusting the magnitude of the power supply voltage (e.g., voltage scaling) to the circuit(s).

[0037] The terms "substantially," "close," "approximately," "near," and "about," generally refer to being within +/- 10% of a target value. Unless otherwise specified the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely

indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0038] It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein.

[0039] For the purposes of the present disclosure, phrases “A and/or B” and “A or B” mean (A), (B), or (A and B). For the purposes of the present disclosure, the phrase “A, B, and/or C” means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C). The terms “left,” “right,” “front,” “back,” “top,” “bottom,” “over,” “under,” and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions.

[0040] For purposes of the embodiments, the transistors in various circuits, modules, and logic blocks may be Tunneling FETs (TFETs) or some transistors of various embodiments may comprise metal oxide semiconductor (MOS) transistors, which include drain, source, gate, and bulk terminals. The transistors may also include Tri-Gate and FinFET transistors, Gate All Around Cylindrical Transistors, Square Wire, or Rectangular Ribbon Transistors or other devices implementing transistor functionality like carbon nano tubes or spintronic devices. MOSFET symmetrical source and drain terminals i.e., are identical terminals and are interchangeably used here. A TFET device, on the other hand, has asymmetric Source and Drain terminals. Those skilled in the art will appreciate that other transistors, for example, Bi-polar junction transistors—BJT PNP/NPN, BiCMOS, CMOS, etc., may be used for some transistors without departing from the scope of the disclosure.

[0041] **Fig. 2A** illustrates top view 200 of a configurable interconnect, in accordance with some embodiments of the disclosure. **Fig. 2B** illustrates side view 220 of cross-section AA' of the configurable interconnect of **Fig. 2A**, in accordance with some embodiments of the disclosure.

[0042] In some embodiments, the configurable interconnect of **Figs. 2A-B** comprise a first interconnect 201a (e.g., interconnect on metal layer 5 (M5)), a second interconnect 201b (e.g., another interconnect extending parallel to first interconnect 201a), first MIT via 202a, second MIT via 202b, third MIT via 202aa, fourth MIT via 202bb, third interconnect 203a (e.g.,

interconnect on a different metal layer than first and second interconnect 201a/b), and fourth interconnect 203aa. Here, interconnects 201a/b and 203a/aa can be formed of any suitable conducting material (e.g., Cu, Al, or any suitable alloy). In some embodiments, MIT vias 202a/b couple first and second interconnects 201a/b to third interconnect 203a. In some embodiments, MIT vias 202aa/bb couple first and second interconnects 201a/b to fourth interconnect 203aa. So as not to obscure the various embodiments, cross-section AA' is described.

[0043] In some embodiments, MIT vias 202a/b (which are also known as metal-oxide-transition (MOT or MOTT) vias) couple first and second interconnects 201a/b, respectively, with third interconnect 203a. In some embodiments, MIT vias 202a/b can change their conducting characteristics according to an application of a stimulus (e.g., change in temperature, electric field, electric current, pressure, etc.). As such, MIT vias 202a/b can transition from metal to an insulator or vice versa. In some embodiments, MIT vias 202a/b are formed of one of: VO₂, V_xO_y, Ti-doped V₂O₃, Fe₃O₄, FeS, Ti_xO_y, TiS₂, LaCoO₃, SmNiO₃, EuO, doped semiconductors such as Si:P, Si:As, Si:B, and Si:Ga. In some embodiments, MIT vias 202a/b comprises a material selected from a group consisting of: VO₂, V_xO_y, Fe₃O₄, FeS, Ti_xO_y, TiS₂, LaCoO₃, SmNiO₃, and EuO. In some embodiments, the selected material further comprises trace dopant or other impurity species.

[0044] In some embodiments, third interconnect 203a has lower than or same resistivity as first and second interconnects 201a/b. For example, third interconnect 203a is formed on higher metal layer (e.g., metal layer 6 (M6) while first and second interconnects 201a/b are formed of metal layers 5 (M5)). In some embodiments, third interconnect 203a has higher than or same resistivity as first and second interconnects 201a/b. For example, third interconnect 203a is formed on a lower metal layer (e.g., metal layer 4 (M4) while first and second interconnects 201a/b are formed on M5). In some embodiments, third interconnect 203a extends orthogonal to first and second interconnects 201a/b. In some embodiments, interconnects 201a/b are formed on different metal layers. In some embodiments, interconnects 201a/b have different cross-sectional dimensions. In some embodiments, interconnects 201a/b have different spacing to adjacent interconnects. In some embodiments, the first, second, and third interconnects comprise a material selected from a group consisting of Cu or Al. In some embodiments, the material further comprises a dopant, alloying material, or other impurity species.

[0045] In some embodiments, the temperature sensitivity of MIT vias 202a/b can be arranged to be closer to where the design wants to move from high resistance and low capacitance to low resistance and slightly higher capacitance. When MIT vias 202a/b are formed of VO₂, the transition from metal to insulator and back is close to 300 Kelvins (K). In this example, for temperature higher than 300 K, MIT vias 202a/b become metal to use two parallel interconnects (e.g., interconnects 201a/b).

[0046] In some embodiments, MIT vias 202a/b are designed to change characteristics at a temperature threshold (e.g., 75 degrees Celsius). For example, at temperatures higher than 75 degrees Celsius, MIT vias 202a/b transition from insulator to metal. As such, in some embodiments, at temperatures above 75 degrees Celsius, MIT vias 202a/b electrically couple first and second interconnect 201a to third interconnect 203a. In some embodiments, at temperatures below 75 degrees Celsius, MIT vias 202a/b transition from metal to insulator and as such electrically decouple first and second interconnect 201a/b from third interconnect 203a. In this example, at higher temperatures, the reconfigurable interconnect is configured to have lower resistance to cope with generally higher effect of interconnect resistivity on performance at higher temperatures.

[0047] Fig. 3A illustrates circuit 300 having configurable interconnect configured to have high resistivity due to change in stimulus, in accordance with some embodiments. It is pointed out that those elements of Fig. 3A having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0048] In some embodiments, circuit 300 comprises buffer 301, buffer 302, first reconfigurable via or interconnect 303, second reconfigurable via or interconnect 304, first interconnect 305a (e.g., 201a), and second interconnect 305b (e.g., 201b). For purposes of simplifying the circuit, buffers 301 and 302 are shown. In other embodiments, other kinds of input and output drivers may be used instead of buffers 301 and 302 that receive input "In" and provide output "Out." The embodiments are not limited to the use cases discussed here. The reconfigurable interconnect of various embodiments can be used in numerous use cases.

[0049] In some embodiments, first and second reconfigurable vias or interconnect 303/304 are same as MIT vias 202a/b. In some embodiments, first and second reconfigurable via or interconnect 303/304 are MEMS or NEMS as described with reference to Figs. 7-8.

Referring back to **Fig. 3A**, in some embodiments during low power mode or for designs meant for low power operation, first and second reconfigurable vias or interconnect 303/304 are configured to be insulator-like. As such, first and second interconnects 305a/b are electrically decoupled from one another.

[0050] In some such embodiments, buffer 301 drives its output signal to buffer 302 by way of using first interconnect 305a. Here, input to buffer 301 is “In” and output of buffer 302 is “Out.” In some embodiments, where lower interconnect resistance is desired (e.g., for high supply or higher performance designs), first and second reconfigurable vias or interconnect 303/304 are configured to be metal like as shown in **Fig. 3B**. **Fig. 3B** illustrates circuit 320 having the configurable interconnect of **Fig. 3A** configured to have low resistivity due to change in stimulus, in accordance with some embodiments. Here, the first and second reconfigurable vias or interconnect 303/304 are relabeled as first and second reconfigurable vias or interconnect 323/324, respectively. Vias or interconnect 303/304 have no line passing through them to indicate insulating state (e.g., an open circuit) while vias or interconnect 323/324 have a line passing through them to indicate conductance (e.g., a short circuit). The configuration of **Fig. 3B** may result in lower overall interconnect resistance ‘R’ due to parallel combination of first and second interconnects 305a/b. In this configuration, interconnect capacitance ‘C’ may increase due to parallel combination of capacitances of first and second interconnects 305a/b.

[0051] In some embodiments, a MIT (metal-insulator-transition) or MEMS placed in the back-end metallization can serve as a configurable via. In some embodiments, this via can: Strap (e.g., connect) multiple metal lines in parallel improving net resistance (e.g., for high-Vdd performance); disconnect strapped metal lines improving net capacitance (e.g., for low-Vdd performance and energy); route the long wire line to the optimally buffers positioned in optimal places for each supply voltage; connect additional buffers to drive a long wire line (e.g., for improving high-Vdd performance); and/or disconnect additional buffers to drive a long wire line (e.g., for improving low-Vdd power/performance).

[0052] In some embodiments, if the reconfigurable interconnect using MIT or MEMS is needed by design teams before the availability of MIT or MEMS process options, the configuration can be provided by use of a via-option processing mask to enable to designs that are substantially the same to be optimized for different market segments. This near-term

approach with vias may allow for fabrication time configuration, in accordance with some embodiments.

[0053] **Fig. 4** illustrates cross-sectional view 400 of a configurable interconnect which is configurable via application of an electric field, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 4** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0054] In some embodiments, configurable interconnect comprises first interconnect 401a, second interconnect 401b, metal wires 402a/b and 403a/b, transistors MP1 and MP2, and MIT vias 404a/b. In some embodiments, MIT vias 404a/b are made of the same material as those described with reference to MIT vias 202a/b. In some embodiments, metal wires 402a/b and 403a/b are orthogonal to MIT vias 404a/b. In some embodiments, metal wires 403a/b are coupled to ground (Vss). In some embodiments, metal wires 402a/b are coupled to transistors MP1 and MP2, respectively. In some embodiments, first interconnect 401a extends parallel to second interconnect 401b. In some embodiments, metal wires 402a/b and 403a/b are orthogonal to first and second interconnects 401a/b. In this example, first interconnect 401a is on metal layer 5 (M5), second interconnect 401b is on metal layer 7 (M7) while metal wires 402a/b and 403a/b are on metal layer 6 (M6). In other embodiments, other metal layers can be used.

[0055] In some embodiments, transistors MP1 and MP2 are operable to turn on by pulsed signals HP. In some embodiments, the drain terminals of transistors MP1 and MP2 are coupled to wires 402a/b, respectively. In some embodiments, the source terminal of transistors MP1 and MP2 are coupled to Vdd. In some embodiments, the gate terminals of transistors MP1 and MP2 are coupled to HP. Here, reference to signals and nodes are interchangeably used. For example, HP may refer to signal HP or node HP depending on the context of the sentence.

[0056] In some embodiments, when transistors MP1 and MP2 are turned on, electric field is formed between metal wires 402a and 403a, and between metal wires 402b and 403b. In some embodiments, the metal wires 402a/b and 403a/b are positioned so that the electric field passes through and/or around MIT vias 404a/b. This electric field causes MIT vias 404a and 404b to transition from being an insulator to being a metal. In some embodiments, in the absence of the electric field, MIT vias 404a and 404b to transition from being metals to being insulators.

[0057] In some embodiments, the pulse width of HP is adjustable or programmable (e.g., by firmware, software, and/or hardware). In some embodiments, the duration of the pulse width of HP is according to a power mode. For example, during high power mode (e.g., Turbo mode) the pulse duration is as long as the power mode duration. As such, interconnects 401a and 401b are electrically coupled to provide lower resistance and faster signal propagation during high power mode. In some embodiments, during low power mode, the HP is kept logical high as long as the duration of the low power mode. As such, interconnects 401a and 401b are electrically decoupled from one another in such a mode.

[0058] While the embodiment of Fig. 4 is illustrated with reference to p-type transistors MP1 and MP2, the p-type transistors can be replaced with n-type transistors. In some embodiments, instead of coupling the transistors to Vdd (as shown with reference to transistors MP1 and MP2), the transistors (e.g., n-type transistors) can be coupled to ground. In one such embodiment, metal wires 403a/b are coupled to Vdd instead of ground. As such, a complementary version of the embodiment of Fig. 4 can be derived.

[0059] Fig. 5 illustrates cross-sectional view 500 of a configurable interconnect which is configurable via application of current flow, in accordance with some embodiments of the disclosure. It is pointed out that those elements of Fig. 5 having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0060] In some embodiments, configurable interconnect comprises first interconnect 501a (e.g., like 401a), second interconnect 501b (e.g., like 401b), and transistors MP1 and MN1, and MIT via 504a (e.g., 404a). In some embodiments, the drain terminal of transistor MP1 is coupled to second interconnect 501b. In some embodiments, the gate terminal of transistor MP1 is coupled to HP. In some embodiments, the source terminal of p-type transistor MP1 is coupled to Vdd. In some embodiments, the drain terminal of n-type transistor MN1 is coupled to first interconnect 501a. In some embodiments, the gate terminal of transistor MN1 is coupled to HP_b (where HP_b is an inverse of HP). In some embodiments, the source terminal of transistor MN1 is coupled to Vss.

[0061] In some embodiments, when HP is logical low (i.e., when HP_b is logical high), transistors MP1 and MN1 are turned on. As such, a current path from Vdd to ground can be formed if MIT via 504a becomes conductive (i.e., transitions from insulator to metal). In some

embodiments, by turning on transistors MP1 and MN1, MIT via 504a transitions to from being an insulator to a metal. As such, first and second interconnects 501a/b are electrically coupled. In some embodiments, HP (and HP_b) are pulsed signals with pulse durations long enough to cause MIT via 504a to transition from insulator to metal. In some embodiments, as soon as MIT via 504a becomes a metal, HP and HP_b cause transistors MP1 and MN1 to turn off. During that state, signal routed on first interconnect 501a is also routed to second interconnect 501b.

[0062] In some cases, overtime, MIT via 504a transitions back to being an insulator from metal. In some embodiments, just before the transition in MIT via 504a takes place, transistors MP1 and MN1 are turned on again to maintain metal characteristics of MIT via 504a. This process may be akin to a refresh operation. In some embodiments, depending on the architecture that uses first and second interconnects 501a/b, HP and HP_b are provided as pulsed signals again to transistors MP1 and MN1 to refresh the metal characteristics of MIT via 504a.

[0063] In some embodiments, the pulsed signals HP and HP_b are provided during high power mode (e.g., Turbo mode) when both interconnects are needed for signal transmission (or propagation). In some embodiments, during low power mode, when signal propagation is through one interconnect, then transistors MP1 and MN1 are kept turned off.

[0064] **Fig. 6A** illustrates schematic 600 with configurable interconnects which are configured to bypass a buffer, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 6A** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0065] In some embodiments, schematic 600 comprises buffers 601, 602, 603, and 604, interconnects 607a, 607b, 607c, and 607d, and 607e, and MIT or MEMS vias 605a, 605b, 606a, and 606b. In some embodiments, 605a, 605b, 606a, and 606b are CMOS multiplexers or transmission gates. While the embodiments are explained with reference to either bypassing buffers 603 and 604, or adding those buffers in the signal propagation path, the concept can be used for any circuit topology with different use cases.

[0066] In some embodiments, dynamic reconfiguration is achieved by using MITs or MEMS vias or CMOS transmission gates 605a, 605b, 606a, and 606b which can be made conductor-like metal (or low resistance or short) or insulator-like dielectric (or high resistance or open) depending on different product targets. In some embodiments, dynamic reconfiguration is

achieved by using schemes of alternate sub-circuits selected to operate depending on the supply voltage mode.

[0067] In some embodiments, during low voltage operation, buffers 603 and 604 can be bypassed to reduce power, in accordance with some embodiments. For example, MIT vias 605a and 605b are configured as insulators using any of the schemes discussed with reference to various embodiments (e.g., by changing temperature, pressure, providing electric field, and/or providing pulsed current flow) while MIT vias 606a and 606b are configured as metals. As such, during low performance, signals bypass buffers 603 and 604.

[0068] In some embodiments, at low voltage, interconnect is reconfigured to have long spacing between buffers 601 and 602 for high performance/watt and performance at low voltage. The long spacing or long path is provided by interconnects 607a, 607d, and 607e. For example, at low voltage it may be best to size wires to minimize wire capacitance. In some embodiments, at high-voltage, interconnect is reconfigured to have short spacing between buffers for high performance at high voltage. The short spacing or short path is provided by interconnects 607a, 607b, 607c and 607e. For example, at high voltage it may be best to size wires to minimize resistance.

[0069] Here, **Fig. 6A** illustrates the case where MIT vias 606a and 606b are configured as metal while MIT vias 605a and 605b are configured as insulators. **Fig. 6B** illustrates schematic 620 with configurable interconnects which are configured to incorporate buffers 603 and 604 at higher supply voltages, in accordance with some embodiments of the disclosure.

[0070] In some embodiments, buffers 603 and 604 may be added to drive interconnects 607e during high voltage operation. For example, MIT vias 605a and 605b are configured as metals using any of the schemes discussed with reference to the various embodiments (e.g., by changing temperature, pressure, providing electric field, and/or providing pulsed current flow) while MIT vias 606a and 606b are configured as insulators. As such, during high performance (e.g., Turbo mode), signals are buffered via buffers 603 and 604.

[0071] **Fig. 7** illustrates top view 700 of a MEMS or NEMS based configurable interconnect based network, in accordance with some embodiments of the disclosure. It is pointed out that those elements of **Fig. 7** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such. **Fig. 7** is described with reference to **Figs. 6A-B**.

[0072] In some embodiments, the arrangement of interconnects and MEMS/NEMS of top view 700 comprises MEMS strips 701a and 701b, metal interconnects (e.g., Cu, Al, and the like) 702, 703, 704, 705, 706a/b, 707, 708, and 709. In some embodiments, interconnect 702 is the same interconnect as 607d. As such, when MEMS 701a/b electrically couple to interconnect 702, buffers 603 and 604 are bypassed.

[0073] MEMS strips 701a and 701b are also referred to as micro-machine or micro system technology (MST). Any suitable material can be used for fabricating MEMS strips 701a/b. For example, gold, nickel, aluminum, copper, chromium, titanium, tungsten, platinum, silver, nitrides of silicon, aluminum and titanium as well as silicon carbide and other ceramics can be used for forming MEMS strips 701a/b.

[0074] In some embodiments, interconnect 703 is a selector which is used to control MEMs 701a/b. In some embodiments, interconnect 707 is a selector_b which is used to control MEMs 701a/b, where selector_b is an inverse of selector. For example, when selector interconnect 703 is biased by a high voltage (e.g., Vdd), selector_b interconnect 707 is biased at a low voltage (e.g., ground). In some embodiments, when selector is biased at a high voltage, then MEMs 701a/b bends in one direction as described with reference to **Figs. 8A-C**.

[0075] Referring back to **Fig. 7**, in some embodiments, input is received by interconnect 704. In some embodiments, interconnect 704 is coupled to interconnect 706a which in turn is coupled to MEMS strip 701a. In some embodiments, interconnect 705 is connected to an output. In some embodiments, interconnect 705 is coupled to interconnect 706b which in turn is coupled to MEMS strip 701b. In some embodiments, interconnect 708 is coupled to the input of buffer 603. In some embodiments, interconnect 709 is coupled to the output of buffer 604.

[0076] **Figs. 8A-C** illustrate cross-sections along dashed line BB of **Fig. 7**, in accordance with some embodiments. It is pointed out that those elements of **Figs. 8A-C** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0077] **Fig. 8A** illustrates cross-section 800 along the dashed line BB (of **Fig. 7**) of part of the network of the MEMS based configurable interconnect, in accordance with some embodiments of the disclosure. **Fig. 8B** illustrates cross-section 820 along dashed line BB (of **Fig. 7**) of part of the network of the MEMS based configurable interconnect in a first configuration, in accordance with some embodiments of the disclosure. In this configuration,

selector interconnect 703 is biased at a high voltage while selector_b interconnect 707 is biased at a low voltage (e.g., ground). As such, MEMS strip 701a bends towards interconnect 702 and electrically couples to it. The same also occurs to MEMS strip 701b. As such, buffers 603 and 604 are bypassed (e.g., interconnect 607a electrically couples to interconnect 607d and interconnect 607d electrically couples to interconnect 607e).

[0078] **Fig. 8C** illustrates cross-section 830 along the dashed line BB (of **Fig. 7**) of part of the network of the MEMS based configurable interconnect in a second configuration, in accordance with some embodiments of the disclosure. In this configuration, selector_b interconnect 707 is biased at a high voltage while selector interconnect 703 is biased at a low voltage (e.g., ground). As such, MEMS strip 701a bends towards interconnect 708 and electrically couples to it. The same also occurs to MEMS strip 701b. As such, buffers 603 and 604 are included (e.g., interconnect 607a electrically couples to interconnect 607b and interconnect 607c electrically couples to interconnect 607e).

[0079] **Fig. 9** illustrates flowchart 900 of a method for configuring resistivity and/or capacitance of a configurable interconnect using electric field, in accordance with some embodiments of the disclosure. Flowchart 900 is described with reference to **Fig. 4**. It is pointed out that those elements of **Fig. 9** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0080] Although the blocks in the flowchart with reference to **Fig. 9** are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/blocks may be performed in parallel. Some of the blocks and/or operations listed in **Fig. 9** are optional in accordance with certain embodiments. The numbering of the blocks presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur. Additionally, operations from the various flows may be utilized in a variety of combinations.

[0081] At block 901, a first electric field is applied across first MIT via 404a. For example, HP pulse is applied which turns on transistor MP1 which in turn charges wire 402a. The charged wire 402a causes electric field to be generated around MIT via 404a. As such, the resistance of MIT via 404a is changed from high to low resistance or open circuit to short circuit. At block 902, first interconnect 401a is electrically coupled to second interconnect 401b via first

MIT via 404a in response to the applied electric field. At block 903, a second electric field is applied across second MIT via 404b. For example, HP pulse is applied which turns on transistor MP2 which in turn charges wire 402b. The charged wire 402b causes electric field to be generated around MIT via 404b. At block 904, first interconnect 401a is electrically coupled to third interconnect 401b via second MIT via 404b in response to the applied electric field. In some embodiments, when transistors MP1 and MP2 are turned off, the electric field is removed and so first interconnect 401a is electrically de-coupled from second interconnect 401b.

[0082] **Fig. 10** illustrates flowchart 1000 of a method for configuring resistivity and/or capacitance of a configurable interconnect using change in temperature, in accordance with some embodiments of the disclosure. Flowchart 1000 is described with reference to **Figs. 2A-B**. It is pointed out that those elements of **Fig. 10** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0083] Although the blocks in the flowchart with reference to **Fig. 10** are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/blocks may be performed in parallel. Some of the blocks and/or operations listed in **Fig. 10** are optional in accordance with certain embodiments. The numbering of the blocks presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur. Additionally, operations from the various flows may be utilized in a variety of combinations.

[0084] At block 1001, temperature is increased. As such, temperature of first and second MIT vias 202a/b rises above a threshold (e.g., 75°C). At block 1002, first interconnect 201a is electrically coupled to third interconnect 203a via first MIT via 202a in response to increasing the temperature. At block 1003, second interconnect 201b is electrically coupled to third interconnect 203a via second MIT via 202b in response to increasing the temperature.

[0085] At block 1004, temperature is decreased below the threshold. As such, temperature of first and second MIT vias falls below the threshold (e.g., 75°C). At block 1005, first interconnect 201a is electrically de-coupled from third interconnect 203a via first MIT via 202a in response to decreasing the temperature, and second interconnect 201b is electrically uncoupled from third interconnect 203a via second MIT via 202b in response to decreasing the temperature.

[0086] In some embodiments, configurable interconnects may be enabled by a single configuration layer. For example, configurable via 7 may enable configuration of signals routed predominantly in the metal layer 8 (M8). In some embodiments a single configuration layer may enable configuration of signals routed in two or more metal layers. For example, a configurable via 7 may enable configuration of M8 routes or metal layer 7 (M7) routes. This may be useful to allow configuration of layers routed in orthogonal directions with a single configuration layer. In some embodiments, multiple configuration layers can enable configuration of more metal layers. For example, configuration of metal layer 10 (M10) can enable RC (time constant) and repeater optimization of global signals. In another example, configuration of metal layer 3 (M3) may enable RC/buffer optimization of both local and global signals by enabling efficient configurable buffer insertion.

[0087] In some embodiments, configuration of the via can occur after completion of most of the manufacturing steps but before sale to a customer in order to configure the die with a particular application. In some embodiments, the configuration is performed based upon the die power and/or performance and yield metrics measured during a testing process. For example, higher performance die may be binned for high-voltage applications and be configured to exhibit even higher performance at high voltage. In some embodiments, the MIT material of 504a can be replaced with a fuse.

[0088] In some embodiments, passing a high current through transistors MP1, MN1, and MIT via 504a transforms MIT via 504a to a high resistance via. This may enable the low-power/low-voltage products. Otherwise, the high resistance via transformation may enable a high-voltage/high-performance product. In some other embodiments, passing a high current through transistors MP1 and MN1 and MIT via 504a transforms MIT via 504a to a low resistance. This may enable the high-performance/high-voltage products. Fuse material can be SiO₂, a high-K oxide material, copper or metal wires, in accordance with various embodiments.

[0089] **Fig. 11** illustrates a smart device or a computer system or a System-on-Chip (SoC) 1600 with one or more configurable interconnects, according to some embodiments. It is pointed out that those elements of **Fig. 11** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0090] Fig. 11 illustrates a block diagram of an embodiment of a mobile device in which flat surface interface connectors could be used. In some embodiments, computing device 1600 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-phone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain components are shown generally, and not all components of such a device are shown in computing device 1600.

[0091] In some embodiments, computing device 1600 includes a first processor 1610 with one or more configurable interconnects, according to some embodiments discussed. Other blocks of the computing device 1600 may also include one or more configurable interconnects, according to some embodiments. The various embodiments of the present disclosure may also comprise a network interface within 1670 such as a wireless interface so that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant.

[0092] In one embodiment, processor 1610 (and/or processor 1690) can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 1610 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting the computing device 1600 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0093] In one embodiment, computing device 1600 includes audio subsystem 1620, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. In some embodiments, audio subsystem 1620 includes apparatus and/or machine executable instructions to avoid self-hearing, according to some embodiments. Devices for such functions can be integrated into computing device 1600, or connected to the computing device 1600. In one embodiment, a user interacts with the computing device 1600 by providing audio commands that are received and processed by processor 1610.

[0094] Display subsystem 1630 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device 1600. Display subsystem 1630 includes display interface 1632, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1632 includes logic separate from processor 1610 to perform at least some processing related to the display. In one embodiment, display subsystem 1630 includes a touch screen (or touch pad) device that provides both output and input to a user.

[0095] I/O controller 1640 represents hardware devices and software components related to interaction with a user. I/O controller 1640 is operable to manage hardware that is part of audio subsystem 1620 and/or display subsystem 1630. Additionally, I/O controller 1640 illustrates a connection point for additional devices that connect to computing device 1600 through which a user might interact with the system. For example, devices that can be attached to the computing device 1600 might include microphone devices, speaker or stereo systems, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0096] As mentioned above, I/O controller 1640 can interact with audio subsystem 1620 and/or display subsystem 1630. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the computing device 1600. Additionally, audio output can be provided instead of, or in addition to display output. In another example, if display subsystem 1630 includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 1640. There can also be additional buttons or switches on the computing device 1600 to provide I/O functions managed by I/O controller 1640.

[0097] In one embodiment, I/O controller 1640 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in the computing device 1600. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0098] In one embodiment, computing device 1600 includes power management 1650 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 1660 includes memory devices for storing information in

computing device 1600. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory subsystem 1660 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of the computing device 1600.

[0099] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 1660) for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium (e.g., memory 1660) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[00100] Connectivity 1670 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable the computing device 1600 to communicate with external devices. The computing device 1600 could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[00101] Connectivity 1670 can include multiple different types of connectivity. To generalize, the computing device 1600 is illustrated with cellular connectivity 1672 and wireless connectivity 1674. Cellular connectivity 1672 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity (or wireless interface) 1674 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication.

[00102] Peripheral connections 1680 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that the computing device 1600 could be a peripheral device ("to" 1682) to other computing devices, as well as have peripheral devices ("from" 1684) connected to it. The computing device 1600 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on computing device 1600. Additionally, a docking connector can allow computing device 1600 to connect to certain peripherals that allow the computing device 1600 to control content output, for example, to audiovisual or other systems.

[00103] In addition to a proprietary docking connector or other proprietary connection hardware, the computing device 1600 can make peripheral connections 1680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

[00104] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[00105] Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[00106] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. For example, other memory architectures e.g., Dynamic RAM (DRAM) may use the embodiments discussed. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[00107] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[00108] The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

[00109] For example, an apparatus is provided which comprises: a first interconnect; a second interconnect; a third interconnect; a first via comprising a metal-insulator-transition (MIT) material, wherein the first via is to couple the first interconnect to the third interconnect; and a second via comprising MIT material, wherein the second via is to couple the second interconnect to the third interconnect. In some embodiments, the MIT material comprises a material selected from a group consisting of: VO_2 , V_xO_y , Fe_3O_4 , FeS , Ti_xO_y , TiS_2 , LaCoO_3 , SmNiO_3 , and EuO .

[00110] In some embodiments, the selected material further comprises trace dopant or other impurity species. In some embodiments, the first, second, and third interconnects comprise a material selected from a group consisting of: Cu and Al. In some embodiments, the selected material further comprises a dopant, alloying material, or other impurity species. In some

embodiments, the apparatus comprises: a fourth interconnect; a fifth interconnect coupled to ground, wherein the fourth and fifth interconnects are disposed on either sides of the first via; and a transistor coupled to the fourth interconnect.

[00111] In some embodiments, the fourth and fifth interconnects are formed on the same metal layer. In some embodiments, the transistor is operable to apply an electric field to the first via. In some embodiments, the apparatus comprises: a first transistor coupled to the first interconnect and ground; and a second transistor coupled to the third interconnect and a supply node. In some embodiments, the apparatus comprises: a pulse generator to apply: a first pulse to the first transistor; and a second pulse to the second transistor. In some embodiments, the first and second vias are operable to electrically couple the first and second interconnects to the third interconnect when a temperature rises above a threshold.

[00112] In another example, a memory; a processor coupled to the memory, the processor having an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[00113] In another example, an apparatus is provided which comprises: first and second nano-electrical-mechanical system (NEMS) strips; an input interconnect adjacent to the first NEMS strip; an output interconnect adjacent to the second NEMS strip; a first interconnect positioned next to a first end of the first and second NEMS strips; a second interconnect positioned next to a second end of the first NEMS strip; and a third interconnect positioned next to a second end of the second NEMS strip. In some embodiments, the apparatus comprises a circuitry including: an input coupled to the second interconnect; and an output coupled to the third interconnect. In some embodiments, the circuitry is a buffer. In some embodiments, the apparatus comprises fourth and fifth interconnects positioned next to the first and second NEMS strips.

[00114] In another example, a memory; a processor coupled to the memory, the processor having an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[00115] In another example, a method is provided which comprises: applying a first electric field across a first via which comprises a metal-insulator-transition (MIT) material; and coupling a first interconnect to a third interconnect via the first via in response to applying the first electric field. In some embodiments, the method comprises: applying a second electric field

across a second via which comprises a MIT material; and coupling a second interconnect to the third interconnect via the second via in response to applying the second electric field.

[00116] In some embodiments, applying the first and second electric fields comprises applying a same electric field across the first and second vias. In some embodiments, the MIT material comprises a material selected from a group consisting of: VO_2 , V_xO_y , Fe_3O_4 , FeS , Ti_xO_y , TiS_2 , LaCoO_3 , SmNiO_3 , and EuO . In some embodiments, the selected material further comprises trace dopant or other impurity species. In some embodiments, the first, second, and third interconnects comprise a material selected from a group consisting of: Cu and Al . In some embodiments, the material further comprises: a dopant, alloying material, or other impurity species.

[00117] In another example, a method is provided which comprises: increasing temperature of first and second vias above a threshold, the first and second vias formed of metal-insulator-transition (MIT) material; coupling a first interconnect to a third interconnect via the first via in response to increasing the temperature; and coupling a second interconnect to the third interconnect via the second via in response to increasing the temperature.

[00118] In some embodiments, the method comprises: decreasing the temperature of the first and second vias below the threshold; electrically uncoupling the first interconnect from the third interconnect via the first via in response to decreasing the temperature; and electrically uncoupling the second interconnect from the third interconnect via the second via in response to decreasing the temperature. In some embodiments, the MIT material comprises a material selected from a group consisting of: VO_2 , V_xO_y , Fe_3O_4 , FeS , Ti_xO_y , TiS_2 , LaCoO_3 , SmNiO_3 , and EuO . In some embodiments, the selected material further comprises trace dopant or other impurity species. In some embodiments, the first, second, and third interconnects comprise a material selected from a group consisting of Cu or Al . In some embodiments, the material further comprises a dopant, alloying material, or other impurity species.

[00119] In another example, an apparatus is provided which comprises: means for increasing temperature of first and second vias above a threshold, the first and second vias formed of metal-insulator-transition (MIT) material; means for coupling a first interconnect to a third interconnect via the first via in response to increasing the temperature; and means for coupling a second interconnect to the third interconnect via the second via in response to increasing the temperature. In some embodiments, the apparatus comprises: means for

decreasing the temperature of the first and second vias below the threshold; means for electrically uncoupling the first interconnect from the third interconnect via the first via in response to decreasing the temperature; and means for electrically uncoupling the second interconnect from the third interconnect via the second via in response to decreasing the temperature.

[00120] In some embodiments, the MIT material comprises a material selected from a group consisting of: VO_2 , V_xO_y , Fe_3O_4 , FeS , Ti_xO_y , TiS_2 , LaCoO_3 , SmNiO_3 , and EuO . In some embodiments, the selected material further comprises trace dopant or other impurity species. In some embodiments, the first, second, and third interconnects comprise a material selected from a group consisting of: Cu and Al . In some embodiments, the material further comprises a dopant, alloying material, or other impurity species.

[00121] In another example, a memory; a processor coupled to the memory, the processor having an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[00122] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:
 - a first interconnect;
 - a second interconnect;
 - a third interconnect;
 - a first via comprising a metal-insulator-transition (MIT) material, wherein the first via is to couple the first interconnect to the third interconnect; and
 - a second via comprising MIT material, wherein the second via is to couple the second interconnect to the third interconnect.
2. The apparatus of claim 1, wherein the MIT material comprises a material selected from a group consisting of: VO_2 , V_xO_y , Fe_3O_4 , FeS , Ti_xO_y , TiS_2 , LaCoO_3 , SmNiO_3 , and EuO .
3. The apparatus of claim 2, wherein the selected material further comprises trace dopant or other impurity species.
4. The apparatus of claim 1, wherein the first, second, and third interconnects comprise a material selected from a group consisting of: Cu and Al.
5. The apparatus of claim 4, wherein the selected material further comprises a dopant, alloying material, or other impurity species.
6. The apparatus of claim 1 comprises:
 - a fourth interconnect;
 - a fifth interconnect coupled to ground, wherein the fourth and fifth interconnects are disposed on either sides of the first via; and
 - a transistor coupled to the fourth interconnect.
7. The apparatus of claim 6, wherein the fourth and fifth interconnects are formed on the same metal layer.

8. The apparatus of claim 6, wherein the transistor is operable to apply an electric field to the first via.
9. The apparatus of claim 1 comprises:
 - a first transistor coupled to the first interconnect and ground; and
 - a second transistor coupled to the third interconnect and a supply node.
10. The apparatus of claim 9 comprises a pulse generator to apply:
 - a first pulse to the first transistor; and
 - a second pulse to the second transistor.
11. The apparatus of claim 1, wherein the first and second vias are operable to electrically couple the first and second interconnects to the third interconnect when a temperature rises above a threshold.
12. An apparatus comprising:
 - first and second nano-electrical-mechanical system (NEMS) strips;
 - an input interconnect adjacent to the first NEMS strip;
 - an output interconnect adjacent to the second NEMS strip;
 - a first interconnect positioned next to a first end of the first and second NEMS strips;
 - a second interconnect positioned next to a second end of the first NEMS strip; and
 - a third interconnect positioned next to a second end of the second NEMS strip.
13. The apparatus of claim 12 comprises a circuitry including:
 - an input coupled to the second interconnect; and
 - an output coupled to the third interconnect.
14. The apparatus of claim 13, wherein the circuitry is a buffer.

15. The apparatus of claim 12 comprises fourth and fifth interconnects positioned next to the first and second NEMS strips.
16. A method comprising:
 - applying a first electric field across a first via which comprises a metal-insulator-transition (MIT) material; and
 - coupling a first interconnect to a third interconnect via the first via in response to applying the first electric field.
17. The method of claim 16 comprises:
 - applying a second electric field across a second via which comprises a MIT material; and
 - coupling a second interconnect to the third interconnect via the second via in response to applying the second electric field.
18. The method of claim 17, wherein applying the first and second electric fields comprises applying a same electric field across the first and second vias.
19. The method of claim 17, wherein the MIT material comprises a material selected from a group consisting of: VO_2 , V_xO_y , Fe_3O_4 , FeS , Ti_xO_y , TiS_2 , LaCoO_3 , SmNiO_3 , and EuO .
20. The method of claim 19, wherein the selected material further comprises trace dopant or other impurity species.
21. The method of claim 18, wherein the first, second, and third interconnects comprise a material selected from a group consisting of: Cu and Al.
22. The method of claim 21, wherein the material further comprises: a dopant, alloying material, or other impurity species.
23. A system comprising:
 - a memory;

a processor coupled to the memory, the processor having an apparatus according to any one of apparatus claims 1 to 11; and

a wireless interface for allowing the processor to communicate with another device.

24. A system comprising:

a memory;

a processor coupled to the memory, the processor having an apparatus according to any one of apparatus claims 12 to 15; and

a wireless interface for allowing the processor to communicate with another device.

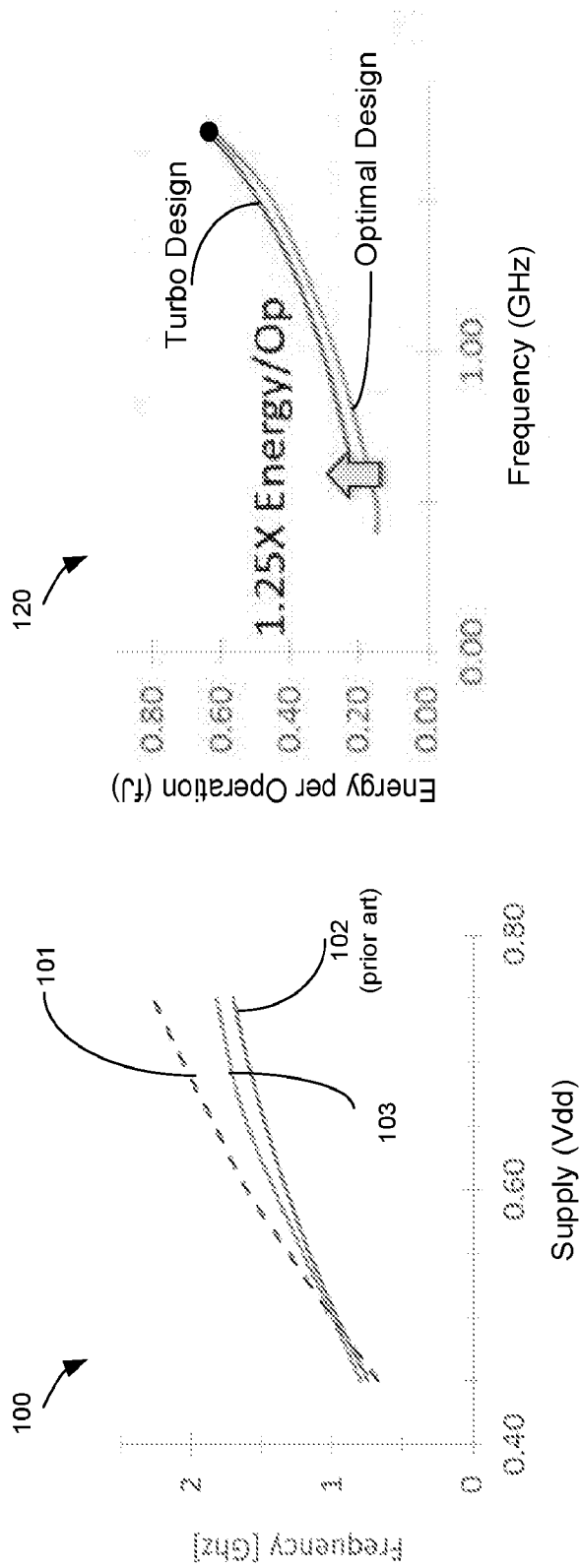


Fig. 1B

Fig. 1A

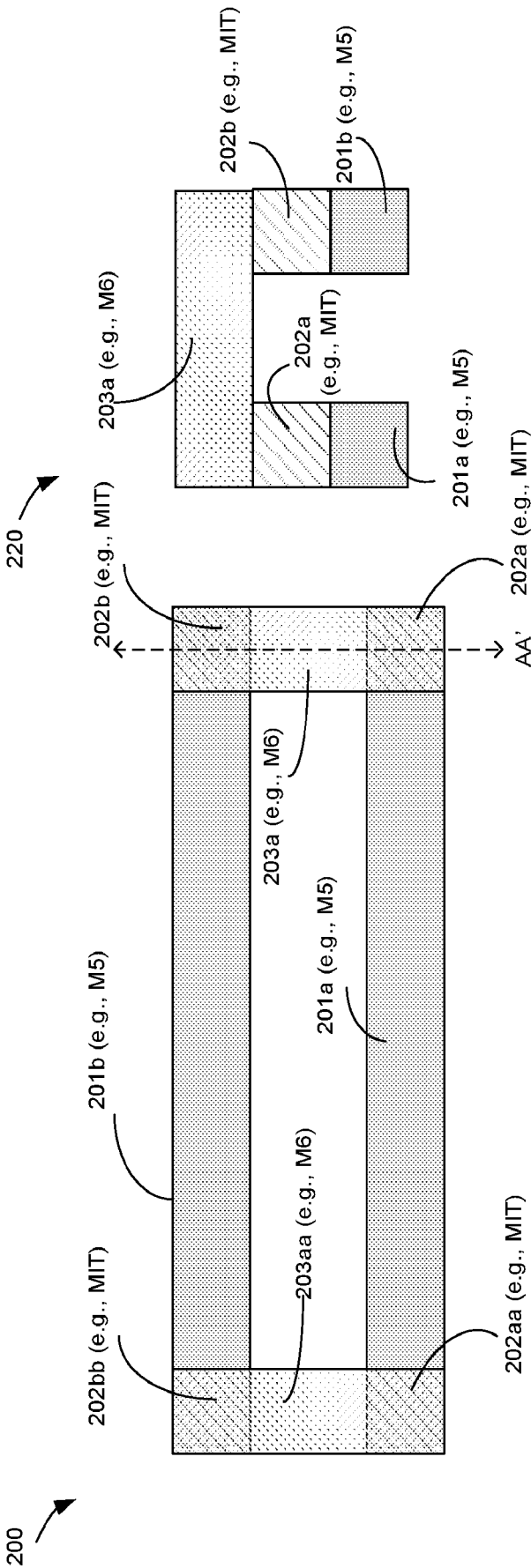
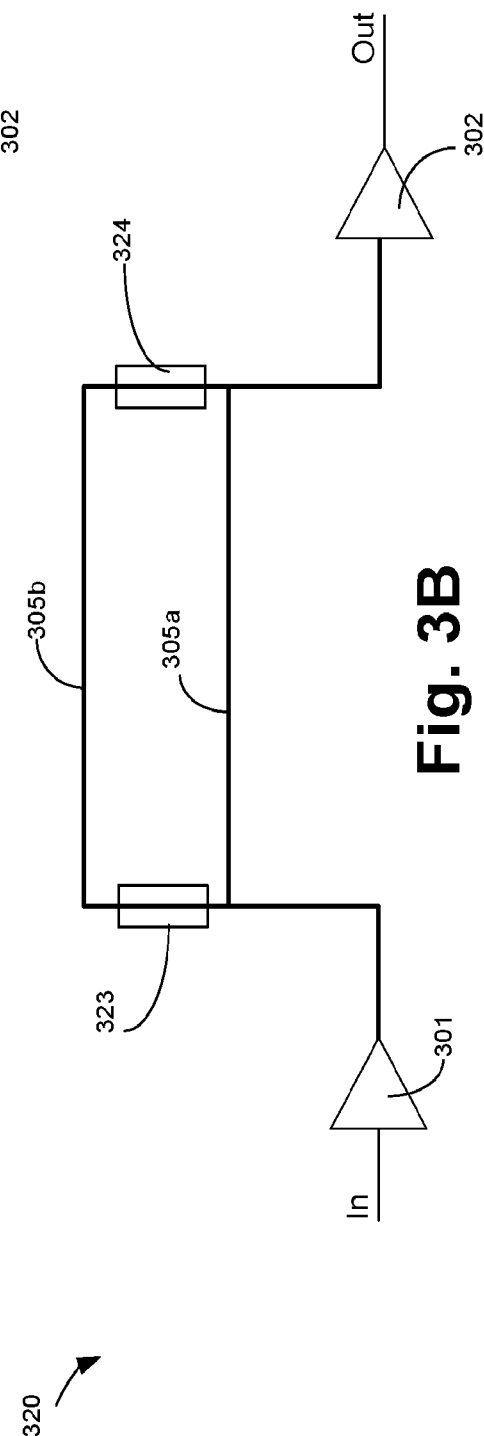
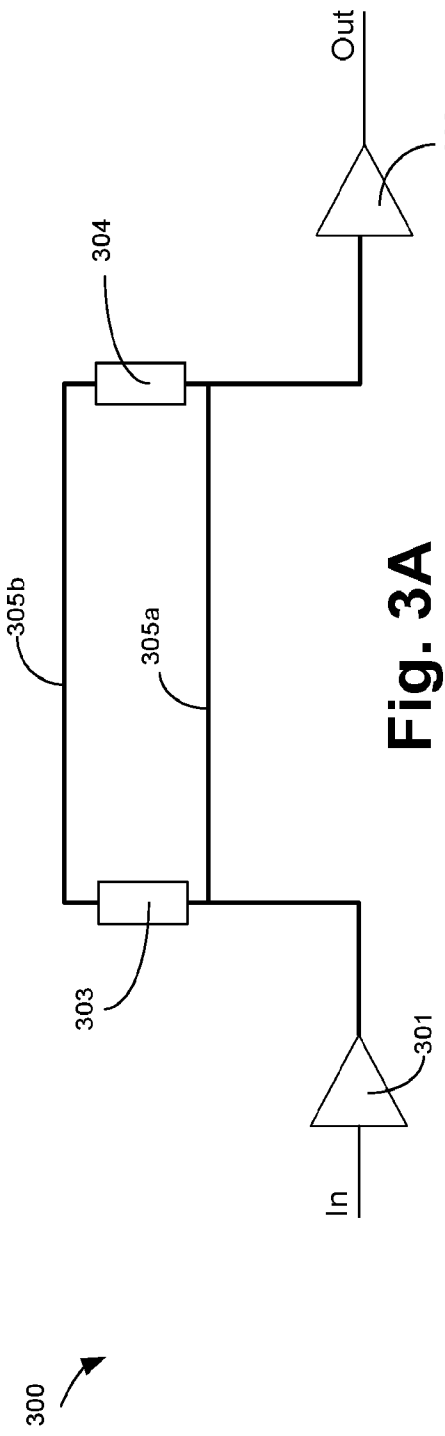


Fig. 2B

Fig. 2A



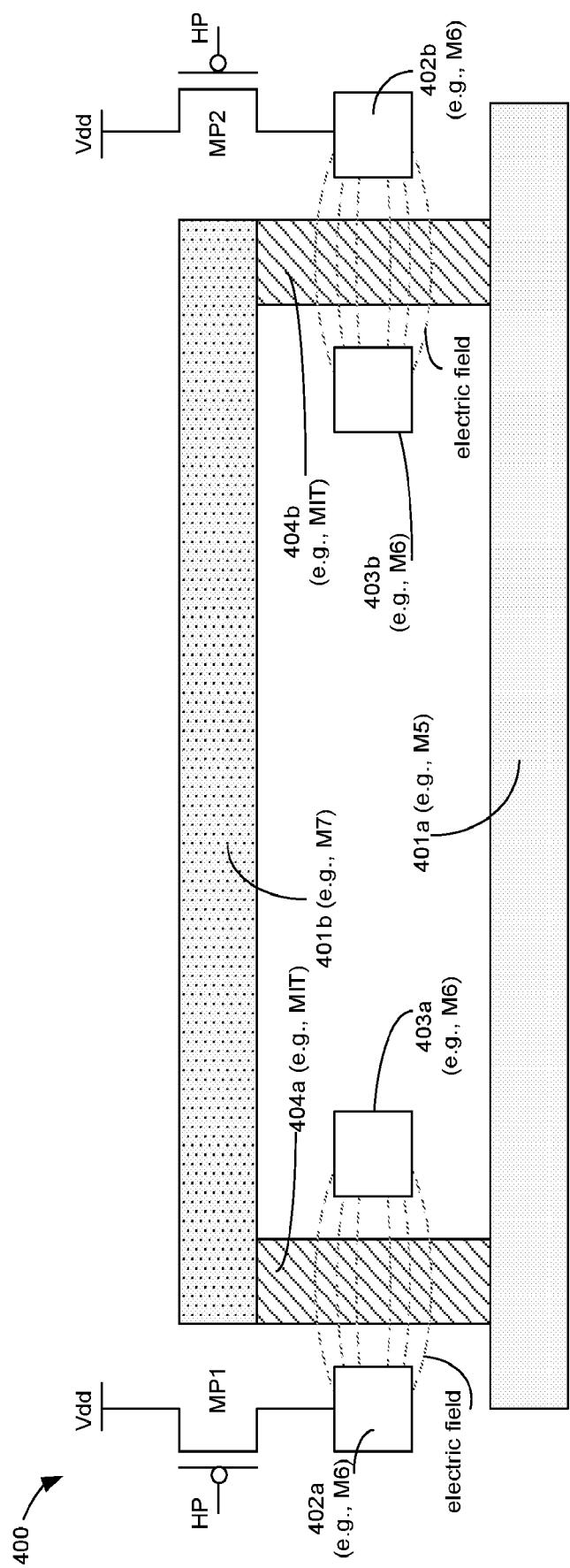


Fig. 4

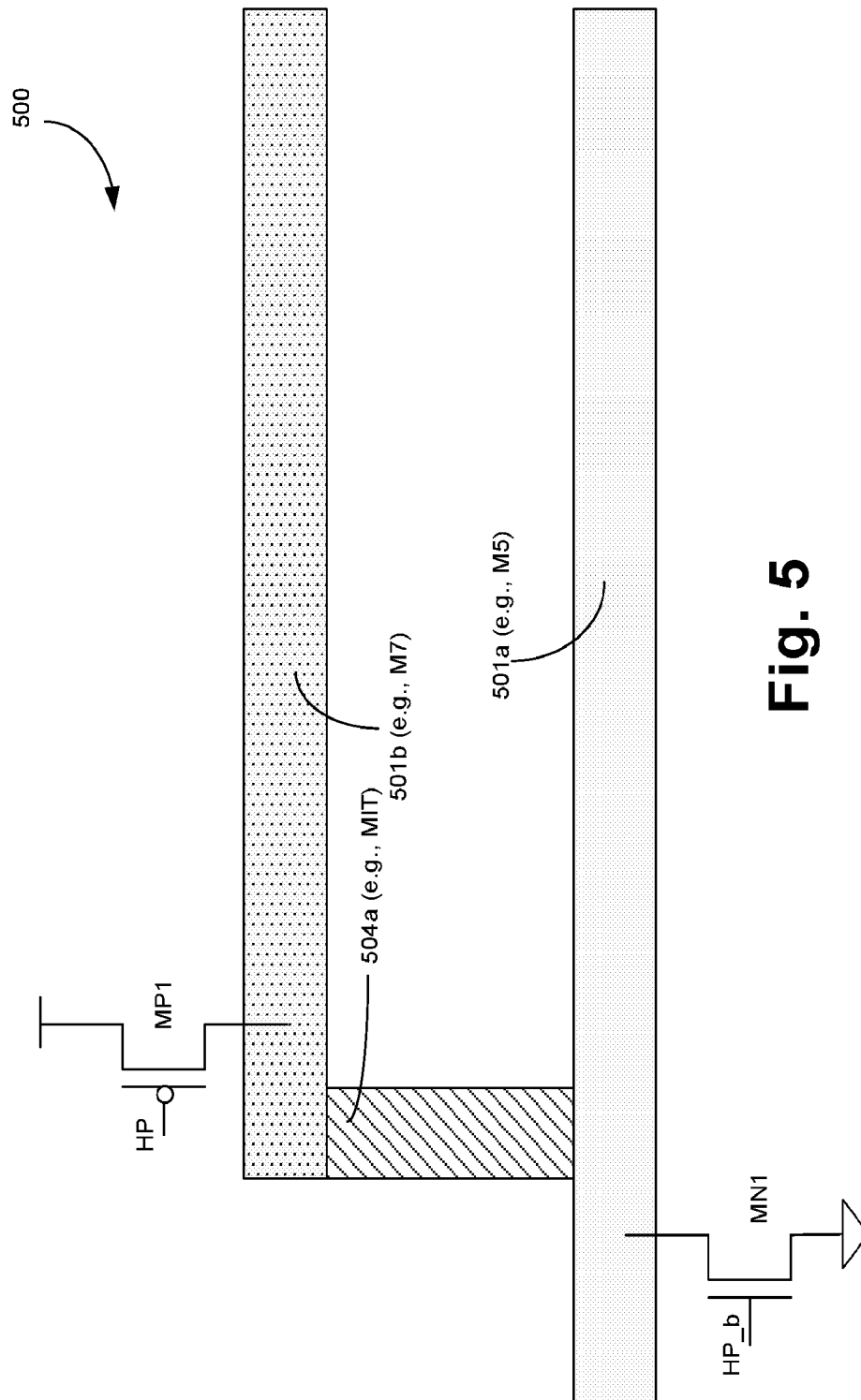
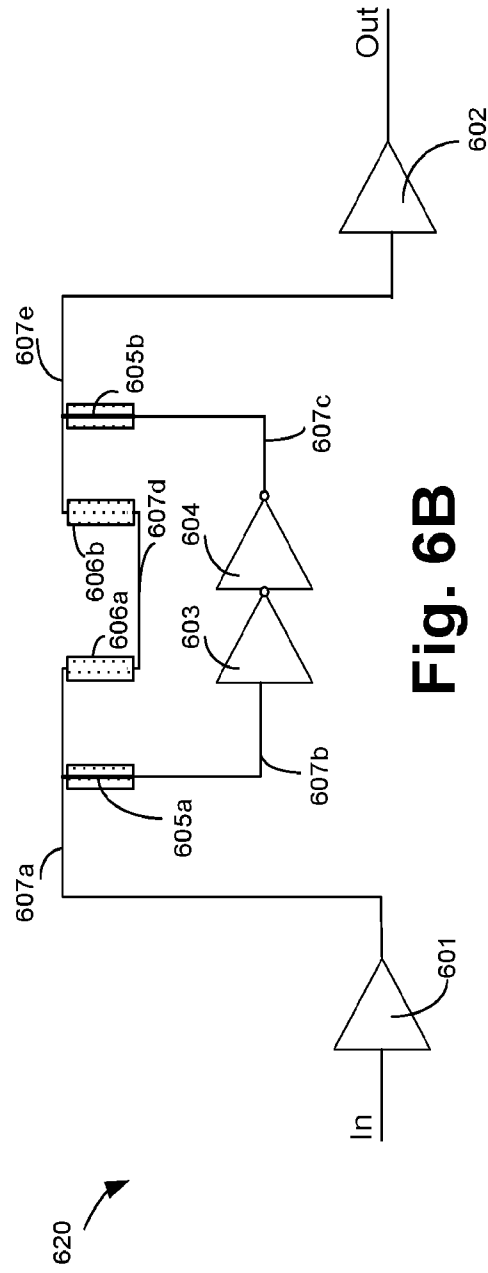
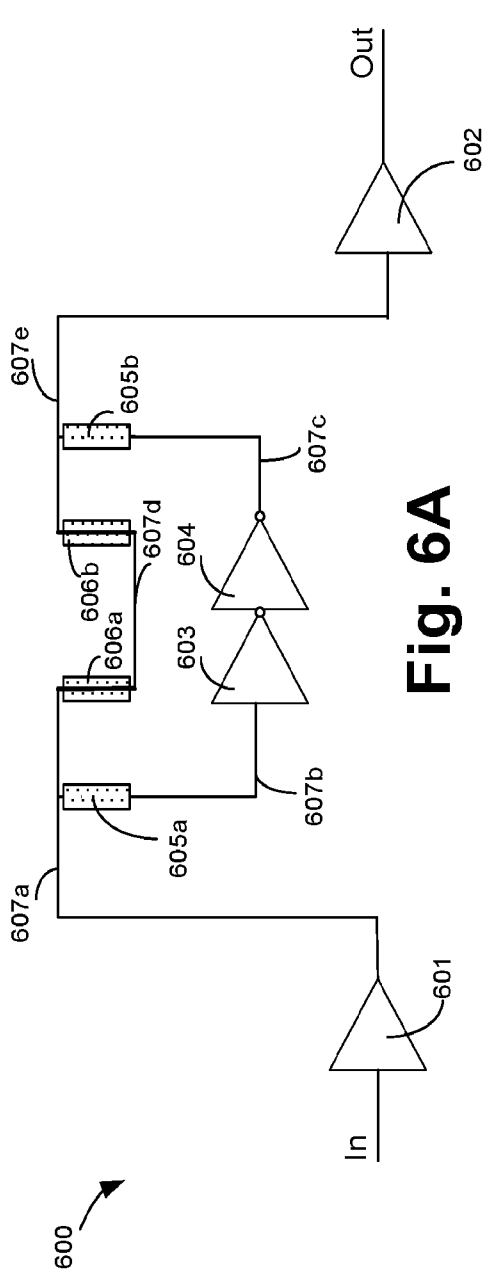


Fig. 5



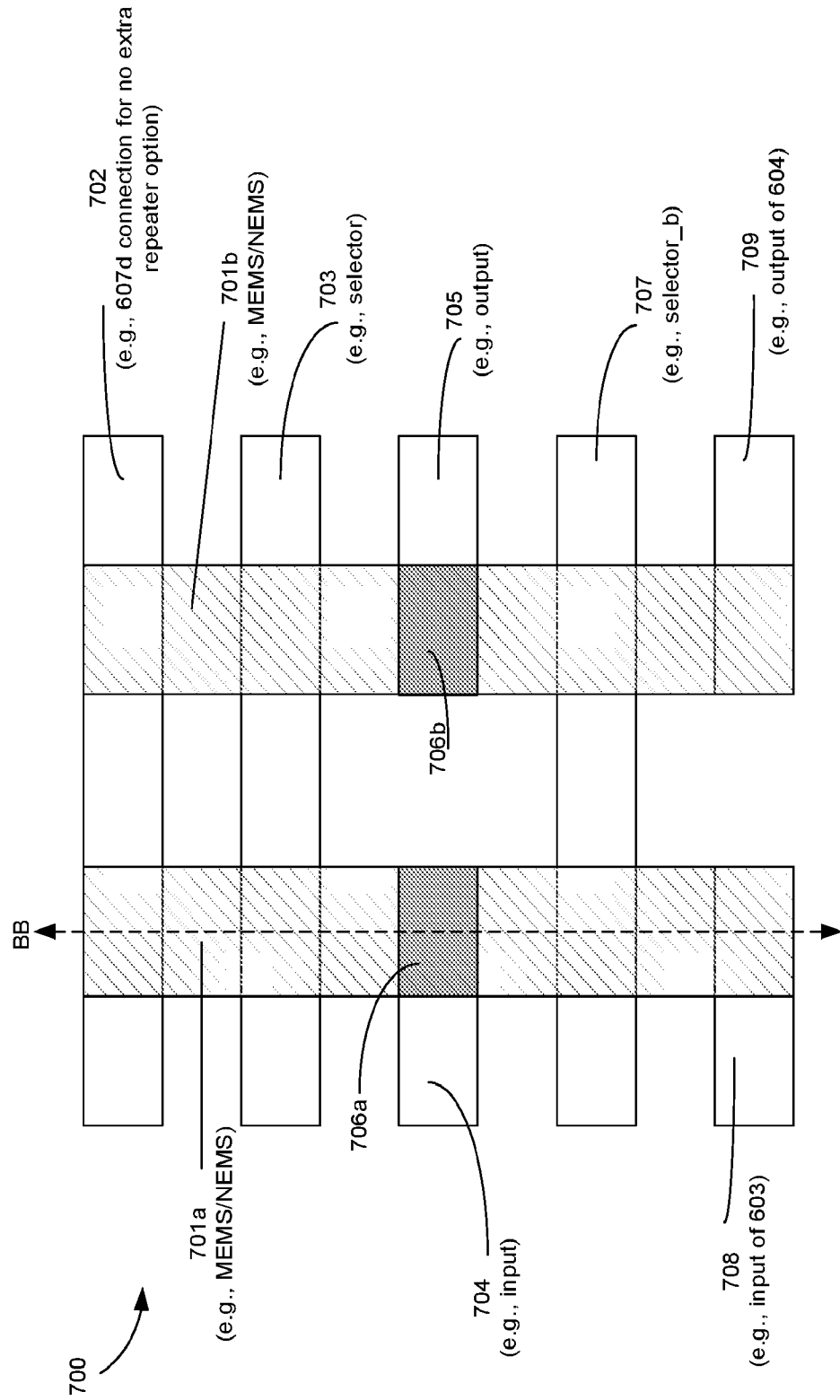


Fig. 7

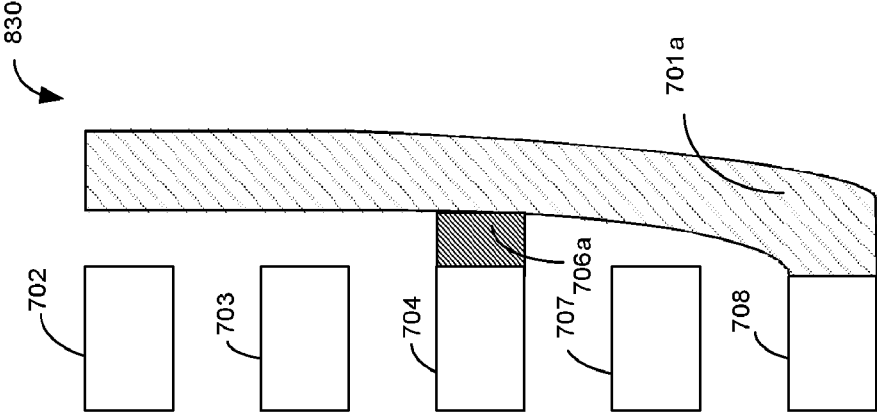


Fig. 8A

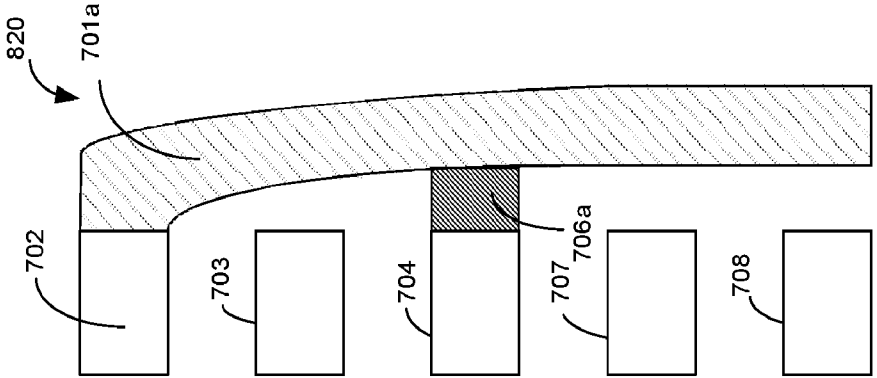


Fig. 8B

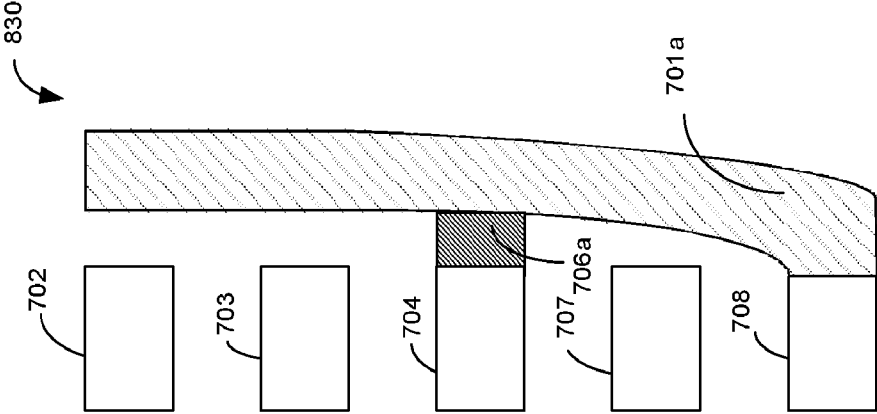
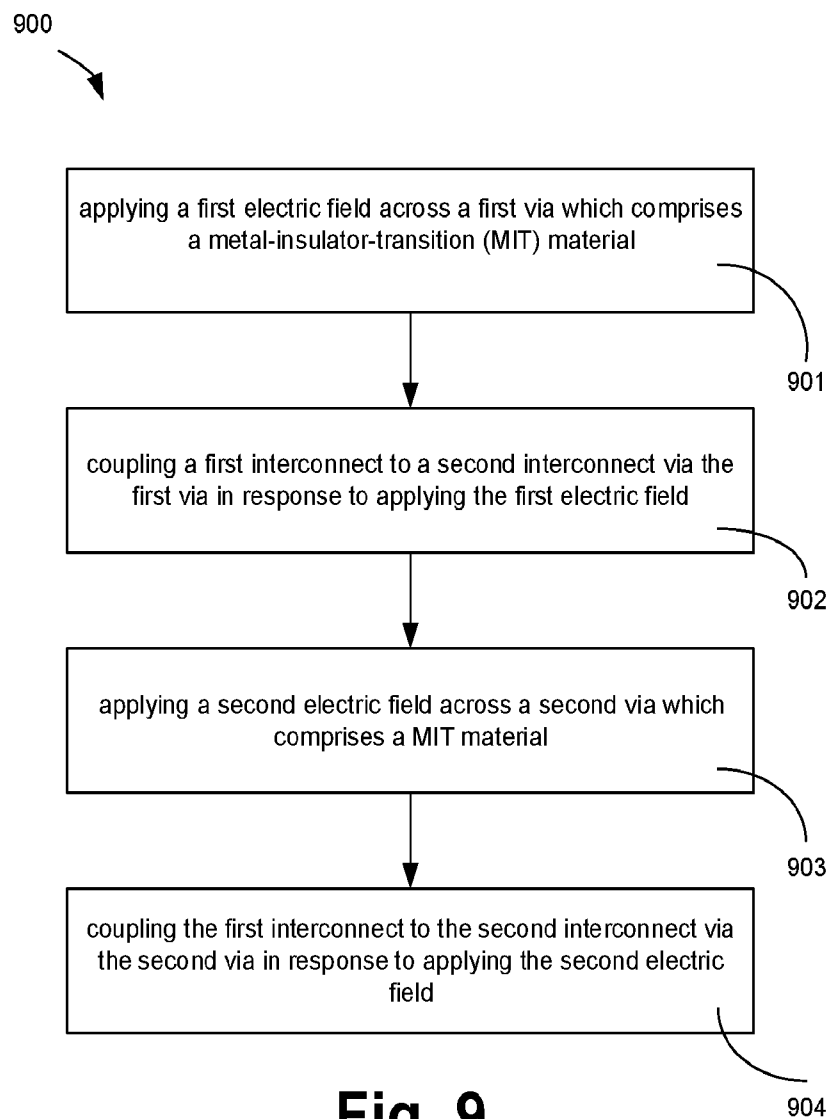
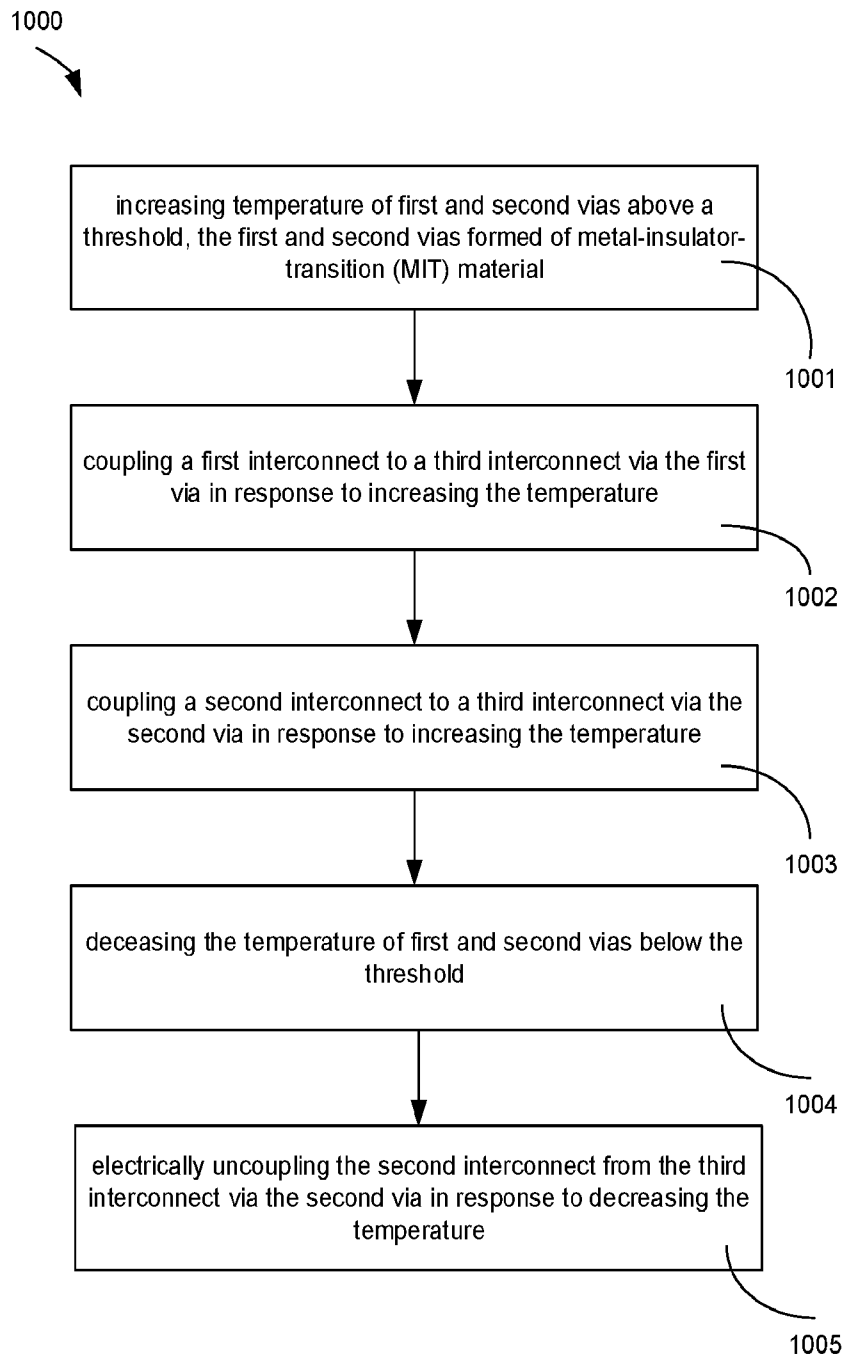


Fig. 8C



**Fig. 10**

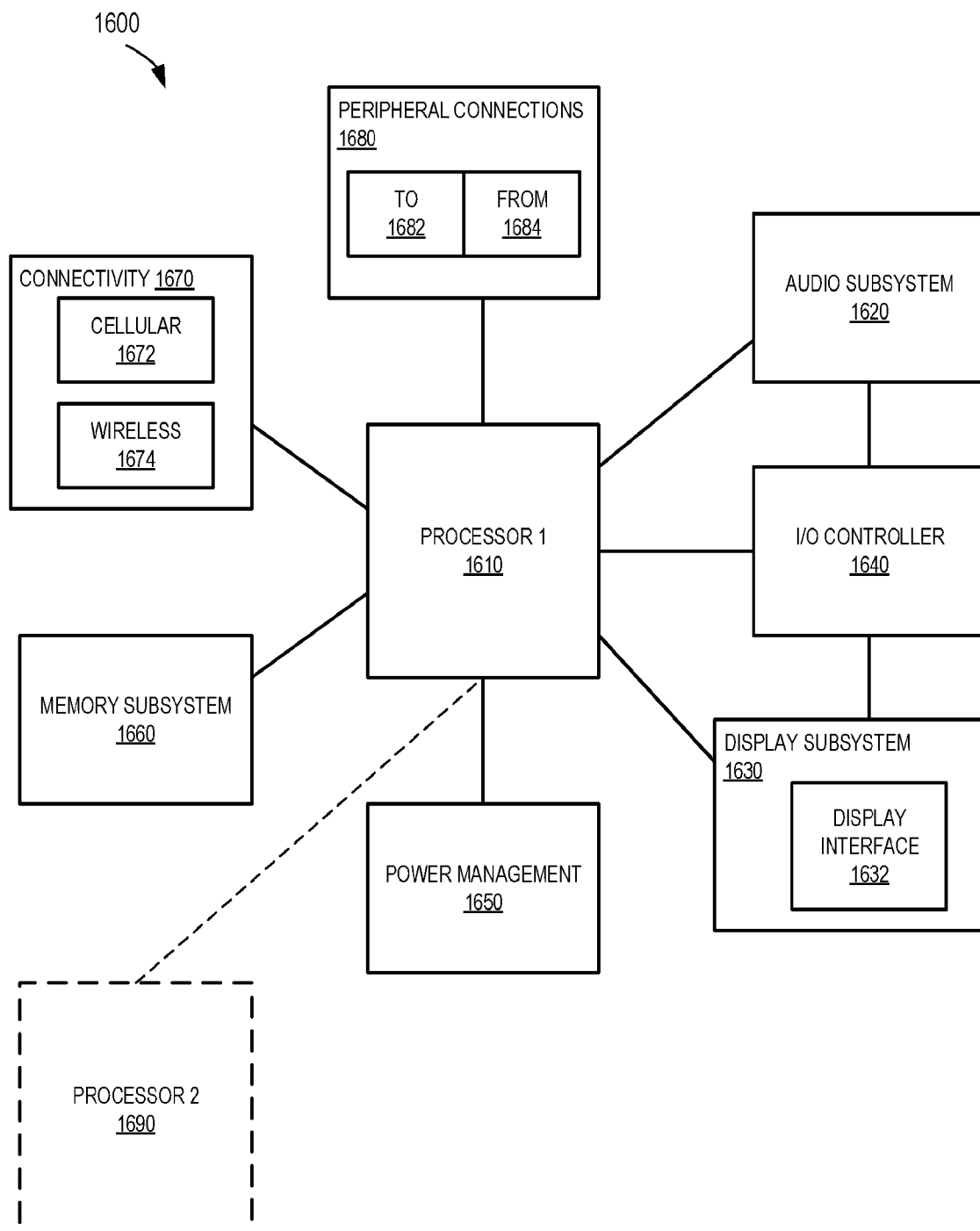


Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/000511**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/768(2006.01)i, G06F 15/78(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/768; H05H 1/24; H01L 29/51; H01L 29/82; H01L 33/00; H05K 1/02; H01L 29/76; H01L 21/00; G06F 15/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: MIT, metal insulator material, interconnect, NEMS, substrate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009-0072246 A1 (STEFANOVICH GENRIKH et al.) 19 March 2009 See abstract, paragraphs [0034]-[0044] and figures 4-6.	1-24
A	US 2009-0091003 A1 (JUNG WOOK LIM et al.) 09 April 2009 See abstract, paragraphs [0043]-[0069] and figures 1-4.	1-24
A	US 2004-0238907 A1 (JOSEPH F. PINKERTON et al.) 02 December 2004 See abstract, paragraphs [0085]-[0097] and figures 9A-10.	1-24
A	US 2003-0178228 A1 (RAYMOND JI-TUNG SUNG et al.) 25 September 2003 See abstract, paragraphs [0039]-[0047] and figures 1-6.	1-24
A	US 2008-0142900 A1 (HYUN TAK KIM et al.) 19 June 2008 See abstract, paragraphs [0034]-[0051] and figures 1-4.	1-24



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 September 2016 (23.09.2016)

Date of mailing of the international search report

23 September 2016 (23.09.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/000511

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