(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(10) International Publication Number
WO 2020/081397 A1

(43) International Publication Date
23 April 2020 (23.04.2020)

(51) International Patent Classification:
H01L 21/02 (2006.01) *C23C 16/455* (2006.01)
H01L 21/324 (2006.01) *H01J 37/32* (2006.01)
H01L 21/28 (2006.01) *H01L 21/67* (2006.01)

(21) International Application Number: PCT/US2019/055920

(22) International Filing Date: 11 October 2019 (11.10.2019)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/748,085 19 October 2018 (19.10.2018) US

(71) Applicant: LAM RESEARCH CORPORATION [US/US]; 4650 Cushing Parkway, M/S CA-1, Fremont, California 94538 (US).

(72) Inventors: **SIMS, James S.**; 13537 SW Michelle Court, Tigard, Oregon 97223 (US). **TANG, Shane**; 19763 Bennington Court, West Linn, Oregon 97068 (US). **RAI, Vikrant**; 12505 SW North Dakota Street, Tigard, Oregon 97223 (US). **MCKERROW, Andrew**; 2640 Palisades Crest Drive, Lake Oswego, Oregon 97034 (US). **QIU, Huatan**; 17479 Brookhurst Drive, Lake Oswego, Oregon 97034 (US).

(74) Agent: **LEE, Michael**; BEYER LAW GROUP LLP, P.O. Box 51887, Palo Alto, California 94303-1887 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) **Title:** METHOD OF DEPOSITING SILICON NITRIDE FILMS

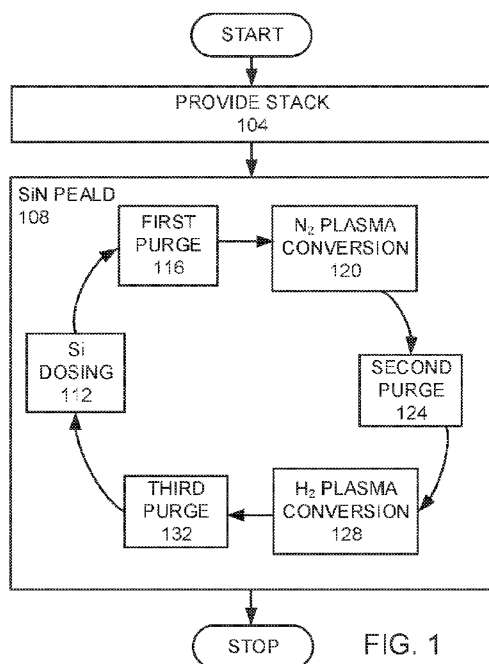
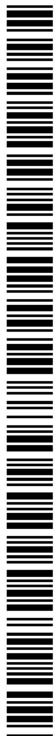


FIG. 1

(57) **Abstract:** A method for depositing a silicon nitride layer on a stack is provided. The method comprises providing an atomic layer deposition, comprising a plurality of cycles, wherein each cycle comprises dosing the stack with a silicon containing precursor by providing a silicon containing precursor gas, providing an N_2 plasma conversion, and providing an H_2 plasma conversion.


WO 2020/081397 A1

[Continued on next page]

WO 2020/081397 A1

Published:

— *with international search report (Art. 21(3))*

METHOD OF DEPOSITING SILICON NITRIDE FILMS

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority of U.S. Application No. 62/748,085, filed October 19, 2018, which is incorporated herein by reference for all 5 purposes.

BACKGROUND

[0002] The disclosure relates to methods of depositing silicon nitride films. More specifically the disclosure relates to depositing silicon nitride films using atomic layer deposition.

10 SUMMARY

[0003] To achieve the foregoing and in accordance with the purpose of the present disclosure, a method for depositing a silicon nitride layer on a stack is provided. The method comprises providing an atomic layer deposition, comprising a plurality of cycles, wherein each cycle comprises dosing the stack with a silicon containing 15 precursor by providing a silicon containing precursor gas, providing an N_2 plasma conversion, and providing an H_2 plasma conversion.

[0004] In another manifestation, an apparatus for depositing a silicon nitride atomic layer deposition on a stack is provided. A process chamber is provided. A substrate support is within the process chamber. A gas inlet provides a gas into the process 20 chamber. A gas source provides the gas to the gas inlet, where the gas source comprises a silicon containing precursor source, an N_2 gas source, and an H_2 gas source. An exhaust pump is provided for pumping gas from the process chamber. An electrode provides RF power in the process chamber. At least one power source provides power to the electrode. A controller is controllably connected to the gas 25 source and the at least one power source. The controller comprises at least one processor and computer readable media. The computer readable media comprises computer code for depositing by atomic layer deposition a silicon nitride layer on a stack by providing a plurality of cycles, wherein each of the cycles of the plurality of cycles, comprises dosing the stack with a silicon containing precursor by providing a 30 silicon containing precursor gas from the silicon containing precursor source, providing an N_2 plasma conversion and providing an H_2 plasma conversion.

[0005] These and other features of the present disclosure will be described in more detail below in the detailed description of the disclosure and in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

5 **[0006]** The present disclosure is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0007] FIG. 1 is a high level flow chart of an embodiment.

[0008] FIGS. 2A-B are schematic cross-sectional views of a stack processed 10 according to an embodiment.

[0009] FIG. 3 is a schematic view of a process chamber that may be used in an embodiment.

[0010] FIG. 4 is a schematic view of a computer system that may be used in practicing an embodiment.

15 DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0011] The present disclosure will now be described in detail with reference to a few exemplary embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be apparent, however, to one 20 skilled in the art, that the present disclosure may be practiced without some or all of these specific details. In other instances, well-known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present disclosure.

[0012] Conformal plasma-enhanced atomic layer deposition (PEALD) of silicon 25 nitride (SiN) films deposited between 150° C and 450° C face the challenge of achieving a low wet etch rate (WER) targets with simultaneous high growth rates. Since halide-based silicon precursors are the only atomic layer deposition (ALD) SiN silicon precursors known to be able to achieve 100% conformality in this temperature regime, simultaneous low WER and high growth rate films typically require some 30 combination of nitrogen (N_2) and ammonia (NH_3) in the nitride conversion plasma. N_2 plasma leads to low WER, while NH_3 plasma leads to high growth rates and conformality. Unfortunately, the use of NH_3 results in undesired side effects. The high

reactivity of NH_3 can lead to upstream particle generation and metals corrosion when the NH_3 reacts with residual halide-based silicon precursors. These reactions lead to excessive particle generation and the liberation of volatile halide-based acid byproducts that can attack metal chamber components. Removing NH_3 from the
5 conversion plasma results in low growth rates (< 0.3 Å/cycle) and requires long radio frequency (RF)-on times to get a fully conformal film (> 8 seconds (s)). Both of these effects lead to very low throughput (tpt) that makes the film commercially unattractive.

[0013] The current low WER, high growth rate conformal ALD SiN processes
10 typically use a combination of N_2 and NH_3 plasmas to convert the Si-X (X = halide or hydrogen atoms) ligands to -Si-N- bonds. The problems associated with NH_3 are high particle generation and high chamber corrosion rates. For encapsulation applications, NH_3-plasma is known to promote high elemental loss when deposited on top of sensitive chalcogenide materials. In addition, NH_3 plasmas, in general, promote the
15 incorporation of large amounts of -NH_x moieties that lead to high WERs in dilute hydrofluoric acids (dHF).

Example

[0014] To facilitate understanding, FIG. 1 is a high level flow chart of an embodiment. A stack is provided (step 104). FIG. 2A is a schematic cross-sectional
20 view of a stack 200 in an embodiment. The stack 200 may comprise a substrate 204 with structures 208 formed over the substrate 204. In this example, the stack 200 forms a phase-change random access memory (PRAM).

[0015] A SiN layer is deposited over the stack 200 by a SiN ALD process (step 108). In this embodiment, the SiN ALD process is a SiN PEALD process. The SiN
25 layer is used to encapsulate the PRAM. In this embodiment, the ALD process comprises a plurality of cycles. Each cycle has a step of dosing the stack with a silicon containing precursor gas (step 112). In this example, the dosing of the stack comprises heating the stack to a temperature of about 400° C. In this example, the silicon containing precursor case is a diiodosilane (H_2SiI_2) vapor. For between about
30 0.5 to 1.5 seconds, the dosing is completed and the flow of the silicon containing precursor gas is stopped. In this embodiment, the dosing of the stack (step 112) is a plasmaless or plasma free process. A plasma-free dose enables a more conformal,

saturated half-reaction than a process that uses a plasma by ensuring that the adsorption of the Si-containing species is self-limiting.

[0016] After the dosing (step 112) is completed and the flow of the silicon containing precursor gas is stopped, a first purge is provided (step 116) to purge the silicon containing precursor gas. In this example, the first purge (step 116) comprises flowing a first purge gas. In this example, the first purge gas is N_2. In this example, the first purge is a plasmaless or plasma free process. The process is plasma free to prevent forming a silicon containing plasma. After about 0.25 seconds, the first purge (step 116) is stopped.

[0017] After the first purge (step 116) is completed an N_2 plasma conversion is provided (step 120). In this example, the flow of N_2 during the first purge (step 116) continues, however, the N_2 plasma conversion provides a plasma. In this example, sufficient RF power is provided to transform N_2 gas into an N_2 plasma. No bias is applied. The stack is exposed to the N_2 plasma to provide the silicon nitride conversion. By using a hydrogen-free conversion, the film has very few NH_x bonds, which results in a low WER in dilute HF acid. The N_2 plasma conversion is provided for between 3 to 5 seconds. After the N_2 plasma conversion (step 120) is completed the flow of N_2 is stopped.

[0018] In this example, after the N_2 plasma conversion (step 120) is completed and the flow of N_2 gas is stopped, an optional second purge may be provided (step 124). In this example, a second purge gas of Ar may be provided. In this example, the RF power is continued in order to maintain a plasma.

[0019] After the second purge is completed (step 124) a hydrogen (H_2) plasma conversion is provided (step 128). In this example, an H_2 gas is flowed. The H_2 gas is transformed into an H_2 plasma. In this embodiment, the RF power provided during the H_2 plasma conversion (step 128) is higher than the RF power provided during the N_2 plasma conversion (step 120). No bias is applied. The stack is exposed to the H_2 plasma to hydrogenate the surface and make it more reactive to an incoming halide molecule. The H_2 plasma conversion is provided for between 1 to 2 seconds. After the H_2 plasma conversion (step 128) is completed the flow of H_2 is stopped.

[0020] In this example, after the H_2 plasma conversion (step 128) is completed and the flow of H_2 gas is stopped, a third purge is provided (step 132). In this example, a

third purge gas of N_2 is provided. In this example, the RF power is stopped to extinguish the plasma. In this example, the third purge is provided for between about 0.25 to 0.75 seconds. After the third purge is completed, the flow of the third purge gas is stopped and the cycle is completed. The cycle again goes back to the Si dosing (step 112) and the process is performed for a plurality of cycles.

[0021] FIG. 2B is a schematic cross-sectional view of the stack 200 after a SiN layer 212 has been conformally deposited on the stack through the SiN ALD process (step 108). The PEALD process provides a highly conformal SiN layer 212.

[0022] The resulting SiN layer 212 may be formed with a high throughput. Various embodiments eliminate NH_3 from the process and still have a conformal ALD SiN film with the same high growth rate as with an NH_3 plasma, the same low WER as with an N_2 plasma, low particles, and no upstream metal corrosion. This is done by inserting an H_2 plasma step after the initial N_2 plasma step. Note that this is not simply a mixture of N_2 and H_2 in the plasma, but a discrete H_2 plasma step with its own optimized flow, pressure, and power, done in such a way that very high throughputs can be obtained with the aforementioned high growth rates and low WERs. It is expected that a short, dilute H_2 plasma may be less reactive toward PRAM chalcogenide materials and allow the development of bi-layer encapsulation layers, with the high-throughput N_2/H_2 ALD SiN process being deposited on top of a protective layer of N_2-only ALD SiN. This hybrid stack would have much higher throughput and better oxidation resistance than an N_2-only film of an equivalent thickness.

[0023] Various embodiments provide an NH_3-free process that meets the low WER (<4 angstroms per minute (Å/min) in 200:1 diluted hydrofluoric acid (dHF)) and high growth rate (> 0.7 A/cycle) requirements by inserting a second H_2 plasma conversion step after the initial N_2 plasma conversion step. H_2 has the advantage of not being as thermally reactive with halide precursors as NH_3. This means there is no upstream particle generation in the gas distribution plenum (GDP). In addition, there is no upstream liberation of hydrogen iodide (HI) and hydrogen chloride (HCl) volatile byproducts that lead to metal corrosion. The H_2 plasma conversion adds enough reactive ligands to the growing SiN film surface to promote the next cycle of silicon

precursor adsorption without incorporating excessive -NHx bonds that lead to high wet etch rates.

[0024] What is unexpected about this ALD SiN deposition process is that this embodiment can still achieve high conformality and high growth rates with a much less reactive nitrogen source than NH_3. In addition, the in-film particle adders have been reduced by 2-3 orders of magnitude. Various embodiments enable the optimization of sequential N_2 and H_2 plasma steps that result in best in class film properties and productivity. The elimination of NH_3 can also lead to large cost reductions in tool costs since the expectation is that less aggressive metals reduction strategies can be employed, and the need for expensive dual-plenum designs to separate NH_3 from the residual silicon precursor is eliminated.

[0025] In some embodiments, the second purge (step 124) may be eliminated. In such an embodiment, the N_2 gas is flowed first. The H_2 gas is flowed after the start of the flow of the N_2 gas and while the N_2 gas continues to flow so that the H_2 gas and N_2 gas flow together for some of the time. In another embodiment, the flow of the N_2 gas is stopped before the flow of the H_2 begins. However, without a second purge (step 124) there is some mixing of remaining N_2 gas with H_2 gas. The elimination of the second purge (step 124) reduces processing time and increases throughput.

[0026] In various embodiments, the silicon containing precursor is at least one of a silicon halide. In various embodiments, silicon iodides, such as diiodosilane (H_2SiI_2), triiodosilane ($HSiI_3$), iodosilane (H_3SiI), or tetraiodosilane (SiI_4,), would provide a preferred silicon containing precursor. In other embodiments, the silicon halide may be silicon chlorides or silicon bromides. Preferably, in addition to the silicon halide having at least one halogen attached to at least one silicon atom, the silicon halide may also have one or more hydrogen atoms attached to the at least one silicon atom. In other embodiments, the silicon halide may at least one halogen attached to at least one silicon atom and at least one of an atom of another element attached to the at least one silicon atom. These other silicon containing precursors could be amino-, amido- or alkyl-based subgroups that can act as either leaving groups, cross-linking promoters or dopants. In various embodiments, the substrate is heated to a temperature of at least 150° C during the dosing (step 112). More specifically, the substrate is heated to a temperature of between 200° C to 400° C. The heating

provides activation energy to the silicon containing precursor to cause the silicon containing precursor to form a saturated conformal monolayer.

[0027] FIG. 3 is a schematic view of a process chamber that may be used in an embodiment. In one or more embodiments, a process chamber 300 comprises a gas distribution plate 306 providing a gas inlet and a substrate support 308, within a chamber 349, enclosed by a chamber wall 352. Within the chamber 349, a stack 200 is positioned over the substrate support 308. An edge ring 309 surrounds the substrate support 308. A gas source 310 is connected to the chamber 349 through the gas distribution plate 306. In this example, the gas source 310 comprises a silicon containing precursor source 311, an N_2 gas source 312, and an H_2 gas source 316. A support temperature controller 350 is connected to a heater 351 for heating the substrate support 308. A radio frequency (RF) source 330 provides RF power to an upper electrode. In this embodiment, the upper electrode is the gas distribution plate 306. In an exemplary embodiment, 400 kilohertz (kHz), 13.56 megahertz (MHz), and optionally 2 MHz, 27 MHz power sources make up the RF source 330. In this embodiment, the substrate support 308 is grounded. In this embodiment, one generator is provided for each frequency. In other embodiments, the generators may be in separate RF sources, or separate RF generators may be connected to different electrodes. For example, the upper electrode may have inner and outer electrodes connected to different RF sources. Other arrangements of RF sources and electrodes may be used in other embodiments. A controller 335 is controllably connected to the RF source 330, an exhaust pump 320, and the gas source 310. An example of such a chamber is the Striker™ system manufactured by Lam Research Corporation of Fremont, CA.

[0028] FIG. 4 is a high level block diagram showing a computer system 400 suitable for implementing a controller 335 used in embodiments. The computer system may have many physical forms ranging from an integrated circuit, a printed circuit board, and a small handheld device up to a huge supercomputer. The computer system 400 includes one or more processors 402, and further can include an electronic display device 404 (for displaying graphics, text, and other data), a main memory 406 (e.g., random access memory (RAM)), storage device 408 (e.g., hard disk drive), removable storage device 410 (e.g., optical disk drive), user interface devices 412

(e.g., keyboards, touch screens, keypads, mice or other pointing devices, etc.), and a communications interface 414 (e.g., wireless network interface). The communications interface 414 allows software and data to be transferred between the computer system 400 and external devices via a link. The system may also include a communications infrastructure 416 (e.g., a communications bus, cross-over bar, or network) connected to the aforementioned devices/modules.

[0029] Information transferred via communications interface 414 may be in the form of signals such as electronic, electromagnetic, optical, or other signals capable of being received by communications interface 414, via a communication link that carries signals and may be implemented using wire or cable, fiber optics, a phone line, a cellular phone link, a radio frequency link, and/or other communication channels. With such a communications interface, it is contemplated that the one or more processors 402 might receive information from a network, or might output information to the network in the course of performing the above-described method steps. Furthermore, method embodiments may execute solely upon the processors or may execute over a network such as the Internet, in conjunction with remote processors that shares a portion of the processing.

[0030] The term “non-transient computer readable medium” is used generally to refer to media such as main memory, secondary memory, removable storage, and storage devices, such as hard disks, flash memory, disk drive memory, CD-ROM, and other forms of persistent memory and shall not be construed to cover transitory subject matter, such as carrier waves or signals. Examples of computer code include machine code, such as produced by a compiler, and files containing higher-level code that are executed by a computer using an interpreter. Computer readable media may also be computer code transmitted by a computer data signal embodied in a carrier wave and representing a sequence of instructions that are executable by a processor.

[0031] While this disclosure has been described in terms of several preferred embodiments, there are alterations, modifications, permutations, and various substitute equivalents, which fall within the scope of this disclosure. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present disclosure. It is therefore intended that the following appended claims be interpreted as including all such alterations, modifications,

permutations, and various substitute equivalents as fall within the true spirit and scope of the present disclosure.

CLAIMS

What is claimed is:

1. A method for depositing a silicon nitride layer on a stack, comprising providing an atomic layer deposition, comprising a plurality of cycles, wherein each cycle comprises:

dosing the stack with a silicon containing precursor by providing a silicon containing precursor gas;

providing an N_2 plasma conversion; and

providing an H_2 plasma conversion.

2. The method, as recited in claim 1, wherein the silicon containing precursor is a silicon halide.

3. The method, as recited in claim 1, wherein during the dosing the stack, the stack is maintained at a temperature of at least 150° C.

4. The method, as recited in claim 1, wherein the dosing the stack is plasmaless.

5. The method, as recited in claim 1, wherein each cycle is NH_3 free.

6. The method, as recited in claim 1, wherein the providing the N_2 plasma conversion, comprises:

flowing an N_2 gas;

transforming the N_2 gas into an N_2 plasma;

exposing the stack to the N_2 plasma; and

stopping the flow of the N_2 gas.

7. The method, as recited in claim 6, wherein the providing the H_2 plasma conversion, comprises:

flowing an H_2 gas;

transforming the H_2 gas into an H_2 plasma;

exposing the stack to the H_2 plasma; and

stopping the flow of the H_2 gas.

8. The method, as recited in claim 7, wherein the flowing the N_2 gas is before the flowing the H_2 gas.

9. The method, as recited in claim 1, wherein the silicon containing precursor is a silicon iodide.

10. The method, as recited in claim 1, wherein the silicon containing precursor is a

silicon chloride or silicon bromide.

11. The method, as recited in claim 1, further comprising purging an H_2 plasma formed by the H_2 plasma conversion, after providing the H_2 plasma conversion and before dosing the stack.

5 12. The method, as recited in claim 1, further comprising purging the silicon containing precursor gas after dosing the stack and before providing the N_2 plasma conversion.

13. An apparatus for depositing a silicon nitride atomic layer deposition on a stack, comprising

10 a process chamber;

a substrate support within the process chamber;

a gas inlet for providing a gas into the process chamber;

a gas source for providing the gas to the gas inlet, wherein the gas source comprises:

15 a silicon containing precursor source;

an N_2 gas source; and

an H_2 gas source;

an exhaust pump for pumping gas from the process chamber;

an electrode for providing RF power in the process chamber;

20 at least one power source for providing power to the electrode; and

a controller controllably connected to the gas source and the at least one power source, wherein the controller comprises:

at least one processor; and

computer readable media, comprising:

25 computer code for depositing by atomic layer deposition a silicon nitride layer on a stack by providing a plurality of cycles, wherein each of the cycles of the plurality of cycles, comprises:

dosing the stack with a silicon containing precursor by providing a silicon containing precursor gas from the silicon containing precursor

30 source;

providing an N_2 plasma conversion; and

providing an H_2 plasma conversion.

14. The apparatus, as recited in claim 13, further comprising a heater for heating the substrate support.

15. The apparatus, as recited in claim 14, wherein the computer readable media further comprises computer code for heating the substrate support to a temperature of
5 at least 150° C.

16. The apparatus, as recited in claim 13, wherein the gas source is NH_3 free.

17. The apparatus, as recited in claim 13, wherein the providing the N_2 plasma conversion, comprises:

flowing an N_2 gas;

10 transforming the N_2 gas into an N_2 plasma;

exposing the stack to the N_2 plasma; and

stopping the flow of the N_2 gas.

18. The apparatus, as recited in claim 17, wherein the providing the H_2 plasma conversion, comprises:

15 flowing an H_2 gas;

transforming the H_2 gas into an H_2 plasma;

exposing the stack to the H_2 plasma; and

stopping the flow of the H_2 gas.

19. The apparatus, as recited in claim 13, wherein each of the cycles of the
20 plurality of cycles, comprises:

purging the silicon containing precursor gas after dosing the stack and before providing the N_2 plasma conversion; and

purging the H_2 plasma, after providing the H_2 plasma conversion and before dosing the stack.

25

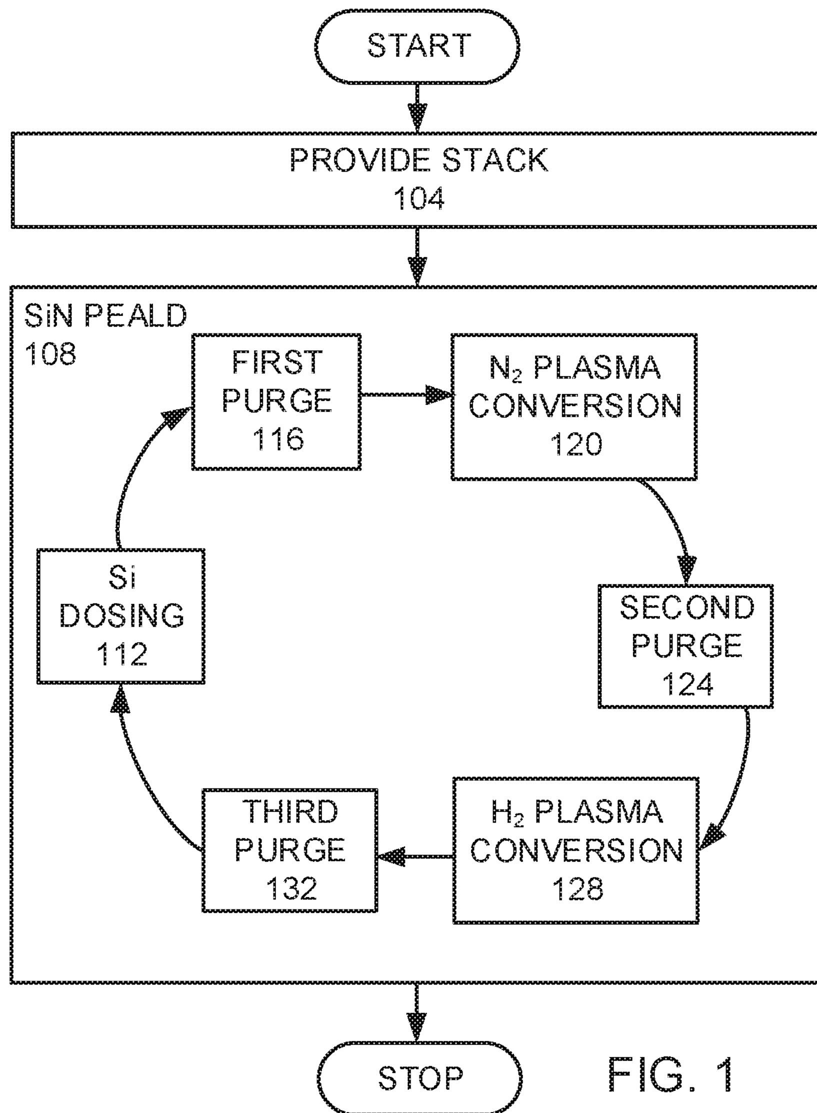


FIG. 1

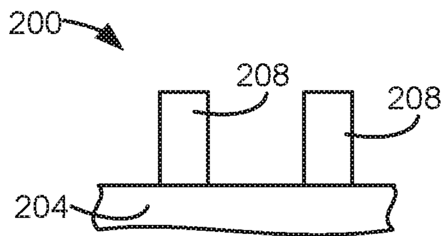


FIG. 2A

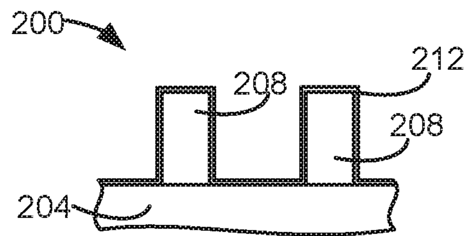


FIG. 2B

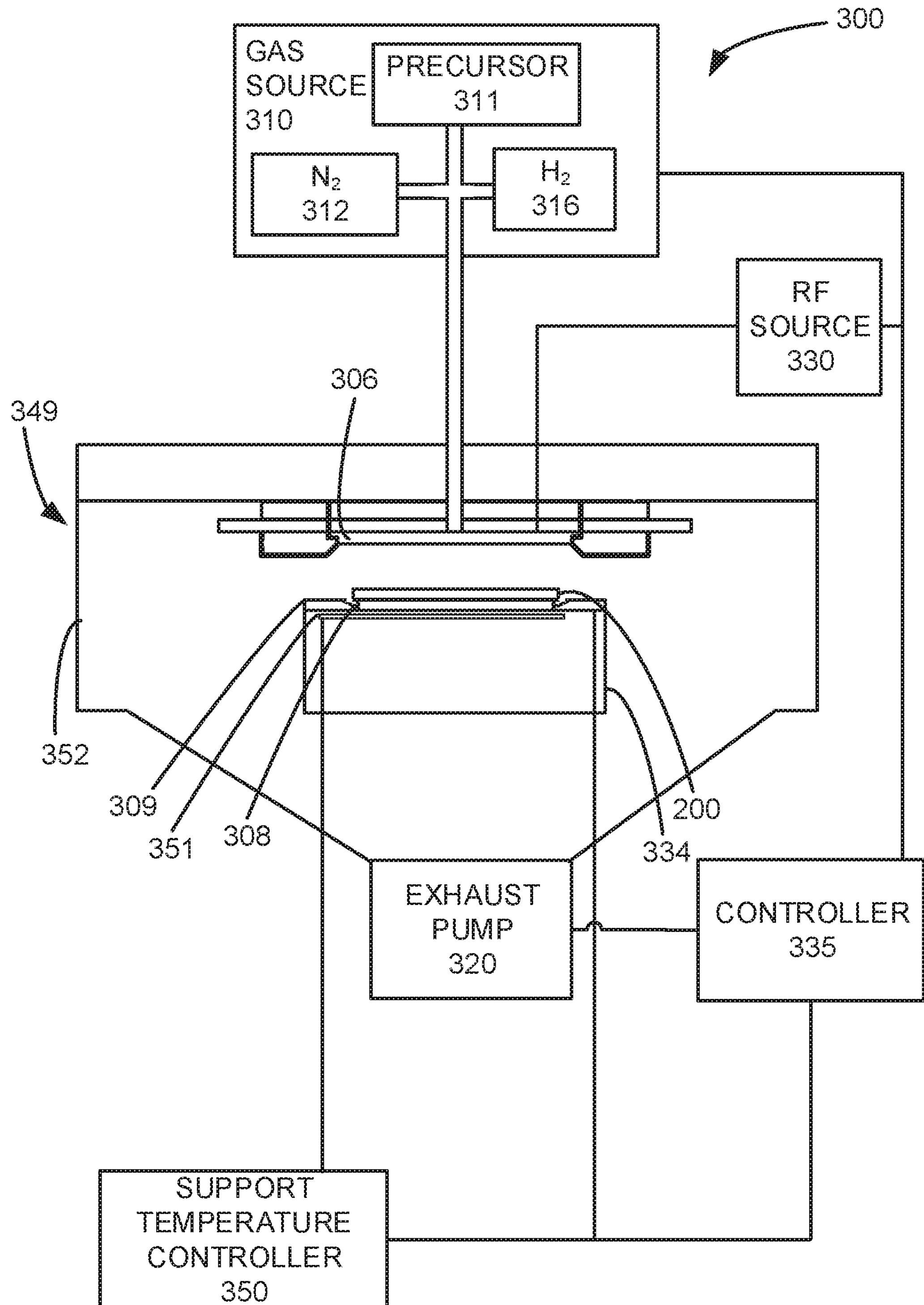


FIG. 3

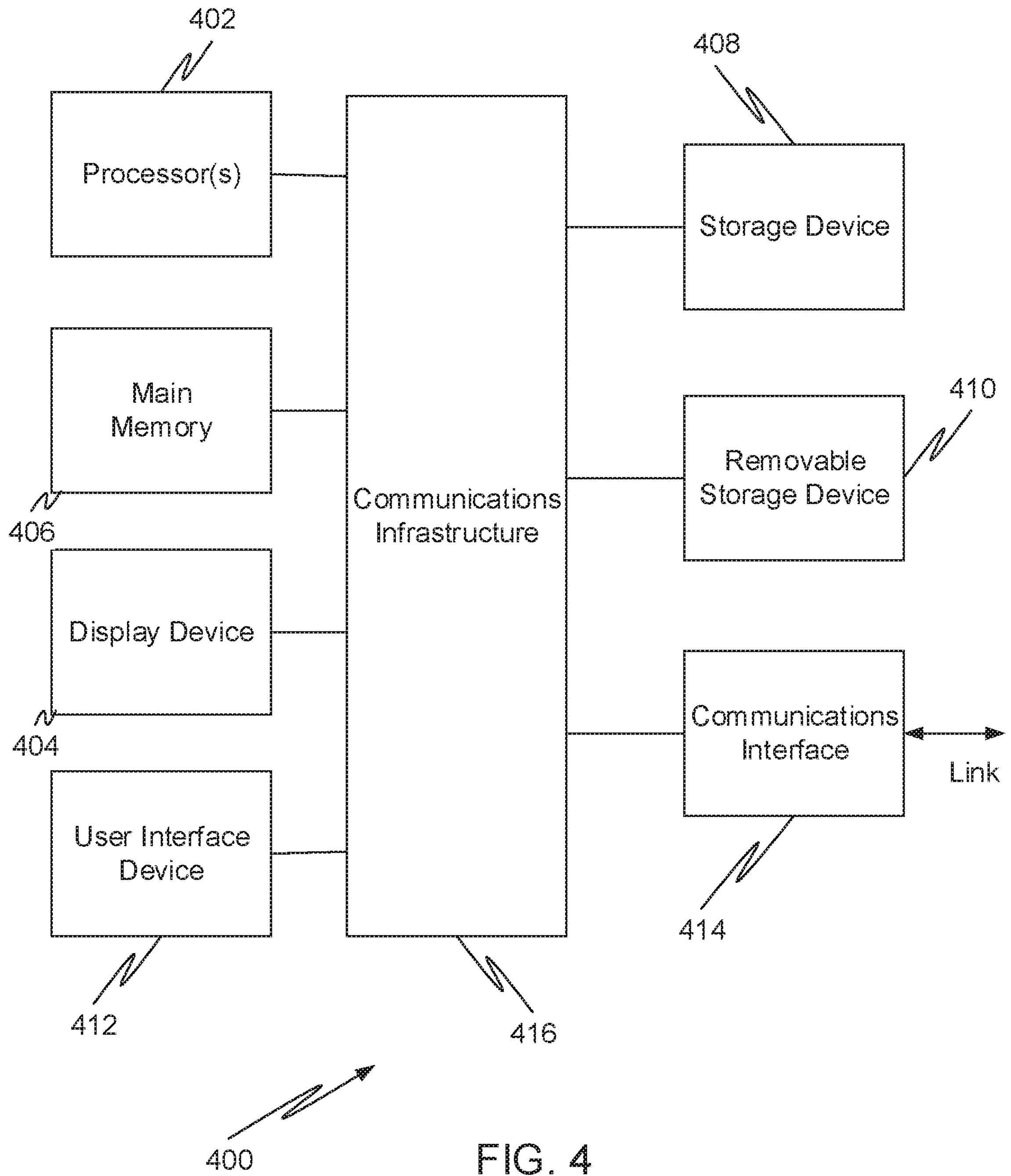


FIG. 4

INTERNATIONAL SEARCH REPORT	International application No. **PCT/US2019/055920**

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/02(2006.01)i, H01L 21/324(2006.01)i, H01L 21/28(2006.01)i, C23C 16/455(2006.01)i, H01J 37/32(2006.01)i, H01L 21/67(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/02; C23C 16/34; C23C 16/44; C23C 16/505; H01L 21/3065; H01L 21/31; H01L 21/324; H01L 21/28; C23C 16/455; H01J 37/32; H01L 21/67

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: PEALD, silicon-nitride, temperature, NH3-free

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016-0148806 A1 (LAM RESEARCH CORPORATION) 26 May 2016 Paragraphs 32-85; claims 1-8; and figures 2-4.	1,3-8,11-19
Y		2,9-10
Y	US 2016-0079054 A1 (ASM IP HOLDING B.V.) 17 March 2016 Paragraph 28.	2,9-10
A	US 2013-0210241 A1 (ADRIEN LAVOIE et al.) 15 August 2013 The entire document.	1-19
A	US 9984869 B1 (ASM IP HOLDING B.V.) 29 May 2018 The entire document.	1-19
A	KR 10-2017-0038429 A (WONIK IPS CO., LTD.) 07 April 2017 The entire document.	1-19

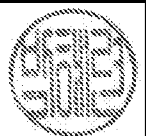
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 January 2020 (29.01.2020)	**30 January 2020 (30.01.2020)**

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
PARK, Hye Lyun

Telephone No. +82-42-481-3463

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2016-0148806 A1	26/05/2016	KR 10-2016-0061890 A	01/06/2016
		TW 201632650 A	16/09/2016
		US 9589790 B2	07/03/2017
US 2016-0079054 A1	17/03/2016	JP 2016-063232 A	25/04/2016
		KR 10-2016-0033057 A	25/03/2016
		TW 201617471 A	16/05/2016
		US 10262854 B2	16/04/2019
		US 2017-0372886 A1	28/12/2017
		US 2018-0068844 A1	08/03/2018
		US 2019-0295838 A1	26/09/2019
		US 9576792 B2	21/02/2017
US 2013-0210241 A1	15/08/2013	CN 103243310 A	14/08/2013
		CN 103243310 B	12/04/2017
		KR 10-2013-0093569 A	22/08/2013
		KR 10-2019-0126256 A	11/11/2019
		KR 10-2031377 B1	11/10/2019
		SG 10201506346 A	29/09/2015
		SG 193097 A1	30/09/2013
		TW 201348502 A	01/12/2013
		TW I612172 B	21/01/2018
		US 2014-0209026 A1	31/07/2014
		US 8728955 B2	20/05/2014
US 9984869 B1	29/05/2018	CN 108728824 A	02/11/2018
		KR 10-2018-0116761 A	25/10/2018
		TW 201903190 A	16/01/2019
KR 10-2017-0038429 A	07/04/2017	None	