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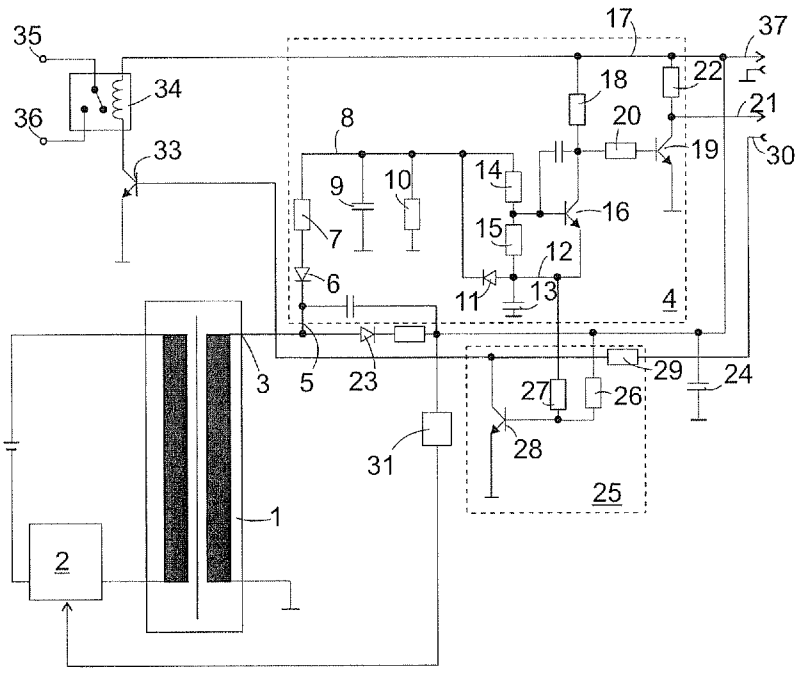
(54) **Title:** POWER FAILURE DETECTION CIRCUIT



(57) **Abstract:** A power failure detection circuit (4) comprises an input port (5) for applying a voltage signal to be monitored; a voltage rate of change detecting circuit (6-15) connected to said input port (5) for deriving a signal representative of a rate of change of said voltage signal, and a first comparator (14-16) for comparing said representative signal to a predetermined limit and for outputting a first power failure signal if said representative signal exceeds a predetermined limit.

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Power Failure Detection Circuit

The present invention relates to a power failure detection circuit for monitoring a supply voltage or a signal which is representative of such a supply voltage, and which circuit is adapted to detect a failure of this supply voltage before the failure causes apparatus powered by that supply voltage to become inoperable. If the failure is detected early enough, a power failure signal from the detection circuit can be used for triggering operations in the apparatus such as saving data, moving sensitive mechanical components into a parking position, etc. while such operations can still be carried out, powered e.g. by residual energy stored in the apparatus.

A power failure detection circuit disclosed in JP 2001 2643 67 comprises an input port for applying a voltage signal to be monitored; a comparator for comparing the voltage-divided voltage signal to a reference level and for outputting a signal if the voltage-divided voltage signal is below the reference level.

In order to detect a voltage failure early, the difference between the voltage-divided voltage signal and the first reference level must be made small. However, such a small difference will cause the output of the first comparator to toggle in case of transient fluctuations of the supply voltage. In order to prevent misdetection of such transient fluctuations as power failures, the output of the first comparator is passed through a low-pass filter, and the output of the low-pass filter is applied to a second comparator for comparison to a second reference level. Due to the low-pass filter, detection of a power failure by this conventional circuit is slow. A power failure may be detected more quickly based on

the output of the first comparator, but this detection is not reliable.

The object of the present invention is therefore to provide a power failure detection circuit by which a power failure can be detected both quickly and reliably.

This object is achieved according to the invention by a power failure detection circuit comprising an input port for applying a voltage signal to be monitored; a voltage rate of change detecting circuit connected to said input port for deriving a signal representative of a rate of change of said power signal, and a first comparator for comparing said representative signal to a predetermined limit and for outputting a first power failure signal if said representative signal exceeds a predetermined limit.

The invention is based on the idea that in case of a power failure the rate of change of the voltage signal tends to be much higher than the rate of change of slow mains variations which may be present in the voltage signal. Therefore, by evaluating the rate of change, a voltage change can be judged to be caused by a power failure or by a slow mains variation very quickly, while the deviation from a desired supply voltage is still small.

According to a preferred embodiment, the voltage rate of change detecting circuit comprises a first storage member connected to said input port by a first rectifier for storing a rectified voltage level, a second storage member connected to said input port by a second rectifier for storing said rectified voltage level, and first dissipating means for decreasing the voltage level stored in said first storage member at a first rate, and the rate of change representative signal is a

voltage between the input sides of said first and second storage members. If the voltage signal is a DC signal, the rectifiers are effective to hold the storage members at the level of the voltage signal. If the level of the voltage signal drops due to a power failure, the rectifiers will block, and the first dissipating means cause the voltage level at the first and second storage members to become different. This difference then forms the rate of change representative signal. In case of the voltage signal being an AC voltage, the rectifiers are effective to recharge the storage members to the peak level of the voltage signal in each oscillation period thereof, so that although part of this peak voltage may be dissipated by the first dissipating means in the course of an oscillation period, the difference between the stored voltages remains small. In case of a power failure, the storage means are not recharged, and the difference between the respective voltages comes to exceed the predetermined limit, so that the power failure is detected.

The power failure detection circuit may further comprise second dissipating means for decreasing the voltage level stored in the second storage member at a second rate lower than that first rate. In this way, a transient excess voltage will not be permanently stored in the second storage member, but will be dissipated so that it will not cause erroneous detection of a power failure.

The first and second rectifiers may be connected directly to the input port. Alternatively, the second rectifier is connected between input sides of said first and second storage members. Due to this circuit design, the voltage between the input sides of the storage members is not zero at normal operating conditions, but corresponds to a voltage drop in the

second rectifier. This non-zero voltage allows for very simple design of the first comparator, as will become apparent later.

According to a simple but effective embodiment, the storage members are capacitors and the dissipating means are resistors connected in parallel to an associated one of the capacitors.

The comparator preferably comprises a voltage divider connected between the input sides of said first and second storage members and a switch controlled by a potential at an intermediate node of the voltage divider. By setting the division ratio of the voltage divider, the sensitivity of the power failure detection circuit can be controlled.

The switch preferably is a transistor having current terminals connected to a supply voltage and to the first side of one of the storage members, respectively, and a control terminal connected to the intermediate node. As pointed out above, since the voltage between the input sides of the storage members is never zero if the second rectifier is connected between them, there is always a non-zero voltage between the control terminal and the current terminal of the transistor which is connected to one of the storage members, so that a small variation of the voltage at the control terminal is sufficient to switch the transistor on and off.

The first and second rectifiers may be half-wave rectifiers such as e. g. diodes. These half-wave rectifiers preferably transmit half-waves of a same first polarity type of said voltage signal.

In a power supply comprising the power failure detection circuit defined above, a third rectifier may be provided for deriving a DC supply potential.

In such a power supply, a second voltage divider may be connected between the input side of one of said first and second storage members and said supply potential, the supply potential having a polarity opposite to that of said one input side, and a second comparator may be provided for deriving a second power failure signal based on a comparison of a voltage at an intermediate node of said second voltage divider and a ground voltage.

The third rectifier preferably also is a half-wave rectifier which derives said supply potential from half-waves of said voltage signal having a second polarity type opposite to the first type.

Further features and advantages of the invention will become apparent from the subsequent description of embodiments thereof referring to the appended drawing.

Fig. 1 is a circuit diagram of a power supply comprising a power failure detection circuit according to the present invention.

Fig. 2 is a schematic block diagram of an electronic device comprising the power supply of Fig. 1.

The power supply of Fig. 1 comprises a transformer 1, a primary winding of which receives a pulsed DC current controlled by a flyback converter controller 2. A secondary winding of transformer 1 has one of its two terminals connected to ground; the other terminal 3 outputs a secondary AC voltage. A power failure detection circuit 4 has an input port 5 directly connected to this secondary voltage.

In the power failure detection circuit 4, a diode 6 and a current limiting resistor 7 are connected in series between the input port 5 and a first circuit node 8. The orientation of said diode 6 is such that it transmits negative half-waves of the secondary voltage to the circuit node 8 which thus tends to assume a constant negative potential corresponding to the peak negative potential of the secondary AC voltage.

A first storage capacitor 9 and a resistor 10 are connected in parallel between circuit node 8 and ground. A second diode 11 is connected between the first circuit node 8 and a second circuit node 12. The orientation of the diode 11 is such that the potential of the second circuit node 12 tends to be more positive by the junction voltage of the diode 11 than the potential of node 8. A second storage capacitor 13 is connected between the second circuit node 12 and ground. A voltage divider formed of resistors 14, 15 is placed between the two nodes 8, 12 in parallel to diode 11. A first transistor 16 has its emitter connected to the second node 12, its base connected to an intermediate note of the voltage divider 14, 15, and its collector connected to a positive DC supply line 17 by resistor 18 and to the base of a second transistor 19 by a resistor 20. The emitter of transistor 19 is grounded. Its collector is connected directly to an output port 21 of detection circuit 4 and to supply line 17 by a resistor 22.

The positive supply line 17 is driven by the secondary output voltage via a third diode 23. It supplies controlled DC power to a load, not shown in Fig. 1, at a connector 37. An electrolytic capacitor 24 is connected between the supply line 17 and ground for reducing ripple and for preventing an excessively fast voltage decay on supply line 17 in case of a power failure.

An optocoupler 31 is coupled to a supply line 17 for feeding back a control signal representative of the potential of supply line 17 to flyback converter control circuit 2. The flyback converter control circuit 2 is of a conventional type, e.g. VIPER22ADIP available from SGS Thomson Microelectronics. In a conducting state, the controller 2 allows a current to flow through the primary winding of transformer 1, the intensity of which increases linearly with time while this current is flowing, and in that time a negative half-wave is output at the secondary terminal 3 of the transformer 1. When the controller 2 switches into a blocking state, a positive voltage is generated at secondary terminal 3. Adjusting the duration of the conducting phase according to the feedback signal from optocoupler 31 allows to keep the magnitude of the positive voltage at secondary terminal 3 constant at a desired level of e.g. +5V, whereas the voltage of the negative half-wave at secondary terminal 3 is substantially independent of the duration of the conducting phase of controller 2 and is directly proportional to the DC primary voltage applied to controller 2.

Under normal operating conditions, a current flows from circuit node 8 to input port 5 and through diode 6 each time when the secondary AC voltage at input port 5 is close to its negative peak value, causing the circuit node 8 to assume a negative potential, the magnitude of which is less than the peak value of the secondary voltage by the junction voltage of diode 6. The potential of the second circuit node 12 is more positive than that of the first node 8 by the junction voltage of diode 11.

When the secondary AC voltage has passed its negative peak, diode 6 blocks. Charge accumulated in storage capacitor 9 is gradually dissipated to ground by resistor 10, causing the po-

tential at circuit node 8 to become less negative. In this state, diode 11 blocks, too, and charge accumulated in storage capacitor 13 is dissipated via resistors 14, 15. Since the voltage across resistors 14, 15 is much smaller than that across resistor 10, the resistance values of resistors 14, 15 are higher than that of resistor 10, and the capacitance of electrolytic capacitor 13 is much higher than that of capacitor 9, the rate of change of the potential at circuit node 12 is much slower than that of circuit node 8.

Under normal operating conditions, capacitors 9, 13 are recharged when the secondary AC voltage reaches its negative peak the next time, so that the voltage between first and second circuit node 8, 12 cannot become large. Specifically, resistance values of resistors 10, 14, 15 and capacitances of capacitors 9, 13 must be selected so that the voltage across resistor 15 will not exceed 0.7 volts within a time interval of at least one period of the secondary AC voltage. Transistor 16 is permanently nonconductive, so that the potential at the base of transistor 19 is close to that of positive supply line 17. Transistor 19 is thus held in a conductive state, and the output port 21 outputs ground potential.

If capacitor 9 is not recharged due to a power failure, the voltage between circuit nodes 8, 12 gradually increases, and finally the voltage across resistor 15 becomes high enough to cause transistor 16 to switch into a conducting state. The collector potential of transistor 16 thus becomes negative. This causes transistor 19 to switch into a blocking state. The collector potential of transistor 19 becomes identical to the potential of supply line 17. A power failure is thus indicated by the output port 21 switching from ground to the positive supply potential.

The power failure signal thus obtained by power failure detection circuit 4 does not depend on the magnitude of the secondary voltage, but only on its rate of change. If this rate of change exceeds a threshold which depends on the difference of the discharge rates of the capacitors 9, 13, a supply voltage failure will be detected although the magnitude of the voltage may still be in a range where circuitry powered by the secondary voltage is still safely operable. In this way, the time available for shutdown measures triggered by the power failure signal at output port 21 is increased.

Although the circuit 4 is completely sufficient to detect a power failure in most circumstances, a second power failure detection circuit 25, as shown in Fig. 1, may be provided for detecting a power failure in case of a slow decrease of the secondary voltage. In the embodiment of Fig. 1, such a circuit 25 comprises a voltage divider formed of resistors 26, 27 connected between the positive supply line 17 and the second circuit node 12 and a transistor 28 which has its base connected to an intermediate node of the voltage divider 26, 27, its emitter connected to ground and its collector connected to a normally positive potential via a resistor 29. This normally positive potential might be that of supply line 17; in the present case, it is input into the power supply at an input port 30.

In case of a slow decrease of the primary voltage which is too slow to be detected by detection circuit 4, the feedback signal from optocoupler 31 to flyback converter controller 2 initially decreases, causing the controller 2 to adapt the duration of its conductive phase, so that the potential of supply line 17 is maintained at its desired level of +5V. The negative secondary output voltage, being directly proportional to the primary voltage, becomes more positive in such a case, and

so does the base of transistor 28. When the base potential of transistor 28 becomes positive, the transistor 28 becomes conductive, and its collector potential drops to ground. I.e. a second power failure signal is obtained at the collector of transistor 28, which is positive under normal operating conditions and which drops to zero abruptly if the primary voltage drops below a predetermined limit.

This second power failure signal might be logically combined with the first one from circuit 4 in order to derive a third power failure signal which is sensitive both to an abrupt change as well as to a slow but excessive decrease of the primary voltage. In the embodiment shown in Fig.1, however, this second power failure signal controls a transistor 33 which is connected in series with a relay 34 between the positive supply line 17 and ground. When the transistor 33 is conductive, the current flowing through relay 34 maintains a switch between terminals 35, 36 closed. When the transistor 33 becomes nonconductive, the switch opens automatically.

Fig. 2 is a block diagram of an electronic device in which the power supply of Fig. 1 is used. The device of Fig. 2 can be of practically any type. To give a specific example, a video cassette recorder or a video hard disc recorder will be discussed below. The power supply of Fig. 1, denoted 40 in Fig. 2, provides operating power to a microcontroller 41 of the recorder by the positive DC supply line 17 and connector 37. The microcontroller 41 controls the operation of drive motors, recording/reproducing heads, a TV tuner etc. of the recorder, jointly represented by box 42. Operating power for the components of the box 42 is provided by a second power supply 43 which may comprise a conventional transformer connected to AC mains via terminals 35, 36 and relay 34.

Under normal operating conditions, the microcontroller 31 is capable of switching power supply 43 on and off by a signal it provides to input port 30. If this signal is positive, so is the base potential of transistor 33, so that the contact between terminals 35, 36 is closed and AC power is provided to power supply 43. If the signal at input port 30 is zero, transistor 33 is nonconductive, relay 34 is open and power supply 43 is off. Based e. g. pre-registered timing information for recording a predetermined TV program, microcontroller 41 may thus switch the power supply 43 on at a predetermined instant in order to enable recording of the program, and switch power supply 43 off again when the recording is finished.

In case of the microcontroller 41 receiving a power failure signal via output port 21, it controls safety measures such as backing up data from volatile memory in permanent memory, placing mobile components of box 42 in a parking position, etc., and at an appropriate instant, depending on the nature and sequence of the safety measures, it commands power supply 43 to be switched off by the signal at input port 30.

Claims

1. A power failure detection circuit (4) comprising
an input port (5) for applying a voltage signal to be monitored;
a voltage rate of change detecting circuit (6-15) connected to said input port (5) for deriving a signal representative of a rate of change of said voltage signal, and
a first comparator (14-16) for comparing said representative signal to a predetermined limit and for outputting a first power failure signal if said representative signal exceeds a predetermined limit.

2. The power failure detection circuit of claim 1, wherein the voltage rate of change detecting circuit (6-15) comprises
a first storage member (9) connected to said input port (5) by a first rectifier (6) for storing a rectified voltage level,
a second storage member (13) connected to said input port (5) by a second rectifier (11) for storing said rectified voltage level,
first dissipating means (10) for decreasing the voltage level stored in said first storage member (9) at a first rate,
and the rate of change representative signal is a voltage between the input sides of said first and second storage members (9, 13).

3. The power failure detection circuit of claim 2, further comprising second dissipating means (10, 14, 15) for decreasing the voltage level stored in said second storage member (13) at a second rate lower than said first rate.

4. The power failure detection circuit of claim 2 or 3, wherein said second rectifier (11) is connected between input sides (8; 12) of said first and second storage members (9; 13).

5. The power failure detection circuit of one of claims 2 to 4, wherein said storage member is a capacitor (9; 13) and said dissipating means is a resistor (10; 10, 14, 15) connected in parallel to said capacitor (9; 13).

6. The power failure detection circuit of one of claims 2 to 5, wherein the comparator (14-16) comprises a voltage divider (14, 15) connected between the input sides (8; 12) of said first and second storage members (9; 13) and a switch (16) controlled by a potential at an intermediate node of said voltage divider (14, 15).

7. The power failure detection circuit of claim 6, wherein said switch (16) is a transistor (16) having current terminals connected to a supply voltage (17) and to the first side (12) of one of said storage members (13), respectively, and a control terminal connected to said intermediate node of said voltage divider (14, 15).

8. The power failure detection circuit of one of claims 2 to 7, wherein the first and second rectifiers (6 11) are half-wave rectifiers that transmit half-waves of a same first polarity type of said voltage signal.

9. A power supply comprising the power failure detection circuit of one of claims 2 to 8 and a third rectifier (23) for deriving a DC supply potential (17).

10. The power supply of claim 9, wherein said a second voltage divider (26, 27) is connected between the input side (12) of one (13) of said first and second storage members and said supply potential (17), the supply potential (17) having a polarity opposite to that of said one input side (12), and a second comparator (28) is provided for deriving a second power failure signal based on a comparison of a voltage at an intermediate node of said second voltage divider (26, 27) and a ground voltage.

11. The power supply of claim 9 or 10, wherein said third rectifier (23) is a half-wave rectifier which derives said supply potential from half-waves of said voltage signal having a second polarity type opposite to the first type.

12. The power supply of one of the preceding claims, wherein the voltage signal to be monitored is a secondary voltage of a transformer (1) having a flyback converter controller (2) connected to a primary side thereof.

Fig. 1

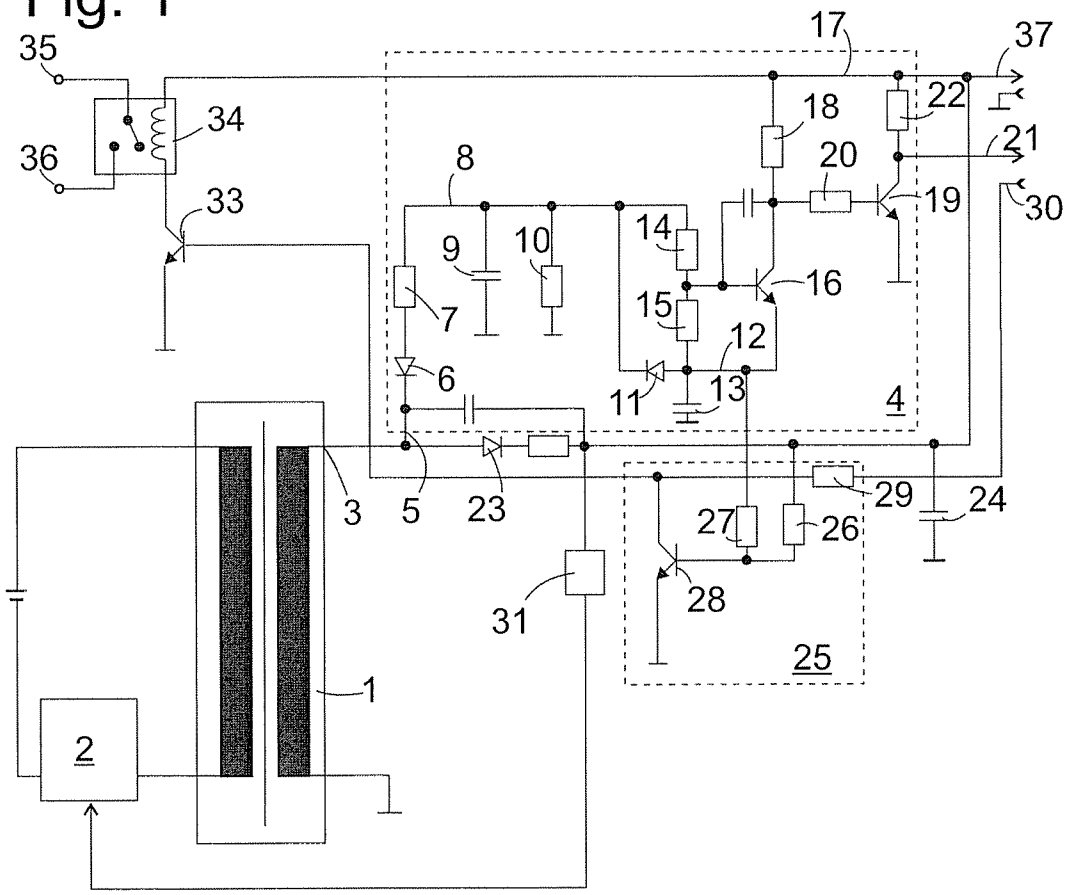
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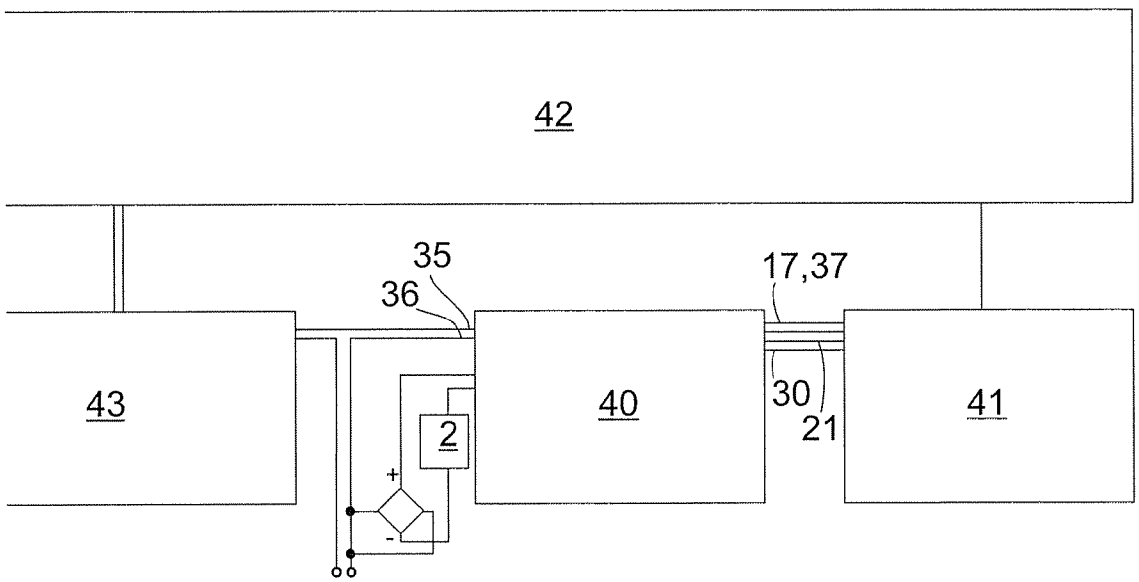
Fig. 2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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/068844

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02H3/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R H02H G06F H02J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
24 August 2007	03/09/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Fritz, Stephan C.

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/068844

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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INTERNATIONAL SEARCH REPORT

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