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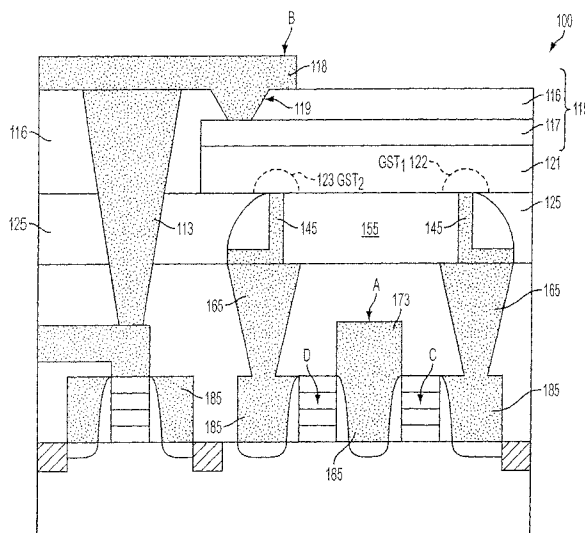


FIG. 2

(57) Abstract: A variable resistance memory element and method of forming the same is disclosed. The memory element includes a substrate supporting a bottom electrode (145) having a small bottom contact area. A variable resistance material (121) is formed over the bottom electrodes such that the variable resistance material has a surface that is in electrical communication with the bottom electrode and a top electrode (117) is formed over the variable resistance material. The small bottom electrode contact area reduces the reset current requirement which in turn reduces the write transistor size for each bit.

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## VARIABLE RESISTANCE MEMORY DEVICE HAVING REDUCED BOTTOM CONTACT AREA AND METHOD OF FORMING THE SAME

### FIELD OF THE INVENTION

[0001] Embodiments of the invention relate to semiconductor devices, and in particular to variable resistance memory elements and methods of forming and using the same.

### BACKGROUND OF THE INVENTION

[0002] Non-volatile memories are important elements of integrated circuits due to their ability to maintain data absent a power supply. Several different typical resistance memory elements using different materials have been suggested for such use. Variable resistance memory elements can be programmed to a resistance value as a way of storing logic data. One suggested type of resistance memory employs phase change materials such as chalcogenide alloys, which are capable of stably transitioning between amorphous and crystalline phases. Each phase exhibits a particular resistance state and the resistance states distinguish the logic values of the memory element. Specifically, an amorphous state exhibits a relatively high resistance, and a crystalline state exhibits a relatively low resistance.

[0003] FIG. 1A shows a basic composition of a variable resistance memory cell 10, which may be implemented using a variable resistance material, and which is constructed over a substrate 11. A variable resistance material 16 is formed between a bottom electrode 14 and a top electrode 18. The bottom electrode is located within an insulating layer 12. The material used to form the electrodes 14, 18 can be selected from a variety of conductive materials, such as tungsten, nickel, tantalum, titanium, titanium nitride, aluminum, platinum, or silver, among others.

[0004] Much research has focused on variable resistance memory devices using chalcogenides. Chalcogenides are alloys of Group VI elements of the periodic table, such as tellurium ("Te") or selenium ("Se") or germanium ("Ge"). A specific chalcogenide currently used in rewriteable compact discs ("CD-RWs") is  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ . In addition to having valuable optical properties that are utilized in CD-RW discs,  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  also has desirable physical properties as a variable resistance material, i.e., phase change material or GST material. For example, various

combinations of Ge, antimony (“Sb”) and Te may be used as variable resistance materials. Specifically, GST material can change structural phases between an amorphous phase and two crystalline phases. The resistance of the amorphous phase (“a-GST”) and the resistances of the cubic and hexagonal crystalline phases (“c-GST” and “h-GST, ” respectively) can differ significantly. The resistance of amorphous GST is greater than the resistances of either cubic GST or hexagonal GST, whose resistances are similar to each other. Thus, in comparing the resistances of the various phases of GST, GST may be considered a two-state material (amorphous GST and crystalline GST), with each state having a different resistance that can be equated with a corresponding binary state. A variable resistance material such as GST whose resistance changes according to its material phase is referred to as a phase change material. The transition from one GST phase to another occurs in response to temperature changes of the GST material.

[0005] In a variable resistance memory cell, heating and cooling of the GST material can occur by causing differing amplitudes of current to flow through the GST material. The GST material is placed in a crystalline state by passing a crystallizing current through the GST material, thus warming the GST material to a temperature wherein a crystalline structure may grow. A stronger melting current is used to melt the GST material for subsequent cooling to an amorphous state. As the typical phase change memory cell uses the crystalline state to represent one logic value, e.g., a binary “1,” and the amorphous state to represent another logic value, e.g., a binary “0,” the crystallizing current is typically referred to as a write current  $I_W$  and the melting current is referred to as an erase or reset current  $I_{RST}$ . One skilled in the art will understand, however, that the assignment of GST states to binary values may be switched if desired.

[0006] The state of the GST material is determined by applying a small read voltage  $V_r$  across the two electrodes and by measuring the resultant read current  $I_r$ . A lower read current  $I_r$  corresponds to a higher resistance  $I_r$  where the GST material is in an amorphous state and a relatively high read current  $I_r$  corresponds to a lower resistance where the GST material is in a crystalline state.

[0007] The phase-changing current is applied to the GST material via a pair of electrodes. In FIG. 1B, for example, the phase-changing currents are applied via the bottom

electrode 14 and the top electrode 18. Because of the configurations of the bounding surface areas of the two electrodes 14, 18, current densities 50 within the GST material are not equally distributed. In particular, current densities 50 near the bottom electrode 14 are greater than the densities near the top electrode 18. Furthermore, areas of the GST material that are directly in between the two electrodes 14, 18 have higher current densities 50 than areas that are not directly in between the two electrodes 14, 18 such as areas near the lower corners of the GST material.

[0008] A sought after characteristic of non-volatile memory is low power consumption. Often, however, conventional variable resistance memory elements require large operating currents. It is therefore desirable to provide variable resistance memory elements with reduced current requirements. For variable resistance memory elements, it is necessary to have a current density that will heat the variable resistance material past its melting point and quench it in an amorphous state. One way to increase current density is to decrease the size of the bottom electrode. These methods maximize the current density at the bottom electrode interface to the variable resistance material. Although conventional solutions are typically successful, it is desirable to further reduce the overall current in the variable resistance memory element, thereby reducing power consumption in certain applications.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIGS. 1A and 1B illustrate a prior art variable resistance memory cell.

[0010] FIG. 2 illustrates an embodiment of the invention described herein.

[0011] FIG. 3 illustrates the embodiment of FIG. 2 at an initial stage of processing.

[0012] FIG. 4 illustrates the embodiment of FIG. 2 at a stage of processing subsequent to that shown in FIG. 3.

[0013] FIG. 5 illustrates the embodiment of FIG. 2 at a stage of processing subsequent to that shown in FIG. 4.

[0014] FIG. 6 illustrates the embodiment of FIG. 2 at a stage of processing subsequent to that shown in FIG. 5.

[0015] FIG. 7 illustrates the embodiment of FIG. 2 at a stage of processing subsequent to that shown in FIG. 6.

[0016] FIG. 8 illustrates the embodiment of FIG. 2 at a stage of processing subsequent to that shown in FIG. 7.

[0017] FIG. 9 illustrates the embodiment of FIG. 2 at a stage of processing subsequent to that shown in FIG. 8.

[0018] FIG. 10 illustrates the embodiment of FIG. 2 at a stage of processing subsequent to that shown in FIG. 9.

[0019] FIG. 11 illustrates the embodiment of FIG. 2 at a stage of processing subsequent to that shown in FIG. 10.

[0020] FIG. 12 illustrates the embodiment of FIG. 2 at a stage of processing subsequent to that shown in FIG. 11.

[0021] FIGS. 13A illustrates a top-down perspective view at the processing state illustrated in FIG. 12 and FIG. 13B illustrates a top-down view at a stage of processing subsequent to that shown in FIG. 13A, of a memory array according to an embodiment described herein.

[0022] FIG. 14 illustrates an electrical schematic of a memory cell according to an embodiment described herein.

[0023] FIG. 15 illustrates an array of phase change memory bit structures according to an embodiment described herein.

[0024] FIG. 16 illustrates a processor system that includes a memory device according to an embodiment described herein.

## DETAILED DESCRIPTION OF THE INVENTION

[0025] In the following detailed description, reference is made to various specific embodiments. These embodiments are described with sufficient detail to enable those skilled in the art to practice the claimed invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made.

[0026] The term “substrate” used in the following description may include any supporting structure including, but not limited to, a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures, including those made of semiconductors other than silicon. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation. The substrate also need not be semiconductor-based, but may be any support structure suitable for supporting an integrated circuit structure, including, but not limited to, metals, alloys, glasses, polymers, ceramics, and any other supportive materials as is known in the art.

[0027] The embodiments of the invention are now explained with reference to the figures, which throughout which like reference numbers indicate like features. FIGS. 2-14 illustrate an example process for forming a variable resistance memory element 100 which has smaller electrodes than other phase change memory devices and which can operate with reset currents which are smaller compared with other phase change memory devices.

[0028] In order to reduce the reset current requirement for a writing bit, the embodiments herein describe process flows for producing a sub 1000 nm<sup>2</sup> bottom contact area that provides excellent contact area uniformity across a wafer. The small bottom electrode contact area reduces the reset current requirement, which in turn reduces the write transistor size for each bit. The resulting contact area is very scalable and the only variation is the critical dimension (“CD”) control of the bit lines in one direction. Several methods of contact area reduction are known in the art including contact hole CD reduction using a spacer, annular donut shaped contacts, and edge

contacts. The embodiments described herein, however, provide advantages over the known methods and results in CD/area uniformity control and printing and etching only straight lines with only one direction CD control.

[0029] The resulting variable resistance memory element, e.g., phase change memory element, shown in an embodiment depicted by FIG. 2, includes a substrate supporting bottom electrodes 145 having a sub 1000 nm<sup>2</sup> bottom contact area. A phase change material 121 is formed over the bottom electrodes 145 such that the phase change material 121 has a surface that is in electrical communication with the bottom electrode 145. A top electrode 117 is formed over the phase change material 121 and is in electrical communication with phase change material 121 and bottom electrode 145. One method of forming the FIG. 2 structure is now described.

[0030] Referring to FIG. 3, a gate oxide material 130 is formed on top of a substrate 110 having STI regions 120 formed therein. The gate oxide material 130 is removed from above the STI regions 120. Next, as shown in FIG. 4, a conductive material 140, e.g., a polysilicon material, is blanket deposited, and then a metal material 150, i.e., a Ti/WN material, is blanket deposited. Then, a tungsten (W) material 160 is blanket deposited, and finally a nitride material 170 is blanket deposited. Each material is blanket deposited above the previously formed material. Blanket deposition can be done by known methods. Materials 130, 140, 150, 160 and 170 comprise the materials that will form transistor gate stacks (described below). It should be appreciated that the gate stacks can also be formed in a number of different combinations and/or of different materials.

[0031] As shown in FIG. 5, nitride material 170 is etched except for areas above where the desired gate stacks will be formed. Any etching method known in the art can be used such as using photolithography mask and wet or dry etching techniques. Using nitride material 170 as a mask, materials 140, 150 and 160 are etched by any technique, as shown in FIG. 6, to form the desired gate stacks 171. Then, source/drain regions 180 are formed in the substrate 110 on both sides of the gate stacks 171. It should be appreciated that the source/drain regions 180 are preferably formed after gate stacks 171 have been formed, however, they may be also formed before the gate stack materials 130, 140, 150, and 160 are blanket deposited. A nitride spacer 190 is then

deposited and etched to form sidewalls 191 of the gate stacks 171. An insulating material 195 is deposited and planarized to fill-in the space between each gate stack 171, as shown in FIG. 7. The insulating material 195 is typically formed of a boron-phosphate-silicon-glass (BPSG), but can be formed using any other known insulating material. Subsequently, as shown in FIG. 8, conductive plugs 185 (also referred to as local interconnects) are formed. The conductive plugs 185 are formed by etching trenches in insulating layer 195 and then filling the trenches with a metal or conductive material followed by planarizing any excess metal material from above insulating material 195. Chemical mechanical planarization (CMP) or other known methods can be used to remove the excess metal material from the surface of the insulating material 195. The conductive plugs 185 may be any generally known conductive material that is used in the art such as tungsten, platinum, gold, copper, aluminum, etc.

[0032] As shown in FIG. 9, an insulating material 174 is blanket deposited above insulating material 195. Within insulating material 174, a trench is etched and filled with a bit line 173 above one of the conductive plugs 185. Then, another layer of insulating material 175 is deposited above insulating material 195, the previously deposited insulating material 174 and the metal bit line 173. After insulating material 175 is deposited, another set of trenches are etched into insulating material 175 and another set of conductive plugs 165 are formed. The conductive plugs 165 are formed by filling the trenches with a metal or conductive material and planarizing the excess material from above insulating material 175. Conductive plugs 165 extend conductive plugs 185 to the top surface of insulating material 175.

[0033] Referring to FIG. 10, another insulating material 155 is formed above insulating material 175 and conductive plugs 165. Then, trenches 147 are etched into insulating material 155 being a patterned area 155' on either side of the trenches. Any etching method known in the art can be used to etch the trenches. A metal material 145, preferably TiN, is deposited within the trenches 147 and above insulating materials 155 and 175. Then, a nitride material 135 is blanket deposited above metal material 145. The nitride material 135 and metal material 145 are etched back and removed, preferably a spacer etch, from above insulating material 155, as shown in FIG. 11.



[0034] The surface of insulating material patterned area 155' and portions of insulating material 175 are exposed. FIG. 12 shows another insulating material 125 which is formed above insulating materials 155 and 175. FIGS. 13A and 13B illustrate a memory array 101 from a top-down perspective view at the processing state illustrated in FIG. 12. As shown in the top-down perspective of FIG. 13A, the top edges of metal material 145 remains exposed at the surface of insulating material 125. Materials 125, 145 are patterned etched perpendicular to the formed metal material 145 lines and etched down to insulating area 155' and portions of insulating material 175. Then, an insulating material is blanket deposited and is planarized to the top level of insulating area 155' (FIG. 13B) to expose the top edges of the formed metal material 145. The resulting metal material 145, which forms a bottom electrode, is preferably formed in an I-shaped configuration (FIG. 2). Metal material 145, however, can be formed in a number of various shapes given that the top surface or exposed surface of the shape provides a small contact area. Each contact, bottom electrode 145 is individually isolated by the insulating material 125. In other words, no direct conductive path exists from one bottom electrode 145 to another.

[0035] The metal material 145, which serves as a bottom electrode to the formed phase change memory element 100 (FIG. 2), is visible at predetermined spaced distances throughout the array 101. The remaining visible surface of the array 101 is comprised of insulating material 125 and areas 155'.

[0036] Referring back to FIG. 2, a phase change material 121 is thereafter deposited onto the planarized bottom electrodes 145 and the insulating materials 125, 155'. The phase change material 121 may be any of the various variable resistance materials listed above or may be a specific composition of GST. A top electrode 117 is deposited on top of the phase change material 121 by any method. For example, the phase change material 121 and top electrode 117 may be blanket deposited one after the other and then etched back to the top level of insulating material 155 to form memory elements with a top electrode. Thereafter, another insulating layer 116 is formed and planarized and trenches 119, 113 etched and filled with a conductive material 118. The top electrode 117 is generally, but not required to be, formed of the same material as the bottom electrode 145. Metal material 118 connects and provides an electrical connection through trench

119 to top electrode 117. Metal material 118 is blanket deposited and patterned such that a portion is removed from insulating material 116.

[0037] Referring to FIGS. 2 and 14, the final structure comprises electrodes A, B respectively forming a bit line and cell select line, phase change memory elements GST1, GST2, 122, 123 as well as transistor gates C, D formed as respective word lines. FIG. 14 reflects an electrical schematic corresponding to the structure depicted in FIG. 2. Conductive plugs 165, 185 form an electrical communication between bit line 173 and electrodes 145, 117. Electrodes 145, 177 can continue electrical communication via conductive materials 118, 119 to periphery circuitry through periphery conductive plugs such as conductive plug 113. The described electrical communication paths correspond to the electrical schematics and illustrations of FIGS. 14-16.

[0038] The resulting phase change memory element has a low power consumption and provides reduced current requirements by achieving a small bottom contact area for electrodes 145 which, as noted, has an area of less than  $1000 \text{ nm}^2$ . Although having a smaller bottom contact area than other phase change memory elements, the memory element still achieves an increased current density that will heat the phase change material past its melting point and quench it in an amorphous state. This maximizes the current density at the bottom electrode interface to the phase change material.

[0039] FIG. 14 also labels one memory cell 1315 as having a bit line 1340, a cell select line 1320, a word line 1330 and a memory element 1310. The memory element 1310 is connected to a cell select line 1320 via top electrode B. The other memory element electrode 145 is connected to an access transistor 1350. The access transistor 1350 is gated by a word line 1330. Bit line 1340 provides a source to the access transistor 1350 and is connected to the memory element 1310 when the access transistor 1350 is activated by the word line 1330.

[0040] The memory cell 1315 of FIG. 14 may be arranged in an array of like memory cell structures, as illustrated in FIG. 15. In FIG. 15, a memory device 1400 includes one or more arrays of memory bit structures 1315a-1315p. The memory cell structures 1315a-1315p are arranged in rows and columns. The rows and columns may be partially staggered or may be aligned as a simple parallel grid as in FIG. 15. The memory cell structures 1315a-1315p along any given

cell select line 1420a-1420d do not share a common word line 1430a-1430d. Additionally, the memory cell structures 1315a-1315p along any given cell select line 1420a-1420d do not share a common bit line 1440a-1440d. In this manner, each memory bit structure is uniquely identified by the combined selection of the word line to which the gate of the memory cell access device is connected, and the cell select line to which the memory cell is connected.

[0041] Each word line 1430a-1430d is connected to a word line driver in the form of a row decoder 1460 for selecting the respective word line for an access operation. Similarly, each cell select line 1420a-1420d is coupled to a driver in the form of a column decoder 1450. The current passing through a selected memory bit structure 1315a-1315p is measured by sense amplifiers 1470a, 1470d connected respectively to the cell select lines 1420a-1420d.

[0042] For simplicity, FIG. 15 illustrates a memory array having only four rows of memory cell structures 1315a-1315p on four cell select lines 1420a-1420d and four columns of memory cell structures 1315a-1315p on four word lines 1430a-1430d. However, it should be understood that in practical applications, the memory device 1400 has significantly more memory cell structures in one or more arrays.

[0043] It should be appreciated that the improved phase change memory cell 100 may be fabricated as part of an integrated circuit. The corresponding integrated circuits may be utilized in a typical processor system. For example, FIG. 16 illustrates a simplified processor system 1500 which includes a memory device 1400 employing improved phase change memory cells in accordance with the above described embodiments. A processor system, such as a computer system, generally comprises a central processing unit (CPU) 1510, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 1520 over a bus 1590. The memory device 1400 communicates with the CPU 1510 over bus 1590, typically through a memory controller.

[0044] In the case of a computer system, the processor system may include peripheral devices such as removable media devices 1550 which communicate with CPU 1510 over the bus 1590. Memory device 1400 is preferably constructed as an integrated circuit, which includes one or

more phase change memory devices. If desired, the memory device 1400 may be combined with the processor, for example CPU 1510, as a single integrated circuit.

[0045] It should also be appreciated that various embodiments have been described as using a phase change material as an exemplary variable resistance material. The invention may also be used in other types of resistive memory to improve current flow through whatever variable resistance material is used.

[0046] The above description and drawings should only be considered illustrative of example embodiments that achieve the features and advantages described herein. Modification and substitutions to specific process conditions and structures can be made. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

## CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of fabricating a variable resistance memory element comprising:
  - forming an insulating material having a sidewall;
  - forming a first electrode on the sidewall of the insulating material and having a top surface;
  - forming an insulating spacer on a side of the first electrode opposite the sidewall;
  - forming a variable resistance material having a first surface and a second surface, the first surface abutting the top surface of the first electrode and portions of the insulating material; and
  - forming a second electrode in electrical contact with the second surface of the variable resistance material.
2. The method of claim 1, wherein forming the first electrode comprises forming the first electrode with a top surface of less than  $1000 \text{ nm}^2$ .
3. The method of claim 1, wherein forming the first electrode comprises forming the first electrode to be configured in a l-shape.
4. The method of claim 1, wherein forming the first electrode and forming the variable resistance material comprise blanket depositing the first electrode and the variable resistance material one after the

other and then etching back both materials to the top level of the formed insulating spacer.

5. The method of claim 4, further comprising:

forming a second insulating material above the second electrode;

etching at least one trench into the formed second insulating material;

and

filling the at least one trench with a conductive material.

6. The method of claim 1, wherein forming the variable resistance material comprises forming the variable resistance material between the first electrode and second electrode.

7. The method of claim 1, further comprising:

forming a memory bit line;

forming at least one access transistor coupled between the bit line and one of the first and second electrodes; and

forming a cell select line coupled to the either of the first and second electrodes.

8. The method of claim 1, further comprising:

forming a memory bit line;

forming at least one access transistor coupled between the bit line and the first electrode; and

forming a cell select line coupled to the second electrode.

9. A method of fabricating a variable resistance memory cell comprising:
  - forming a bottom electrode having a contact area of less than  $1000 \text{ nm}^2$  and an l-shape within an insulating material;
  - forming a variable resistance area from variable resistance material over a top surface of the bottom electrode and a top surface of the insulating layer proximate the bottom electrode; and
  - forming a top electrode over a top surface of the variable resistance area.
10. The method of claim 9, wherein forming a variable resistance area comprises forming the area from a phase change material.
11. The method of claim 9, wherein forming the variable resistance area comprises forming the variable resistance area between the top and bottom electrodes.
12. A method of fabricating a phase change memory cell comprising:
  - forming a first electrode having a contact area of less than  $1000 \text{ nm}^2$  within an insulating material;
  - forming a phase change area from phase change material deposited over a first surface of the first electrode and a first surface of the insulating layer proximate the first electrode; and
  - forming a second electrode over a first surface of the phase change area.
13. The method of claim 12, wherein forming the first electrode and forming the second electrode comprise forming first and second electrodes from different materials.

14. The method of claim 12, wherein forming the first electrode comprises forming the first electrode in an l-shaped configuration.
15. A variable resistance memory cell comprising:
  - an insulating material element;
  - a first electrode on a sidewall of the insulating material element and having a top surface;
  - an insulating spacer material on a side of the electrode opposite the sidewall;
  - a variable resistance material having a first surface and a second surface, the first surface abutting the top surface of the first electrode and portions of the insulating material element; and
  - a second electrode in electrical contact with the second surface of the variable resistance material.
16. The variable resistance memory cell of claim 15, further comprising a memory bit line, at least one access transistor coupled between the bit line and one of the first and second electrodes, and a cell select line coupled to the either of the first and second electrodes.
17. The variable resistance memory cell of claim 15, further comprising a memory bit line, at least one access transistor coupled between the bit line and the first electrode, and a cell select line coupled to the second electrode.
18. The variable resistance memory cell of claim 15, wherein the variable resistance material is a phase change material.



19. The variable resistance memory cell of claim 15, wherein the top surface of said first electrode is approximately  $1000 \text{ nm}^2$ .
20. The variable resistance memory cell of claim 15, wherein the first electrode is l-shaped.
21. The variable resistance memory cell of claim 15, further comprising a second memory cell formed adjacent to the first memory cell, the first and second memory cells being paired cells in parallel electrical connection, each being contacted by separate word lines.
22. The variable resistance memory cell of claim 21, wherein the first and second memory cells share the same variable resistance material.
23. A phase change memory array comprising:
  - a plurality of word lines;
  - a plurality of cell select lines;
  - a plurality of bit lines; and
  - a plurality of phase change memory bit structures, each structure including an access device and a phase change memory element, the memory element being connected with one of the plurality of cell select lines and coupled with one of the plurality of bit lines through the access device gated by one of the plurality of word lines, each memory element comprising:
    - an insulating structure;
    - a bottom electrode formed between the insulating structure and a nitride spacer;

a variable resistance material with a first surface and a second surface, the first surface abutting a top portion of the bottom electrode and portions of the insulating layer; and

a top electrode in electrical communication with the second surface of the variable resistance material.

24. The phase change memory array of claim 23, wherein the top portion of said bottom electrode has a contact area of less than  $1000 \text{ nm}^2$ .
25. The phase change memory array of claim 23, wherein the bottom electrode has an l-shaped configuration.
26. The phase change memory array of claim 23, wherein the variable resistance material is a phase change material.

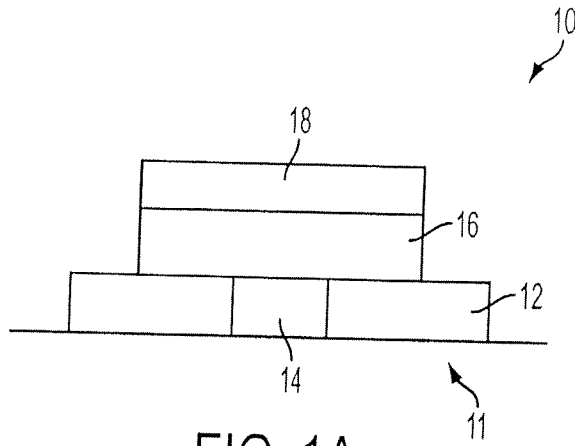


FIG. 1A

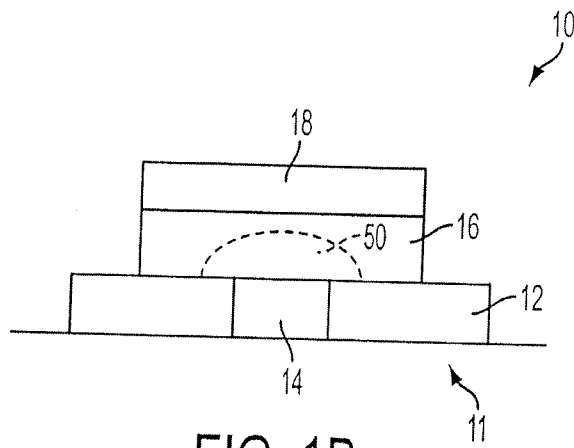


FIG. 1B

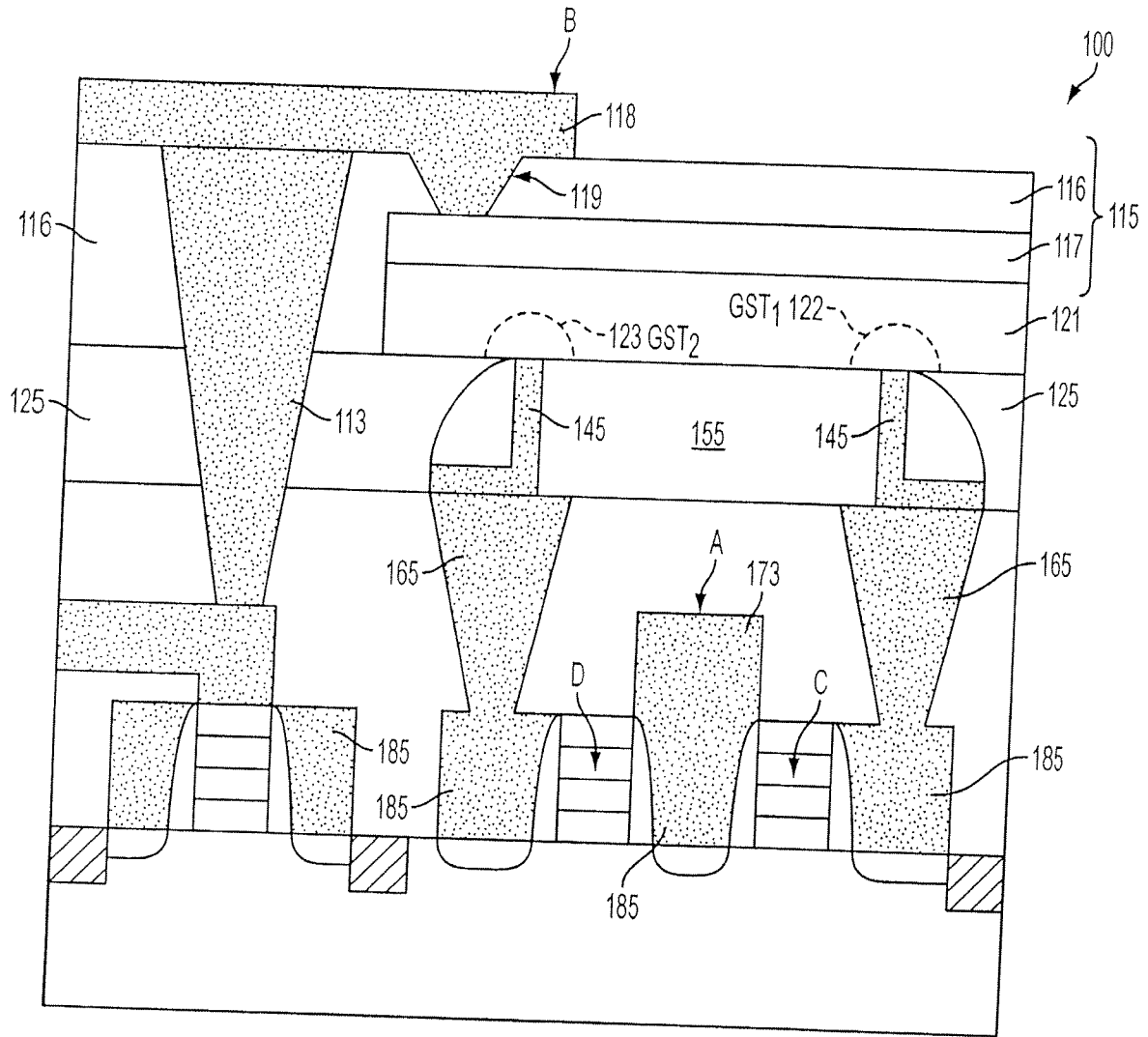


FIG. 2

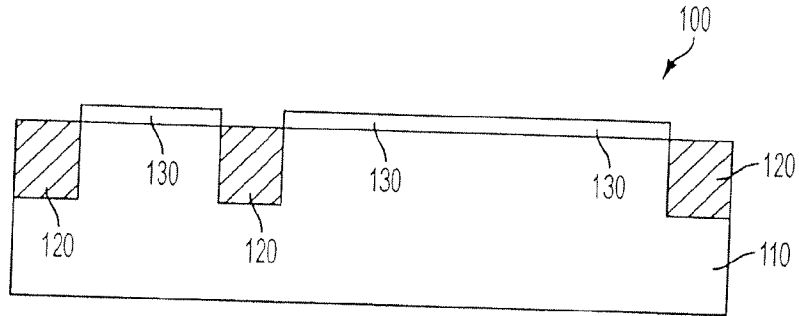


FIG. 3

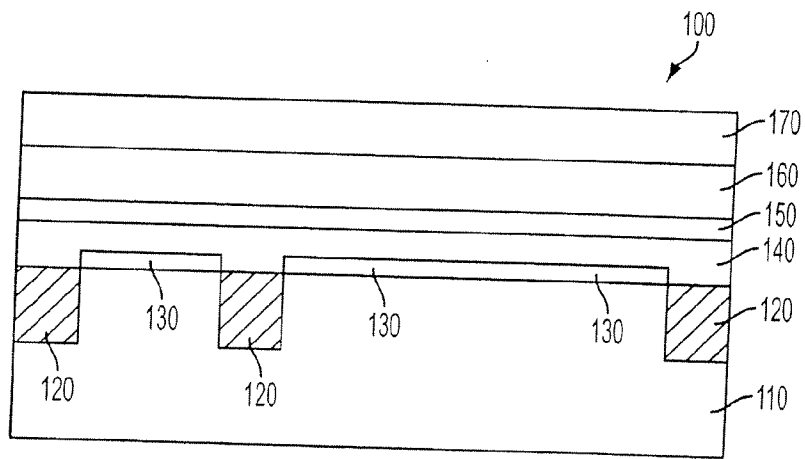


FIG. 4

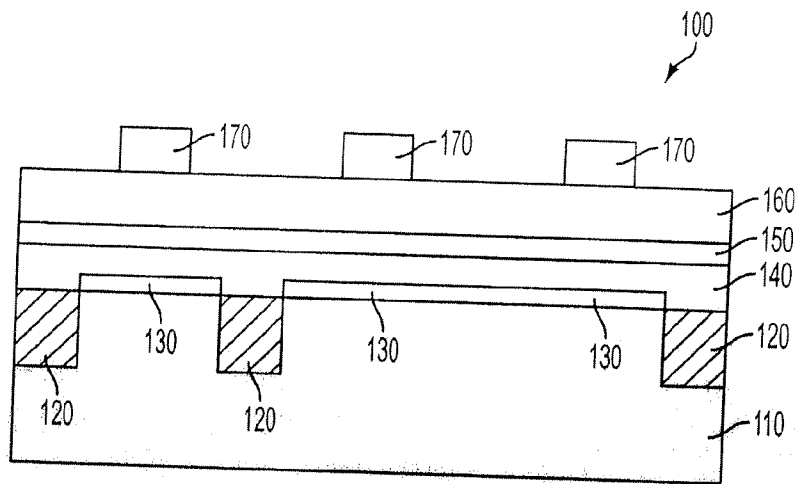


FIG. 5

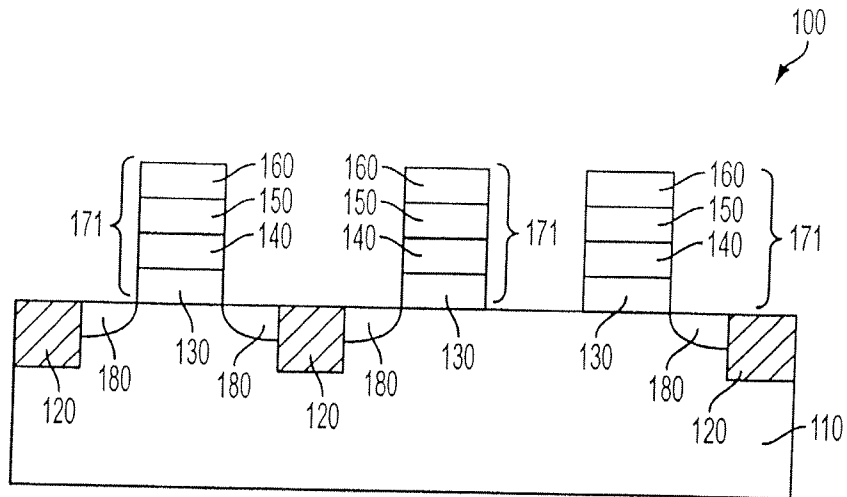


FIG. 6

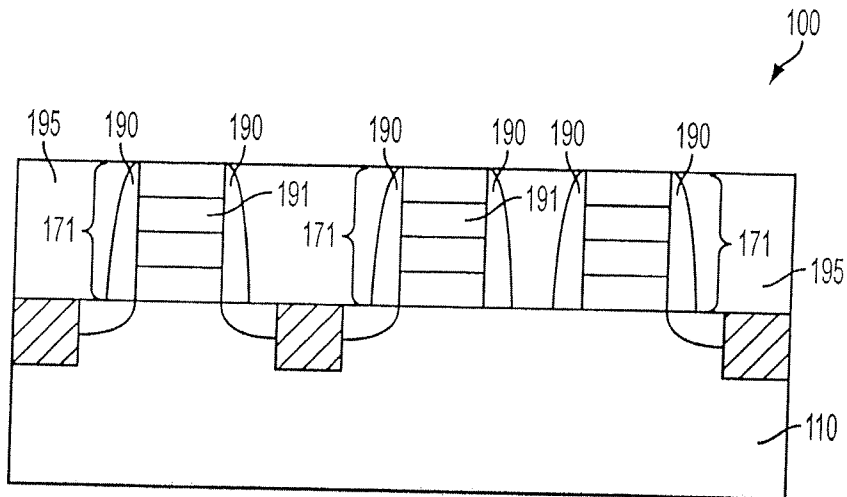


FIG. 7

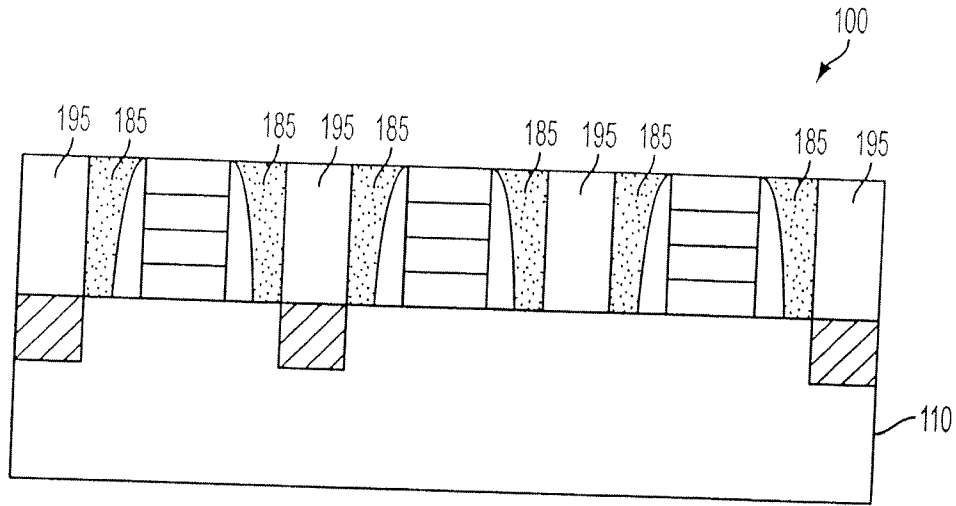


FIG. 8

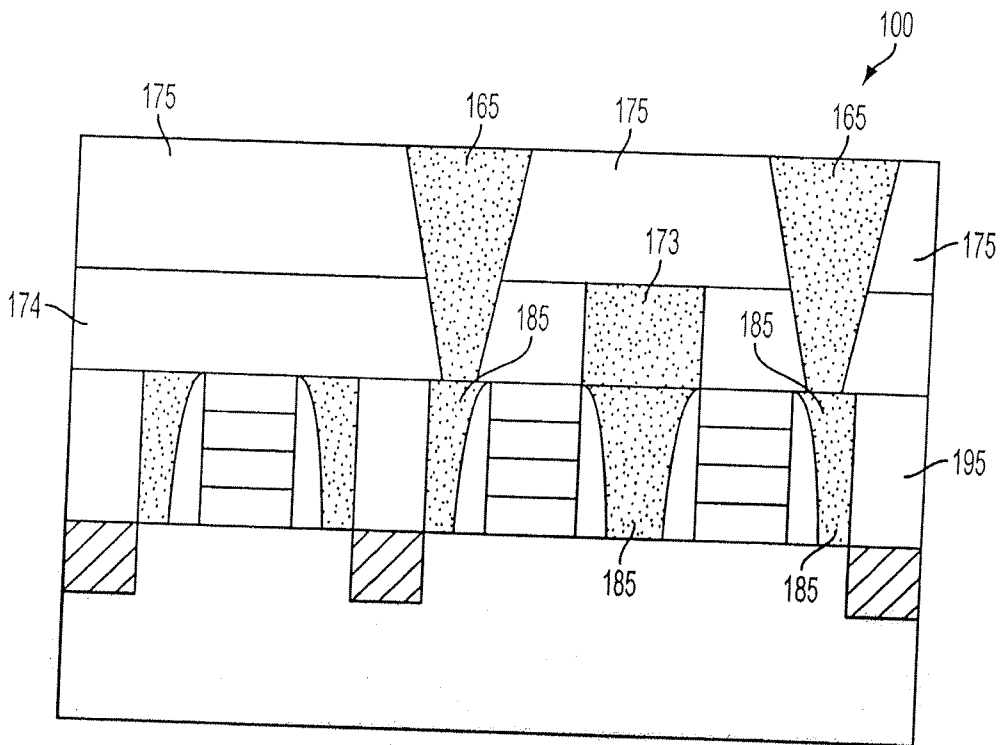


FIG. 9

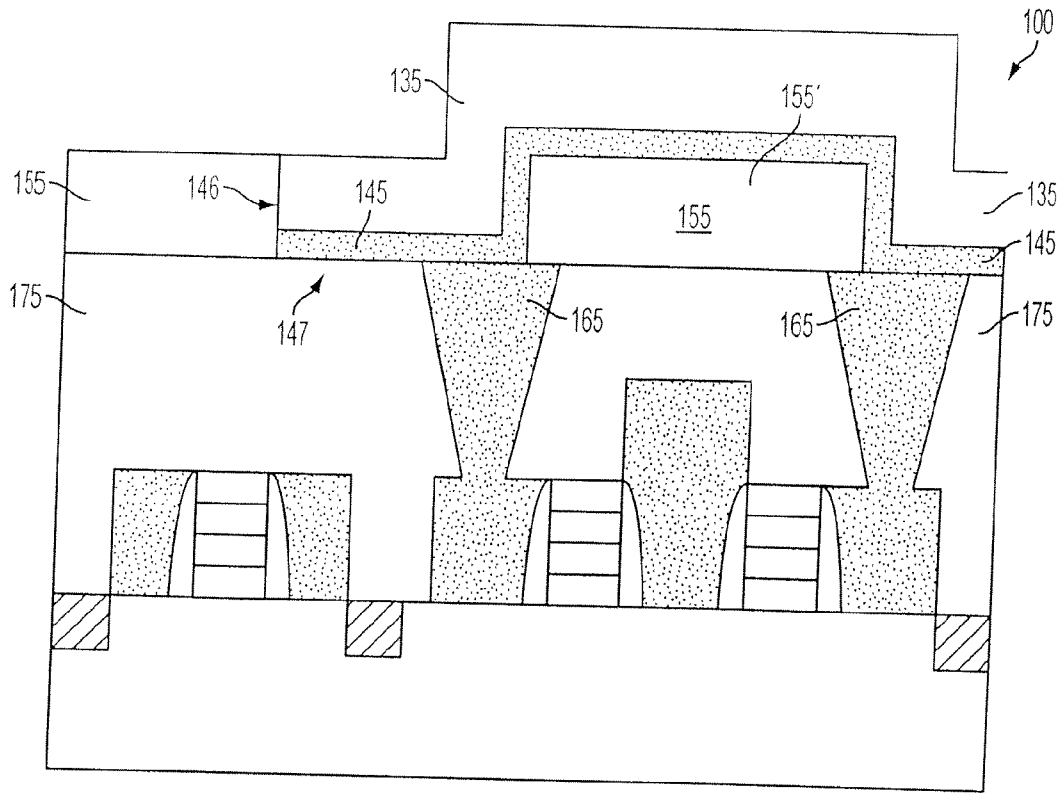


FIG. 10

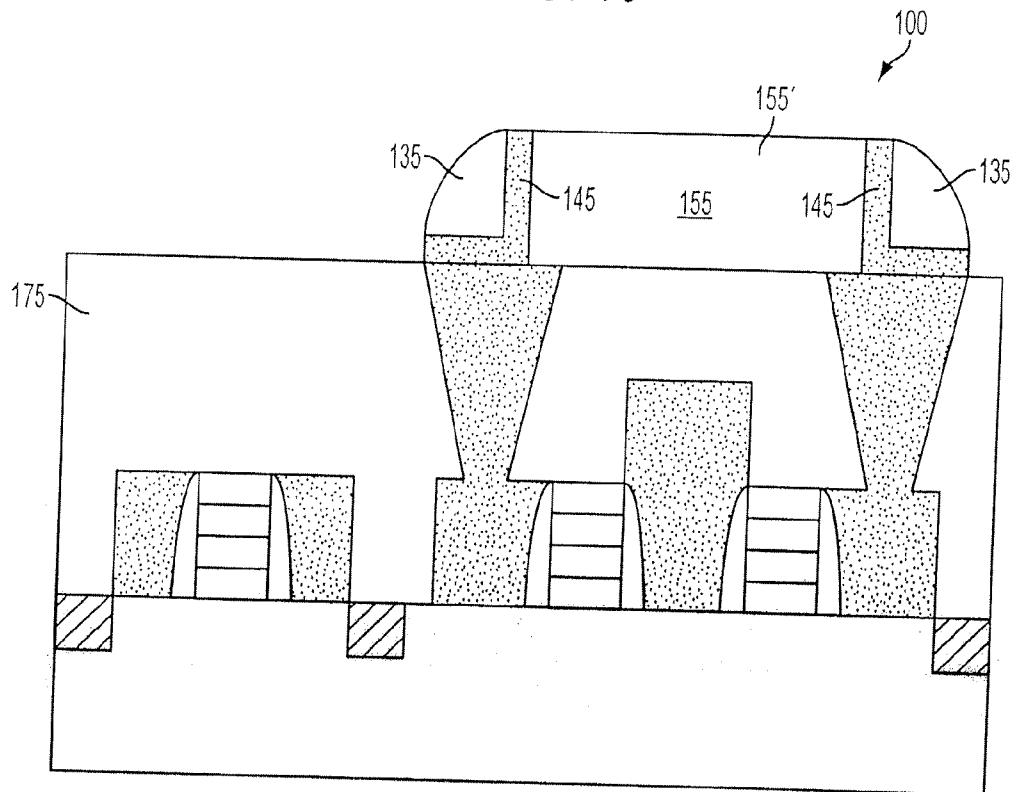


FIG. 11



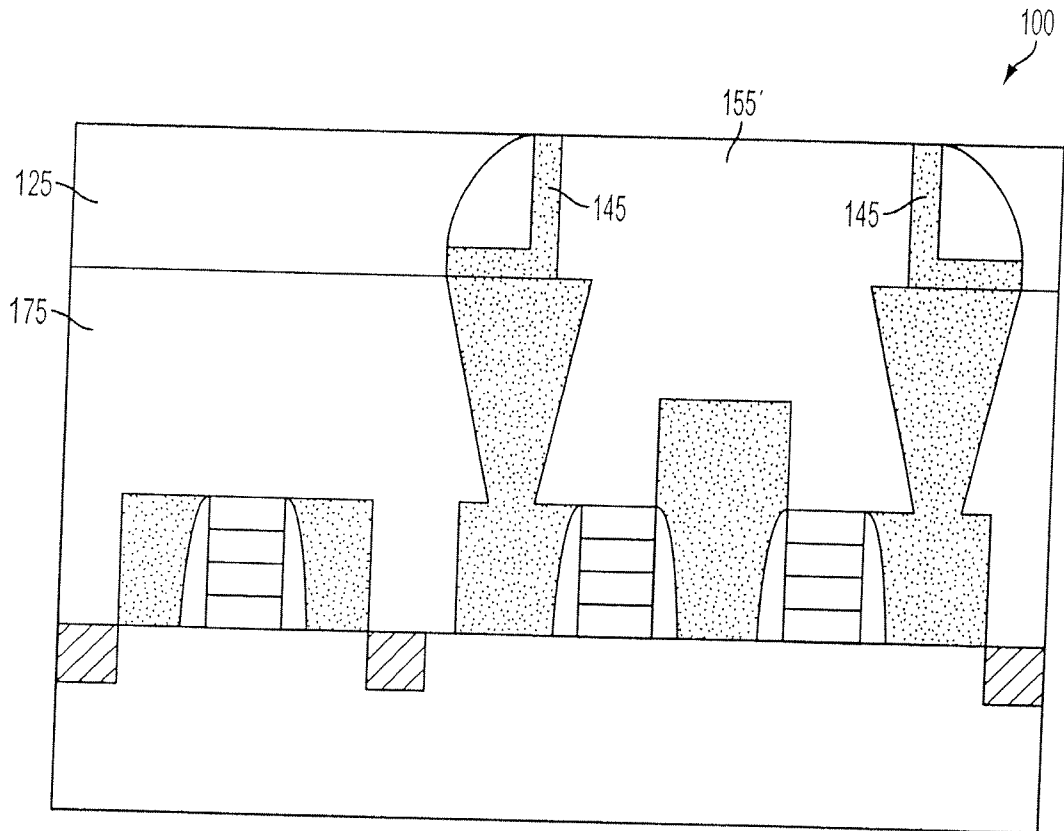


FIG. 12

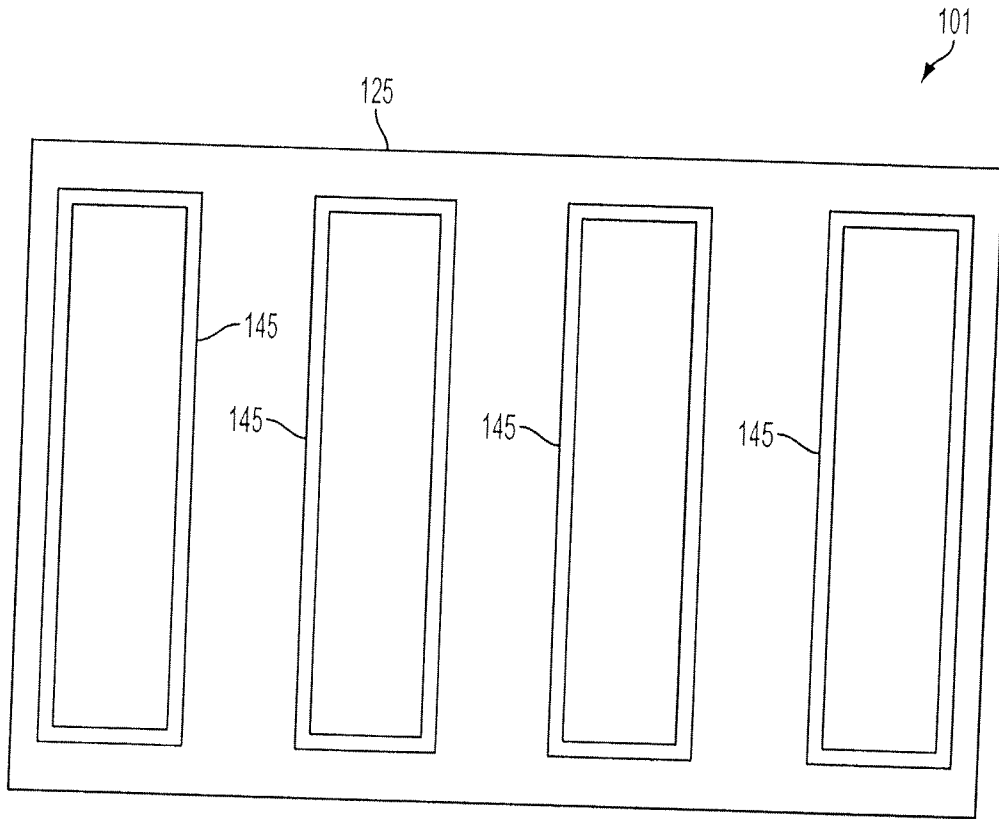


FIG. 13A

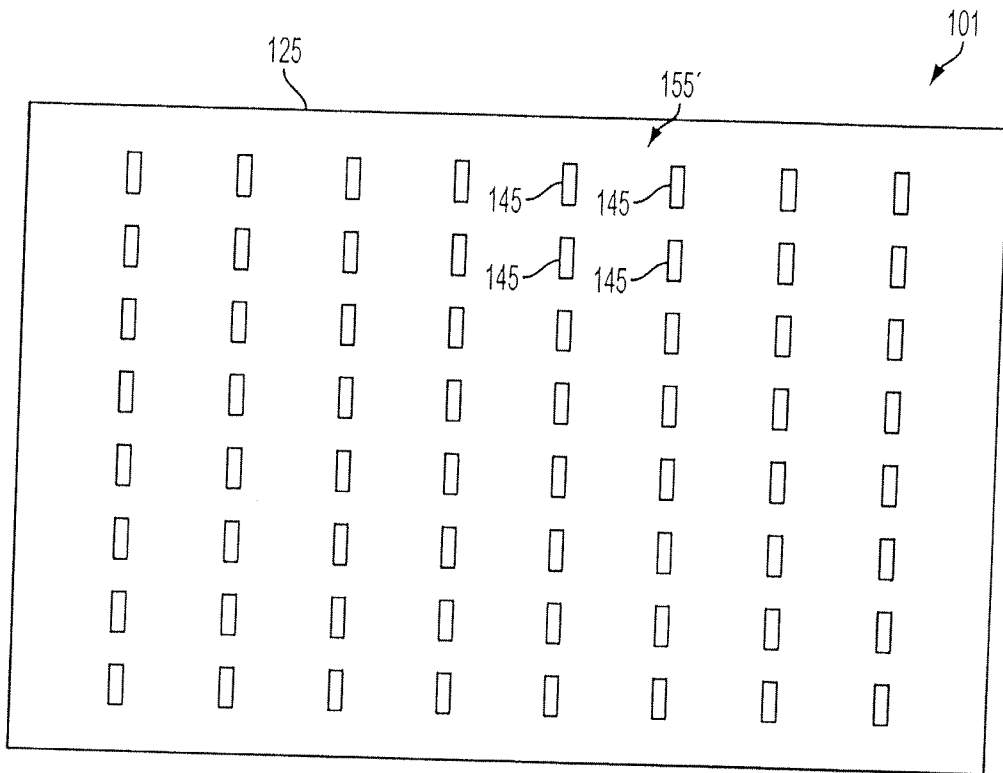


FIG. 13B

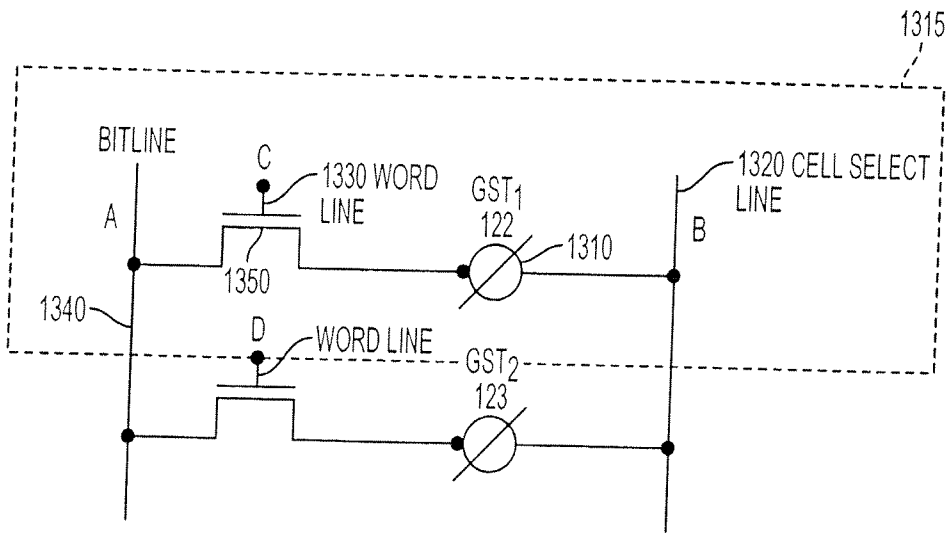


FIG. 14

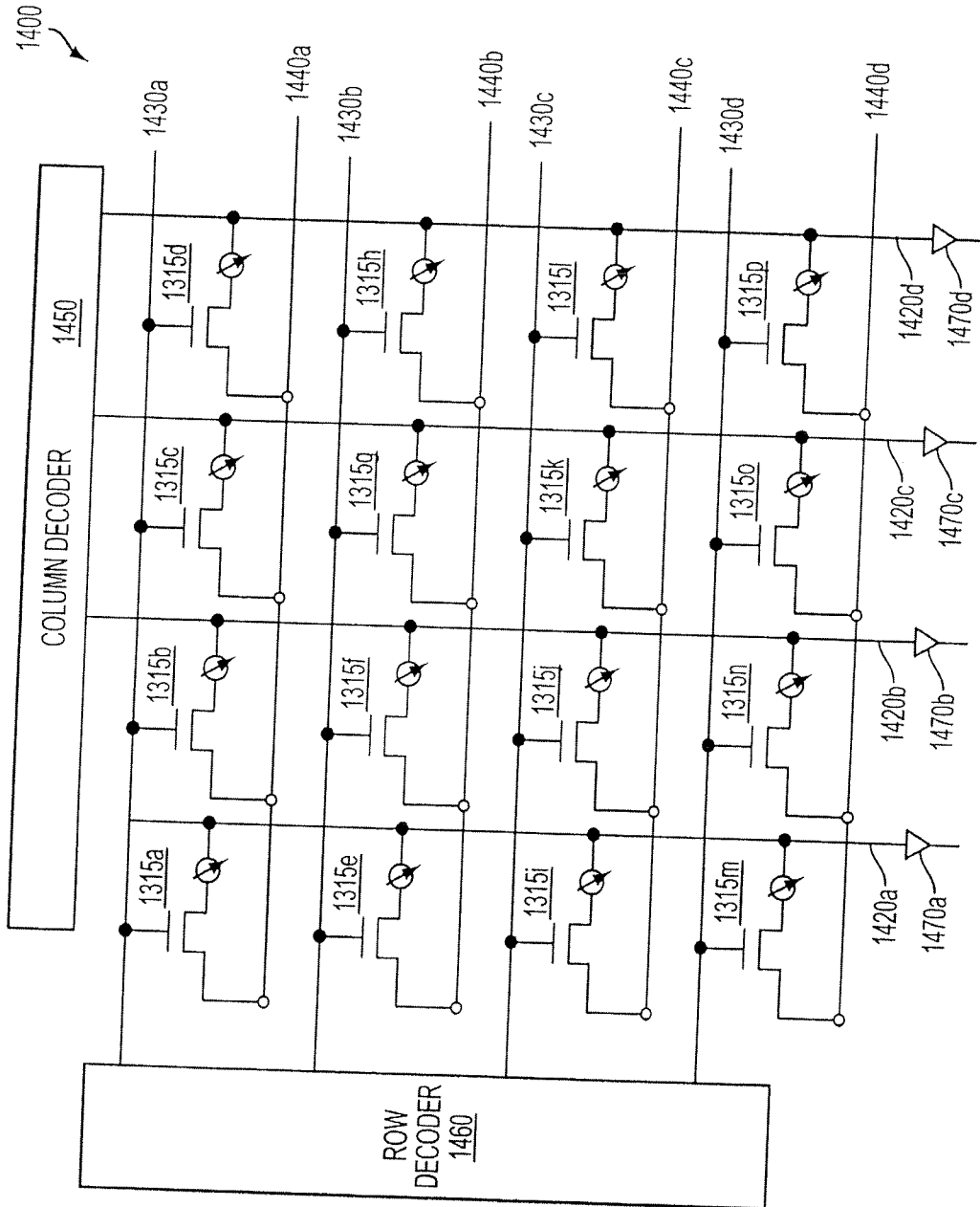


FIG. 15

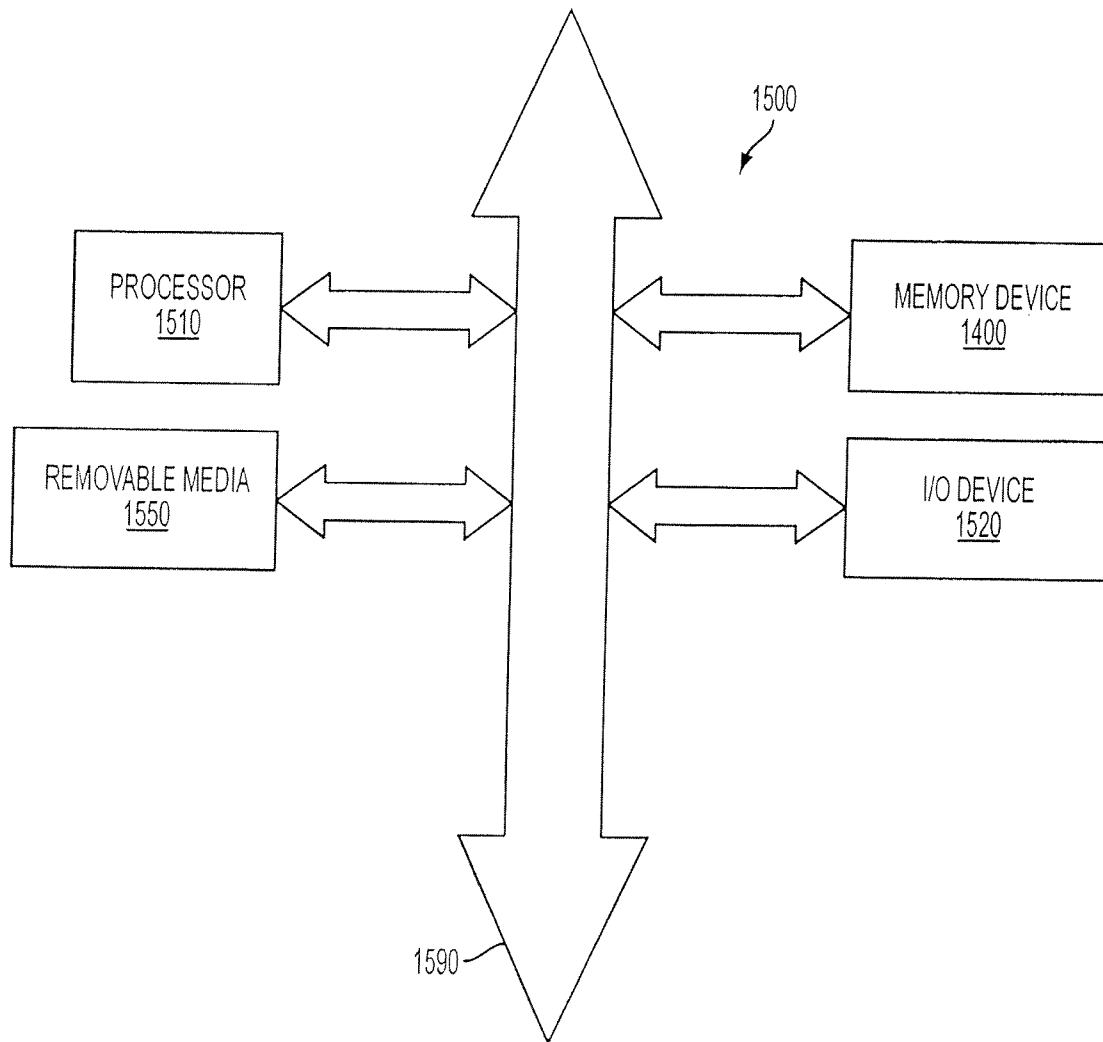


FIG. 16

**INTERNATIONAL SEARCH REPORT**

International application No  
PCT/US2008/061841

**A. CLASSIFICATION OF SUBJECT MATTER**  
INV. H01L45/00 H01L27/24

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                  | Relevant to claim No.     |
|-----------|---|---------------------------|
| X         | US 2006/138467 A1 (LUNG HSIANG-LAN [TW])<br>29 June 2006 (2006-06-29)   | 1-4, 6,<br>9-15,<br>18-20 |
| Y         | paragraphs [0036], [0037], [0045] -<br>[0048]; figures 1,6-12,20-22   | 5,7,8,<br>16,17,<br>21-26 |
| Y         | US 2006/209585 A1 (TANIZAKI HIROAKI [JP]<br>ET AL) 21 September 2006 (2006-09-21)<br>figures 10,11,43,44A           | 7,8,16,<br>17,21-26       |
| Y         | US 2006/176724 A1 (ASANO ISAMU [JP] ET AL)<br>10 August 2006 (2006-08-10)<br><br>figures 16,17                      | 5,7,8,<br>16,17,<br>23-26 |
| A         | US 2007/020799 A1 (CHOI SUK-HUN [KR] ET<br>AL) 25 January 2007 (2007-01-25)<br>paragraphs [0064], [0065]; figure 5F | 23                        |

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See patent family annex.

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Date of the actual completion of the international search

Date of mailing of the international search report

17 September 2008

26/09/2008

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International application No  
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| Patent document<br>cited in search report |    | Publication<br>date |    | Patent family<br>member(s) |  | Publication<br>date |
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