

- [54] **PHASE-LOCK-LOOP FM-STEREO DECODER INCLUDING STEREOPHONIC/MONOPHONIC BLEND SYSTEM FOR REDUCING AUDIO DISTORTION**
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- [51] Int. Cl. .... **H04h 5/00**
- [58] Field of Search ..... **179/15 BT; 329/122, 50, 329/123; 325/305, 400, 427, 420, 472**

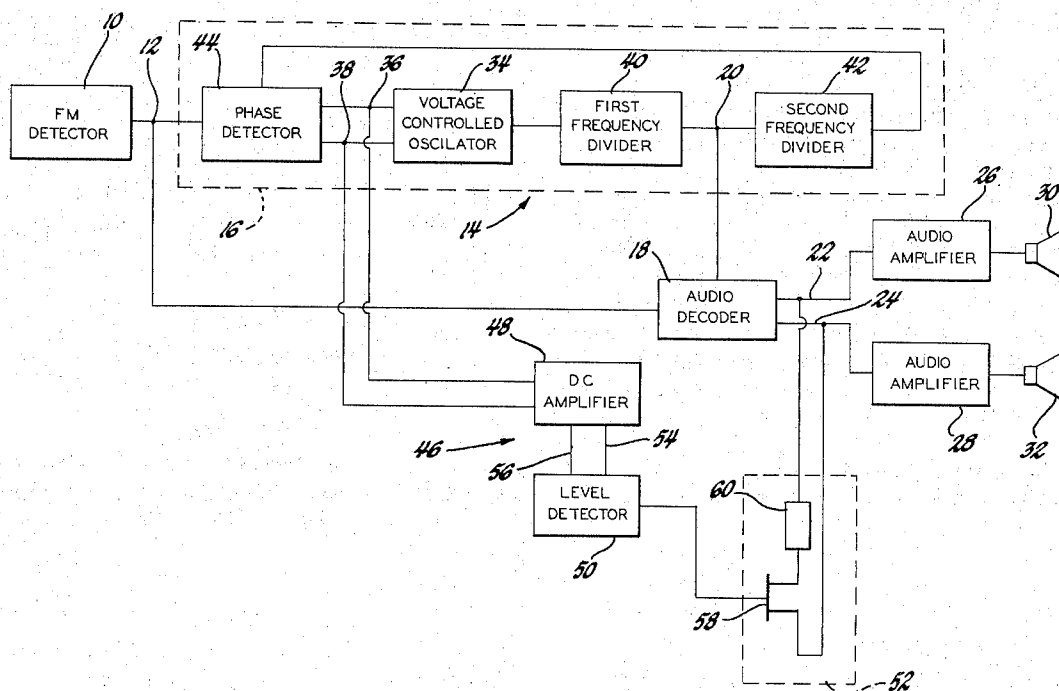
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- [57] **ABSTRACT**
- An FM-stereo decoder includes a phase-lock-loop for providing an error voltage and an audio decoder hav-

ing L and R output channels upon which L and R audio signals are developed, respectively. In response to an initial predetermined increase in the error voltage due to the initiation of distorted reception, the separation between the L and R output channels is substantially instantaneously decreased to less than full channel separation thereby to rapidly shift toward full monophonic operation for reducing the discernible audio distortion resulting from the distorted reception. Further, in response to a subsequent predetermined decrease in the error voltage due to the termination of distorted reception, the separation between the L and R output channels is relatively gradually increased to full channel separation thereby to slowly shift to full stereophonic operation for reducing the discernible audio disruption resulting from the shift to full stereophonic operation. Preferably, the separation between the L and R output channels of the audio decoder is varied during distorted reception from full channel separation to an intermediate channel separation which is greater than zero channel separation in proportion to the frequency of the L and R audio signals thereby to provide blended stereophonic/monophonic operation for reducing the discernible audio disruption resulting from the rather sudden shift toward full monophonic operation and for maximizing the amount of stereophonic operation over the lower frequencies of the L and R audio signals while minimizing the discernible audio distortion resulting from the higher frequencies of the L and R audio signals.

4 Claims, 9 Drawing Figures



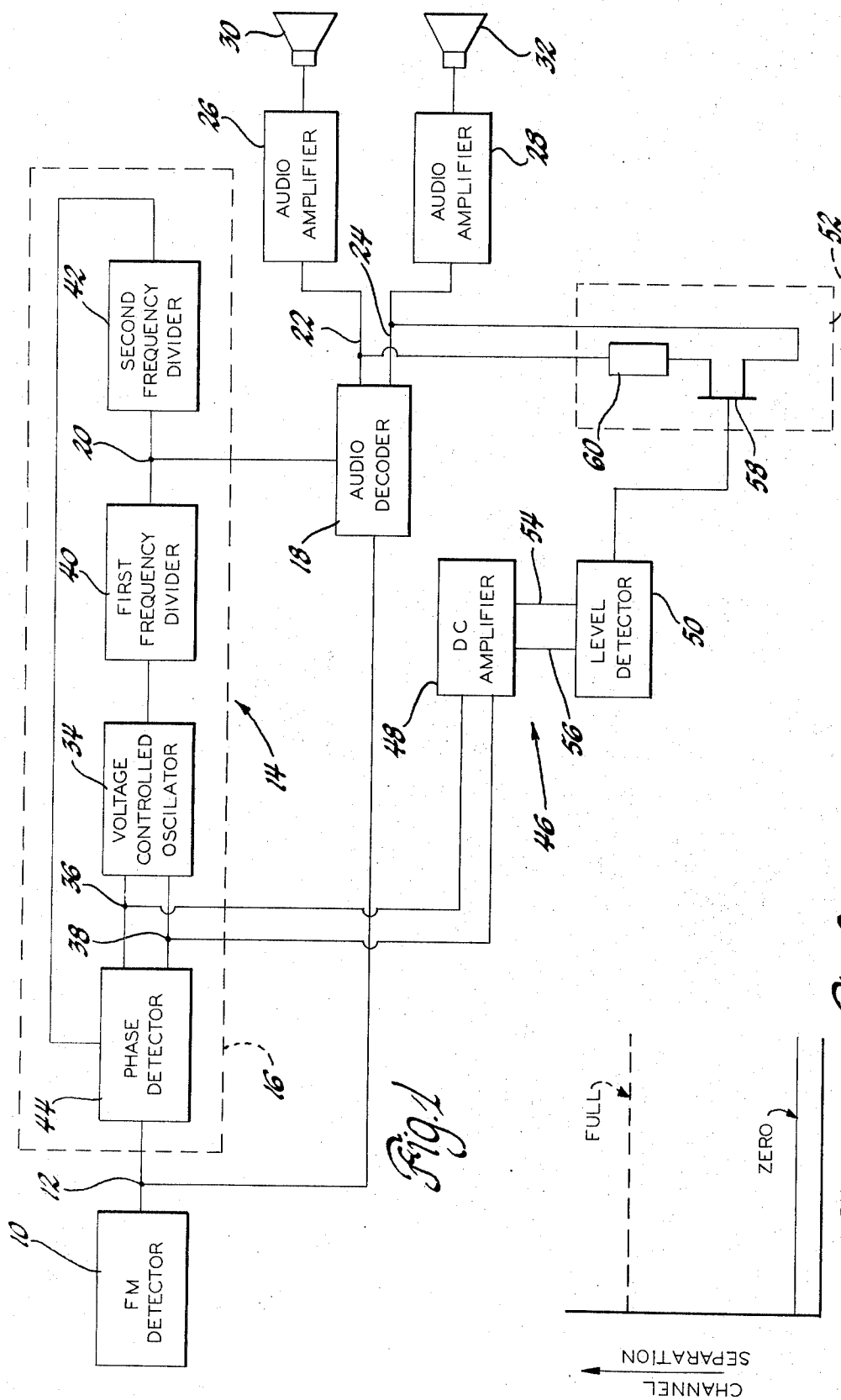
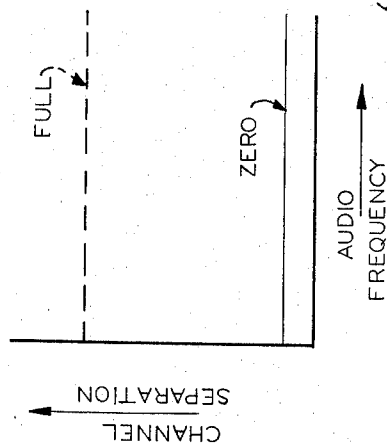
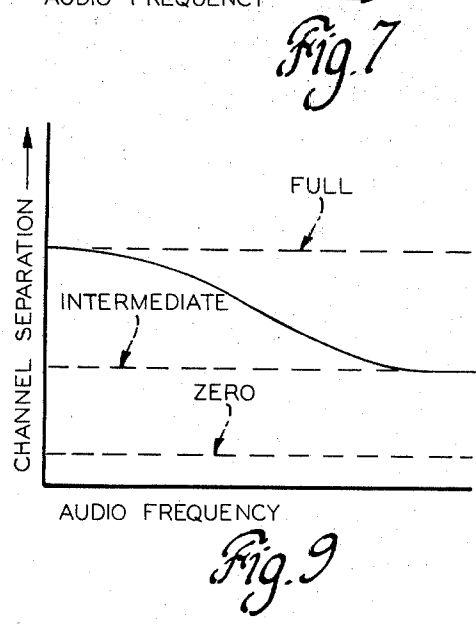
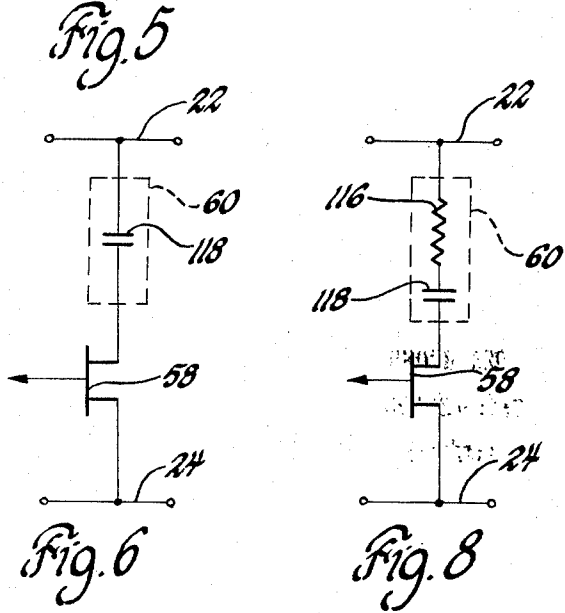
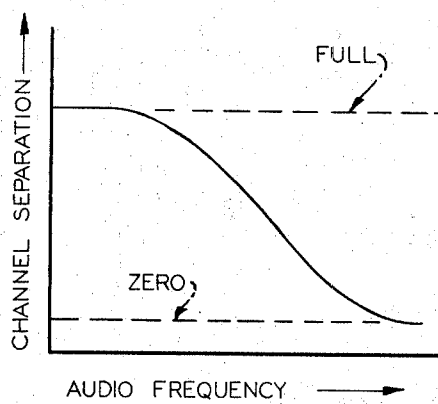
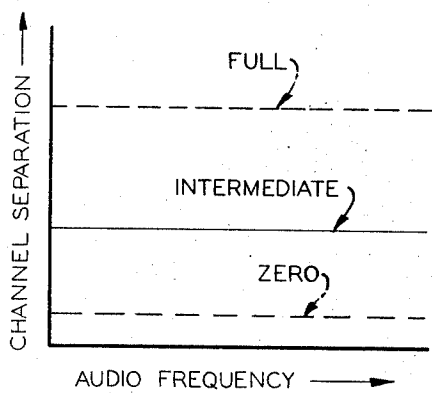
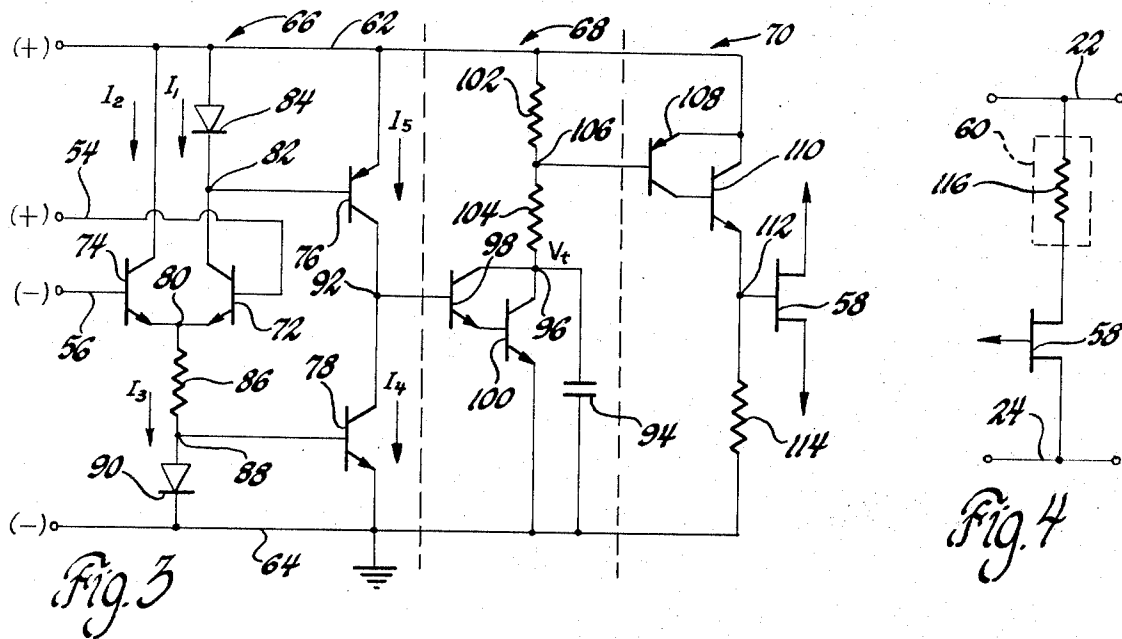


Fig. 2





# **PHASE-LOCK-LOOP FM-STEREO DECODER INCLUDING STEREOPHONIC/MONOPHONIC BLEND SYSTEM FOR REDUCING AUDIO DISTORTION**

This invention relates to an FM-stereo decoder for demodulating a standard composite stereophonic signal including an L + R signal, an L - R modulated 38 KHz suppressed subcarrier signal, and a 19 KHz pilot signal.

In FM-stereo reception, the composite stereophonic signal, including the 19 KHz pilot signal, is erratically phase shifted by multipath reception as well as various forms of "overload" reception. Overload reception occurs when a modulation product of one or more strong undesired stations interferes with the reception of a desired station. With either multipath reception or overload reception, the result is corresponding audio distortion of a nature which is readily discernible by a listener. Since audio distortion is inherently less perceptible during monophonic operation than during stereophonic operation, it is desirable to switch from full stereophonic operation toward full monophonic operation in response to the occurrence of distorted reception, whether multipath reception or some form of overload reception.

In a known FM-stereo decoder, a phase-lock-loop generates a local 38 KHz demodulating signal in phase synchronization with the 19 KHz pilot signal. Further, an audio decoder demodulates the L + R signal and the L - R modulated 38 KHz suppressed subcarrier signal in response to the local 38 KHz demodulating signal to provide an L audio signal on an L output channel and an R audio signal on an R output channel. Ordinarily, the phase-lock-loop includes a phase detector which provides an error voltage having an amplitude which is proportional to the phase difference between the received 19 KHz pilot signal and the local 38 KHz demodulating signal.

According to one aspect of the invention, the separation between the L and R output channels of the audio decoder is substantially instantaneously defined at less than full channel separation in response to a predetermined increase in the amplitude of the phase-lock-loop error voltage due to the initiation of distorted reception, whether multipath reception or a form of overload reception. This "fast attack" feature of the invention is desirable in order to shift from full stereophonic operation toward full monophonic operation in time to reduce the discernible audio distortion resulting from the distorted reception.

In another aspect of the invention, the separation between the L and R output channels of the audio decoder is relatively gradually restored to full channel separation in response to a predetermined decrease in the amplitude of the phase-lock-loop error voltage due to the termination of distorted reception. This "slow retreat" feature of the invention is desirable in order to reduce the discernible audio disruption resulting from the return to full stereophonic operation following the excursion toward full monophonic operation.

In an embodiment of the preceding aspects of the invention, a coupling network including an electronic switch is connected across the L and R output channels of the audio decoder for establishing full channel separation when the electronic switch is turned off and for establishing less than full channel separation when the electronic switch is turned on. Further, a level detector

is responsive to an initial increase in the amplitude of the error voltage due to the initiation of distorted reception to substantially instantaneously turn on the electronic switch. The level detector includes a timing network which is responsive to a subsequent decrease in the amplitude of the error voltage due to the termination of distorted reception to relatively gradually turn off the electronic switch. Preferably, the electronic switch is a field-effect transistor.

As contemplated by another aspect of the invention, the minimum separation between the L and R output channels of the audio decoder during distorted reception is defined at an intermediate channel separation located between full channel separation and zero channel separation. This feature of the invention is desirable in order to reduce the discernible audio disruption resulting from the sudden shift from full stereophonic operation toward full monophonic operation.

In an embodiment of the preceding aspect of the invention, the coupling network includes at least one resistive element connected with the electronic switch for defining the intermediate channel separation in proportion to the resistance of the resistive element when the electronic switch is turned on. When the separation between the L and R output channels of the audio decoder is at the intermediate channel separation, blended stereophonic/monophonic operation is provided.

In another aspect of the invention, the separation between the L and R output channels of the audio decoder is varied during distorted reception from full channel separation to less than full channel separation in direct proportion to the frequency of the L and R audio signals such that channel separation decreases with increases in audio frequency. Since the greatest portion of the L and R audio signals is composed of lower frequency components while the major portion of the audio distortion of the L and R audio signals results from higher frequency components, this feature of the invention is desirable in order to maximize total stereophonic operation and yet minimize overall audio distortion.

In an embodiment of the preceding aspect of the invention, the coupling network includes at least one reactive element connected with the electronic switch for defining the separation between the L and R output channels of the audio decoder in proportion to the reactance of the reactive element as defined in proportion to the frequency of the L and R audio signals when the electronic switch is turned on. Preferably, the reactive element is a capacitor.

These and other aspects and advantages of the invention may be best understood by reference to the following detailed description of the preferred embodiments when taken in conjunction with the accompanying drawings.

In the drawings:

FIG. 1 is a block diagram of an FM-stereo decoder including an inventive stereophonic/monophonic blend system incorporating one embodiment of a unique coupling network.

FIG. 2 is a graphic diagram of the operating characteristic of the embodiment of the coupling network illustrated in FIG. 1.

FIG. 3 is a schematic diagram of an embodiment of a level detector incorporated within the inventive

stereophonic/monophonic blend system illustrated in FIG. 1.

FIGS. 4, 6, and 8 are schematic diagrams of other embodiments of the coupling network incorporated within the inventive stereophonic/monophonic blend system illustrated in FIG. 1.

FIGS. 5, 7, and 9 are graphic diagrams of the operating characteristics of the various embodiments of the coupling network illustrated in FIGS. 4, 6, and 8.

Referring to FIG. 1, an FM-stereo radio receiver includes an FM detector 10 for developing a standard composite stereo signal including a 19 KHz pilot signal, an L + R signal and an L - R modulated 38 KHz suppressed subcarrier signal at a junction 12. An FM-stereo decoder 14 includes a phase-lock-loop 16 and an audio decoder 18. The phase-lock-loop 16 is connected to the junction 12 for developing a 38 KHz demodulating signal or subcarrier signal at a junction 20 in phase synchronization with the 19 KHz pilot signal. The audio decoder 18 is connected to the junctions 12 and 20 for demodulating the L + R signal and the L - R modulated 38 KHz signal in response to the 38 KHz demodulating signal to provide an L audio signal on an L output channel 22 and an R audio signal on an R output channel 24. A pair of audio amplifiers 26 and 28 are connected to the L and R output channels 22 and 24, respectively, for amplifying and applying the L and R audio signals to L and R stereo speakers 30 and 32, respectively.

More specifically, the phase-lock-loop 16 includes a voltage controlled oscillator 34 for producing a 76 KHz reference signal having a phase defined in proportion to the amplitude of a differential error voltage appearing between a pair of junctions 36 and 38. A first frequency divider 40 is connected to the oscillator 34 for dividing the 76 KHz reference signal by a factor of (2) to provide the 38 KHz demodulating signal at the junction 20 in phase with the 76 KHz reference signal. A second frequency divider 42 is connected to the junction 20 for dividing the 38 KHz demodulating signal by a factor of (2) to provide a 19 KHz reference signal in quadrature to the 38 KHz demodulating signal. A phase detector 44 is connected to the junction 12 and to the second frequency divider 42 for developing the differential error voltage between the junctions 36 and 38 such that the amplitude of the error voltage is defined in proportion to the difference between the phase of the 19 KHz pilot signal and the phase of the 19 KHz reference signal as determined by the phase of the 38 KHz demodulating signal.

The FM-stereo decoder 14 may be provided by a Fairchild uA758 FM-stereo decoder which is commercially available as a monolithic integrated circuit from Fairchild Semiconductor Corporation. A more detailed description of the uA758 FM-stereo decoder may be obtained by reference to "The uA758, A Phase Locked Loop FM Stereo Multiplex Decoder" by Larry Blaser and Bill Cocke, as published in application Note 319, June, 1972, Fairchild Semiconductor Corporation. A similar FM-stereo decoder is described in "A Monolithic Phase-Lock-Loop Stereo Decoder," by Michael J. Gay, as published in I.E.E.E. Transactions on Broadcast and TV Receivers, November, 1971.

In the presence of distorted reception, whether "multipath reception" or a form of "overload reception," the 19 KHz signal as well as the rest of the composite stereophonic signal is severely phase distorted. Multi-

path reception occurs when two identical signals emanating from the same transmitting antenna arrive at the same receiving antenna out of phase after traveling over different propagation paths. Ordinarily, one of the signals is received directly from the transmitting antenna while the other of the signals is received indirectly after reflection from an object disposed between the transmitting and receiving antennas. At the receiving antenna, the direct and reflected signals vectorially add to form a resultant signal which is phase distorted. Overload distortion may take a number of forms, but in general, it may be characterized as occurring when at least two unwanted signals mix together to provide a beat signal having a frequency component which vectorially adds with a wanted signal to form a resultant signal which is phase distorted. In either multipath reception or overload reception, the ultimate phase distortion of the composite stereophonic signal is manifested by a corresponding amplitude distortion of the L and R audio signals which, in turn, produces a derivative audible distortion from the stereo speakers 30 and 32.

It is well known that the signal-to-noise ratio of monophonic operation is inherently greater than the signal-to-noise ratio of stereophonic operation. In other words, given the same amount of phase distortion of an FM signal, the resulting audio distortion is less discernible to a listener during monophonic operation than during stereophonic operation. Therefore, it is desirable to shift from full stereophonic operation toward full monophonic operation during distorted reception. Further, as the phase of the 19 KHz pilot signal is initially shifted in response to the onset of distorted reception, the amplitude of the error voltage appearing between the junctions 36 and 38 of the phase-lock-loop 16 increases sharply. Seizing upon the foregoing facts and circumstances, the present invention provides a stereophonic/monophonic blend system 46 for reducing the separation between the L and R output channels 22 and 24 of the audio decoder 18 in response to an increase in the amplitude of the error voltage indicative of distorted reception thereby to shift from full stereophonic operation toward full monophonic operation so as to reduce the discernible audio distortion resulting from the distorted reception.

Referring again to FIG. 1, the stereophonic/monophonic blend system 46 includes a DC amplifier 48, a level detector 50, and a coupling stage 52. The DC amplifier 48 is responsive to the error voltage appearing between junctions 36 and 38 to provide an amplified replica of the error voltage between a pair of lines 54 and 56. Conveniently, the DC amplifier 48 may be provided by a Westinghouse WC-115-P differential amplifier which is commercially available as a monolithic integrated circuit from Westinghouse Electric Corporation. Alternately, where the FM-stereo decoder 14 is provided by a Fairchild uA758 FM-stereo decoder, the DC amplifier 48 may be provided by a DC amplifier which is internal to the voltage controlled oscillator 34 of the uA758 integrated circuit.

The coupling stage 52 is connected across the L and R output channels 22 and 24 of the audio decoder 18. Preferably, the coupling stage 52 includes an electronic switch 58 provided by a field-effect transistor having gate, source and drain electrodes. Further, an impedance device 60 is connected between the source electrode of the transistor 58 and the L output channel 22

of the audio decoder 18. The drain electrode of the transistor 52 is connected directly to the R output channel 24 of the audio decoder 18. Of course, since the field-effect transistor 52 is a bilateral device, the source and drain electrodes are interchangeable. Further, at this point, it is to be understood that the field-effect transistor 58 may be replaced by any suitable electronic switch such as a junction bipolar transistor and that the impedance device 60 may or may not be present within the coupling network 52 as will become more apparent hereinafter.

The level detector 50 is connected between the gate electrode of the field-effect transistor 58 and the lines 54 and 56 emanating from the DC amplifier 48. When the amplitude of the error voltage appearing between the lines 54 and 56 increases in a manner indicative of the presence of distorted reception, the level detector 50 applies a bias voltage to the gate electrode of the field-effect transistor 58 to render the transistor 58 fully conductive. Conversely, when the amplitude of the error voltage appearing between the lines 54 and 56 decreases in a manner indicative of the absence of distorted reception, the level detector 50 withdraws the bias voltage from the gate electrode of the field-effect transistor 58 to render the transistor 58 fully nonconductive.

With the transistor 58 normally turned off, the separation between the L and R output channels 22 and 24 of the audio decoder 18 is defined at substantially full channel separation thereby to provide full stereophonic operation. Alternately, when the transistor 58 is turned on in response to distorted reception, the separation between the L and R output channels 22 and 24 of the audio decoder 18 is defined at less than full channel separation thereby to provide less than full stereophonic operation for reducing the discernible audio distortion resulting from the distorted reception. If the impedance device 60 is absent from the coupling state 52, the separation between the L and R output channels 22 and 24 is defined at substantially zero channel separation when the transistor 58 is turned on. FIG. 2 illustrates the operating characteristic (i.e. a graph of channel separation versus audio frequency) of the coupling stage 52 where the impedance device 60 is absent and the transistor 58 turned on.

In order to shift from full stereophonic operation toward full monophonic operation in time to reduce discernible distortion resulting from distorted reception, it is necessary that the level detector 50 have a "fast attack" capability; that is, the level detector 50 must be responsive to an initial increase in the amplitude of the error voltage due to the initiation of distorted reception to substantially instantaneously turn on the transistor 58 to decrease the separation between the L and R output channels 22 and 24 of the audio decoder 18 thereby to rapidly shift to less than full stereophonic operation. On the other hand, in order to minimize the discernible audio disruption resulting from the transition to full stereophonic operation following the excursion toward full monophonic operation, it is required that the level detector 50 have a "slow retreat" capability; that is the level detector 50 must relatively gradually turn off the transistor 58 to increase the separation between the L and R output channels 22 and 24 of the audio decoder 18 thereby to slowly restore full stereophonic operation. FIG. 3 illustrates an embodiment of the level detector 50 which possesses the de-

sired "fast attack" and "slow retreat" features, and which is suitable for fabrication within a monolithic integrated circuit.

Referring to FIG. 3, the level detector 50 includes a high potential line 62 and a low potential line 64 across which a direct current supply voltage is applied. Preferably, the low potential line 64 is grounded. Where the FM-stereo decoder 14 is provided by a Fairchild uA758-stereo decoder, the DC supply voltage may be derived from a power supply internal to the uA758 integrated circuit. In fact, the level detector 50 may be fabricated upon the same semiconductor chip as the uA758 FM-stereo decoder.

The level detector 50 includes a level sensor 66, a timing network 68 and a buffer stage 70. The level sensor 66 includes a differential voltage switch provided by a pair of voltage switching transistors 72 and 74 of the NPN junction type and a complementary current switch provided by a pair of current switching transistors 76 and 78 of the PNP and NPN junction type, respectively. The base electrodes of the transistors 72 and 74 are connected directly to the lines 54 and 56, respectively, emanating from the DC amplifier 48. The emitter electrodes of the transistors 72 and 74 are connected together at a junction 80. The collector electrode of the transistor 72 is connected directly to a junction 82. The collector electrode of the transistor 74 is connected directly to the high potential line 62. A bias diode 84 is connected between the high potential line 62 and the junction 82. The base electrode of the transistor 76 is connected directly to the junction 82. The emitter electrode of the transistor 76 is connected directly to the high potential line 62. The collector electrode of the transistor 76 is connected directly to a junction 92. A bias resistor 86 is connected between the junction 80 and a junction 88. A bias diode 90 is connected between the junction 88 and the low potential line 64. The base electrode of the transistor 78 is connected directly to the junction 88. The emitter electrode of the transistor 78 is connected directly to the low potential line 64. The collector electrode of the transistor 78 is connected directly to the junction 92.

The timing network 68 includes a timing capacitor 94 across which a timing voltage  $V_t$  is developed. The timing capacitor 94 is connected between a junction 96 and the low potential line 64. A Darlington switch is provided by a pair of transistors 98 and 100 of the NPN junction type. Specifically, the base electrode of the transistor 98 is connected directly to the junction 92. The collector electrode of the transistor 98 and the collector electrode of the transistor 100 are connected together to the junction 96. The emitter electrode of the transistor 98 is connected directly to the base electrode of the transistor 100. The emitter electrode of the transistor 100 is connected directly to the low potential line 64. A pair of bias resistors 102 and 104 are connected in series between the high potential line 68 and the junction 96 such that a junction 106 is defined between the resistors 102 and 104.

The buffer stage 70 includes a buffer switch formed by a pair of transistors 108 and 110 of the PNP and NPN junction type, respectively. The base electrode of the transistor 108 is connected directly to the junction 106. The emitter electrode of the transistor 108 and the collector electrode of the transistor 110 are connected together to the high potential line 62. The collector

electrode of the transistor 108 is connected directly to the base electrode of the transistor 110. The emitter electrode of the transistor 110 is connected directly to a junction 112. A bias resistor 114 is connected between the junction 112 and the low potential line 64. Further, the gate electrode of the field-effect transistor 58 in the coupling network 52 is connected directly to the junction 112.

In the level sensor 66, the base-emitter junction area of the transistor 74 is greater than the base-emitter junction area of the transistor 72 by a factor of (3). Assuming for the moment, that the amplitude of the error voltage defined between lines 54 and 56 is substantially zero (i.e., the base electrode of the transistor 72 is essentially shorted to the base electrode of the transistor 74), a current  $I_1$  flows through the transistor 72 and the diode 84 and a current  $I_2$  approximately equal to (3)  $I_1$  flows through the transistor 74. In addition, a current  $I_3$  approximately equal to the summation of the currents  $I_2$  and  $I_2$  or (4)  $I_1$  flows through the resistor 86 and the diode 90. The anode-cathode junction area of the diode 90 is greater than the base-emitter junction area of the transistor 78 by a factor of (2). Thus, since the current  $I_3$  flowing through the diode 90 is approximately equal to (4)  $I_1$ , a current  $I_4$  approximately equal to (2)  $I_1$  flows through the transistor 78 out of the junction 92. The anode-cathode junction area of the diode 84 is the same as the base-emitter junction area of the transistor 76. Hence, a current  $I_5$ , which is approximately equal to the current  $I_1$  flowing through the diode 84, flows through the transistor 76 into the junction 92.

When the amplitude of the error voltage appearing between lines 54 and 56 is at a predetermined magnitude indicative of distorted reception, whether multipath reception or a form of overload reception, the current  $I_1$  flowing through the transistor 72 is approximately equal to the current  $I_2$  flowing through the transistor 74. As a result, the current  $I_3$  flowing through the diode 90 is equal to (2)  $I_1$  and the current  $I_4$  flowing through the transistor 78 is equal to  $I_1$ . Likewise, the current  $I_5$  flowing through the transistor 76 is equal to  $I_1$ . Therefore, the current  $I_5$  flowing into the junction 92 out of transistor 76 is approximately equal to the current  $I_4$  flowing out of junction 92 into the transistor 78. As the amplitude of the error voltage appearing between the lines 54 and 56 exceeds the predetermined magnitude indicative of distorted reception, the current  $I_5$  flowing through the transistor 76 into the junction 92 exceeds the current  $I_4$  flowing through the transistor 78 out of the junction 92. Conversely, as the amplitude of the error voltage appearing between the lines 54 and 56 decreases below the predetermined magnitude indicative of distorted reception, the current  $I_4$  flowing through the transistor 78 out of the junction 92 exceeds the current  $I_5$  flowing through the transistor 78 into the junction 92.

When the current  $I_4$  flowing out of the junction 92 exceeds the current  $I_5$  flowing into the junction 92, the Darlington switch formed by the transistors 98 and 100 is rendered fully nonconductive. With the transistors 98 and 100 turned off, the capacitor 94 is maintained fully charged through the resistors 102 and 104 so that the amplitude of the timing voltage  $V_t$  developed across the capacitor 94 is at a maximum voltage level. With the timing voltage  $V_t$  at a maximum voltage level, the potential at the junction 106 is held at a relatively high

voltage level by the voltage divider action of the resistors 102 and 104. With the junction 106 at a relatively high voltage level, the buffer switch formed by the transistors 108 and 110 is rendered fully nonconductive.

With the transistors 108 and 110 turned off, bias voltage is withheld from across the resistor 114 at the junction 112 so that the field-effect transistor 58 is rendered fully nonconductive. With the transistor 58 turned off, the separation between the L and R output channels 22 and 24 of the stereo decoder 18 is defined at substantially full channel separation thereby to provide full stereophonic operation.

As the current  $I_5$  flowing through the junction 92 exceeds the current  $I_4$  flowing out of the junction 92 in response to an initial increase in the amplitude of the error voltage appearing between lines 54 and 56 above the predetermined magnitude indicative of distorted reception, the Darlington switch formed by the transistors 98 and 100 is rendered fully conductive. With the transistors 98 and 100 turned on, the timing capacitor 94 is substantially instantaneously discharged to rapidly decrease the amplitude of the timing voltage  $V_t$  to a minimum voltage level defined just above the voltage level on the low potential line 64 by an amount equal to the saturation voltage drop of the transistors 98 and 100. With the timing voltage  $V_t$  at a minimum voltage level, the potential at the junction 106 is dropped to a relatively low voltage level defined by the voltage divider action of the resistors 102 and 104. With the junction 106 at a relatively low voltage level, the buffer switch formed by the transistors 108 and 110 is rendered fully conductive. With the transistors 108 and 110 turned on, a bias voltage is applied across the resistor 114 at the junction 112 to substantially instantaneously render the transistor 58 fully conductive. As the transistor 58 is turned on, the separation between the L and R output channels 22 and 24 of the audio decoder 18 is substantially instantaneously decreased to less than full channel separation thereby to shift toward full monophonic operation so as to reduce the audio distortion resulting from the distorted reception.

When the current  $I_4$  flowing out of the junction 92 exceeds the current  $I_5$  flowing into the junction 92 in response to a subsequent decrease in the amplitude of the error voltage appearing between lines 54 and 56 below the predetermined magnitude indicative of distorted reception, the Darlington switch formed by the transistors 98 and 100 is rendered fully nonconductive. With the transistors 98 and 100 turned off, the timing capacitor 94 charges through the resistors 102 and 104 to relatively gradually increase the amplitude of the timing voltage  $V_t$  from the minimum voltage level back to the maximum voltage level in accordance with the RC time constant provided by the resistance of the resistors 102 and 104 and the capacitance of the capacitor 94. As the amplitude of the timing voltage  $V_t$  increases, the potential at the junction 106 likewise increases to slowly render the buffer switch formed by the transistors 108 and 110 fully nonconductive. As the transistors 108 and 110 are turned off, the bias voltage applied across the resistor 114 at the junction 112 is withdrawn to relatively gradually turn off the field-effect transistor 58. As the transistor 58 turns off, the separation between the L and R output channels 22 of the audio decoder 18 is relatively gradually increased back to full channel separation thereby to slowly shift to full stereophonic operation so as to reduce the audio dis-

tortion resulting from the transition from less than full stereophonic operation back to full stereophonic operation.

It will now be appreciated that the substantially instantaneous decrease in the separation between the L and R output channels 22 and 24 of the audio decoder 18 in response to the initiation of distorted reception, can itself be a source of perceptible audio distortion. In other words, the rather sudden shift from full stereophonic operation toward full monophonic operation may cause discernible audio disruption, particularly where the shift is from full stereophonic operation all the way to full monophonic operation. FIG. 4 illustrates an embodiment of the impedance device 60 for reducing the discernible audio disruption resulting from the shift to less than full stereophonic operation from full stereophonic operation.

Referring to FIG. 4, the impedance device 60 comprises a resistor 116 which is connected in series with the field-effect transistor 58 between the L and R output channels 22 and 24 of the audio decoder 18. When the transistor 58 is turned on, the separation between the L and R output channels 22 and 24 is established at an intermediate channel separation defined below full channel separation and above zero channel separation. Actually, the intermediate channel separation is defined below full channel separation in inverse proportion to the resistance of the resistor 116, or alternatively, is defined above zero channel separation in direct proportion to the resistance of the resistor 116. Thus, the resistor 116 provides blended stereophonic/monophonic operation for reducing the discernible audio disruption resulting from the rapid shift toward full monophonic operation from full stereophonic operation. FIG. 5 illustrates the operating characteristic of the coupling network 52 where the impedance device 60 includes the resistor 116 and the transistor 58 is turned on.

Further, it is well known that the major portion of the L and R audio signals is composed of lower frequency components while most of the audio distortion in the L and R audio signals results from the higher frequency components. FIG. 6 illustrates an embodiment of the impedance device 60 for maximizing the amount of stereophonic operation over the lower frequencies of the L and R audio signals thereby to enhance the total stereophonic effect while maximizing the amount of monophonic operation over the high frequencies of the L and R audio signals thereby to reduce the resulting audio distortion.

Referring to FIG. 6, the impedance device 60 comprises a reactive element provided by a capacitor 118 which is connected in series with the field-effect transistor 58 between the L and R output channels 22 and 24 of the audio decoder 18. When the transistor 58 is turned on, the separation between the L and R output channels 22 and 24 is variably defined between full channel separation and zero channel separation in direct proportion to the frequency of the L and R audio signals. More specifically, the separation between the L and R output channels 22 and 24 is variably established in inverse proportion to the reactance of the capacitor 118 which, in turn, is determined in inverse proportion to the frequency of the L and R audio signals.

At the lower frequencies of the L and R audio signals, the reactance of the capacitor 118 is relatively high for

increasing the separation between the L and R output channels 22 and 24 thereby to maximize the amount of stereophonic operation. On the other hand, at the higher frequencies of the L and R audio signals, the reactance of the capacitor 118 is relatively low for decreasing the separation between the L and R output channels 22 and 24 thereby to maximize the amount of monophonic operation. Accordingly, the capacitor 116 provides blended stereophonic/monophonic operation for maximizing total stereophonic effect while minimizing overall audio distortion. FIG. 7 illustrates the operating characteristic of the coupling network 52 where the impedance device 60 comprises the capacitor 118 and where the transistor 58 is turned on.

FIG. 8 illustrates an embodiment of the impedance device 60 which is a combination of the embodiments shown in FIGS. 4 and 6 for providing all of the advantages of the embodiments shown in FIGS. 4 and 6. Referring to FIG. 8, the impedance device 60 comprises the series connection of the resistor 116 and the capacitor 118 with the field-effect transistor 58 across the L and R output channels 22 and 24 of the audio decoder 18. When the transistor 58 is turned on, a minimum separation between the L and R output channels 22 and 24 is established at an intermediate channel separation located below full channel separation and above zero channel separation as determined by the resistance of the resistor 116. Further, when the transistor 58 is turned on, the separation between the L and R output channels 22 and 24 is variably defined from full channel separation to the intermediate channel separation in direct proportion to the frequency of the L and R audio signals as determined by the reactance of the capacitor 118. FIG. 9 illustrates the operating characteristic of the coupling network 52 where the impedance device 60 comprises the series combination of the resistor 116 and the capacitor 118 and where the transistor 58 is turned on.

It will now be appreciated that the illustrated embodiments of the invention are shown for demonstrative purposes only and that various alterations and modifications may be made to these embodiments without departing from the spirit and scope of the invention.

What is claimed is:

1. In an FM-stereo decoder for demodulating a standard composite stereophonic signal including an L + R signal, an L - R modulated 38 KHz suppressed subcarrier signal, and a 19 KHz pilot signal; the combination comprising: means including a phase-lock-loop for generating a 38 KHz demodulating signal in phase synchronization with the 19 KHz pilot signal, the phase-lock-loop including a phase detector for producing an error voltage having an amplitude defined as a function of the phase difference between the 19 KHz pilot signal and the 38 KHz demodulating signal such that the amplitude of the error signal increases in response to shifts in the phase of the 19 KHz pilot signal caused by distorted reception; means including an audio decoder having L and R output channels for demodulating the L + R signal and the L - R modulated 38 KHz suppressed subcarrier signal in response to the 38 KHz demodulating signal to provide an L audio signal on the L output channel and an R audio signal on the R output channel; a coupling network including an electronic switch connected across the L and R output channels of the audio decoder for establishing the separation be-

tween the L and R output channels at substantially full channel separation when the electronic switch is turned off and for establishing the separation between the L and R output channels at less than full channel separation when the electronic switch is turned on; and a level detector responsive to an initial predetermined increase in the amplitude of the error voltage due to the initiation of distorted reception to substantially instantaneously turn on the electronic switch thereby to rapidly shift toward full monophonic operation for reducing the discernible audio distortion resulting from the distorted reception, the level detector including a timing network responsive to a subsequent predetermined decrease in the amplitude of the error voltage due to the termination of distorted reception to relatively gradually turn off the electronic switch thereby to slowly shift to full stereophonic operation for reducing the discernible audio disruption resulting from the shift back to full stereophonic operation.

2. In an FM-stereo decoder for demodulating a standard composite stereophonic signal including an L + R signal, an L - R modulated 38 KHz suppressed subcarrier signal, and a 19 KHz pilot signal; the combination comprising: means including a phase-lock-loop for generating a 38 KHz demodulating signal in phase synchronization with the 19 KHz pilot signal, the phase-lock-loop including a phase detector for producing an error voltage having an amplitude defined as a function of the phase difference between the 19 KHz pilot signal and the 38 KHz demodulating signal such that the amplitude of the error signal increases in response to shifts in the phase of the 19 KHz pilot signal caused by distorted reception; means including an audio decoder having L and R output channels for demodulating the L + R signal and the L - R modulated 38 KHz suppressed subcarrier signal in response to the 38 KHz demodulating signal to provide an L audio signal on the L output channel and an R audio signal on the R output channel; a coupling network including an electronic switch connected across the L and R output channels of the audio decoder for establishing the separation between the L and R output channels at substantially full channel separation when the electronic switch is turned off and for establishing the separation between the L and R output channels at less than full channel separation when the electronic switch is turned on; and a level detector responsive to an initial predetermined increase in the amplitude of the error voltage due to the initiation of distorted reception to substantially instantaneously turn on the electronic switch thereby to rapidly shift toward full monophonic operation for reducing the discernible audio distortion resulting from the distorted reception, the level detector including a timing network responsive to a subsequent predetermined decrease in the amplitude of the error voltage due to the termination of distorted reception to relatively gradually turn off the electronic switch thereby to slowly shift to full stereophonic operation for reducing the discernible audio disruption resulting from the shift to full stereophonic operation; the coupling network including a resistive element for establishing a minimum separation between the L and R output channels of the audio decoder when the electronic switch is turned on at an intermediate channel separation defined below full channel separation and above zero channel separation thereby to provide blended stereophonic/monophonic operation for reducing the discernible audio distortion

resulting from the sudden shift toward full monophonic operation from full stereophonic operation.

3. In an FM-stereo decoder for demodulating a standard composite stereophonic signal including an L + R signal, an L - R modulated 38 KHz suppressed subcarrier signal, and a 19 KHz pilot signal; the combination comprising: means including a phase-lock-loop for generating a 38 KHz demodulating signal in phase synchronization with the 19 KHz pilot signal, the phase-lock-loop including a phase detector portion for producing an error voltage having an amplitude defined as a function of the phase difference between the 19 KHz pilot signal and the 38 KHz demodulating signal such that the amplitude of the error signal increases in response to shifts in the phase of the 19 KHz pilot signal caused by distorted reception; means including an audio decoder having L and R output channels for demodulating the L + R signal and the L - R modulated 38 KHz suppressed subcarrier signal in response to the 38 KHz demodulating signal to provide an L audio signal on the L output channel and an R audio signal on the R output channel; a coupling network including an electronic switch connected across the L and R output channels of the audio decoder for establishing substantially full channel separation when the electronic switch is turned off thereby to provide full stereophonic operation and for establishing less than full channel separation when the electronic switch is turned on thereby to provide less than full stereophonic operation; and a level detector responsive to an initial predetermined increase in the amplitude of the error voltage due to the initiation of distorted reception to substantially instantaneously turn on the electronic switch thereby to rapidly shift toward full monophonic operation for reducing the audio distortion resulting from the distorted reception, the level detector including a timing network responsive to a subsequent predetermined decrease in the amplitude of the error voltage due to the termination of distorted reception to relatively gradually turn off the electronic switch thereby to slowly shift to full stereophonic operation for reducing the audio disruption resulting from the shift to full stereophonic operation; the coupling network further including a reactive element for varying the separation between the L and R output channels of the audio decoder from full channel separation to less than full channel separation as a direct function of the frequency of the L and R audio signals thereby to provide blended stereophonic/monophonic operation for maximizing the stereophonic reproduction of the lower frequencies of the L and R audio signals while minimizing the audio distortion resulting from the higher frequencies of the L and R audio signals.

4. In an FM-stereo decoder for demodulating a standard composite stereophonic signal including an L + R signal, an L - R modulated 38 KHz suppressed subcarrier signal, and a 19 KHz pilot signal; the combination comprising: means including a phase-lock-loop for generating a 38 KHz demodulating signal in phase synchronization with the 19 KHz pilot signal, the phase-lock-loop including a phase detector for producing an error voltage having an amplitude defined as a function of the phase difference between the 19 KHz pilot signal and the 38 KHz demodulating signal such that the amplitude of the error signal increases in response to shifts in the phase of the 19 KHz pilot signal caused by distorted reception; means including an audio decoder

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having L and R output channels for demodulating the L + R signal and the L - R modulated 38 KHz suppressed subcarrier signal in response to the 38 KHz demodulating signal to provide an L audio signal on the L output channel and an R audio signal on the R output channel; a coupling network including an electronic switch and at least one resistive element connected across the L and R output channels of the audio decoder for establishing full channel separation when the electronic switch is turned off thereby to provide full stereophonic operation and for establishing less than full channel separation when the electronic switch is turned on thereby to provide less than full stereophonic operation; and a level detector responsive to an initial predetermined increase in the amplitude of the error voltage due to the initiation of distorted reception to substantially instantaneously turn on the electronic switch thereby to rapidly shift toward full monophonic operation for reducing the audio distortion resulting from the distorted reception, the level detector including a timing network responsive to a subsequent predetermined decrease in the amplitude of the error voltage due to the termination of distorted reception to relatively gradually turn off the electronic switch thereby to slowly shift to full stereophonic operation for reducing

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ing audio disruption resulting from the shift to full stereophonic operation; the coupling network including a resistive element for establishing a minimum separation between the L and R output channels of the audio decoder when the electronic switch is turned on at an intermediate channel separation defined below full channel separation and above zero channel separation by the resistance of the resistive element thereby to provide blended stereophonic/monophonic operation for reducing the audio distortion resulting from the sudden shift toward full monophonic operation, the coupling network also including a capacitive element for varying the separation between the L and R output channels of the audio decoder when the electronic switch is turned on from full channel separation to the intermediate channel separation as determined by the reactance of the capacitor thereby to provide blended stereophonic/monophonic operation for maximizing stereophonic operation at the lower frequencies of the L and R audio signals and for maximizing monophonic operation at the higher frequencies of the L and R audio signals so as to maximize the total stereophonic effect and minimize the overall audio distortion.

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