



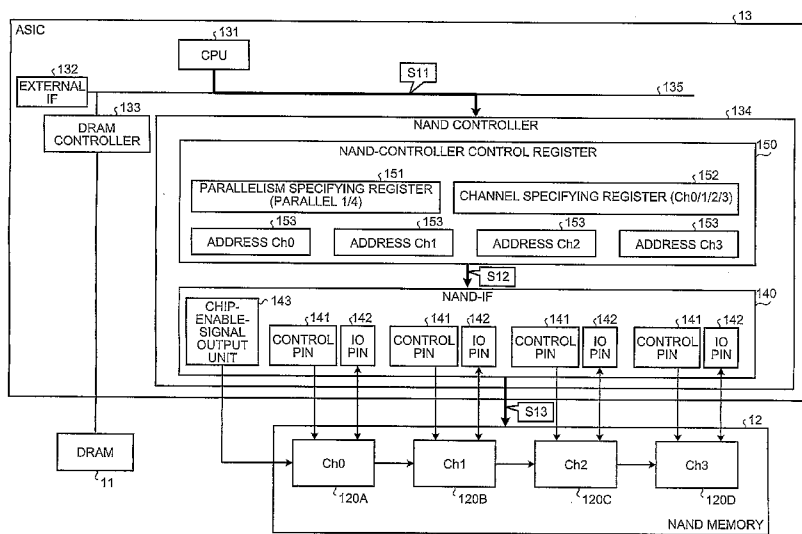
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FIG.5



(57) **Abstract:** A memory system according to an embodiment of the present invention comprises a DRAM 11, a NAND memory 12, a controller 134 having a control register 150 that specifies parallel-operating element specifying information indicating parallel operating elements 120A to 120D in the NAND memory 12 to be used at the time of data access and an address of data with respect to a NAND interface 140, the NAND interface 140 connected in parallel to the respective parallel operating elements 120A to 120D, and a CPU 131 that sets the parallel-operating element specifying information in the control register 150 according to the type of data to be accessed.

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## DESCRIPTION

## MEMORY SYSTEM

## 5 TECHNICAL FIELD

The present invention relates to a memory system configured by using a nonvolatile semiconductor memory.

## BACKGROUND ART

10 Recently, NAND-type flash memory has attracted attention as a type of nonvolatile semiconductor memory. Writing/erasing operations of the NAND-type flash memory are faster than those of NOR-type flash memory. Further, due to the development of manufacturing techniques of  
15 semiconductor devices, downsizing of semiconductor elements has been advanced, and memory capacity per unit area has been increasing. Large capacity memory systems using the NAND-type flash memory have been already commercialized.

Generally in a NAND-type flash memory, a plurality of  
20 pages are collected to form one block. A writing/reading process is performed in a unit of page, and an erasing process is performed in a unit of block (for example, see Patent Document 1).

Further, with recent development of information  
25 technology, many large capacity files, for example, of a size exceeding several megabytes, such as image files, music files, and video files are stored in a secondary storage device such as a personal computer. In the case of applying a memory system using a NAND-type flash memory,  
30 for example, with a page size of 4 kilobytes as the secondary storage device, and when a file considerably larger than a page size, which is a write unit in the NAND-type flash memory, is written, there is a problem that writing must be performed for each page (4 kilobytes), and  
35 therefore it requires a long time for writing the file. On the other hand, if a write size per page is increased to

improve the efficiency of writing of a large-capacity file, an unused area is generated in a page at the time of writing a file smaller than the page size.

Further, a rewriting process of data in the NAND-type flash memory requires processes of saving the data once in a memory such as a dynamic random access memory (DRAM), updating a page to be rewritten on the memory, writing data constituting a block including the updated page in a block from which data has already been erased and different from the block currently storing the data, and erasing an original block. Therefore, at the time of writing a file having a small capacity as compared to the block size and having high rewriting frequency, an unused area is generated in a page and the number of useless erasure increases. Accordingly, the writing efficiency, which is a ratio of an amount of data erased to an amount of data written, decreases to deteriorate a cell constituting the block.

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It is an object of the present invention to provide a memory system that can store data smaller than a block size as well as data larger than the block size, without deteriorating the writing efficiency.

## DISCLOSURE OF INVENTION

A memory system according to an embodiment of the present invention comprises: a volatile first storage unit; a nonvolatile second storage unit that stores data transmitted from a host device via the first storage unit, in which a memory area includes a plurality of parallel operating elements; and a controller that performs data transfer between the first storage unit and the second storage unit, or within the second storage unit, wherein the controller includes: an interface specifying unit that specifies parallel-operating element specifying information indicating the parallel operating element in the second

storage unit to be used for accessing the data and an address of the data to be accessed, with respect to an interface unit; the interface unit connected in parallel to the respective parallel operating elements in the second storage unit for accessing the address of one or a plurality of parallel operating elements in the second storage unit, selected based on the parallel-operating element specifying information and the address specified by the interface specifying unit; and a control unit that sets the parallel-operating element specifying information used for the data access to the interface specifying unit according to type of the data to be accessed, at a time of data access.

A memory system according to an embodiment of the present invention comprises: a volatile first storage unit; a nonvolatile second storage unit that stores data transmitted from a host device via the first storage unit, in which a memory area includes a plurality of parallel operating elements; and a controller that includes: an interface specifying unit that specifies an address to be used for accessing the data with respect to an interface unit; the interface unit connected in parallel to the respective parallel operating elements in the second storage unit for accessing the data based on the address specified by the interface specifying unit; and a control unit that sets the address of a destination in the second storage unit to the interface specifying unit at the time of data access, and that controls transfer of data between the first storage unit and the second storage unit, or within the second storage unit, wherein the control unit determines the parallel operating element to be used for the data access between the interface unit and the second storage unit according to the type of the data to be accessed at the time of the data access, and sets a valid address for the parallel operating element to be used and an invalid address for the parallel operating element not

to be used, with respect to the interface specifying unit.

#### BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a block diagram of one example of a  
5 configuration of a memory system according to a first  
embodiment of the present invention;

Fig. 2 is a circuit diagram of one configuration  
example of one block included in a NAND memory;

Fig. 3 is one configuration example of a NAND-  
10 controller control register according to the first  
embodiment;

Fig. 4 is a block diagram of one example of a  
functional configuration of a CPU;

Fig. 5 is one example of a data transfer process in  
15 the memory system;

Figs. 6(a) and 6(b) depict a processing state of data  
access control in a case of an 8-bit normal mode;

Figs. 7(a) and 7(b) depict a processing state of data  
access control in a case of a 32-bit double speed mode;

Fig. 8 is an example of an address allocating method  
20 according to a second embodiment of the present invention;

Figs. 9(a) and 9(b) are an example of an addressing  
method according to the second embodiment;

Fig. 10 is an example of an address allocating method  
25 in a NAND memory according to a third embodiment of the  
present invention;

Figs. 11(a) and 11(a) are an example of an address  
specifying method according to the third embodiment;

Fig. 12 is an example of area segmentation according  
30 to a parallelism in the NAND memory;

Fig. 13 is an example of a data transfer process in a  
memory system according to a fourth embodiment of the  
present invention;

Fig. 14 schematically depicts one configuration  
35 example of a NAND-controller control register according to  
a fifth embodiment of the present invention; and

Figs. 15(a) and 15(b) are an example when a size of a low-parallelism storage area is varied.

BEST MODE(S) FOR CARRYING OUT THE INVENTION

5 Exemplary embodiments of a memory system according to the present invention will be explained below in detail with reference to the accompanying drawings. The present invention is not limited to the embodiments.

10 A memory system according to a first embodiment of the present invention includes a nonvolatile semiconductor memory, and is used as a secondary storage device (solid state drive (SSD)) of a host device such as a personal computer. The memory system has a function for storing data, for which a writing request has been issued from the  
15 host device, and reading data, for which a reading request has been issued from the host device, to output the data to the host device. Fig. 1 is a block diagram of one example of a configuration of the memory system according to the first embodiment. A memory system 10 includes a DRAM 11 as  
20 a first storage unit, a NAND-type flash memory (hereinafter, "NAND memory") 12 as a second storage unit, and a drive control circuit (denoted as "ASIC" in the drawings) 13.

The DRAM 11 is used as a storage unit for data transfer or for recording management information.  
25 Specifically, the storage unit for data transfer is used for temporarily storing data, for which a writing request has been issued from the host device, before writing the data in the NAND memory 12, or for reading the data, for which a reading request has been issued from the host  
30 device, from the NAND memory 12 and temporarily storing the data. The storage unit that records the management information is used for storing management information for managing a storage position of the data to be stored in the DRAM 11 and the NAND memory 12.

35 The NAND memory 12 is used as the storage unit for storing data. Specifically, the NAND memory 12 stores data

from the host device or stores the management information managed by the DRAM 11 for backup. Fig. 1 depicts a case that the NAND memory 12 includes four parallel operating elements 120A to 120D. Each one of parallel operating elements 120A to 120D includes two packages 121 in which eight chips 122 having a memory capacity of predetermined size are put into one. The two packages 121 in one parallel operating element shares a control pin 141 and an input/output pin 142 of a NAND controller 134, and are connected to the drive control circuit 13 in parallel via a bus. The bus connected to the respective parallel operating elements 120A to 120D function as channels 15A to 15D at the time of transferring the data. In the explanations below, a width of the respective buses to be connected to the respective parallel operating elements 120A to 120D is assumed to be 8 bits.

The drive control circuit 13 controls the DRAM 11 and the NAND memory 12. In the first embodiment, the drive control circuit 13 has such a configuration that a central processing unit (CPU) 131 that performs various types of processing, an external interface (denoted as external IF in the drawings) 132 that transfers data between an external device such as the host device and the drive control circuit 13, a DRAM controller 133 that controls the DRAM 11, and the NAND controller 134 that controls the NAND memory 12 are connected with each other via an internal bus 135.

The NAND controller 134 includes a NAND interface (denoted as NAND-IF in the drawings) 140 that transfers the data between the NAND memory 12 and the NAND controller 34, and a NAND-controller control register 150 that controls the operation of the NAND controller 134. The NAND interface 140 has the control pin 141 and the input and output (IO) pin 142 for each of the parallel operating elements 120A to 120D constituting the NAND memory 12, and is connected to the parallel operating elements 120A to

120D via the channels 15A to 15D. The NAND interface 140 has a chip-enable-signal output unit 143, and is connected to the respective parallel operating elements 120A to 120D. In an example shown in Fig. 1, a chip enable signal line  
5 CE0 connected to chips 122-0 to 122-3 of the respective parallel operating elements 120A to 120D, a chip enable signal line CE1 connected to chips 122-4 to 122-7, a chip enable signal line CE2 connected to chips 122-8 to 122-11, and a chip enable signal line CE3 connected to chips 122-12  
10 to 122-15 are provided.

A configuration of the NAND memory 12 is explained here. The NAND memory 12 is configured by arranging a plurality of blocks, which is a unit of data erasure, on a substrate. Fig. 2 is a circuit diagram of one  
15 configuration example of one block included in the NAND memory. In Fig. 2, right and left direction on the drawing is designated as an X direction, and a direction vertical to the X direction on the drawing is designated as a Y direction.

20 Each block BLK of the NAND memory 12 includes  $(m+1)$  NAND strings NS ( $m$  is an integer equal to or larger than 0) arranged sequentially along the X direction. The respective NAND strings NS include  $(n+1)$  ( $n$  is an integer equal to or larger than 0) memory cell transistors MT0 to  
25 MT $n$  and selection transistors ST1 and ST2 arranged on opposite ends of a line of the  $(n+1)$  memory cell transistors MT0 to MT $n$ .

The respective memory cell transistors MT0 to MT $n$  include a field effect transistor having a laminate gate  
30 structure formed on a semiconductor substrate. The laminate gate structure includes a charge accumulating layer (floating gate electrode) formed on the semiconductor substrate with a gate dielectric film put therebetween, and a control gate electrode formed on the charge accumulating  
35 layer with an intergate dielectric film therebetween. The memory cell transistors MT0 to MT $n$  are respectively a

multi-level memory, in which a threshold voltage changes according to the number of electrons accumulated in the floating gate electrode, and data equal to or larger than 2 bits can be stored according to a difference of the  
5 threshold voltage. In the embodiments described below, a case that the memory cell transistor MT is the multi-level memory is explained as an example; however, the memory cell transistor MT can have a structure for storing 1 bit (binary).

10 Word lines WL0 to WLn are respectively connected to the control gate electrodes of the memory cell transistors MT0 to MTn constituting the NAND string NS, and the memory cell transistors MTi (i=0 to n) in respective NAND strings NS are commonly connected with each other by the same word  
15 lines WLi (i=0 to n). That is, the control gate electrodes of the memory cell transistors MTi on the same line in the block BLK are connected to the same word line WLi. The (m+1) memory cell transistors MTi connected to the same word line WLi are handled as one page, and the page becomes  
20 a minimum unit of writing and reading of data in the NAND memory 12.

The respective bit lines BL0 to BLm are connected to a drain of each of the (m+1) selection transistors ST1 in one block BLK, and a selection gate line SGD is commonly  
25 connected to the gate thereof. A source of the selection transistor ST1 is connected to the drain of the memory cell transistor MT0. Likewise, a source line SL is commonly connected to the source of each of the (m+1) selection transistors ST2 in one block BLK, and a selection gate line  
30 SGS is commonly connected to the gate thereof. The drain of the selection transistor ST2 is connected to the source of the memory cell transistor MTn.

Although not shown, a bit line BLj (j=0 to m) in one block BLK commonly connects to the drains of the selection  
35 transistors ST1 among the bit lines BLj of other blocks BLK. That is, the NAND strings NS on the same line in a

plurality of blocks BLK are connected by the same bit line BL<sub>j</sub>.

In the NAND memory 12, the minimum unit of writing and reading is the page including the memory cell transistors MT<sub>i</sub> connected to the same word line WLi, and the minimum unit of erasure is one block (physical block) including a predetermined number of pages. A plurality of blocks constitutes a plane together, and a plurality of planes constitutes one of parallel operating elements 120A to 120D. The parallel operating elements 120A to 120D constitutes one NAND memory 12. In an example shown in Fig. 1, a case that the number of the parallel operating elements (that is, the number of channels) is four and the number of planes is 2 is shown. The chips 122 constitute the parallel operating elements 120A to 120D; however, the plane and the block are present together in one chip 122.

The respective parallel operating elements 120A to 120D constituting the NAND memory 12 can operate in any mode of a normal mode and a double speed mode at the time of writing and reading. In the normal mode, writing and reading of data is performed for each block in one of parallel operating elements 120A to 120D. For example, writing of data to the block corresponding to a first plane in one parallel operating element is performed in a unit of page with respect to an instructed block, after the data is accumulated for one page in a buffer for the first plane. Likewise, writing of data to the block corresponding to the second plane is performed in a unit of page with respect to the instructed block, after the data is accumulated for one page in a buffer for the second plane. Reading of data is also performed for one page.

The double speed mode is for simultaneously performing writing and reading of data for two blocks by using respective blocks in two planes in one of the parallel operating elements 120A to 120D. For example, when writing of data for two blocks is to be performed with respect to

one parallel operating element, data for one page of the first block is accumulated in the buffer for the first plane, and data for one page of the second block is accumulated in the buffer for the second plane. The pieces  
5 of data accumulated in the buffers for the first and second planes are then written in the first block of the first plane and the second block of the second plane, respectively (executes a program). In this manner, the data for two pages can be written in one program time.  
10 Reading of data can be performed in the same manner.

Because the parallel operating elements 120A to 120D are respectively connected to the drive control circuit 13 in parallel via the channel, the parallel operating elements 120A to 120D can be accessed in parallel, or the  
15 data can be transferred only to one channel to access the parallel operating element.

In the first embodiment, in the case of Fig. 1, writing/reading speed of data and a parallelism of channels are combined, to provide two types of access modes.

20 (1) 8-bit normal mode

In this mode, only one channel of the four channels connected to the drive control circuit 13 is operated to perform writing and reading in a unit of 8 bits with respect to the blocks of one parallel operating element. A  
25 unit of writing/reading size of data is page size, and a unit of erasure size is one physical block size.

(2) 32-bit double speed mode

In this mode, four channels connected to the drive control circuit 13 are operated in parallel, and reading and writing are performed by using the double speed mode  
30 using two planes of the respective parallel operating elements. A unit of writing/reading size of data is "page size  $\times$  4 channels  $\times$  2", and a unit of erasure size is 8-physical block size.

35 Writing and reading of data to the NAND memory 12 can be performed by specifying an address at the time of

writing the data to the NAND memory 12, other than the two types of access modes. Fig. 3 is one configuration example of the NAND-controller control register according to the first embodiment. The NAND-controller control register 150  
5 includes a parallelism specifying register 151, a channel specifying register 152, and an address specifying register 153.

The parallelism specifying register 151 sets the number of channels for performing writing and reading at a  
10 time, that is, the parallelism. In this case, either one of one channel and four channels can be set. When one channel is set, the speed of reading and writing becomes that of the normal mode as a necessity, and when four channels are set, the speed of reading and writing becomes  
15 that of the double speed mode. That is, when one channel is set by the parallelism specifying register 151, the access mode is 8-bit normal mode, and when four channels are set, the access mode is 32-bit double speed mode.

The channel specifying register 152 sets the channel  
20 to be used at the time of access without using all the channels simultaneously. In this example, when one channel is set by the parallelism specifying register 151, one channel that performs a writing/reading process or an erasing process is set from the channels 15A to 15D. When  
25 four channels 15A to 15D are set by the parallelism specifying register 151, the channel specifying register 152 indicates "no specification".

The address specifying register 153 sets an address on the parallel operating elements 120A to 120D that performs  
30 the writing/reading process or the erasing process.

A function for the CPU 131 to be set in the NAND-controller control register 150 is explained next. Fig. 4 is a block diagram of one example of a functional configuration of the CPU. The CPU 131 includes a data  
35 transfer processor 1311 that performs data transfer between the DRAM 11 and the NAND memory 12, a management-

information managing unit 1312 that changes or stores the management information with a change of the data to be stored in the DRAM 11 and the NAND memory 12, a management-information recovering unit 1313 that recovers the latest management information based on the management information stored in the NAND memory 12 at the time of power ON, and a processing-condition setting unit 1314 that performs setting of an accessing condition with respect to the NAND memory 12 to the processing-condition setting unit 1314.

5  
10 The processing-condition setting unit 1314 performs setting with respect to the NAND-controller control register 150 according to the type of data to be written in the NAND memory 12 or the type of data to be read from the NAND memory 12. In an example explained below, the processing-condition setting unit 1314 can set such that in the case of data to which an access is instructed from the host device, the processes are performed in the 32-bit double speed mode, and when the data generated in the memory system 10 is written or read, the processes are performed in the 8-bit normal mode.

15  
20 There is management-information storage information, which is a backup of the management information for managing the storage position of the data to be stored in the NAND memory 12, as the data generated in the memory system 10 when the processes are performed in the 8-bit normal mode. The management information is managed on the DRAM 11 by the management-information managing unit 1312 in the CPU 131. The management-information managing unit 1312 stores a snapshot, which is a copy of the management information at a certain point in time, and a log, which is difference information of the management information before and after a change, when the change occurs in the management information, as the management-information storage information in the NAND memory 12. Normally, when the memory system 10 is being operated, a command (flush cache command) for saving the management information on the

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30  
35

DRAM 11 in the NAND memory 12 is frequently issued, and the log, which is an update of the management information, is written in the NAND memory 12. At the time of power OFF, the management information on the DRAM 11 is written in the  
5 NAND memory 12 as the snapshot.

A data transfer operation in the memory system 10 is explained next. Fig. 5 is one example of a data transfer process in the memory system. In this example, a case that the data transfer is performed between the DRAM 11 and the  
10 NAND memory 12 is explained. The processing-condition setting unit 1314 in the CPU 131 obtains the type of data transferred between the DRAM 11 and the NAND memory 12 and the address (chip 122) to be accessed on the NAND memory 12.

The processing-condition setting unit 1314 determines  
15 the type of data to set the parallelism ("1" or "4") with respect to the parallelism specifying register 151 in the NAND-controller control register 150. That is, the processing-condition setting unit 1314 sets the parallelism to "4" in the case of data requested from the host device,  
20 and sets the parallelism to "1" in the case of writing or reading of data generated in the memory system 10. The processing-condition setting unit 1314 sets the channel to be used by the NAND memory 12 (when the parallelism is "1", any one of channels, and when the parallelism is "4", "no specification") to the channel specifying register 152  
25 based on a destination address of the data, and sets the destination address to the address specifying register 153 (Step S11). When setting to the NAND-controller control register 150 by the processing-condition setting unit 1314  
30 is complete, data transfer between the DRAM 11 and the NAND memory 12 is started by the data transfer processor 1311.

Thereafter, the NAND-controller control register 150 transfers a value of the parallelism specifying register 151 and a value of the channel specifying register 152 to  
35 the NAND interface 140 (Step S12). The NAND interface 140 controls the channel specified by the parallelism

specifying register 151 and the channel specifying register 152. The NAND interface 140 then performs control for accessing the data at the address specified by the address specifying register 153 (Step S13). Accordingly, transfer  
5 of data transferred between the DRAM 11 and the NAND memory 12 is controlled.

A data-access control process performed by the NAND controller 134 at Steps S12 and S13 is explained sequentially for the case of the 8-bit normal mode and the  
10 case of the 32-bit double speed mode. Figs. 6(a) and 6(b) depict a processing state of data access control in the case of the 8-bit normal mode, where Fig. 6(a) depicts an outline of data access control state between the NAND controller and the NAND memory, and Fig. 6(b) depicts an  
15 input state of a signal to respective chips constituting the NAND memory. An example in which "1" is set as the parallelism (that is, the 8-bit normal mode is set), "Ch1" (parallel operating element 120B) is specified as the channel, and "chip 122-10" is specified as the address is  
20 explained here. However, in practice, instead of the chip, an address in the chip 122 (the parallel operating elements 120A to 120D) is specified as the address.

As shown in Fig. 6(a), the NAND interface 140 controls a control pin 141A and an input/output pin 142A so that the  
25 signal is transmitted only to Ch1, upon reception of the value of the parallelism specifying register 151 and the value of the channel specifying register 152 from the NAND-controller control register 150. Further, as shown in Fig. 6(b), the chip-enable-signal output unit 143 in the NAND  
30 interface 140 supplies a chip enable signal only to the address in the chip 122-10 specified by the address specifying register 153 via the chip enable signal line CE2. Accordingly, data transfer in the normal mode is performed, not in a parallel mode, between the DRAM 11 and a  
35 predetermined address in the chip 122-10 of the parallel operating element 120B in the NAND memory 12.

Figs. 7(a) and 7(b) depict a processing state of data access control in the case of the 32-bit double speed mode, where Fig. 7(a) depicts an outline of data access control state between the NAND controller and the NAND memory, and  
5 Fig. 7(b) depicts an input state of a signal to respective chips constituting the NAND memory. An example in which "4" is set as the parallelism (that is, the 32-bit double speed mode is set), "No specification" is specified as the channel, and "chip 122-5" is specified as the address is  
10 explained here.

As shown in Fig. 7(a), the NAND interface 140 controls all the control pins 141 and all the input/output pins 142 so that the signal is transmitted to all of the parallel operating elements 120A to 120D, upon reception of the  
15 value of the parallelism specifying register 151 and the value of the channel specifying register 152 from the NAND-controller control register 150. At this time, the NAND interface 140 controls the respective parallel operating elements 120A to 120D so that data writing and reading are  
20 performed in the double speed mode. Further, as shown in Fig. 7(b), the chip-enable-signal output unit 143 in the NAND interface 140 supplies the chip enable signal only to the address in the chip 122-5 specified by the address specifying register 153 via the chip enable signal line CE1.  
25 Accordingly, data transfer in the double speed mode in parallel of four is performed between the DRAM 11 and a predetermined address in the chip 122-5 of all the parallel operating elements 120A to 120D in the NAND memory 12.

The data transfer process is finished when transfer of  
30 data specified by the conditions specified by the NAND-controller control register 150 is finished.

In the above explanations, respective channels in the NAND memory 12 are controlled by the parallelism specifying register 151 including not only the parallelism of the  
35 channels but also the data transfer speed. However, the parallelism specifying register 151 can specify only the

parallelism of the channels, and a transfer-speed specifying register for specifying the transfer speed can be separately provided to change over the normal mode and the double speed mode. According to such a configuration, combinations of the parallelism and the data transfer speed can be made more extensive by separately specifying the parallelism and the data transfer speed. In the above explanations, the parallelism can be selected only either "1" or "4"; however, the parallelism can be made selectable in a range of maximum number of channels.

Further, an example in which the processing-condition setting unit 1314 sets the processing condition such that the data to be accessed from the host device is accessed in the 32-bit double speed mode, and the data generated in the NAND memory 12 is accessed in the 8-bit normal mode has been explained above. However, in the case of the NAND memory 12 having a memory capacity of several tens of gigabytes, the size of the management information increases, and the snapshot as the backup of the management information has a size of around "block size  $\times$  2  $\times$  4 channels". On the other hand, the log generally has a size of around page size, because the log is the difference information. Therefore, the processing-condition setting unit 1314 can set the processing condition such that when writing and reading are performed with respect to the data to be accessed from the host device and the snapshot in the management-information storage information, these pieces of information are accessed in the 32-bit double speed mode, and when writing and reading of the log in the management-information storage information are performed, the information is accessed in the 8-bit normal mode. The same thing applies to embodiments described below.

According to the first embodiment, the parallelism of the channels 15A to 15D and the transfer speed at the time of data access to the NAND memory 12 in the NAND controller 134 are specified according to the type of data by the

parallelism specifying register 151, and the channel to be used when not all the channels 15A to 15D are used is specified by the channel specifying register 152. As a result, when writing of data smaller than the predetermined size, such as the log of data generated in the memory system 10 is performed, one selected channel is used in the 8-bit normal mode, to enable writing into one selected block of the parallel operating elements 120A to 120D in a unit of page, thereby enabling to increase the writing efficiency. Further, in the case of data requiring rewrite, the parallelism is decreased, thereby enabling to avoid useless erasure of a physical block for which rewriting is not performed. On the other hand, when data equal to or larger than a predetermined size, such as data instructed from the host device or the snapshot, is written, read, or rewritten, the transfer speed is set to double the speed of the normal mode, and by increasing the parallelism (for example, parallel of four), data in a fourfold amount can be written or read at a double speed as compared to the 8-bit normal mode. Thus, an efficient writing/reading process can be performed according to the size of data to be accessed, and service life of the memory system 10 can be extended by avoiding useless erasure at the time of rewrite.

In the first embodiment, the parallelism of the channels is specified by the parallelism specifying register 151 in the NAND-controller control register 150, and the channel to be used is specified according to the specified parallelism by the channel specifying register 152. In a second embodiment of the present invention, a method of reducing the number of conditions to be set in the NAND-controller control register 150 by designing an address setting method at the time of performing data transfer by the data transfer processor is explained.

Fig. 8 is an example of an address allocating method according to the second embodiment. In the first

embodiment, a case that a physical address is allocated independently to each of the parallel operating elements 120A to 120D constituting the NAND memory 12 and the range of the physical address is from 0 to 5000 is described as an example. At this time, the data transfer processor 1311 in the CPU 131 has a function for specifying a value among 0 to 5000, which is the valid address range, as an address only for a channel connected to the parallel operating element to be accessed of the parallel operating elements 120A to 120D, and specifying a numerical value outside the valid address range, for example, 5001 as the address for a channel connected to the parallel operating element not to be accessed of the parallel operating elements 120A to 120D.

By specifying the address by the data transfer processor 1311, the parallelism of channels and the channel to be used at the time of performing the data transfer are specified. As a result, the NAND-controller control register 150 does not require the parallelism specifying register 151 and the channel specifying register 152, and needs only the address specifying register 153. Further, the processing-condition setting unit 1314 needs only to specify the address to be accessed by the data transfer processor 1311 in the address specifying register 153.

Figs. 9(a) and 9(b) are an example of the addressing method according to the second embodiment. In this example, the data transfer processor 1311 can only select either "1" or "4" as the parallelism, and the parallelism includes information of the data transfer speed. That is, when addressing specifying the parallelism as "1" is performed, it is regarded that the 8-bit normal mode is selected, and when addressing specifying the parallelism as "4" is performed, it is regarded that the 32-bit double speed mode is selected. In the explanations below, it is assumed that identifiers of channels used for specifying the channel are Ch0, Ch1, Ch2, and Ch3, respectively.

In Fig. 9(a), an address (5001) invalid for

designation to channels Ch0, Ch1, and Ch3 is specified in address designation information at the time of data access by the data transfer processor 1311, and an address effective for designation to channel Ch2 is specified.

5 Therefore, it is regarded that the parallelism "1" is specified and "Ch2" is specified as the channel. As a result, the NAND controller 134 determines that it is a data accessing process in which the parallelism is "1" indicating that only channel Ch2 is used and the data  
10 access speed is the normal mode, to perform processes. At this time, the processing-condition setting unit 1314 sets the specified address in the address specifying register 153. Thus, when the process is performed with the parallelism "1", an address in an address range effective  
15 only for the channel to be used is set, and an address outside the valid address range is specified to other channels in the address designation information.

In Fig. 9(b), because a valid address is set to all the channels Ch0 to Ch3 in the address designation  
20 information by the data transfer processor 1311, the parallelism "4" is specified, and "no specification" is specified as the channel. As a result, the NAND controller 134 determines that it is a data accessing process in which the parallelism is "4" indicating that all the channels Ch0  
25 to Ch3 are used with the data access speed in the double speed mode, to perform processes. At this time, the processing-condition setting unit 1314 sets the specified address in the address specifying register 153.

In the above explanations, the data transfer speed is  
30 included in the specification of the parallelism in the address setting by the data transfer processor 1311. However, the configuration can be such that a pure parallelism without including the data transfer speed is specified in the address setting by the data transfer  
35 processor 1311, and the data transfer speed is set by the processing-condition setting unit 1314 by separately

providing a transfer-speed specifying register in the NAND-controller control register 150.

According to the second embodiment, when an address is set in the access designation information for the data to be accessed by the data transfer processor 1311, a value in an invalid address range is set to the parallel operating element not be accessed of the parallel operating elements 120A to 120D. Therefore, the parallelism specifying register 151 for specifying the parallelism does not need to be provided in the NAND-controller control register 150, thereby enabling to simplify the apparatus configuration of the memory system 10.

In the second embodiment, the address in a range of from 0 to 5000 is respectively allocated to each parallel operating element and an address value outside the valid address range is specified to the channel to be connected to the parallel operating element, which does not perform the data transfer process, to thereby set the parallelism, and therefore the parallelism specifying register and the channel specifying register are not provided. In a third embodiment of the present invention, a case that the parallelism is set by another address specifying method and the parallelism specifying register and the channel specifying register are not provided is explained.

Fig. 10 is an example of the address allocating method in the NAND memory according to the third embodiment. In the second embodiment, as shown in Fig. 8, the address is allocated to each of the parallel operating elements 120A to 120D constituting the NAND memory 12. However, in the third embodiment, as shown in Fig. 10, the addresses 0, 1, 2, 3 are allocated in order from the head of the parallel operating elements 120A, 120B, 120C, and 120D, and the addresses are allocated in this order thereafter to allocate one address as the entire NAND memory 12. That is, when it is assumed that  $n$  is integer equal to or larger than 0, and the address is described in decimal notation,

addresses 0, 4, 8, ...,  $2n$ , ..., are allocated to the parallel operating element 120A (Ch0), addresses 1, 5, 9, ...,  $2n+1$ , ..., are allocated to the parallel operating element 120B (Ch1), addresses 2, 6, 10, ...,  $2n+2$ , ..., are allocated to the parallel operating element 120C (Ch2), and  
5 addresses 3, 7, 11, ...,  $2n+3$ , ... are allocated to the parallel operating element 120D (Ch3).

By allocating the address in this manner, in the decimal notation, when a remainder obtained by dividing the  
10 address by 4 is "0", the parallel operating element 120A (Ch0) is indicated, when the remainder is "1", the parallel operating element 120B (Ch1) is indicated, when the remainder is "2", the parallel operating element 120C (Ch2) is indicated, and when the remainder is "3", the parallel  
15 operating element 120D (Ch3) is indicated. That is, the last two digits of the address in binary notation are "00" in Ch0, "01" in Ch1, "10" in Ch2, and "11" in Ch3. Therefore, these numbers can be used as channel identification information (corresponding to parallel-  
20 operating element identification information in the claims) for identifying the channel. The presence of channel use and the parallelism can be set according to the presence of the channel identification information.

That is, the data transfer processor 1311 performs  
25 addressing so that the channel identification information of the channel is included in the data of the parallel operating element to be accessed of the parallel operating elements 120A to 120D, and the channel identification information of the channel is not included in the data of  
30 the parallel operating element not to be accessed of the parallel operating elements 120A to 120D. Specifically, the data transfer processor 1311 assigns a value (channel identification information) identifying the channel (parallel operating element) to the last two digits of the  
35 address of the data of the parallel operating element to be accessed of the parallel operating elements 120A to 120D,

and assigns a value other than the value (channel identification information) identifying the channel (parallel operating element) to the last two digits of the address of the parallel operating element not to be  
5 accessed of the parallel operating elements 120A to 120D.

Figs. 11(a) and 11(b) are an example of the address specifying method according to the third embodiment. In this example, it is assumed that the data transfer processor 1311 can only select either one of parallelisms  
10 "1" and "4", and the parallelism includes the data transfer speed. That is, when the addressing is performed so that the parallelism is "1", it is regarded that the 8-bit normal mode is selected, and when addressing is performed so that the parallelism is "4", it is regarded that the 32-  
15 bit double speed mode is selected.

In Fig. 11(a), in the access designation information by the data transfer processor 1311, an invalid address is specified as the address of channels Ch0, Ch1, and Ch3. That is, in the respective addresses to be specified to  
20 channels Ch0, Ch1, and Ch3, in the decimal notation, the remainder obtained by dividing the address by 4 should be originally 0, 1, and 3, respectively; however, in this case, the remainder is 2 for all of those channels. On the other hand, the valid address is specified only to the channel  
25 Ch2. That is, the remainder obtained by dividing the address of channel Ch2 in the decimal notation by 4 is 2. As a result, the NAND controller 134 determines that it is a data accessing process in which the parallelism is "1" indicating that only the channel Ch2 is used with the data  
30 access speed in the normal mode, to perform processes. Thus, in the case of a process performed with the parallelism "1", the address is set only to the channel to be used so that the channel identification information set to the channel is included (that is, the address to be  
35 accessed originally is set), and the address not including the channel identification information is set to other

parallel operating elements.

In Fig. 11(b), a valid address is specified to all the channels Ch0 to Ch3 in the address designation information by the data transfer processor 1311. That is, the address  
5 designated to all the channels Ch0 to Ch3 includes the valid channel identification information in the respective channels Ch0 to Ch3. More specifically, the remainder obtained by dividing the respective addresses of the channels Ch0, Ch1, Ch2, and Ch3 in the decimal notation by  
10 4 is 0, 1, 2, and 3, respectively. As a result, the NAND controller 134 determines that it is a data accessing process in which the parallelism is "4" indicating that all the channels Ch0 to Ch3 are used with the data access speed in the double speed mode, to perform processes.

15 In the above explanations, the data transfer speed is included in the specification of the parallelism in the address setting by the data transfer processor 1311. However, the configuration can be such that a pure parallelism without including the data transfer speed is  
20 specified in the address setting by the data transfer processor 1311, and the data transfer speed is set by the processing-condition setting unit 1314 by separately providing a transfer-speed specifying register in the NAND-controller control register 150.

25 According to the third embodiment, when the data transfer processor 1311 sets the address, the parallel operating element not to be accessed is set with an invalid address not including the channel identification information thereof. Therefore, the parallel specifying  
30 register 151 for specifying the parallelism and the channel specifying register 152 for specifying the channel to be used need not be provided in the NAND-controller control register 150, thereby enabling to simplify the apparatus configuration of the memory system 10.

35 In a fourth embodiment of the present invention, a case that an exclusive area for storing data having a low

parallelism is defined in the NAND memory is explained.

Fig. 12 is an example of area segmentation according to the parallelism in the NAND memory. As shown in Fig. 12, a low-parallelism storage area 1210 for storing low-parallelism data and a high-parallelism storage area 1220 for storing high-parallelism data are provided. That is, addressing is performed so that the low-parallelism storage area 1210 is divided. The low-parallelism storage area 1210 is in a range of from addresses 0 to 200, and the high-parallelism storage area 1220 is in a range of from addresses 201 to XXX. It is assumed that the address which becomes a boundary between the low-parallelism storage area 1210 and the high-parallelism storage area 1220 is predetermined. As a specific example of the low-parallelism storage area 1210, for example, an area for storing the management-information storage information, and more specifically, an area for storing the log in the management-information storage information can be mentioned. As a specific example of the high-parallelism storage area 1220, an area for storing data for which storage is instructed from the host device and an area for storing the snapshot in the management-information storage information can be mentioned.

This example indicates a case that the parallelism is set to either "1" or "4", and it is assumed that the parallelism includes the data transfer speed. That is, the low-parallelism storage area 1210 with the parallelism "1" is accessed at a speed in the 8-bit normal mode, and the high-parallelism storage area 1220 with the parallelism "4" is accessed at a speed in the 32-bit normal mode.

Thus, by segmenting the area to be accessed according to the difference in the parallelism, the address can be decoded on the NAND controller 134 side and the transfer parallelism can be recognized. That is, when a destination address is 0 to 200, the area is the low-parallelism storage area 1210, and therefore the NAND interface 140

accesses the low-parallelism storage area 1210 in the 8-bit normal mode with the parallelism "1", and when the destination address is 201 to XXX, the area is the high-parallelism storage area 1220, and therefore the NAND  
5 interface 130 accesses the high-parallelism storage area 1220 in the 32-bit double speed mode with the parallelism "4".

An operation of the data transfer process in the memory system 10 having such a configuration is explained  
10 next. Fig. 13 is an example of the data transfer process in the memory system according to the fourth embodiment. In this example, a case that the data transfer is performed between the DRAM 11 and the NAND memory 12 is explained. The processing-condition setting unit 1314 in the CPU 131  
15 obtains the type and address of data to be transferred between the DRAM 11 and the NAND memory 12.

The processing-condition setting unit 1314 then sets the parallel operating elements 120A to 120D corresponding to the destination address with respect to the channel  
20 specifying register 152 based on the type and address of the data, and sets the destination address with respect to the address specifying register 153 in the NAND-controller control register 150 (Step S31). When setting to the NAND-controller control register 150 by the processing-condition  
25 setting unit 1314 is complete, the data transfer process between the DRAM 11 and the NAND memory 12 by the processing-condition setting unit 1314 is started.

The NAND interface 140 in the NAND controller 134 determines the parallelism for accessing data based on the  
30 channel specified by the channel specifying register 152 and the address specified by the address specifying register 153 in the NAND-controller control register 150, to control the parallel operating elements 120A to 120D to be used (Step S32). That is, when the address is from 0 to  
35 200, because the destination is in the low-parallelism storage area 1210, access is performed in the 8-bit normal

mode, and when the address is from 201 to XXX, because the destination is in the high-parallelism storage area 1220, access is performed in the 32-bit double speed mode.

Accordingly, transfer of data transferred between the DRAM  
5 11 and the NAND memory 12 is controlled. When data access is complete, the data transfer process finished.

At Step S32, the NAND interface 140 determines the parallelism to control the access to the respective channels in the NAND memory 12, however, the NAND-  
10 controller control register 150 can transmit the value of the channel set in the channel specifying register 152 and the destination address set in the address specifying register 153 to the NAND interface 140, so that the NAND-controller control register 150 side controls the channel  
15 (Step S32').

In the above explanations, the data transfer speed is included in the specification of the parallelism. However, the configuration can be such that the pure parallelism without including the data transfer speed is specified, and  
20 the data transfer speed is set by the processing-condition setting unit 1314 by separately providing the transfer-speed specifying register in the NAND-controller control register 150.

According to the fourth embodiment, because the NAND  
25 memory 12 is segmented into areas according to a difference in the parallelism of data to be accessed, the parallelism can be set according to the destination address, and the parallelism specifying register 151 for specifying the parallelism does not need to be provided in the NAND-  
30 controller control register 150, thereby enabling to simplify the apparatus configuration of the memory system 10.

In the fourth embodiment, a case that the low-parallelism storage area and the high-parallelism storage  
35 area are provided in the NAND memory is described. However, in a fifth embodiment of the present invention, such a

configuration that the size of the low-parallelism storage area and the size of the high-parallelism storage area in the NAND memory are made variable is explained.

Fig. 14 schematically depicts one configuration example of the NAND-controller control register according to the fifth embodiment. The NAND-controller control register 150 includes a low-parallelism storage-area specifying register 154 that can vary the address area of the low-parallelism storage area 1210 for storing data with a low parallelism, in addition to the channel specifying register 152 and the address specifying register 153. The low-parallelism storage-area specifying register 154 is set by the processing-condition setting unit 1314 in the CPU 131, and can vary the size of the low-parallelism storage area 1210.

Figs. 15(a) and 15(b) are an example when the size of the low-parallelism storage area is varied. In Fig. 15(a), the low-parallelism storage-area specifying register 154 sets the low-parallelism storage area 1210 to a range of from address 0 to address 200. On the other hand, in Fig. 15(b), the low-parallelism storage-area specifying register 154 sets the low-parallelism storage area 1210 to a range of from address 0 to address 300. In this manner, the size of the low-parallelism storage area 1210 can be changed by arbitrarily setting the value of the low-parallelism storage-area specifying register 154 by the processing-condition setting unit 1314.

In the above explanations, a case that the low-parallelism storage-area specifying register 154 that varies the address range of the low-parallelism storage area 1210 is provided is shown, however, the present invention is not limited thereto. For example, a parallelism storage-area setting register that changes the size of the storage area for storing data of an arbitrary parallelism  $s$  ( $s$  is a natural number) can be provided. Because the data transfer process in the fifth embodiment

is the same as that in the fourth embodiment, explanations thereof will be omitted.

According to the fifth embodiment, because the parallelism storage-area setting register that changes the address range in the parallelism storage area for storing  
5 data with a certain parallelism is provided, the area required for storing data with the certain parallelism can be arbitrarily set.

In the above explanations, an example in which the  
10 memory system using the NAND memory as the second storage unit has been explained, however, the present invention is not limited thereto. The NAND memory can include a memory cell transistor capable of recording multivalued data equal to or larger than 2 bits, instead of including the memory  
15 cell transistor capable of recording the binary value. The above embodiments can be applied to a case that the memory system uses another nonvolatile semiconductor memory as the second storage unit. In the above explanations, the unit of writing and reading of data in the NAND memory 12 is the  
20 unit of page size, and the unit of erasure and the unit of management are the unit of block size, however, the present invention is not limited thereto, and an arbitrary unit can be used respectively.

In the above explanations, an example of the memory  
25 system in which the first storage unit is the DRAM 11, which is a volatile memory, and the second storage unit is the NAND memory 12, which is a nonvolatile memory, has been explained, however, the present invention is not limited thereto. For example, the above embodiments can be applied  
30 to a memory system in which the first storage unit is a nonvolatile memory and the second storage unit is also a nonvolatile memory. In this case, the process of storing the management-information storage information such as the snapshot, which is the backup of the management information  
35 managed by the first storage unit (nonvolatile memory), and the log in the second storage unit (NAND memory) is not

required. However, the parallelism and the data transfer speed can be varied according to the data size.

According to the present invention, data smaller than the block size and data larger than the block size can be  
5 stored without deteriorating the writing efficiency.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and  
10 described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

15

## CLAIMS

1. A memory system comprising:
  - a volatile first storage unit;
  - a nonvolatile second storage unit that stores data
  - 5 transmitted from a host device via the first storage unit, in which a memory area includes a plurality of parallel operating elements; and
  - a controller that performs data transfer between the first storage unit and the second storage unit, or within
  - 10 the second storage unit, wherein
    - the controller includes:
      - an interface specifying unit that specifies parallel-
      - operating element specifying information indicating the parallel operating element in the second storage unit to be
      - 15 used for accessing the data and an address of the data to be accessed, with respect to an interface unit;
      - the interface unit connected in parallel to the respective parallel operating elements in the second storage unit for accessing the address of one or a
      - 20 plurality of parallel operating elements in the second storage unit, selected based on the parallel-operating element specifying information and the address specified by the interface specifying unit; and
      - a control unit that sets the parallel-operating
      - 25 element specifying information used for the data access to the interface specifying unit according to type of the data to be accessed, at a time of data access.
2. The memory system according to claim 1, wherein
- 30 the parallel operating element has a plurality of planes, and is constituted so that a normal mode in which number of planes to be used simultaneously at a time of accessing the parallel operating elements is one and a double speed mode in which the number of planes is plural
- 35 can be changed over,
  - the interface specifying unit further includes a

function for specifying a mode of data in the parallel operating elements in the second storage unit, and

the control unit further includes a function for specifying the mode of the data with respect to the interface specifying unit according to the type of the data at the time of the data access.

3. The memory system according to claim 1, wherein the controller further includes a data transfer processor that performs data access between the host device and the second storage unit via the first storage unit, and

when the data accessed by the data transfer processor is data, to which an access is instructed by the host device, the control unit sets the interface specifying unit to use all the parallel operating elements.

4. The memory system according to claim 1, wherein when data generated in the memory system is accessed, the control unit sets the interface specifying unit to use only one parallel operating element.

5. The memory system according to claim 4, wherein the data generated in the memory system is management information managed by the controller and including a storage position of the data stored in the second storage unit.

6. The memory system according to claim 1, wherein the first storage unit stores management information including a storage position of the data stored in the second storage unit,

the second storage unit has a management information storage area for storing management-information storage information including a snapshot, which is a copy of the management information at a certain point in time, and a log, which is difference information of the management

information before and after a change, when the change occurs in the management information, and

when the log is stored in the management information storage area, the control unit sets the interface specifying unit to use only one parallel operating element in a normal mode, and when the snapshot is stored in the management information storage area, the control unit sets the interface specifying unit to use all the parallel operating elements in a double speed mode.

10

7. The memory system according to claim 1, wherein the first storage unit is a dynamic random access memory (DRAM), and the second storage unit is a NAND-type flash memory.

15 8. A memory system comprising:

a volatile first storage unit;

a nonvolatile second storage unit that stores data transmitted from a host device via the first storage unit, in which a memory area includes a plurality of parallel operating elements; and

20

a controller that includes: an interface specifying unit that specifies an address to be used for accessing the data with respect to an interface unit; the interface unit connected in parallel to the respective parallel operating elements in the second storage unit for accessing the data based on the address specified by the interface specifying unit; and a control unit that sets the address of a destination in the second storage unit to the interface specifying unit at the time of data access, and that controls transfer of data between the first storage unit and the second storage unit, or within the second storage unit, wherein

25

30

the control unit determines the parallel operating element to be used for the data access between the interface unit and the second storage unit according to the type of the data to be accessed at the time of the data

35

access, and sets a valid address for the parallel operating element to be used and an invalid address for the parallel operating element not to be used, with respect to the interface specifying unit.

5

9. The memory system according to claim 8, wherein in the second storage unit, an address is allocated for each of the parallel operating elements.

10 10. The memory system according to claim 8, wherein when an address is allocated to the second storage unit in whole so that parallel-operating element identification information capable of identifying each parallel operating element in the second storage unit is included, the control  
15 unit sets the valid address including the parallel-operating element identification information for the parallel operating element to be used for the data access and sets the invalid address not including the parallel-operating element identification information for the  
20 parallel operating element not to be used, with respect to the interface specifying unit.

11. The memory system according to claim 8, wherein the  
25 respective parallel operating elements in the second storage unit have a data storage area by a parallelism in which a memory area to be accessed is set according to number of parallel operating elements to be used at the time of the data access,

the control unit selects the data storage area by a  
30 parallelism according to the type of the data at the time of the data access and sets the address in the data storage area by a parallelism to the interface specifying unit, and  
the interface unit determines the number of the  
parallel operating elements based on the address set to the  
35 interface specifying unit, to perform the data access between the second storage unit and the interface unit.

12. The memory system according to claim 11, wherein the interface specifying unit further includes a function for specifying a range of the data storage area by a  
5 parallelism provided for the respective parallel operating elements in the second storage unit.
13. The memory system according to claim 8, wherein  
the parallel operating element has a plurality of  
10 planes, and is constituted so that a normal mode in which number of planes to be used simultaneously at a time of accessing the parallel operating elements is one and a double speed mode in which the number of planes is plural can be changed over,  
15 the interface specifying unit further includes a function for specifying a mode of data in the parallel operating elements in the second storage unit, and  
the control unit further includes a function for specifying the mode of the data with respect to the  
20 interface specifying unit according to the type of the data at the time of the data access.
14. The memory system according to claim 8, wherein the controller further includes a data transfer processor that  
25 performs data access between the host device and the second storage unit via the first storage unit, and  
when the data accessed by the data transfer processor is data, to which an access is instructed by the host device, the control unit sets the interface specifying unit  
30 to use all the parallel operating elements.
15. The memory system according to claim 8, wherein when data generated in the memory system is accessed, the control unit sets the interface specifying unit to use only  
35 one parallel operating element.

16. The memory system according to claim 15, wherein the data generated in the memory system is management information managed by the controller and including a storage position of the data stored in the second storage unit.

17. The memory system according to claim 8, wherein the first storage unit stores management information including a storage position of the data stored in the second storage unit,

the second storage unit has a management information storage area for storing management-information storage information including a snapshot, which is a copy of the management information at a certain point in time, and a log, which is difference information of the management information before and after a change, when the change occurs in the management information, and

when the log is stored in the management information storage area, the control unit sets the interface specifying unit to use only one parallel operating element in a normal mode, and when the snapshot is stored in the management information storage area, the control unit sets the interface specifying unit to use all the parallel operating elements in a double speed mode.

18. The memory system according to claim 8, wherein the first storage unit is a dynamic random access memory (DRAM), and the second storage unit is a NAND-type flash memory.

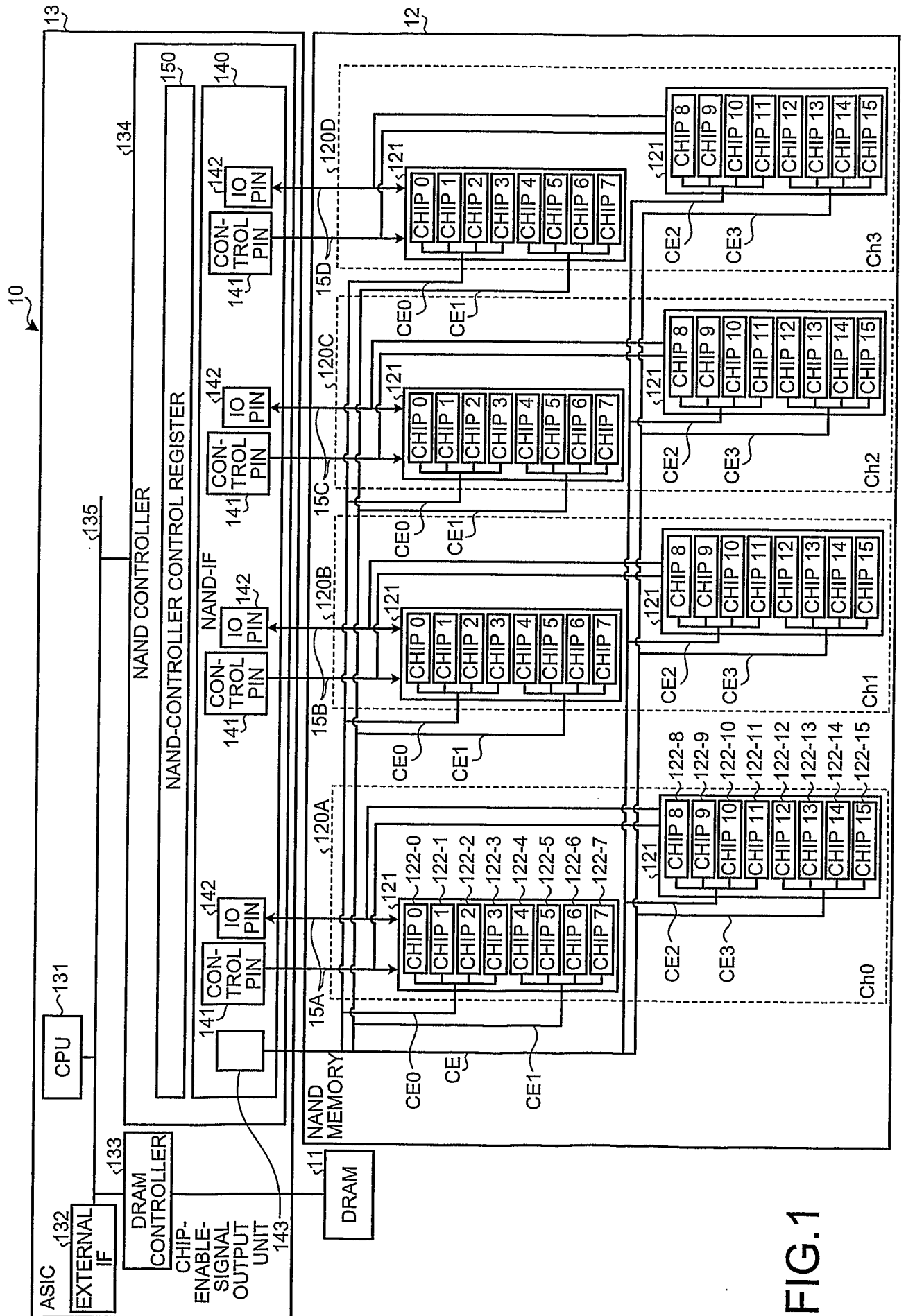


FIG.1

FIG.2

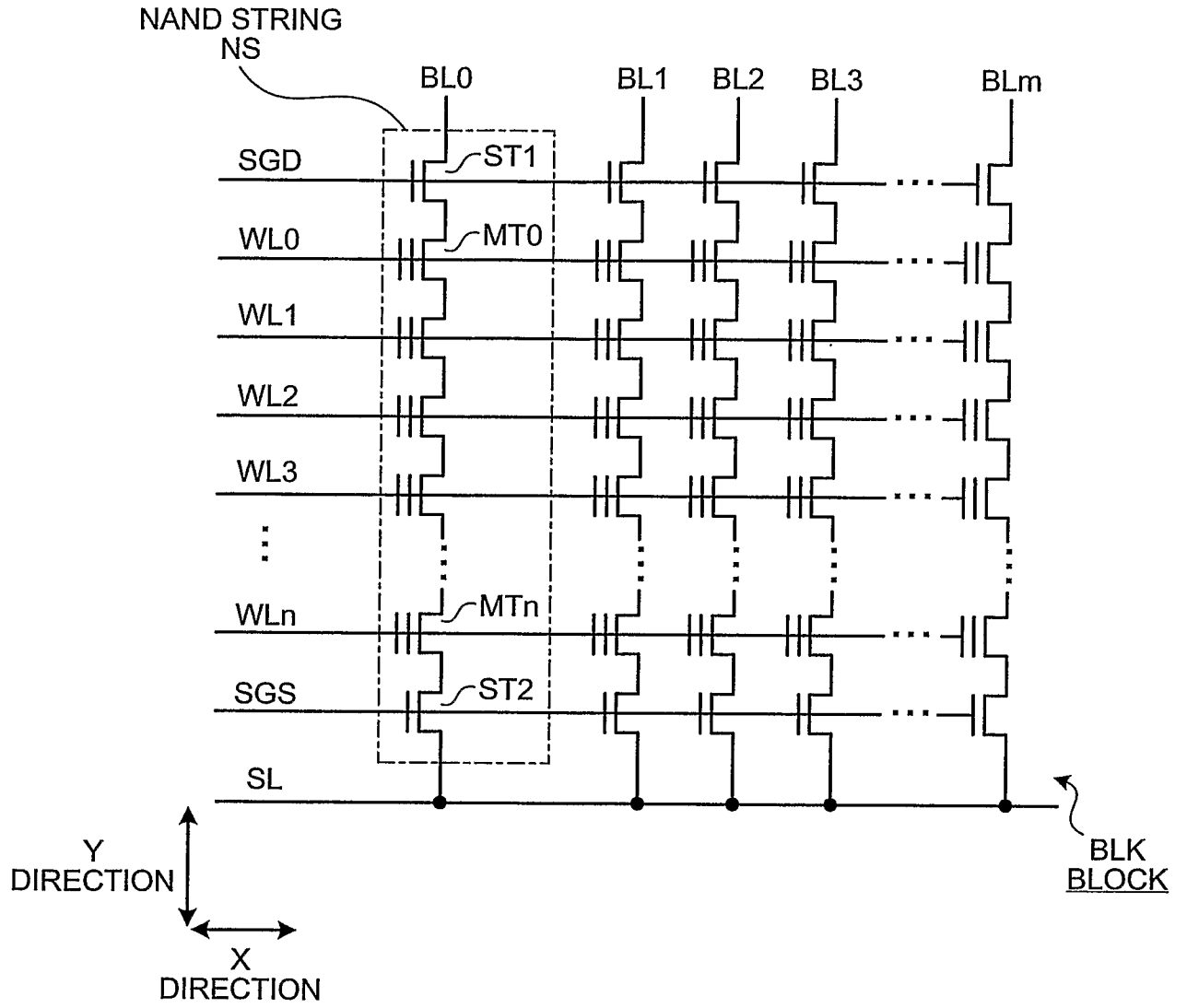


FIG.3

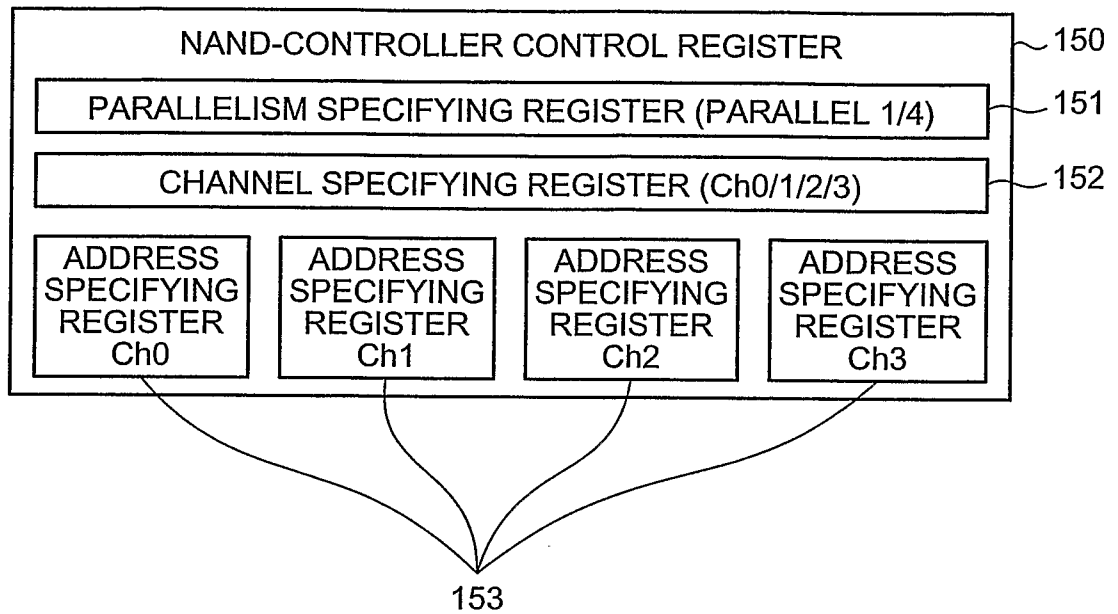


FIG.4

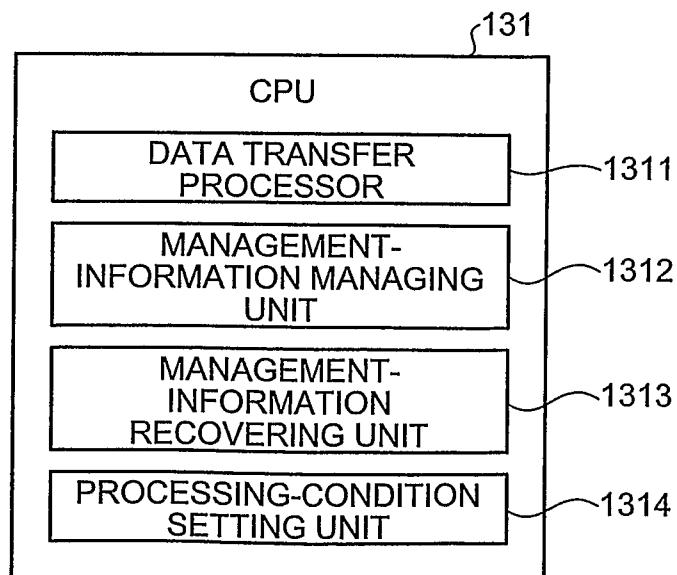


FIG.5

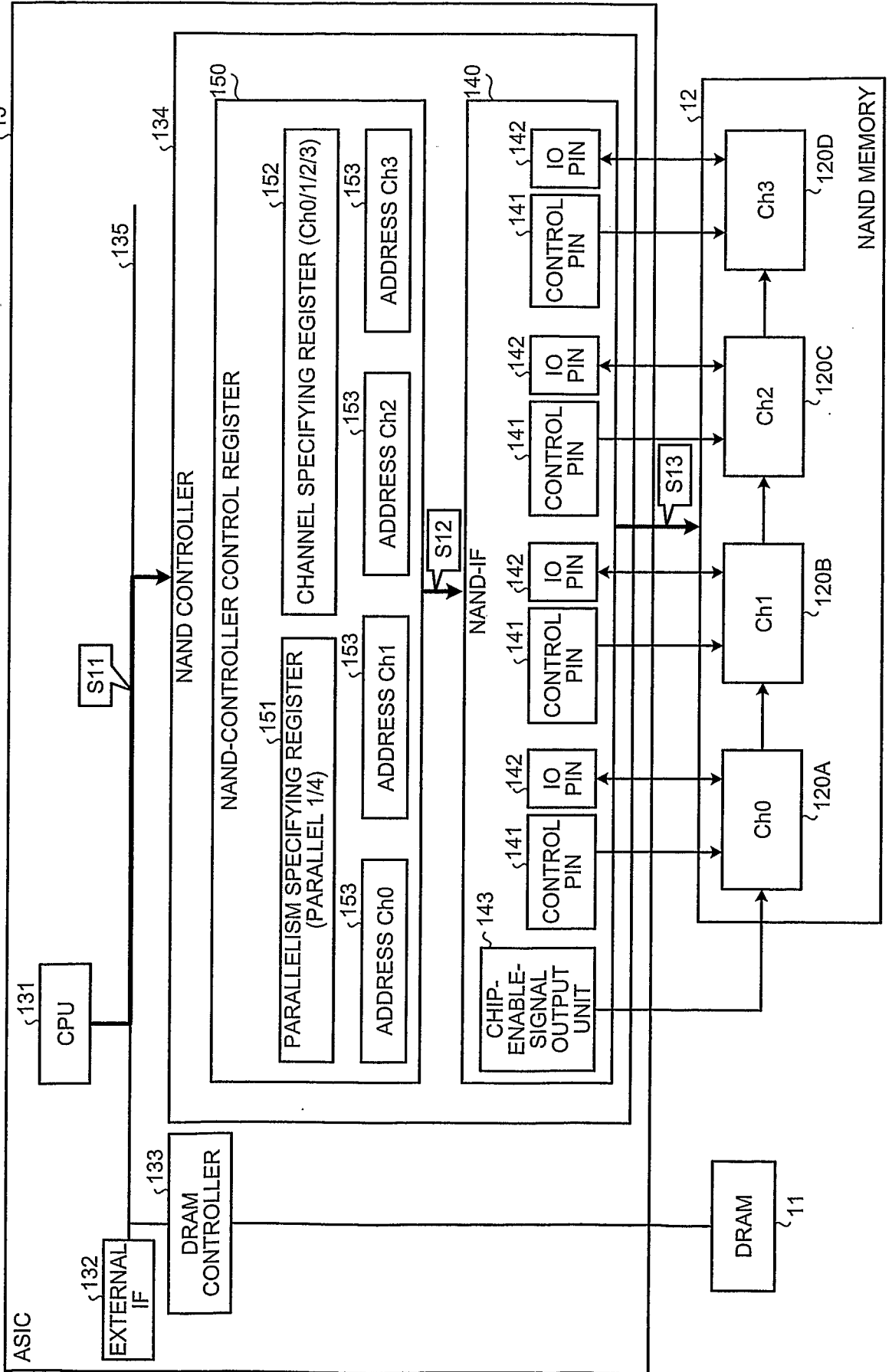


FIG.6

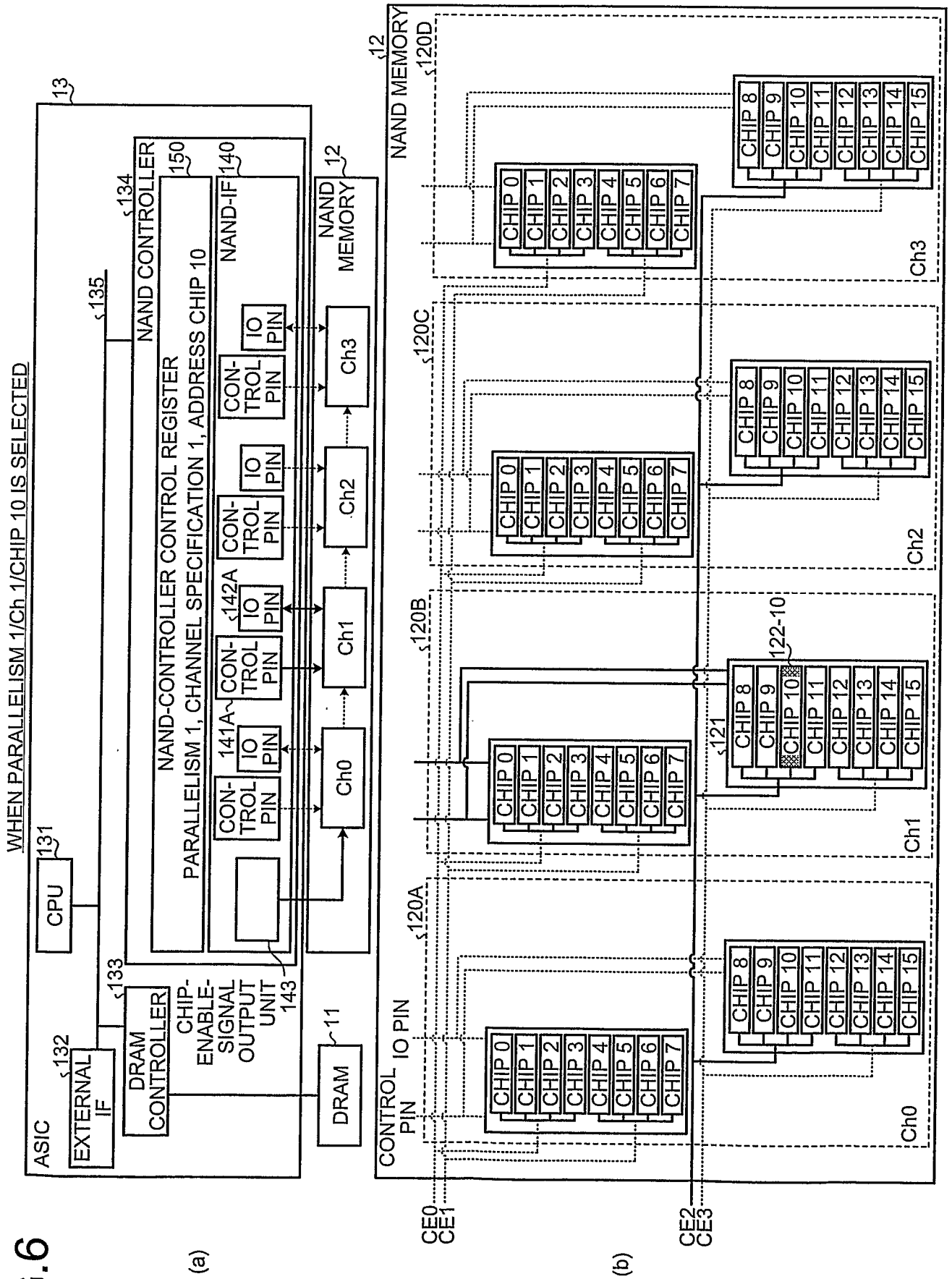




FIG.8

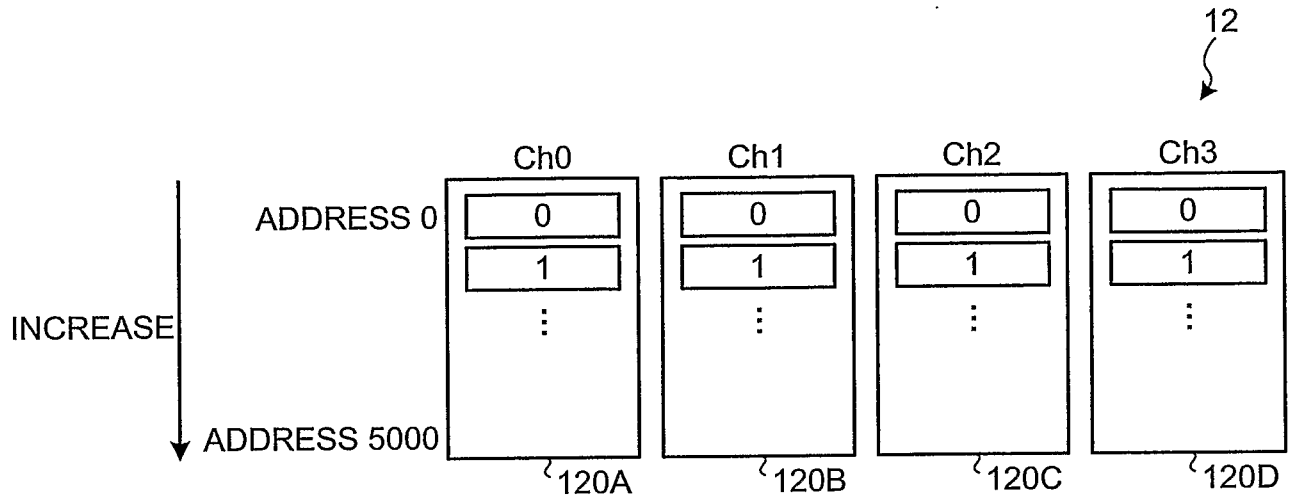


FIG.9

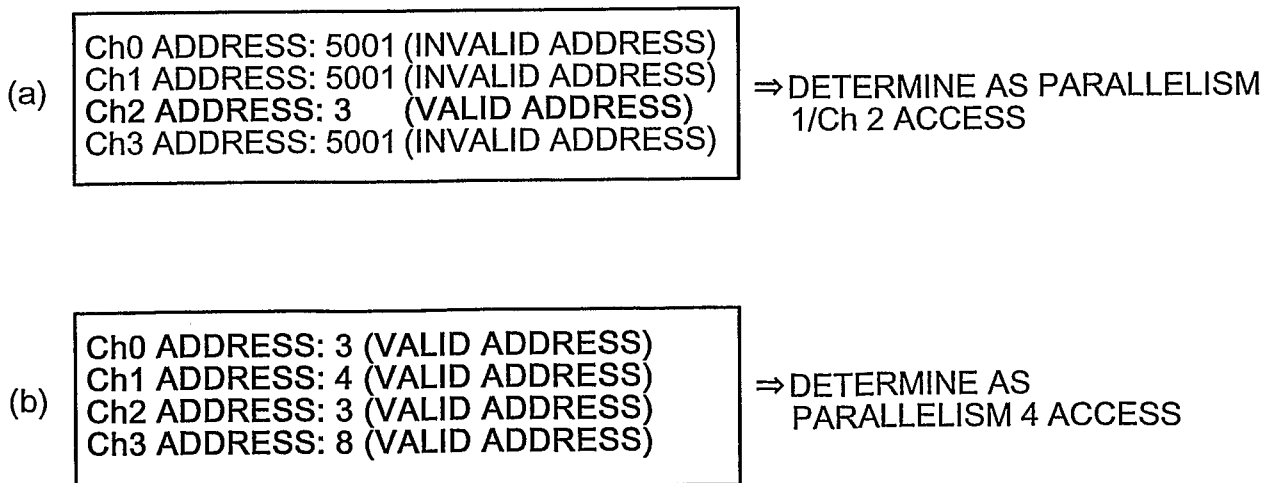


FIG.10

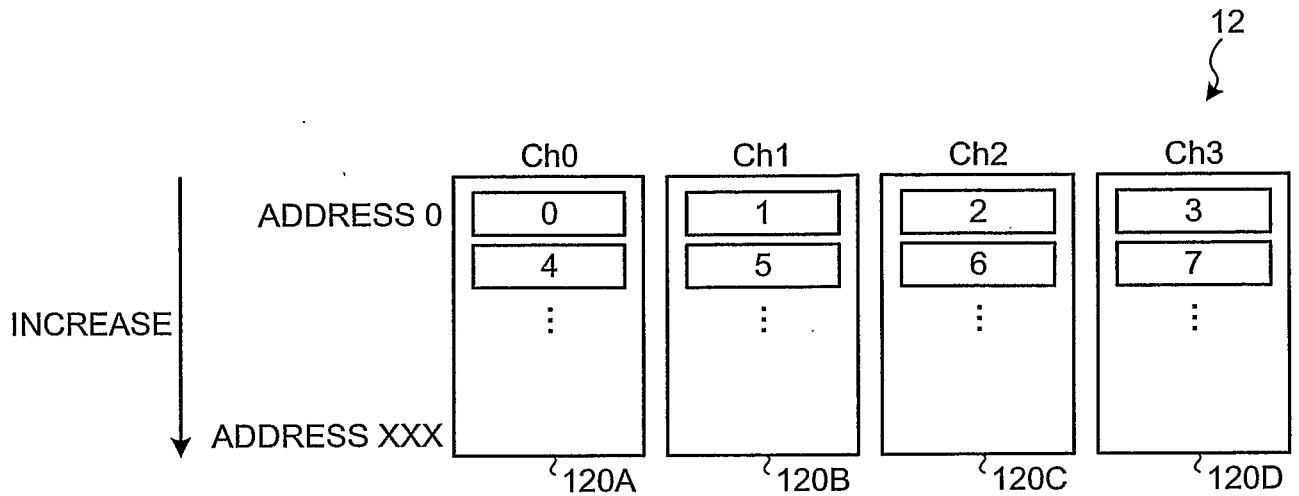


FIG.11

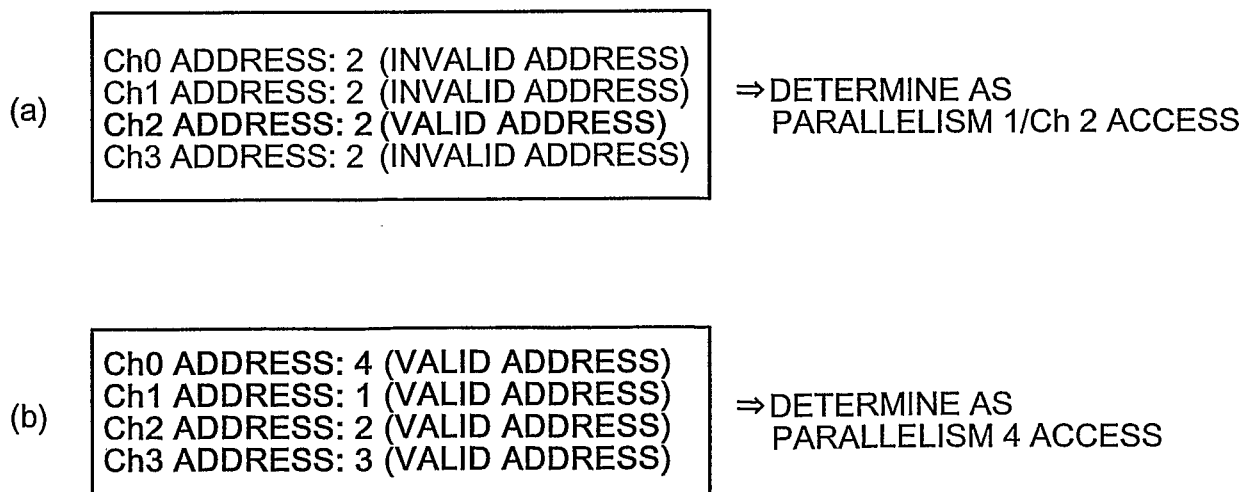


FIG.12

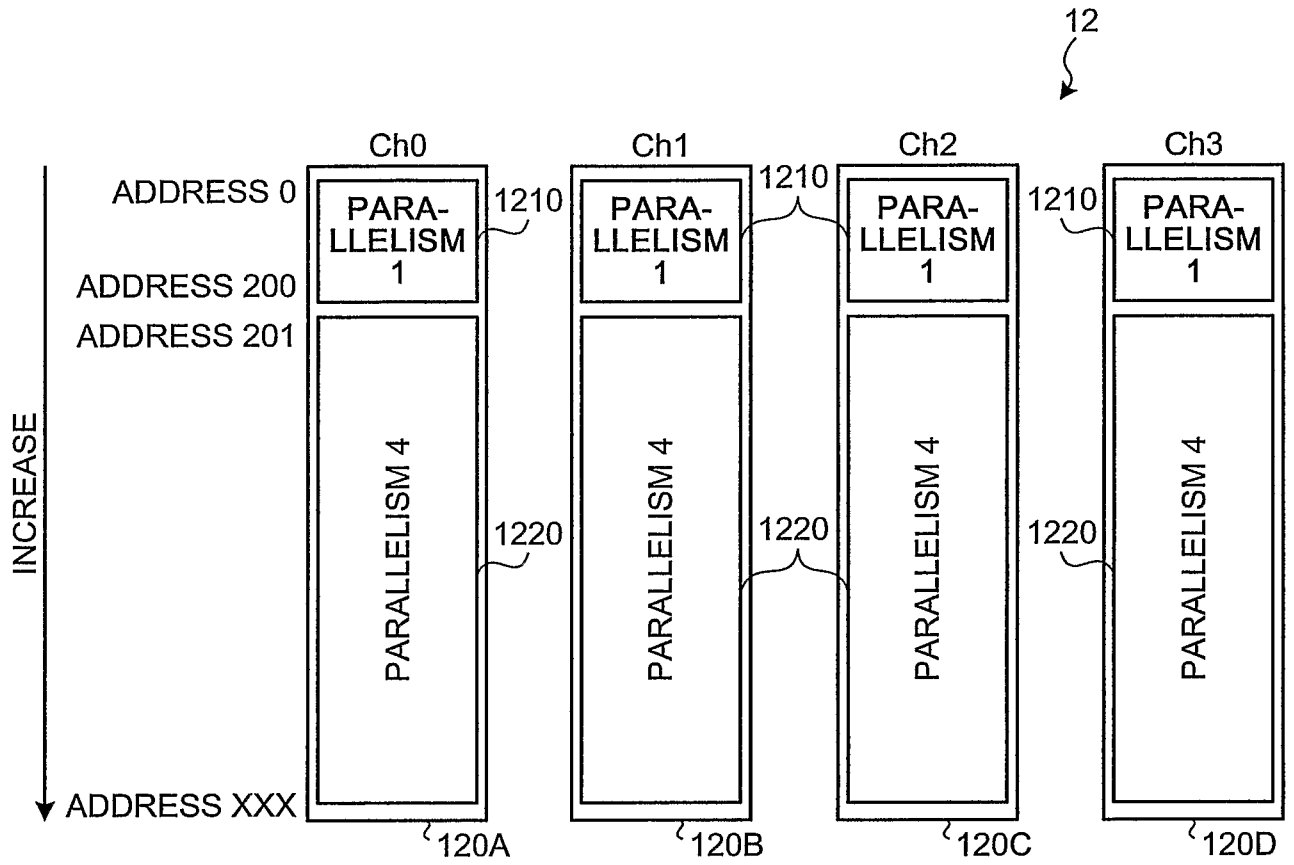


FIG.13

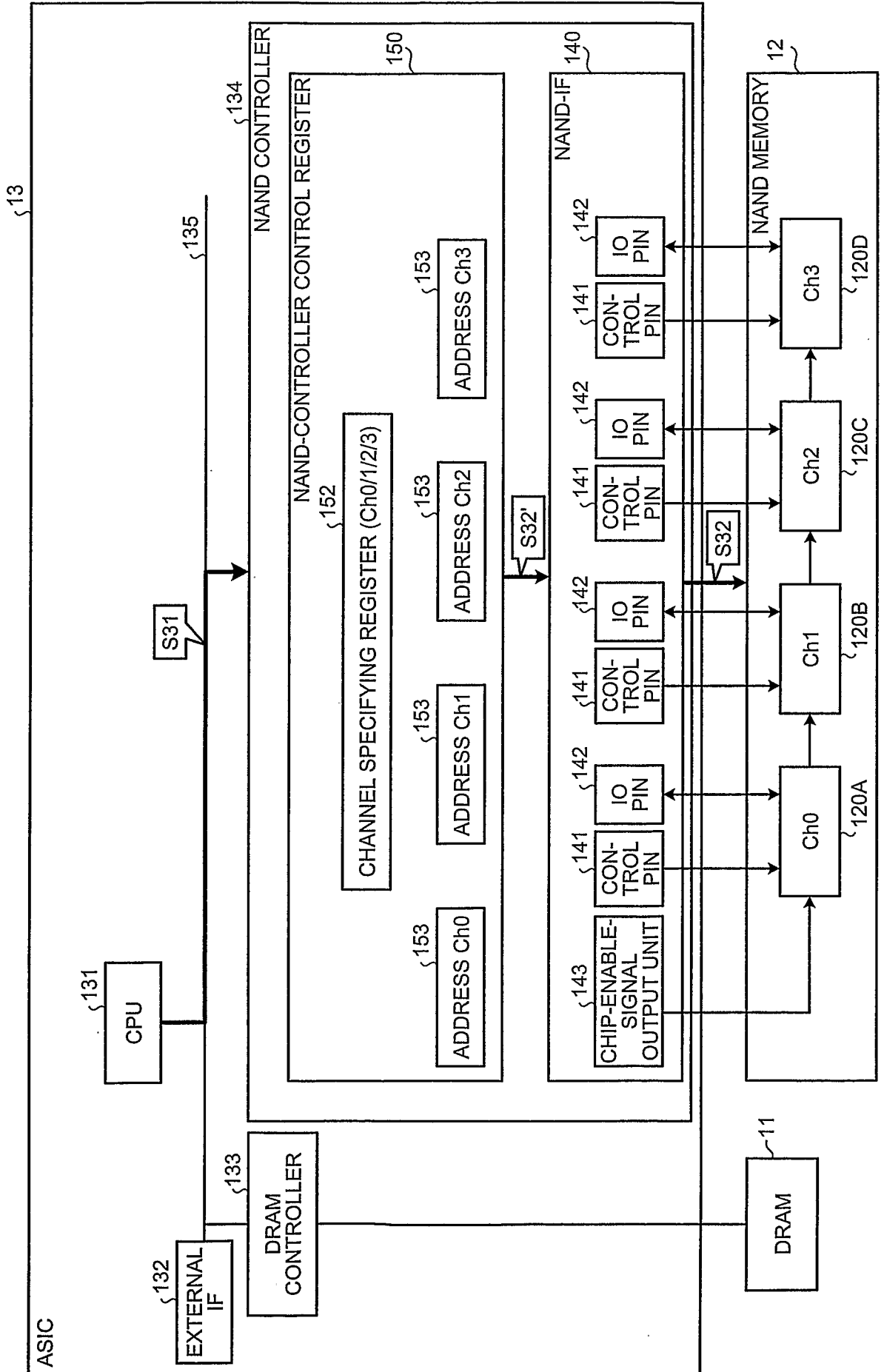


FIG.14

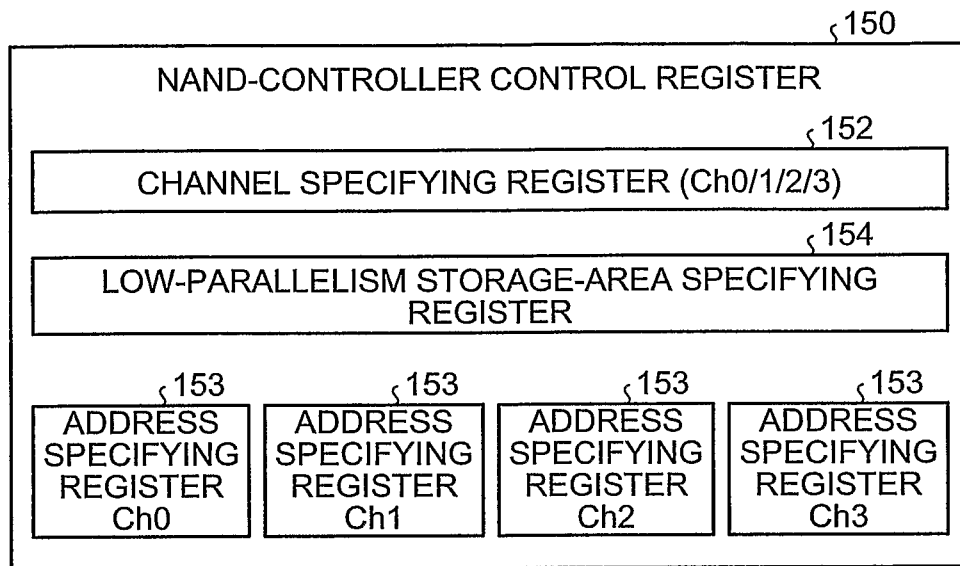
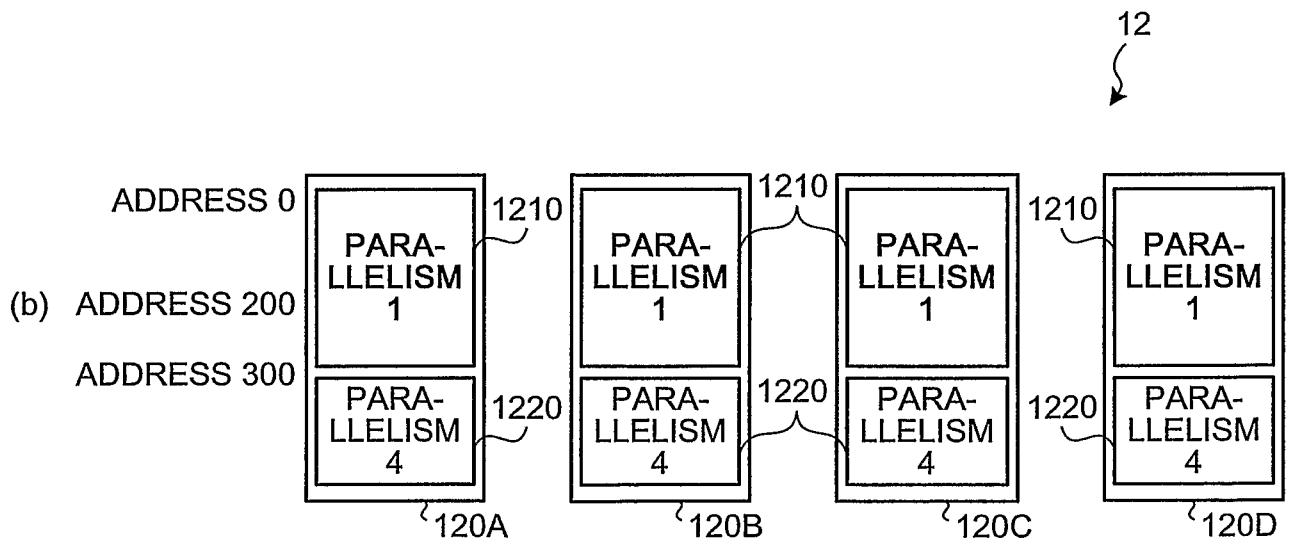
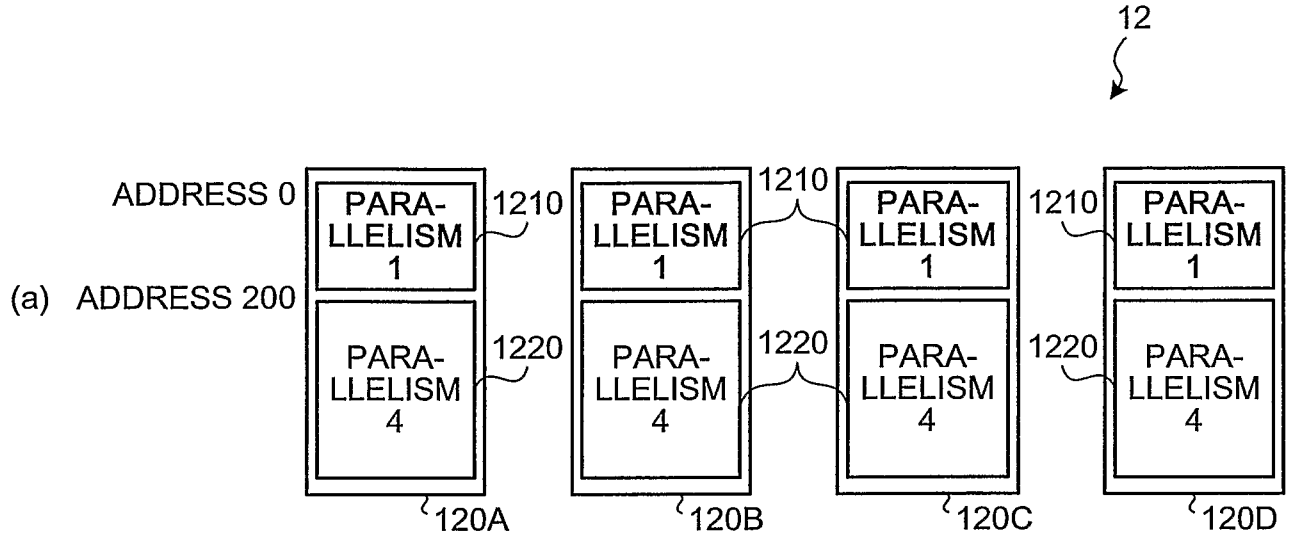


FIG.15



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2009/051139

A. CLASSIFICATION OF SUBJECT MATTER		
Int.Cl. G06F12/06(2006.01) i, G06F12/00(2006.01) i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
Int.Cl. G06F12/06, G06F12/00, G06F3/06, G06F3/08		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Published examined utility model applications of Japan 1922-1996 Published unexamined utility model applications of Japan 1971-2009 Registered utility model specifications of Japan 1996-2009 Published registered utility model applications of Japan 1994-2009		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	WO 2005/066770 A2 (SANDISK CORPORATION) 2005.07.21, the whole document, especially claim 15, paragraphs [0015], [0100], and [0101], figure 1A & JP 2007-517325 A & US 2005/0144357 A1 & US 2005/0144363 A1 & US 2005/0144367 A1 & EP 1700204 A & KR 10-2007-0012630 A & CN 1922571 A & TW 280581 B	1-5, 7 6, 8-18
Y A	JP 10-187359 A (KABUSHIKI KAISHA TOSHIBA) 1998.07.14, claim 3, paragraphs [0015] to [0016], figures 1 and 2 (No Family)	1-5, 7 6, 8-18
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
21.04.2009		12.05.2009
Name and mailing address of the ISA/JP		Authorized officer
<b>Japan Patent Office</b>		5N 9367
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## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/JP2009/051139

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 2006/0184758 A1 (Satori et al.) 2006.08.17, paragraphs [0046] to [0051], figure 5 & JP 2006-195569 A & KR 10-2006-0082040 A & CN 1825271 A	2 6,13,17
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A	US 2007/0168625 A1 (Cornwell et al.) 2007.07.19, the whole document, especially claims 13 and 14, paragraphs [0034] & JP 2007-193810 A & EP 1818830 A2 & CN 101004724 A	1-18
A	US 7024514 B2 (TDK CORPORATION) 2006.04.04, column 36, line 27 to column 38, line 2 & JP 2003-6044 A & US 2006/0064539 A1 & US 2002/0194451 A1	11,12