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(54) PLASMA DISPLAY DRIVE CIRCUIT

(71) We, CONTROL DATA CORPORATION, a Corporation organised and existing under the Laws of the State of Delaware, United States of America, 8100-34th Avenue South, Minneapolis, Minnesota 55440, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:-

This invention relates to plasma display drive circuits for plasma discharge display panels of the alternating current type capacitively coupled to an ionizable gaeous medium.

According to one aspect of the present invention, there is provided a plasma display device circuit for driving a plasma discharge display panel having a plurality of drive electrodes comprising a first group and a second group of drive electrodes in generally orthogonal relationship to said first group in a matrix arrangement and in which orthogonal pairs of said drive electrodes uniquely specify all display elements in the panel, the circuit including: first drive means for selectively providing voltages in matrix interconnection to said first group of drive electrodes, second drive means for selectively providing voltages in matrix interconnection to said second group of drive electrodes; a first voltage modulator means connected with said first drive means for selectively switching a supply voltage to said first drive means between an erase voltage potential and a write voltage potential; a second voltage modulator means connected with said second drive means for selectively switching a supply voltage to said second drive means between an erase voltage potential and a write voltage potential; a first sustain drive means for selectively switching between a sustain drive potential and a ground potential, said sustain drive means being connected with said first drive means; a second sustain drive means for selectively switching between a sustain drive potential and a ground potential, said sustain drive means being connected with said second drive means; aplurality of a first clamp bus selection means connected to said first sustain drive means and connectable in matrix arrangement to said first group of drive electrodes, each of said first clamp bus selection means being, in operation, automatically actuated to switch on by the application of the sustain drive voltage potential from the first sustain drive means and to be actuated selectively by a control signal to allow associated drive electrodes of said first group of drive electrodes to float or to take up a required potential as said first drive means applies a voltage to selected drive electrodes of said first group of drive electrodes; and a plurality of a second clamp bus selection means to said second sustain drive means and connectable in matrix arrangement to said second group of drive electrodes, each of said clamp bus selection means being, in operation, automatically actuated to switch on by the application of the sustain drive voltage potential from the second sustain drive means and to be actuated selectively by a control signal to allow associated drive electrodes of said second group of drive electrodes to float or to take up a required potential as said second drive means applies a voltage to selected electrodes of said second group of drive electrodes.

According to a further aspect of the present invention, there is provided a plasma discharge drive circuit for a plasma discharge display panel having a plurality of drive electrodes comprising a first group and a second group of drive electrodes in generally orthogonal relationship to said first group in matrix arrangement, orthogonal pairs of said drive electrodes uniquely specifying all display elements in the panel, the circuit being

of the matrix selection type and having at least two sustain drive means for each group of drive electrodes; at least two clamp bus selection means associated with each group of drive electrodes, each clamp bus selection means being connected to at least two diodes, each diode being connectable to a single drive electrode, each clamp bus selection means including a first transistor acting as a switch between a clamp bus and a respective said sustain drive means, a bias network associated with said transistor which is such that said transistor is automatically biased to an on condition by said network when a sustain voltage potential is applied to said transistor in its forward direction, and control circuit means connected with said bias network to bias said transistor to an off condition to allow a clamp bus potential to float during application of a write or erase pulse.

One present feature of conventional plasma display drive circuits is their requirement for floating power supplies for certain drive functions of a plasma discharge display panel for the use of transformers on individual drive lines in order to achieve switching operations or superimposed voltages. The present invention may be "ground-referenced" in that switching opertations occur at low voltages with respect to a ground reference level. This eliminates the need for floating power supplies or transformers in the drive circuits.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 shows an overall system schematic diagram of a plasma display drive circuit according to the present invention;

Figure 2 is a detailed circuit diagram of a Y-axis clamp circuit of the drive circuit of Figure 1;

Figure 3 is a detailed circuit diagram of a X-axis clamp circuit of the drive circuit of Figure 1; and

Figure 4 is a diagram showing drive pulses as applied to a plasma discharge display panel using the drive circuit of Figure 1.

Referring now to Figure 1, a plasma discharge display panel 10 may be of the conventional alternating current driven type having orthogonal arrays of drive electrodes arranged with respect to an ionizable gaseous medium and capacitively coupled thereto to define display cells or display elements at the intersections of the drive electrodes. Such panels may be of the type having one array of drive electrodes on one side of the gaseous medium and the other other array of electrodes on the other side of the gaseous medium or of the type in which all drive electrodes are imbedded within a single surface with the gaseous medium disposed against the surface. Of course, other subspecies of such panels or other types of panels having orthogonal drive elements may exist or may be invented which may use the present invention. The display panel illustrated has a four-element by four-element array but conventional design of matrix selection circuits will allow expansion to any desired size using the scheme shown herein. For purposes of illustration, a selected display element 12 is identified within the panel.

A group of X-axis drive electrodes 14, 16, 18, 20 are all connected to an X-axis selection matrix 24 which may be of conventional design. Within the X-axis selection matrix 24 is a group of sustain drive diodes 26, all connected from an X-axis sustain bus 28 to respective drive electrodes 14, 16, 18, 20. Also connected to the drive electrodes 14, 16, 18, 20 are isolation resistors 30 which are connected to X-axis drivers 32, 34. The X-axis drivers 32, 34 may be of conventional design but are connected to an X-axis voltage modulator bus 36. Also connected to the drive electrodes 14, 16, 18, 20 are clamp diodes 38, 40 connected to an X-axis clamp 42 and diodes 44, 46 connected to an X-axis clamp 48. The diodes 38, 40 are connected to an X-axis clamp bus 41. The other terminals of the X-axis clampsare connected to the X-axis sustain driver bus 28. The X-axis drivers 32, 34 are shown as on/off switches, which is schematically accurate of their function. The X-axis clamps 42, 48 are shown as on/off switches which is also schematically accurate of their function, although the circuitry to accomplish this function will be described in detail hereinafter.

An X-axis sustain driver is composed of switches 50, 52 which operate in a conventional manner to provide the sustain drive bus 28 with either a connection to ground or to a source of sustain voltage. An X-axis voltage modulator 54 is connected to a source of voltage and is composed of conventional circuitry which may switch between the source voltage supplied or a lower voltage from a voltage divider as shown schematically.

A Y-axis selection matrix 60 is of conventional design and is similar in design to the X-axis selection matrix 24, but is designed to function with a negative source voltage from a Y-axis voltage modulator 62, whereas, the X-axis selection matrix 24 is designed to function with a positive source voltage from the X-axis voltage modulator 54. The Y-axis selection matrix 60 is connected with drive electrodes 64, 66, 68, 70. The intersection of the drive electrode 66 and the drive electrode 18 defines the display element 12.

Within the Y-axis selection matrix are a plurality of diodes 72 connected from a Y-axis sustain drive bus 74 to the respective drive electrodes 64, 66, 68, 70. Further, there are isolation resistors 76 connected

between the drive electrodes 64, 66 and a Y-axis driver 78 and between drive electrodes 68,70 to a Y-axis driver 80. The Y-axis drivers 78, 80 are connected to the Y-axis voltage modulator 62 to provide a direct source of the negative reference voltage or a slightly reduced negative voltage. A Y-axis sustain driver is composed of switches 82, 84 which provide a source of sustain voltage or a connection to ground for the Y-axis sustain drive bus 74.

The voltage modulators 54, 62, are similar in function in that they provide the source of write voltage or erase voltage required for driving the display panel 10. The full voltage that has not been reduced on each axis is the write voltage which is approximately 110 volts positive supplied to X-axis voltage modulator 54 and approximately -110 volts supplied to Y-axis voltage modulator 62. The reduced voltage in each case represents the erase voltage which according to the present example may be +55 volts for the X-axis and −55 volts for the Y-axis. Symbolically, these are indicated in Figure 1 as $+Vw$, $+Ve$, $-Vw$ and $-Ve$. Similarly, the sustain voltage is indicated schematically in Figure 1 as Vs, and in the present embodiment, may be approximately 110 volts.

Referring now to Figure 2, one Y-axis clamp of the drive circuit of Figure 1 is shown. Thus, the Y-axis clamp shown may be taken to either a Y-axis clamp 86 or a Y-axis clamp 88 shown in Figure 1. The Y-axis clamp has two output terminals one of which is connected to the Y-axis sustain driver bus 74 and the other of which is connected to either a pair of diodes 90, 92 on a Y-axis clamp bus 93 or a pair of diodes 94, 96 on a Y-axis clamp bus 93'. For purposes of convenience of explanation, Figure 2 illustrates the Y-axis clamp 86.

The Y-axis clamp 86 comprises a first transistor 100 with its emitter connected to the Y-axis sustain bus 74 and its collected connected to the Y-axis clamp bus 93. Connected to the base of the transistor 100 is the emitter of a transistor 102 which is also connected through a resistor 104 to the emitter of the transistor 100. The collectors of the transistors 100, 102 are connected together. The transistor 102 serves to form a bias network and amplifier for the transistor 100. A bypass diode 106 is connected between the base and the emitter of transistor 102 to allow the bias circuit to turn off the transistor 100 when it is desired to do so. A resistor 108 provides a negative source of bias voltage to the emitter of the transistor 102. A diode 110 provides a switching signal to the emitter of the transistor 102. The diode 110 is connected to the collector of a transistor 112 which has its emitter connected to a positive voltage source. The transistor 112 receives its input first from a logic decoder output control 114 which is amplified and inverted by a conventional amplifier 116. Resistors 118, 120 form a bias network for the transistor 112. The transistor 112 is normally off during sustain voltage cycling and is turned on by the control 114 in order to maintain the output of the Y-axis clamp in the off condition during selection when the Y-axis sustain bus 74 is at a near zero or ground potential. The Y-axis clamp is in a normally on condition when the output of the Y-axis sustain driver is rising. The transistors 100, 102, controlled by the appropriate bias network as described, thus, are in a normally on conducting condition when the voltage on the Y-axis sustain bus 74 is higher than the voltage on the Y-axis clamp bus 93.

Referring now to Figure 3, an X-axis clamp is shown which has a similar function to that of the Y-axis clamp previously described. However, since the X-axis clamp is to be normally on when the sustain output voltage is falling, the circuit must be of slightly different design in order to be normally on at the desired time. The X-axis clamp shown in Figure 3 may be either the X-axis clamp 42 or the X-axis clamp 48 as shown in Figure 1, but for convenience, is shown as the X-axis clamp 42 connected between the X-axis sustain bus 28 and the X-axis clamp bus 41. The X-axis clamp 42 has a transistor 140 having its emitter connected to the X-axis sustain drive bus 28 and its collector connected to the X-axis clamp bus 41. A bias network for this transistor is formed by a transistor 142 having its emitter connected to the emitter of transistor 140. A blocking diode 144 is placed in the emitter connection of the transistor 140 for voltage breakdown protection when the sustain voltage is rising. The collector of the transistor 142 is connected with the collector of the transistor 140. The emitter of the transistor 142 is connected through a resistor 146 to a source of positive bias voltage and through a diode 148 to the emitter of the transistor 142. A string of diodes 150 provides the proper bias voltage at the base of the transistor 142 when an amplifier 152 has a low output state. This bias voltage will keep the transistors 142, 140 off allowing the selected electrodes to receive the positive write or erase pulse. The amplified 152 is connected to a logic decoder output 154 shown schematically. A diode 156 clamps the output of the amplified 152 to a source of positive reference voltage. When the output of the amplifier 152 is low, and the sustain voltage is low, the X-axis clamp is forced to the off or unclamped condtion. When the output from the amplifier 152 is high, the X-axis clamp turns on and inhibits the write or erase pulse from the X-axis sustain driver. The X-axis clamp turns on automatically during the time a sustain pulse is applied. It turns on

when the sustain voltage is falling and the emitter of the transistor 140 is pulled more negative than its base.

Referring now to Figure 4, a series of pulse trains are shown relating to the operation of the drive circuit described above when operatiing the display panel 10. The top pulse train shows the voltage as applied to the X-axis electrodes, the second wave train shows the voltage applied to the Y-axis electrodes, and the bottom wave train shows the voltages as applied to a given display element in the display panel, such as the display element 12. The first or left most section shows the conventional sustain pulse train as applied to the panel. The second or middle section shows the conventional write pulse train applied immediately after a sustain pulse on the X-axis electrode and before the corresponding sustain pulse on the Y-axis electrode and the summed signal created at the display element. Similarly, the last segment of the wave train display shows the smaller positive half-select erase pulse train applied just before a conventional sustain pulse on the X-axis electrodes simultaneously with the application of the negative half-select erase pulse on the Y-axis electrodes and the resultant full amplitude erase pulse occurring just prior to a similar polarity sustain pulse at the display element.

During sustaining, the X-axis drivers 32, 34 and the Y-axis drivers 78, 80 are open and the X-axis clamps 42, 48 and the Y-axis clamps 86 and 88 are closed. Sustain pulses are coupled to the panel through the closed clamps or through diodes. During writing or erasing, the outputs of the sustain drivers are grounded or are at a near zero voltage by closing switches 52 and 84.

The example in Figure 1 shows the switch positions for selection of the display element 12. The X-axis driver 34 and the Y-axis driver 78 are closed, and the switches 42 and 86 are open. This condition allows one-half of the selection voltage V_w or V_e to be applied to the drive electrode 18 and the other half $-V_w$ or $-V_e$ to be applied to the drive electrode 66. The result is a full selection voltage $2V_w$ or $2V_e$ applied to the display element 12 for either the write function or the erase function. All of the other elements on the display panel have either a half selection voltage or zero voltage. The control 154 controls the various functions as described by providing control signals for the X-axis driver 32,34 and Y-axis drivers 78,80 and the clamps 42, 48, 86, 88. The sustain drivers are driven in conventional fashion. The voltage modulators 54,62 are switched between high and low voltage depending upon whether writing or erasing is being performed. The control 154 receives its input in any conventional fashion, as for example, digital signals from a computer system, for controlling the display.

WHAT WE CLAIM IS:

1. A plasma display drive circuit for driving a plasma discharge display panel having a plurality of drive electrodes comprising a first group and a second group of drive electrodes in generally orthogonal relationship to said first group in a matrix arrangement and in which orthogonal pairs of said drive electrodes uniquely specify all display elements in the panel, the circuit including: first drive means for selectively providing voltages in matrix interconnection to said first group of drive electrodes, second drive means for selectively providing voltages in matrix interconnection to said second group of drive electrodes; a first voltage modulator means connected with said first drive means for selectively switching a supply voltage to said first drive means between an erase voltage potential and a write voltage potential; a second voltage modulator means connected with said second drive means for selectively switching a supply voltage to said second drive means between an erase voltage potential and a write voltage potential; a first sustain drive means for selectively switching between a sustain drive potential and a ground potential, said sustain drive means being connected with said first drive means; a second sustain drive means for selectively switching between a sustain drive potential and a ground potential, said sustain drive means being connected with said second drive means; a plurality of a first clamp bus selection means connected to said first sustain drive means and connectable in matrix arrangement to said first group of drive electrodes, each of said first clamp bus selection means being, in operation, automatically actuated to switch on by the application of the sustain drive voltage potential from the first sustain drive means and to be actuated selectively by a control signal to allow associated drive electrodes of said first group of drive electrodes to float or to take up a required potential as said first drive means applies a voltage to selected drive electrodes of said first group of drive electrodes; and a plurality of a second clamp bus selection means connected to said second sustain drive means and connectable in matrix arrangement to said second group of drive electrodes, each of said clamp bus selection means being, in operation, automatically actuated to switch on by the application of the sustain drive voltage potential from the second sustain drive means and to be actuated selectively by a control signal to allow associated drive electrodes of said second group of drive electrodes to float or to take up a required potential as said second drive means applies a voltage to selected electrodes of said second group of drive electrodes.

2. A circuit as claimed in claim 1 in which each of said first and second clamp bus selection means comprises: a first transistor having its emitter and collector connectable between a matrix arrangement of drive electrodes and a sustain drive means to act as an on/off switch, a second transistor having its emitter connected with the base of the first transistor and at least one other electrical connecting means between said transistors, said second transistor acting to bias said first transistor, and bias means for said second transistor.

3. A circuit as claimed in claim 2 including amplifying means for receiving and amplifying a control signal and means for connecting the output of said amplifying means with said first transistor to bias said first transistor to an off condition upon receipt of a control signal.

4. A plasma display drive circuit for a plasma discharge display panel having a plurality of drive electrodes comprising a first group and a second group of drive electrodes in generally orthogonal relationship to said first group in matrix arrangement, orthogonal pairs of said drive electrodes uniquely specifying all display elements in the panel, the circuit being of the matrix selection type and having at least two sustain drive means for each group of drive electrodes; at least two clamp bus selection means associated with each group of drive electrodes, each clamp bus selection means being connected to at least two diodes, each diode being connectable to a single drive electrode, each clamp bus selection means including a first transistor acting as a switch between a clamp bus and a respective said sustain drive means, a bias network associated with said transistor which is such that said transistor is automatically biased to an on condition by said network when a sustain voltage potential is applied to said transistor in its forward direction, and control circuit means connected with said bias network to bias said transistor to an off condition to allow a clamp bus potential to float during application of a write or erase pulse.

5. A plasma display device circuit substantially as herein described with reference to and as shown in the accompanying drawings.

6. A plasma discharge display panel having a circuit as claimed in any preceding claim.

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1573594 COMPLETE SPECIFICATION
3 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 1

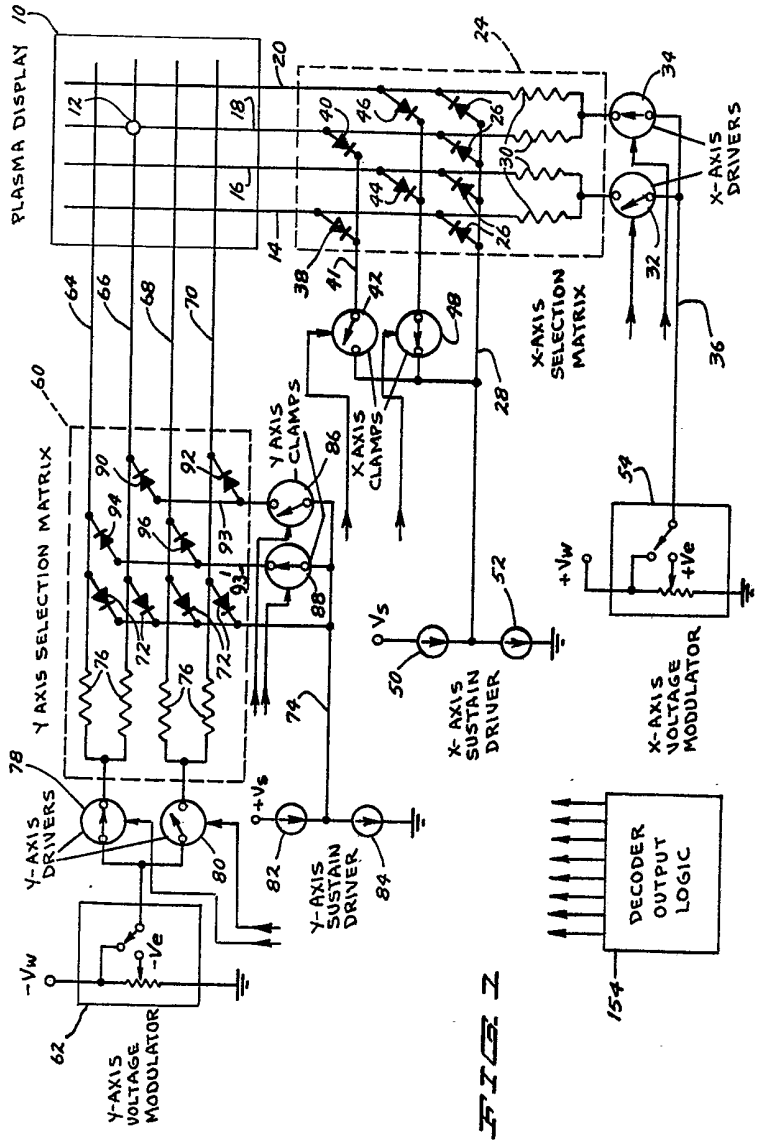

FIG 2

1573594 COMPLETE SPECIFICATION
3 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 2

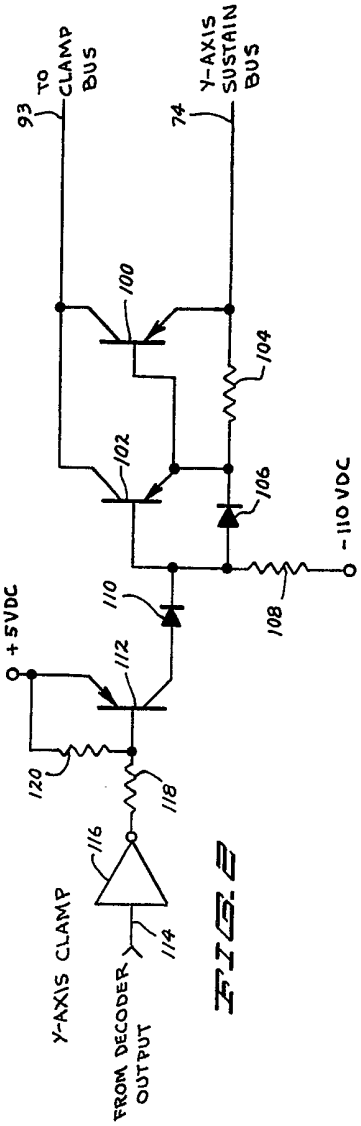

FIG. 2

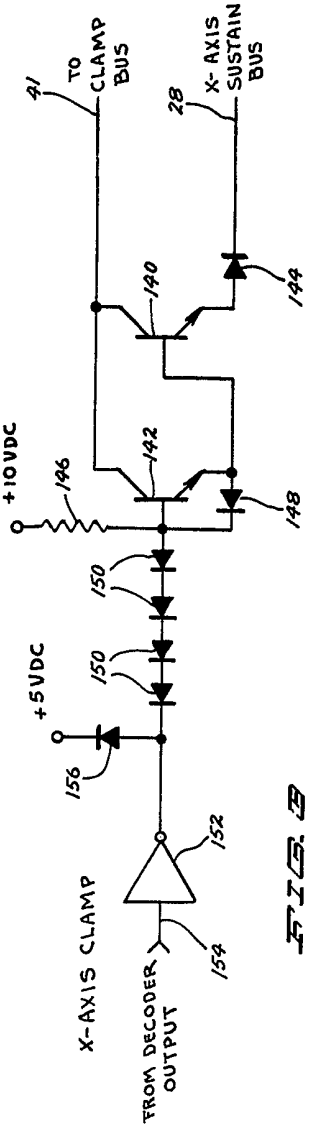

FIG. 3

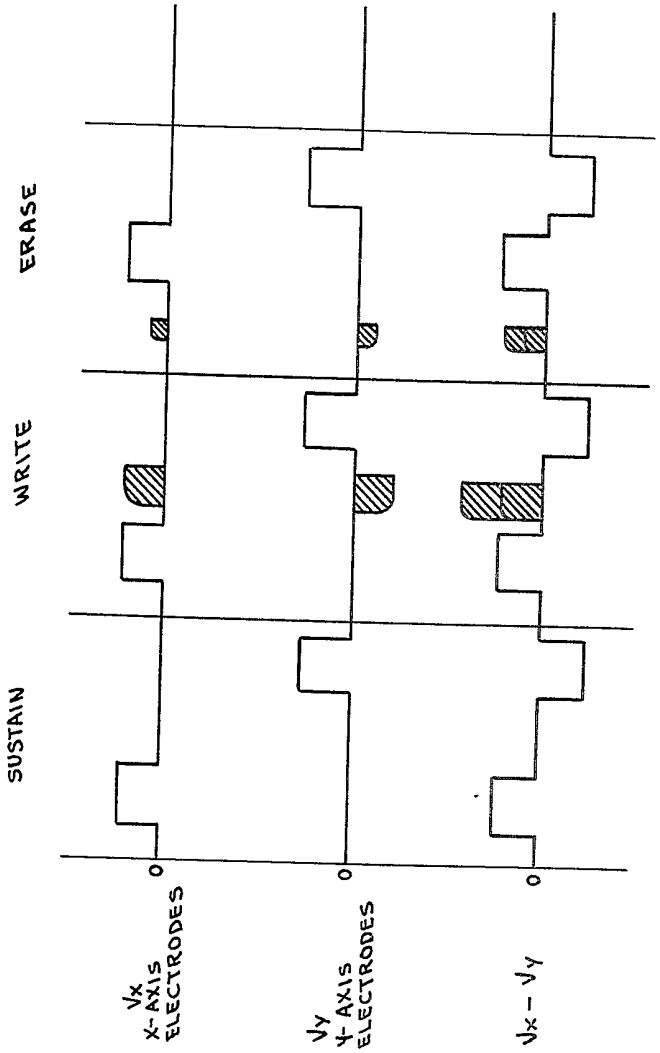
ERASE
WRITE
SUSTAIN
0
0
0
Vx
X-AXIS
ELECTRODES
Vy
Y-AXIS
ELECTRODES
Vx - Vy

FIG. 4