



(51) International Patent Classification:

H01L 21/3065 (2006.01) H01L 21/67 (2006.01)

H01L 21/311 (2006.01) H01J 37/32 (2006.01)

H01L 21/3213 (2006.01) H05H 1/46 (2006.01)

H01L 21/324 (2006.01)

(21) International Application Number:

PCT/US2019/042560

(22) International Filing Date:

19 July 2019 (19.07.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

16/107,752 21 August 2018 (21.08.2018) US

(71) Applicant: LAM RESEARCH CORPORATION

[US/US]; 4650 Cushing Parkway, M/S CA-1, Fremont, California 94538 (US).

(72) Inventors: HUDSON, Eric; 1820 Catalina Avenue, Berkeley, California 94707 (US). PELHOS, Kalman; 1505 Calaveras Avenue, San Jose, California 95126 (US).

(74) Agent: LEE, Michael; BEYER LAW GROUP LLP, P.O. Box 51887, Palo Alto, California 94303-1887 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD FOR ETCHING AN ETCH LAYER

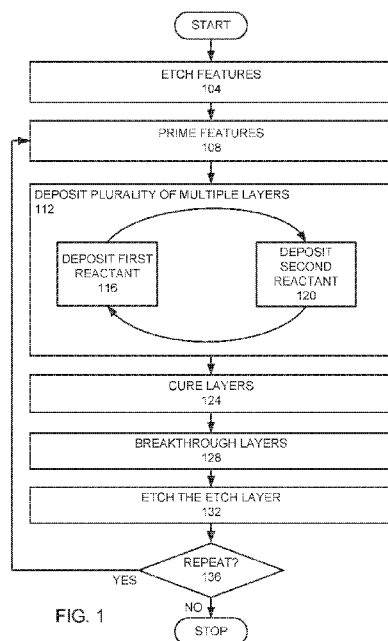


FIG. 1

(57) Abstract: A method of forming a feature in a stack comprising a dielectric material on a substrate is provided. An etch plasma is generated from an etch gas, exposing the stack to the etch plasma and partially etching the feature in the stack. The stack is primed. A protective film is deposited on sidewalls of the feature by repeating for a plurality of cycles the steps of exposing the stack to a first reactant, allowing the first reactant to adsorb onto the stack, and exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack. The etching, priming, and depositing a protective film are repeated until the feature is etched to a final depth.

METHOD FOR ETCHING AN ETCH LAYER

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority of U.S. Application No. 16/107,752, filed August 21, 2018, which is incorporated herein by reference for all
5 purposes.

BACKGROUND

Field

[0002] The disclosure relates to methods of forming semiconductor devices on a semiconductor wafer. More specifically, the disclosure relates to etching recessed
10 features in an etch layer in a stack.

[0003] In forming semiconductor devices, etch layers may be etched to form memory holes or lines. Some semiconductor devices may be formed by etching a stack of bilayers of silicon oxide and silicon nitride (ONON). Such stacks may be used in memory applications, such as in forming dynamic random access memory
15 (DRAM) and three dimensional “negative and” gates (3D NAND). In the formation of such memory structures, plasma processing chambers may be used to etch such memory structures.

SUMMARY

[0004] To achieve the foregoing and in accordance with the purpose of the present
20 disclosure, a method of forming a feature in a stack comprising a dielectric material on a substrate is provided. An etch plasma is generated from an etch gas, exposing the stack to the etch plasma to partially etch the feature in the stack. The stack is primed. A protective film is deposited on sidewalls of the feature by repeating for a plurality of cycles the steps of exposing the stack to a first reactant, allowing the first reactant
25 to adsorb onto the stack, and exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack. The etching, priming, and depositing a protective film are repeated until the feature is etched to a final depth.

[0005] In another manifestation, a method of forming a feature in a stack
30 comprising a dielectric material on a substrate is provided. An etch plasma is generated from an etch gas, exposing the stack to the etch plasma and partially etching the feature in the stack. A protective film is deposited on sidewalls of the

feature by repeating for a plurality of cycles the steps of exposing the stack to a first reactant, allowing the first reactant to adsorb onto the stack, and exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack. The protective film is cured. The steps are
5 repeated until the feature is etched to a final depth.

[0006] In another manifestation, a method of forming a feature in a stack comprising a dielectric material on a substrate is provided. An etch plasma is generated from an etch gas, exposing the stack to the etch plasma and partially etching the feature in the stack. A protective film is deposited on sidewalls of the
10 feature by performing a plurality of cycles, wherein each cycle comprises exposing the stack to a first reactant, allowing the first reactant to adsorb onto the stack, and exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack, wherein the protective film comprises at least one of a metal, sulfur, boron, silicon, nitrogen, or phosphorous.
15 The process is repeated until the feature is etched to a final depth.

[0007] In another manifestation, a method of forming a feature in a stack comprising a dielectric material on a substrate is provided. An etch plasma is generated from an etch gas, exposing the stack to the etch plasma and partially etching the feature in the stack. A protective film is deposited on sidewalls of the
20 feature by performing a plurality of cycles, wherein each cycle comprises exposing the stack to a first reactant, allowing the first reactant to adsorb onto the stack, and exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack. A breakthrough etch is provided, which etches protective film on etch fronts and/or at neck locations. The
25 process is repeated until the feature is etched to a final depth.

[0008] In another manifestation, a method of forming a feature in a stack comprising a dielectric material on a substrate is provided. An etch plasma is generated from an etch gas, exposing the stack to the etch plasma and partially etching the feature in the stack, while cooling the substrate with a coolant cooled in a
30 chiller to a temperature below -20° C. A protective film is deposited on sidewalls of the feature at a temperature of at least 20° C by performing a plurality of cycles, wherein each cycle comprises exposing the stack to a first reactant, allowing the first

reactant to adsorb onto the stack, and exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack. The process is repeated until the feature is etched to a final depth.

[0009] These and other features of the present disclosure will be described in
5 more details below in the detailed description and in conjunction with the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The present disclosure is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference
10 numerals refer to similar elements and in which:

[0011] FIG. 1 is a high level flow chart of an embodiment.

[0012] FIG.2 is a schematic view of a etch chamber that may be used in an embodiment.

[0013] FIG. 3 is a schematic view of a computer system that may be used in
15 practicing an embodiment.

[0014] FIGS. 4A-G are schematic illustrations of a stack processed according to an embodiment.

[0015] FIG. 5 is a more detailed flow chart of a process for depositing a first reactant.

20 [0016] FIG. 6 is a more detailed flow chart of a process for depositing a second reactant.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0017] The present disclosure will now be described in detail with reference to a few exemplary embodiments thereof as illustrated in the accompanying drawings. In
25 the following description, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be apparent, however, to one skilled in the art, that the present disclosure may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present
30 disclosure.

[0018] FIG. 1 is a high level flow chart of an embodiment. In this embodiment, features are partially etched into an etch layer (step 104). The partially etched

features are primed (step 108). A plurality of multiple layers is deposited (step 112), providing a protective film. The depositing of the multiple layers (step 112) comprises a cyclical process, where each cycle comprises depositing a first reactant (step 116) and depositing a second reactant (step 120). The deposited multiple layers are cured (step 124). A breakthrough etch is provided to etch the deposited multiple layers (step 128). The etch layer is partially etched (step 132). A determination is made on whether to continue the etch process (step 136). If the etch process is continued, steps 108 to 132 are repeated. When the etch is complete, the process is stopped.

10 **Example**

[0019] In an exemplary embodiment, FIG. 2 is a schematic view of an etch reactor that may be used in an embodiment. In one or more embodiments, a plasma processing chamber 200 comprises a gas distribution plate 206 providing a gas inlet and an electrostatic chuck (ESC) 208, within an etch chamber 249, enclosed by a chamber wall 252. Within the etch chamber 249, a stack 203 is positioned over the ESC 208. An edge ring 209 surrounds the ESC 208. An ESC temperature controller 250 is connected to a chiller 214. In this embodiment, the chiller 214 provides a coolant to channels 212 in or near the ESC 208. A radio frequency (RF) source 230 provides RF power to a lower electrode, which in this embodiment are the ESC 208.

20 In an exemplary embodiment, 400 kHz and 60 MHz power sources make up the RF source 230. In this embodiment, the upper electrode is grounded. In this embodiment, one generator is provided for each frequency. Other arrangements of RF sources and electrodes may be used in other embodiments. A controller 235 is controllably connected to the RF source 230, an exhaust pump 220, and the etch gas source 210.

25 An example of such an etch chamber is the Flex® etch system manufactured by Lam Research Corporation of Fremont, CA. The process chamber can be a CCP (capacitive coupled plasma) reactor or an ICP (inductive coupled plasma) reactor.

[0020] FIG. 3 is a high level block diagram showing a computer system 300, which is suitable for implementing a controller 235 used in embodiments. The computer system may have many physical forms ranging from an integrated circuit, a printed circuit board, and a small handheld device up to a huge super computer. The computer system 300 includes one or more processors 302, and further can include an

electronic display device 304 (for displaying graphics, text, and other data), a main memory 306 (e.g., random access memory (RAM)), storage device 308 (e.g., hard disk drive), removable storage device 310 (e.g., optical disk drive), user interface devices 312 (e.g., keyboards, touch screens, keypads, mice or other pointing devices, etc.), and a communication interface 314 (e.g., wireless network interface). The communication interface 314 allows software and data to be transferred between the computer system 300 and external devices via a link. The system may also include a communications infrastructure 316 (e.g., a communications bus, cross-over bar, or network) to which the aforementioned devices/modules are connected.

10 **[0021]** Information transferred via communications interface 314 may be in the form of signals such as electronic, electromagnetic, optical, or other signals capable of being received by communications interface 314, via a communication link that carries signals and may be implemented using wire or cable, fiber optics, a phone line, a cellular phone link, a radio frequency link, and/or other communication channels.

15 With such a communications interface, it is contemplated that the one or more processors 302 might receive information from a network, or might output information to the network in the course of performing the above-described method steps. Furthermore, method embodiments may execute solely upon the processors or may execute over a network such as the Internet, in conjunction with remote
20 processors that share a portion of the processing.

[0022] The term “non-transient computer readable medium” is used generally to refer to media such as main memory, secondary memory, removable storage, and storage devices, such as hard disks, flash memory, disk drive memory, CD-ROM and other forms of persistent memory and shall not be construed to cover transitory
25 subject matter, such as carrier waves or signals. Examples of computer code include machine code, such as produced by a compiler, and files containing higher level code that are executed by a computer using an interpreter. Computer readable media may also be computer code transmitted by a computer data signal embodied in a carrier wave and representing a sequence of instructions that are executable by a processor.

30 **[0023]** FIG. 4A is a cross sectional view of a stack 203 with a substrate 404 disposed below an etch layer 408, disposed below a mask 412. In this example, the mask 412 is a hardmask, such as a plasma enhanced chemical vapor deposition

(PECVD) carbon mask. In this example, the etch layer 408 is a dielectric layer, such as silicon oxide (SiO_2). One or more layers (not shown) may be disposed between the substrate 404 and the etch layer 408. One or more layers (not shown) may also be disposed between the etch layer 408 and the mask 412.

5 **[0024]** Features are partially etched into an etch layer 408 (step 104). In this embodiment, the stack 203 is cooled while remaining in the etch chamber 249. The chiller 214 cools a coolant to a temperature below -20°C . The coolant is used to cool the stack 203 and substrate. An example of a recipe for partially etching features into the etch layer 408 provides a pressure of 5-50mT. RF power is provided at a
10 frequency of 60 MHz at a power of 2 kW-8 kW and at a frequency of 400k at a power of 4kW-25 kW. The RF power is pulsed between these powers and lower power levels. An etch gas is provided, which comprises oxygen (O_2), fluorocarbon(s) and/or hydrofluorocarbon(s). The etch gas is formed into an etch plasma by the RF power. FIG. 4B is a cross sectional view of a stack 203 after features 416 have been
15 partially etched.

[0025] The features 416 are primed (step 108). An example in this embodiment provides the priming by exposing the features 416 to a low-power carbon dioxide (CO_2) plasma condition which modifies the surface chemical functionality. FIG. 4C is a cross sectional view of a stack 203 after features 416 have been primed creating a
20 priming layer 420. The priming layer 420 is not drawn to scale to more clearly illustrate the priming layer 420.

[0026] A plurality of multiple layers is deposited (step 112). The depositing of the multiple layers (step 112) comprises a cyclical process with multiple cycles, where each cycle comprises depositing a first reactant (step 116) and depositing a
25 second reactant (step 120). FIG. 5 is a more detailed flow chart of the depositing the first reactant (step 116). The stack 203 is heated (step 504). In this embodiment, the stack 203 is heated while remaining in the etch chamber 249. The ESC temperature controller may heat the ESC 208 to maintain the stack 203 at a temperature of at least 20°C . A first reactant gas is flowed into the etch chamber 249 (step 508). In this
30 example, the first reactant gas is Sebacyl chloride. A pressure of 20 mTorr to 100 mTorr is provided. After 5 seconds, the flow of the first reactant gas is stopped (step 512). FIG. 6 is a more detailed flow chart of the depositing the second reactant (step

120). The stack 203 is heated (step 604). In this embodiment, the stack 203 is heated while remaining in the etch chamber 249. The ESC temperature controller may heat the ESC 208 to maintain the stack 203 at a temperature of at least 20° C. A second reactant gas is flowed into the etch chamber 249 (step 608). In this example, the
5 second reactant gas is 1,3-pentadiamine. A pressure of 20 mTorr to 100 mTorr is provided. After 5 seconds, the flow of the second reactant gas is stopped (step 612). The process is continued for a plurality of cycles. In this example, the cycles are a plasmaless process. FIG. 4D is a cross sectional view of a stack 203 after a plurality of multiple layers 424 is deposited (step 112) to provide a protective film. The
10 plurality of multiple layers 424 is not drawn to scale.

[0027] The multiple layers 424 are then cured (step 124). An example recipe for curing the multiple layers is low power Ne plasma.

[0028] A breakthrough is provided (step 128). An example recipe for providing the breakthrough comprises use of a typical etch process, such as the etch process
15 specified below to partially etch the etch layer 408, with additional 10 sccm of O₂ to increase polymer removal capability. FIG. 4E is a cross sectional view of a stack 203 after a the breakthrough is completed.

[0029] The etch layer 408 is at least partially etched (step 132). In this embodiment, the stack 203 is cooled while remaining in the etch chamber 249. The
20 chiller 214 cools a coolant to a temperature below -20° C. The coolant is used to cool the stack 203. An example of a recipe for partially etching features into the etch layer 408 provides a pressure of 5-50mT. RF power is provided at a frequency of 60 MHz at a power of 2 kW-8 kW and at a frequency of 400k at a power of 4kW-25 kW. The RF power is pulsed between these powers and lower power levels. An etch gas is
25 provided, which comprises O₂, fluorocarbon(s) and/or hydrofluorocarbon(s). FIG. 4F is a cross sectional view of a stack 203 after features 416 have been partially etched. In this example, the priming layer 420 and multiple layers 424 (shown in FIG. 4E) have been removed during the etch (step 132).

[0030] Since the etch is not completed, the process is repeated (step 136)
30 beginning at the priming the features (step 108). The steps are repeated until the etching of the features is completed (step 136) when the etching the features has

reached a final depth. FIG. 4G is a cross sectional view of the stack 203 after the completion of the etching of the features 416.

[0031] In this embodiment, during the etching of the features, a coolant at less than -20° C is used to cool the stack 203, so to provide an improved etch. In this embodiment, the lower temperature processes and higher temperature processes are performed in the same etch chamber. In other embodiments, lower temperature processes may be performed in different process chambers than higher temperature processes. In other embodiments, the etching of the features is performed at about the same temperature as other processes.

10 [0032] In this embodiment, the features are primed (step 108) before the multiple layer deposition. The priming of the features (step 108) modifies the sidewall surface to better facilitate the multiple layer deposition (step 112). In some embodiments, the priming step (step 108) is designed to functionalize the feature sidewall to promote reactions with the atomic layer deposition (ALD) precursors, which are provided in the next step.. Various embodiments include: 1) a short low bias plasma oxidizing plasma to remove some sidewall etch residues formed from an oxidizing gas of at least one of O₂, nitrogen (N₂), CO₂, nitrogen trifluoride (NF₃), sulfur hexafluoride (SF₆), water (H₂O), and/or carbonyl sulfide (COS) 2) a short low power reducing plasma to remove some sidewall etch residue and/or introduce hydroxide (-OH) and/or amide (-NH₂) surface groups, formed from a reducing gas of at least one of hydrogen (H₂), a mixture of nitrogen (N₂) + H₂, hydrazine (N₂H₄), and/or ammonia (NH₃). 3) a non-plasma vapor treatment to functionalize the surface, which could include H₂O, NH₃, O₃, N₂H₄, and/or peroxide (H₂O₂) as reactive vapors. For some ALD processes, a several ALD cycles are needed before a layer is actually deposited. The addition of a priming step may result in less ALD cycles being needed to before a layer is actually deposited. In addition, the priming step may make the process more repeatable, provide a more uniform film, and provide more consistent deposition between different wafers. In other embodiments, the features are not primed.

[0033] In this embodiment, the two reactants comprise carbon, hydrogen, oxygen, and nitrogen to provide an etch resistant sidewall passivation. In other embodiments, one of the two reactants may comprise at least one of a metal, sulfur, boron, silicon, nitrogen, or phosphorous. In some embodiments, one of the two reactants comprises a

metal, which is at least one of aluminum (Al), titanium (Ti), tungsten (W), tantalum (Ta), hafnium (Hf), or ruthenium (Ru). Although the overall metallic content of the resulting plurality of multiple layers 424 may be fairly low, it is expected this metallic content will significantly reduce the lateral removal rate of the passivation in the subsequent breakthrough (step 128) and etch (step 132). Incorporation of these species may reduce the lateral removal rate of the passivation in the subsequent etch (step 132), due to the low removal rate of the added elements and/or the lower removal rate of a cross-linked polymer. In particular, 1) boron (B) and silicon (Si) are known to have lower removal rates than polymer; 2) sulfur (S) is known to induce polymer cross-linking (vulcanization), especially after plasma exposure; and 3) nitrogen (N) functionality is known to reduce polymer removal rates. In particular, metallic elements tend to have low removal rates under typical high aspect ratio etch conditions, especially fluorocarbon based etches for stacks containing SiO₂.

[0034] In other embodiments, the two reactants do not comprise at least one of a metal, sulfur, boron, silicon, nitrogen, or phosphorous, when such an increased passivation is not desired. In other embodiments, specific organic structural groups are incorporated into the organic precursor(s), including branched structures, rings, phenolic groups, polycyclic aromatic groups, carbon double bonds, or carbon triple bonds. Incorporation of these species may reduce the lateral removal rate of the passivation in the subsequent etch, due to 1) steric effects of these structures to impede etch radical transport; 2) increased likelihood of polymeric cross-linking after deposition; and/or 3) formation of polymer cross-linking upon plasma exposure. For example, a precursor containing carbon double bonds may create a surface film which is crosslinked upon activation by ultra violet (UV) radiation from the plasma.

[0035] In other embodiments, one or more polydentate precursors are used instead of the more conventional bidentate precursors which are the basis of ALD. Polydentate means the precursor has 3 or more head groups which can react with the head groups of the other precursor. Upon reaction, these precursors will create branched chains. Therefore, these polydentate precursors should promote formation of cross-linked networks in the resulting polymer, which may reduce the lateral removal rate of the passivation in the subsequent etch. Various embodiments rely entirely on tailoring the chemical precursors to control the etch resistance of passivation films.

[0036] In this embodiment, the deposited multiple layers are cured (step 124). Curing the deposited multiple layers (step 124) make the deposited multiple layers more etch resistant. In various embodiments, the curing (step 124) may be by thermal heating, light irradiation, which may be visible, UV, or infrared irradiation, or may be by exposure to a curing plasma. A post-deposition cure may also add value by converting the sidewall passivation into a more etch resistant form. In particular, the cure step may increase cross-linking in the sidewall polymer and/or remove some hydrogen content to increase the graphitic or carbidic nature of the material. The curing may also densify the deposited plurality of multiple layers 424. A plasma in one embodiment uses a low bias plasma, which includes He, Ne, Ar, Kr, Xe, H₂, and/or N₂ gas. In this context, a low bias plasma has a DC sheath voltage of 25-750 volts. More specifically, a low bias has a DC sheath voltage of 50-400 volts. Additionally, these cures may be more effective at cross-linking, if combined with specific functionality designed into the sidewall passivation, including but not limited to: S groups, carbon (C) double bonds, phenyl groups, polycyclic aromatic groups, and/or epoxides. In other embodiments, the curing may occur after every single ALD cycle. Other embodiments may provide a curing process after a few ALD cycles. These various methods to convert the sidewall passivation into a more etch resistant material will increase the ability of the layer to protect the underlying material, thus improving the overall effectiveness of the passivation layer in producing an etch result with low bowing. In other embodiments, a curing process may not be used.

[0037] In this embodiment, a breakthrough process (step 128) is provided. Deposition of sidewall passivation can have undesirable effects, including reduced neck size and/or deposition of passivation material at the etch front. Smaller necks can interfere with the subsequent etch, by reducing flux of species and/or by causing formation of a capping layer over some fraction of the holes. Passivation at the etch front may prevent subsequent etching in some or all of the holes. To avoid these “etch stop” issues and to create a safer margin for the effectiveness of the etch, a breakthrough process can be introduced after deposition. This breakthrough process removes the deposited passivation at the neck and/or etch front, while substantially preserving the sidewall passivation film. The net outcome is to avoid risk of “etch stop”, providing a wider safe operating window for the overall process. Some

embodiments include additional O₂ or N₂ in a standard etch recipe to increase the capability to etch polymer. Other embodiments reduce the flow of some or all carbon-containing gases in a standard etch recipe, to shift the process towards less passivation. Other embodiments use non-halogen containing plasma comprising O₂ and/or N₂. In these various embodiments, the breakthrough process is used until the excessive neck and/or etch front passivation is removed, and then the conventional etch process can resume. In other embodiments, a breakthrough process is not provided.

[0038] In this embodiment, the partially etching the features (step 104) and etching the etch layer (step 132) are performed at cryogenic temperatures, while the depositing of the multiple layers (step 112) is done at non-cryogenic temperatures. In this embodiment, both processes are performed in the same chamber. In another embodiment, the partially etching the features (step 104) and etching the etch layer (step 132) are performed in one or more chambers at cryogenic temperatures and the depositing of the multiple layers (step 112) is done in one or more chambers at non-cryogenic temperatures. Etching at cryogenic temperatures can improve overall etch performance by increasing the etch rate and/or by increasing the selectivity of the etch to the mask. Depositing multiple layers of passivation may be more effective at non-cryogenic temperature, by avoiding the risks of excessive deposition in the cryogenic regime. In other embodiments, all steps are performed at non-cryogenic temperatures. Cryogenic temperatures are temperatures where a coolant is cooled to a temperature no greater than -20°C.

[0039] While this disclosure has been described in terms of several exemplary embodiments, there are alterations, modifications, permutations, and various substitute equivalents, which fall within the scope of this disclosure. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present disclosure. It is therefore intended that the following appended claims be interpreted as including all such alterations, modifications, permutations, and various substitute equivalents as fall within the true spirit and scope of the present disclosure.

CLAIMS

What is claimed is:

1. A method of forming a feature in a stack comprising a dielectric material on a substrate, the method comprising:
 - 5 (a) generating an etch plasma from an etch gas, exposing the stack to the etch plasma, and partially etching the feature in the stack;
 - (b) after (a), priming the stack;
 - (c) depositing a protective film on sidewalls of the feature by
 - 10 (i) exposing the stack to a first reactant and allowing the first reactant to adsorb onto the stack,
 - (ii) exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack, and
 - (iii) repeating (i) and (ii) in a cyclic manner a plurality of times; and
 - (d) repeating (a)-(c) until the feature is etched to a final depth.
- 15 2. The method, as recited in claim 1, wherein the priming the stack modifies surfaces of the sidewalls to better facilitate the depositing the protective film.
3. The method, as recited in claim 2, wherein the priming the stack comprises at least one of an oxidizing plasma to remove some sidewall etch residue, a reducing plasma to remove some sidewall etch residue, or a non-plasma vapor treatment to
20 functionalize a surface of the stack.
4. The method, as recited in claim 1, wherein the priming the stack comprises providing an oxidizing plasma, comprising:
 - providing an oxidizing gas comprising at least one of O₂, N₂, CO₂, NF₃, SF₆, H₂O, and COS; and
 - 25 forming a plasma from the oxidizing gas.
5. The method, as recited in claim 1, wherein the priming the stack comprises providing a reducing plasma, comprising:
 - providing a reducing gas comprising at least one of H₂, a mixture of N₂ + H₂, N₂H₄, and NH₃; and
 - 30 forming a plasma from the reducing gas.
6. The method, as recited in claim 1, wherein the priming the stack comprises providing a non-plasma vapor treatment to functionalize a surface of the stack,

comprising exposing the surface of the stack to a vapor of at least one of H₂O, NH₃, O₃, N₂H₄, or H₂O₂.

7. The method, as recited in claim 1, further comprising curing the protective film.

5 8. The method, as recited in claim 1, wherein the protective film comprises at least one of a metal, sulfur, boron, silicon, nitrogen, or phosphorous.

9. The method, as recited in claim 1, further comprising performing a breakthrough etch to etch the protective film.

10 10. The method, as recited in claim 1, wherein the generating the etch plasma is performed while cooling the substrate to a temperature below -20° C, and wherein the depositing the protective film is performed while heating the substrate to a temperature above 20° C.

11. A method of forming a feature in a stack comprising a dielectric material on a substrate, the method comprising:

15 (a) generating an etch plasma from an etch gas, exposing the stack to the etch plasma, and partially etching the feature in the stack;

(b) after (a), depositing a protective film on sidewalls of the feature by

(i) exposing the stack to a first reactant and allowing the first reactant to adsorb onto the stack,

20 (ii) exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack, and

(iii) repeating (i) and (ii) in a cyclic manner a plurality of times;

(c) curing the protective film; and

(d) repeating (a)-(c) until the feature is etched to a final depth.

25 12. The method, as recited in claim 11, wherein the curing the protective film is effected by at least one of thermal heating, visible or UV light irradiation, infrared irradiation, or exposure to a curing plasma.

13. The method, as recited in claim 11, wherein the curing the protective film creates cross-links in a polymer forming the protective film.

30 14. The method, as recited in claim 11, wherein the curing the protective film removes some hydrogen content of the protective film to increase the graphitic or carbide nature of the protective film.

15. The method, as recited in claim 11, wherein the curing the protective film densifies the protective film.
16. The method, as recited in claim 11, wherein the curing the protective film is a
5 step in each cycle of the depositing the protective film.
17. The method, as recited in claim 11, wherein the protective film comprises at least one of a metal, sulfur, boron, silicon, nitrogen, or phosphorous.
18. The method, as recited in claim 11, further comprising performing a breakthrough etch to etch the protective film.
- 10 19. The method, as recited in claim 11, wherein the generating the etch plasma is performed while cooling the substrate to a temperature below -20°C , and wherein the depositing the protective film is performed while heating the substrate to a temperature above 20°C .
20. A method of forming a feature in a stack comprising a dielectric material on a
15 substrate, the method comprising:
- (a) generating an etch plasma from an etch gas, exposing the stack to the etch plasma, and partially etching the feature in the stack;
 - (b) after (a), depositing a protective film on sidewalls of the feature by
 - (i) exposing the stack to a first reactant and allowing the first reactant
20 to adsorb onto the stack,
 - (ii) exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack, wherein the protective film comprises at least one of a metal, sulfur, boron, silicon, nitrogen, or phosphorous, and
 - (iii) repeating (i) and (ii) in a cyclic manner a plurality of times; and
 - (c) repeating (a)-(b) until the feature is etched to a final depth.
- 25 21. The method, as recited in claim 20, wherein the protective film comprises at least one of aluminum (Al), titanium (Ti), tungsten (W), tantalum (Ta), hafnium (Hf), or ruthenium (Ru).
- 30 22. The method, as recited in claim 20, further comprising performing a breakthrough etch to etch the protective film.

23. The method, as recited in claim 20, wherein the generating the etch plasma is performed while cooling the substrate to a temperature below -20°C , and wherein the depositing the protective film is performed while heating the substrate to a temperature above 20°C .
- 5 24. A method of forming a feature in a stack comprising a dielectric material on a substrate, the method comprising:
- (a) generating an etch plasma from an etch gas, exposing the stack to the etch plasma, and partially etching the feature in the stack;
 - (b) after (a), depositing a protective film on sidewalls of the feature by
 - 10 (i) exposing the stack to a first reactant and allowing the first reactant to adsorb onto the stack,
 - (ii) exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack, and
 - (iii) repeating (i) and (ii) in a cyclic manner a plurality of times;
 - 15 (c) performing a breakthrough etch to etch the protective film on etch fronts and/or at neck locations; and
 - (d) repeating (a)-(c) until the feature is etched to a final depth.
25. The method, as recited in claim 24, wherein the performing the breakthrough etch comprises exposing the stack to a plasma comprising oxygen.
- 20 26. The method, as recited in claim 24, wherein the performing the breakthrough etch completely removes the protective film on the etch fronts without completely removing the protective film on the sidewalls of the feature.
27. The method, as recited in claim 24, wherein the performing the breakthrough etch completely removes the protective film at the neck locations.
- 25 28. The method, as recited in claim 24, wherein the generating the etch plasma is performed while cooling the substrate to a temperature below -20°C , and wherein the depositing the protective film is performed while heating the substrate to a temperature above 20°C .
29. A method of forming a feature in a stack comprising a dielectric material on a
30 substrate, the method comprising:

(a) generating an etch plasma from an etch gas, exposing the stack to the etch plasma, and partially etching the feature in the stack, while cooling the substrate to a temperature below -20°C ;

5 (b) after (a), depositing a protective film on sidewalls of the feature at a temperature of at least 20°C by

(i) exposing the stack to a first reactant and allowing the first reactant to adsorb onto the stack,

(ii) exposing the stack to a second reactant, wherein the first and second reactants react with one another to form the protective film over the stack, and

10 (iii) repeating (i) and (ii) in a cyclic manner a plurality of times; and

(c) repeating (a)-(b) until the feature is etched to a final depth.

30. The method, as recited in claim 29, wherein the etch gas comprises H_2 and at least one of a fluorocarbon or hydrofluorocarbon.

15

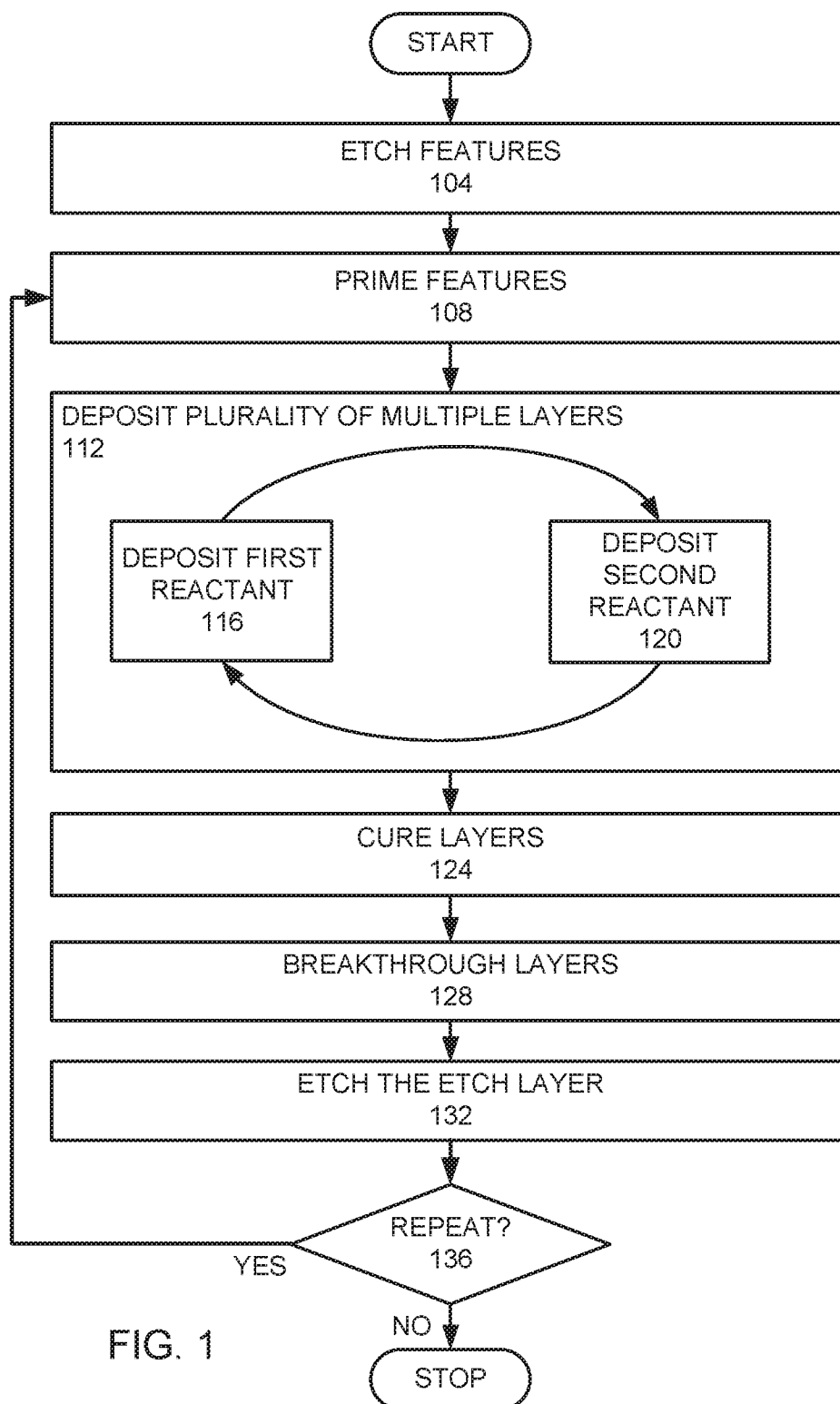


FIG. 1

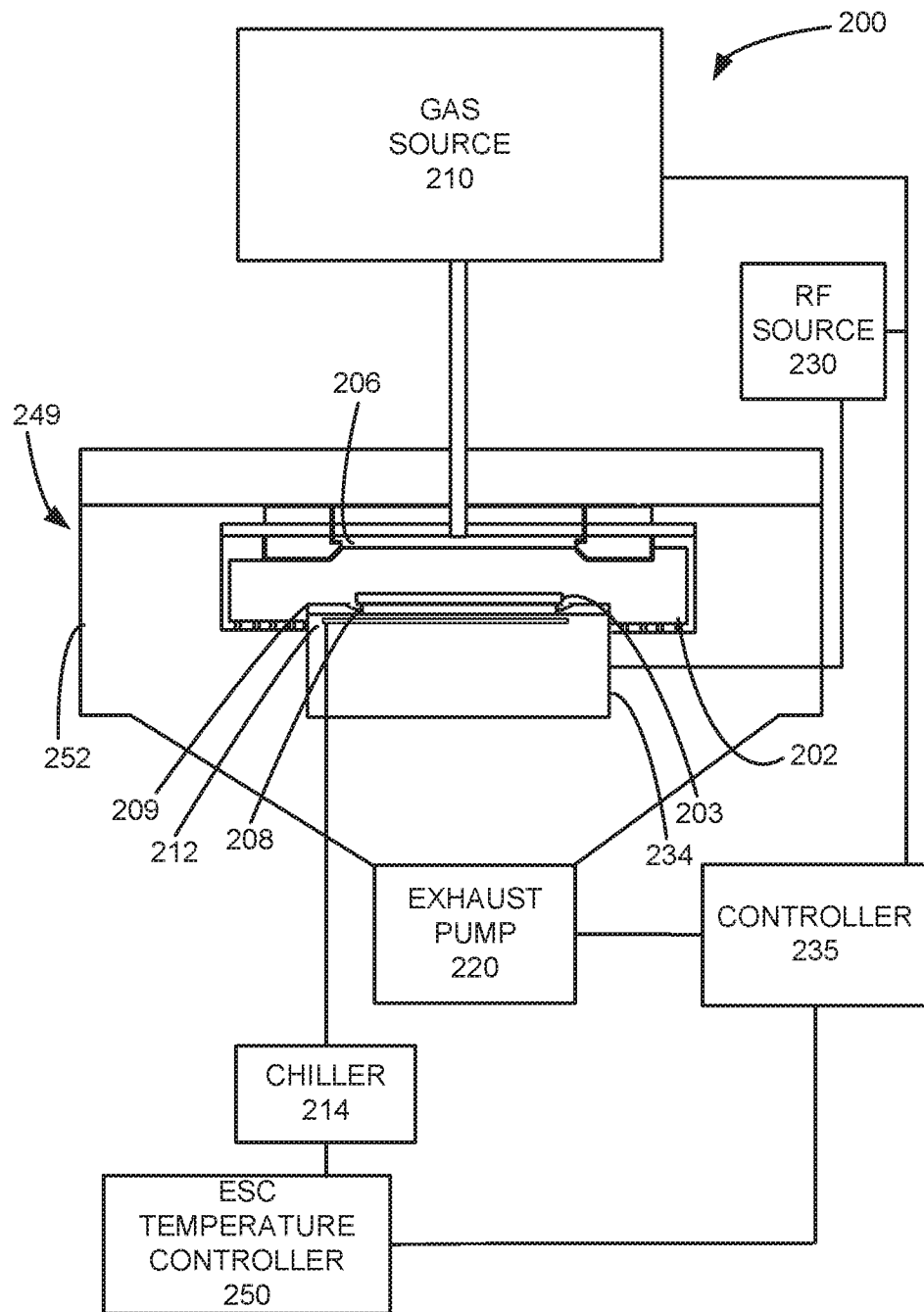


FIG. 2

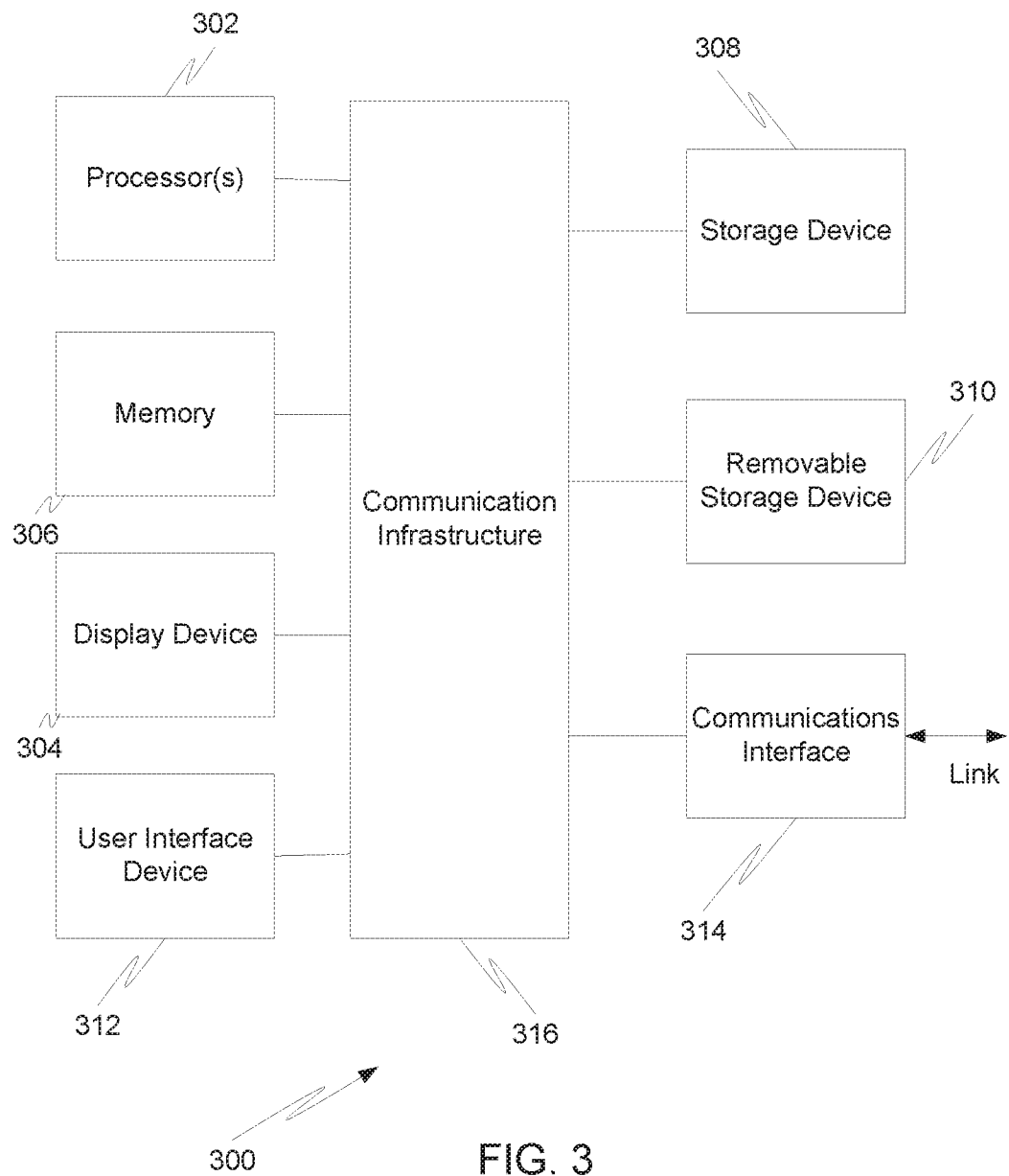


FIG. 3

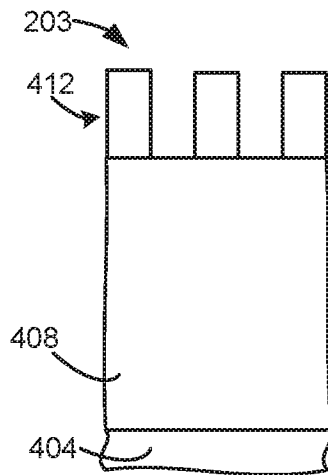


FIG. 4A

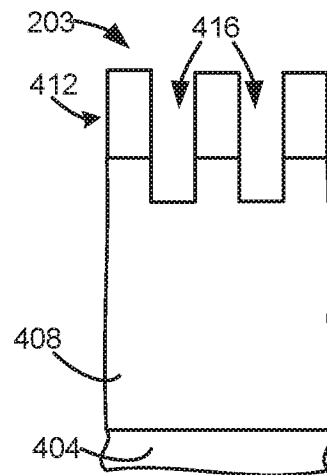


FIG. 4B

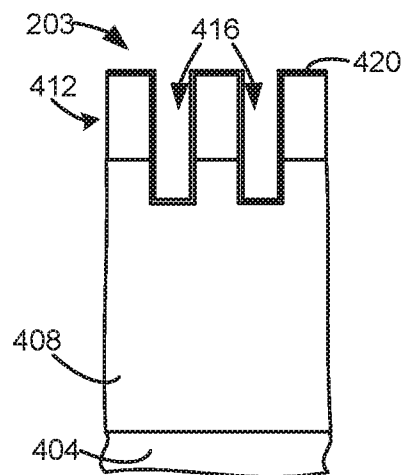


FIG. 4C

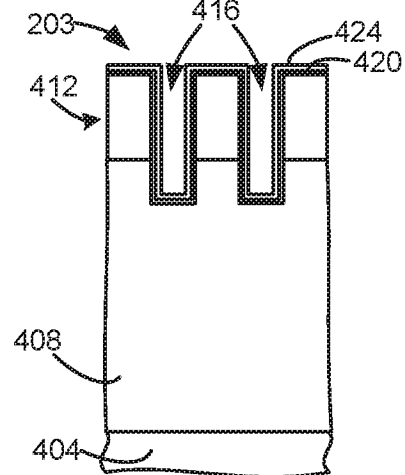


FIG. 4D

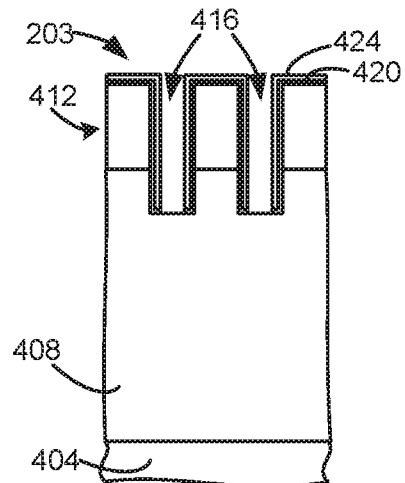


FIG. 4E

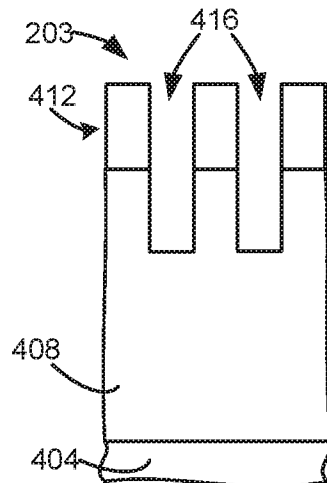


FIG. 4F

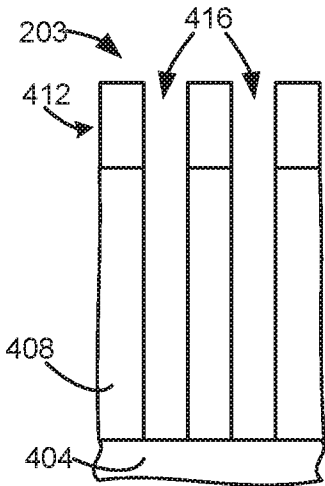
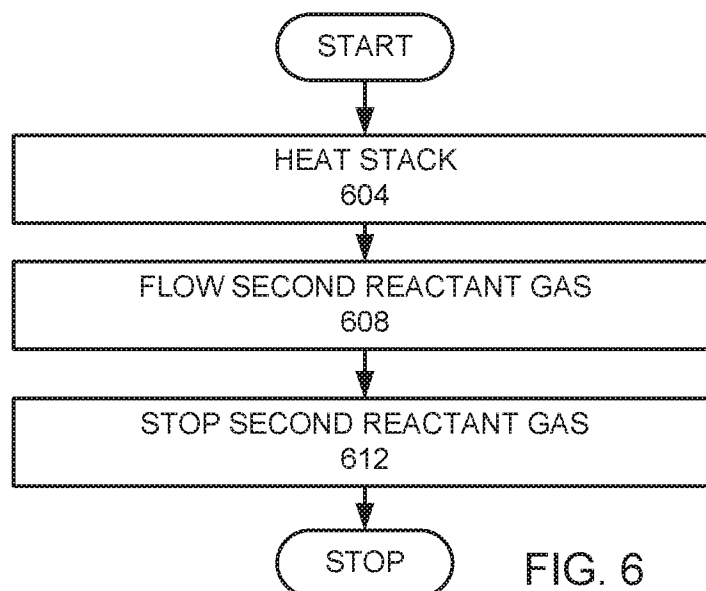
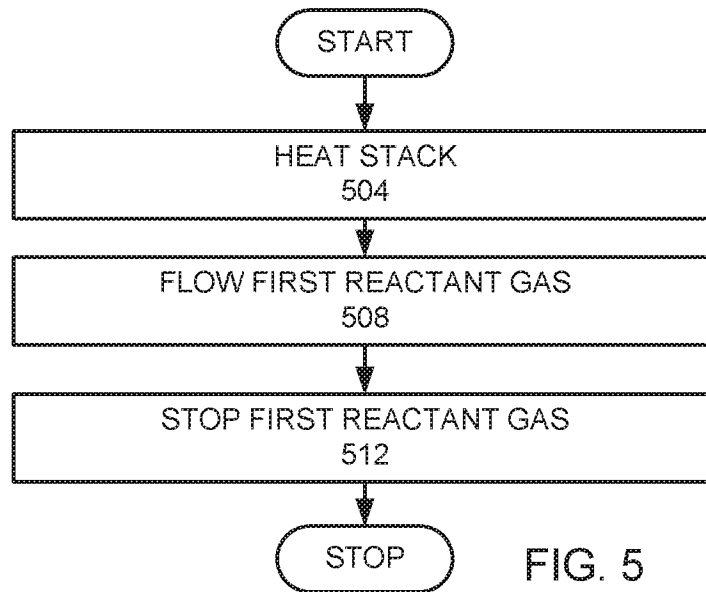


FIG. 4G



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/042560**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/3065(2006.01)i, H01L 21/311(2006.01)i, H01L 21/3213(2006.01)i, H01L 21/324(2006.01)i, H01L 21/67(2006.01)i, H01J 37/32(2006.01)i, H05H 1/46(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/3065; H01L 21/02; H01L 21/033; H01L 21/28; H01L 21/3205; H01L 21/324; H01L 21/67; H01L 21/768; H01L 21/311; H01L 21/3213; H01J 37/32; H05H 1/46

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: etch, protective layer, sidewall, dielectric, plasma, cure

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2017-0076945 A1 (LAM RESEARCH CORPORATION) 16 March 2017 See paragraphs [0010], [0075]-[0079], [0110], [0112], [0128], claims 10, 14 and figures 3A-3D.	20-22, 24-27
Y		1-6, 8-9
A		7, 10-19, 23, 28-30
Y	KR 10-2017-0132671 A (LAM RESEARCH CORPORATION) 04 December 2017 See paragraphs [0033], [0036] and figure 2a.	1-6, 8-9
A	JP 2013-021192 A (TOKYO ELECTRON LTD.) 31 January 2013 See the whole document.	1-30
A	JP 2013-229351 A (HITACHI HIGH-TECHNOLOGIES CORP.) 07 November 2013 See the whole document.	1-30
A	KR 10-2017-0092645 A (BEIJING NAURA MICROELECTRONICS EQUIPMENT CO., LTD.) 11 August 2017 See the whole document.	1-30



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

08 November 2019 (08.11.2019)

Date of mailing of the international search report

08 November 2019 (08.11.2019)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

KANG, Sung Chul

Telephone No. +82-42-481-8405



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/042560

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2017-0076945 A1	16/03/2017	KR 10-2017-0028259 A TW 201724254 A US 9543148 B1	13/03/2017 01/07/2017 10/01/2017
KR 10-2017-0132671 A	04/12/2017	CN 103053011 A CN 103053011 B CN 103053012 A CN 103053012 B CN 103632954 A CN 103632954 B CN 103703870 A CN 103703870 B CN 103890916 A CN 103890916 B CN 104465457 A CN 104465457 B CN 105719932 A CN 105719932 B CN 105845535 A CN 105845535 B CN 106128931 A CN 106128931 B CN 107424900 A CN 109417030 A JP 2013-541177 A JP 2014-057057 A JP 2014-531753 A JP 2015-065434 A JP 2016-167606 A JP 2018-037668 A JP 2019-050413 A JP 5913312 B2 JP 6110540 B2 JP 6382719 B2 JP 6441434 B2 KR 10-1871521 B1 KR 10-1911562 B1 KR 10-1998542 B1 KR 10-2013-0093110 A KR 10-2013-0136962 A KR 10-2014-0027895 A KR 10-2014-0046468 A KR 10-2014-0068055 A KR 10-2015-0032811 A KR 10-2016-0067741 A KR 10-2016-0067742 A KR 10-2016-0067743 A KR 10-2016-0068002 A KR 10-2017-0132666 A	17/04/2013 23/03/2016 17/04/2013 20/04/2016 12/03/2014 11/08/2017 02/04/2014 08/06/2016 25/06/2014 07/09/2016 25/03/2015 14/09/2018 29/06/2016 02/01/2018 10/08/2016 26/12/2017 16/11/2016 27/04/2018 01/12/2017 01/03/2019 07/11/2013 27/03/2014 27/11/2014 09/04/2015 15/09/2016 08/03/2018 28/03/2019 27/04/2016 05/04/2017 29/08/2018 19/12/2018 02/08/2018 04/01/2019 09/07/2019 21/08/2013 13/12/2013 07/03/2014 18/04/2014 05/06/2014 30/03/2015 14/06/2016 14/06/2016 14/06/2016 14/06/2016 04/12/2017

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/042560

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		KR 10-2018-0101204 A	12/09/2018
		KR 10-2018-0118235 A	30/10/2018
		SG 10201405549 A	29/04/2015
		SG 10201505975 A	29/09/2015
		SG 10201506065 A	29/09/2015
		SG 10201601331 A	30/03/2016
		SG 10201602732 A	30/05/2016
		SG 11201400364 A	28/04/2014
		SG 187256 A1	28/03/2013
		SG 187610 A1	28/03/2013
		SG 2013065065 A	28/03/2014
		TW 201214557 A	01/04/2012
		TW 201222635 A	01/06/2012
		TW 201316400 A	16/04/2013
		TW 201330098 A	16/07/2013
		TW 201415560 A	16/04/2014
		TW 201528310 A	16/07/2015
		TW 201630067 A	16/08/2016
		TW 201630072 A	16/08/2016
		TW 201635334 A	01/10/2016
		TW 201639027 A	01/11/2016
		TW 201643955 A	16/12/2016
		TW 201701355 A	01/01/2017
		TW 201711110 A	16/03/2017
		TW 201806028 A	16/02/2018
		TW 201835377 A	01/10/2018
		TW 201842225 A	01/12/2018
		TW I546857 B	21/08/2016
		TW I552222 B	01/10/2016
		TW I562232 B	11/12/2016
		TW I578408 B	11/04/2017
		TW I605495 B	11/11/2017
		TW I608544 B	11/12/2017
		TW I609425 B	21/12/2017
		TW I621186 B	11/04/2018
		TW I647731 B	11/01/2019
		US 10170323 B2	01/01/2019
		US 10170324 B2	01/01/2019
		US 10181412 B2	15/01/2019
		US 10297459 B2	21/05/2019
		US 10304693 B2	28/05/2019
		US 10373840 B2	06/08/2019
		US 2012-0031559 A1	09/02/2012
		US 2012-0034786 A1	09/02/2012
		US 2013-0023064 A1	24/01/2013
		US 2013-0059448 A1	07/03/2013
		US 2014-0054269 A1	27/02/2014
		US 2015-0004793 A1	01/01/2015
		US 2015-0083582 A1	26/03/2015
		US 2015-0206775 A1	23/07/2015

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/042560

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 2015-0357209 A1	10/12/2015
		US 2016-0079039 A1	17/03/2016
		US 2016-0148786 A1	26/05/2016
		US 2016-0163556 A1	09/06/2016
		US 2016-0163557 A1	09/06/2016
		US 2016-0163558 A1	09/06/2016
		US 2016-0163561 A1	09/06/2016
		US 2016-0260617 A1	08/09/2016
		US 2016-0260620 A1	08/09/2016
		US 2016-0268141 A1	15/09/2016
		US 2016-0343580 A1	24/11/2016
		US 2016-0358784 A1	08/12/2016
		US 2017-0076955 A1	16/03/2017
		US 2017-0170026 A1	15/06/2017
		US 2017-0178920 A1	22/06/2017
		US 2017-0213747 A9	27/07/2017
		US 2018-0005852 A1	04/01/2018
		US 2018-0174858 A1	21/06/2018
		US 8869742 B2	28/10/2014
		US 9039911 B2	26/05/2015
		US 9117767 B2	25/08/2015
		US 9184028 B2	10/11/2015
		US 9378971 B1	28/06/2016
		US 9384998 B2	05/07/2016
		US 9418859 B2	16/08/2016
		US 9543158 B2	10/01/2017
		US 9620377 B2	11/04/2017
		US 9793126 B2	17/10/2017
		US 9793128 B2	17/10/2017
		US 9887097 B2	06/02/2018
		US 9997372 B2	12/06/2018
		US 9997373 B2	12/06/2018
		WO 2012-018448 A2	09/02/2012
		WO 2012-018448 A3	05/04/2012
		WO 2012-018449 A2	09/02/2012
		WO 2012-018449 A3	12/04/2012
		WO 2013-012591 A1	24/01/2013
		WO 2013-036371 A2	14/03/2013
		WO 2013-036371 A3	15/05/2014
		WO 2018-026867 A1	08/02/2018
JP 2013-021192 A	31/01/2013	JP 5981106 B2	31/08/2016
		KR 10-1904576 B1	04/10/2018
		KR 10-2014-0050627 A	29/04/2014
		TW 201316408 A	16/04/2013
		TW I459465 B	01/11/2014
		US 2014-0134846 A1	15/05/2014
		US 8975188 B2	10/03/2015
		WO 2013-008824 A1	17/01/2013

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/042560

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2013-229351 A	07/11/2013	None	
KR 10-2017-0092645 A	11/08/2017	CN 105719965 A	29/06/2016
		JP 2017-536701 A	07/12/2017
		JP 6423534 B2	14/11/2018
		SG 11201704068Y A	29/06/2017
		WO 2016-086841 A1	09/06/2016