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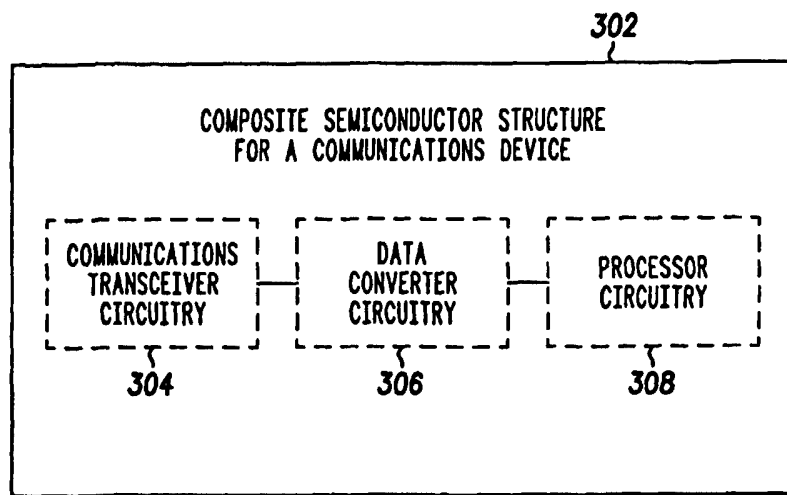
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- (71) Applicant: **MOTOROLA, INC.** [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).
- (72) Inventors: **WARBLE, Keith**; 3215 S. Laguna Drive, Chandler, AZ 85248 (US). **GILLIG, Steven, F.**; 633 West End Road, Roselle, IL 60172 (US). **HEROLD, Barry, W.**; 136 Wedgewood, Barrington, IL 60010 (US).
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(54) Title: INTEGRATED COMMUNICATIONS APPARATUS AND METHODS



(57) Abstract: Integrated communications apparatus and methods are used to receive, transmit, and operate on communications signals. A composite semiconductor structure (302) may be formed for providing an integrated communications device that may include transceiver circuitry (304), data converter circuitry (306), and processor circuitry (308). The data converter circuitry may include an analog-to-digital and/or digital-to-analog data converter that is implemented at least partly using compound semiconductors (e.g., using compound semiconductor transistors for implementing comparators and/or switches in the data converter). The processor circuitry may include some circuitry that is formed from non-compound semiconductors, which is better suited than compound semiconductors to perform digital signal processing operations. The transceiver circuitry may include compound and/or non-compound semiconductor circuitry depending on the signal frequency and whether the signal is optical or electrical.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTEGRATED COMMUNICATIONS APPARATUS AND METHODS

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Field of the Invention

This invention relates generally to semiconductor structures and devices
10 and, and more specifically to semiconductor structures for communications and
communications-related processing.

Background of the Invention

15 The vast majority of semiconductor discrete devices and integrated circuits
are fabricated from silicon, at least in part because of the availability of
inexpensive, high quality monocrystalline silicon substrates. Other semiconductor
materials, such as the so called compound semiconductor materials, have physical
attributes, including wider bandgap and/or higher mobility than silicon, or direct
20 bandgaps that makes these materials advantageous for certain types of
semiconductor devices. Unfortunately, compound semiconductor materials are
generally much more expensive than silicon and are not available in large wafers
as is silicon. Gallium arsenide (GaAs), the most readily available compound
semiconductor material, is available in wafers only up to about 150 millimeters
25 (mm) in diameter. In contrast, silicon wafers are available up to about 300 mm and
are widely available at 200 mm. The 150 mm GaAs wafers are many times more
expensive than are their silicon counterparts. Wafers of other compound

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semiconductor materials are even less available and are more expensive than GaAs.

In many known communications applications, multiple integrated circuits or dies that are each formed using different semiconductor technologies are used to
5 implement a single communications apparatus. Differing semiconductor technologies are used so that the advantages of a particular semiconductor technology can be suitably matched with a particular function that is desired in the communications apparatus.

For example, Group IV monocrystalline semiconductors are typically
10 suitable for electrical digital signal processing and compound semiconductors (e.g., gallium arsenide) are typically suitable for the realization of high frequency transceiver and high speed data converter functions. For signal reception and handling, a suitable semiconductor technology may be selected from Group IV monocrystalline semiconductor technology or compound semiconductor
15 technology based on the frequency of the signals that are involved and whether the signals are optical or electrical. The use of a single integrated circuit that is formed only from either compound semiconductor materials or non-compound semiconductor materials may result in deficiencies in certain desired functions in a communications apparatus. Using multiple integrated circuits causes deficiencies
20 such as increasing packaging parasitics and increasing manufacturing costs.

Compound and non-compound semiconductor materials typically cannot be integrated in a single semiconductor structure using conventional techniques.

Brief Description of the Drawings

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FIGs. 1, 2, 3, 24, 25 illustrate schematically, in cross section, device structures that can be used in accordance with various embodiments of the invention.

FIG. 4 illustrates graphically the relationship between maximum attainable
30 film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer.

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FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of illustrative semiconductor material manufactured in accordance with what is shown herein.

FIG. 6 is an x-ray diffraction taken on an illustrative semiconductor structure manufactured in accordance with what is shown herein.

FIG. 7 illustrates a high resolution Transmission Electron Micrograph of a structure including an amorphous oxide layer.

FIG. 8 illustrates an x-ray diffraction spectrum of a structure including an amorphous oxide layer.

FIGs. 9-12 illustrate schematically, in cross-section, the formation of a device structure in accordance with another embodiment of the invention.

FIGs. 13-16 illustrate a probable molecular bonding structure of the device structures illustrated in FIGs. 9-12.

FIGs. 17-20 illustrate schematically, in cross-section, the formation of a device structure in accordance with still another embodiment of the invention.

FIGs. 21-23 illustrate schematically, in cross section, the formation of a yet another embodiment of a device structure in accordance with the invention.

FIGs. 26-30 include illustrations of cross-sectional views of a portion of an integrated circuit that includes a compound semiconductor portion, a bipolar portion, and a MOS portion in accordance with what is shown herein.

FIGs. 31-37 include illustrations of cross-sectional views of a portion of another integrated circuit that includes a semiconductor laser and a MOS transistor in accordance with what is shown herein.

FIG. 38 illustrates a functional block diagram of a composite semiconductor structure for a communications device in accordance with the present invention.

FIG. 39 illustrates a functional block diagram of a composite semiconductor structure for an optical signal communications device that includes analog-to-digital circuitry in accordance with the present invention.

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FIG. 40 illustrates a functional block diagram of a composite semiconductor structure for an electrical signal communications device that includes analog-to-digital circuitry in accordance with the present invention.

FIG. 41 illustrates a functional block diagram of converter circuitry that includes an analog-to-digital converter for the composite semiconductor structures of FIGs. 38-40 in accordance with the present invention.

FIG. 42 illustrates a schematic of a comparator for the converter circuitry of FIG. 41 in accordance with the present invention.

FIG. 43 illustrates a schematic of a cross-sectional view of one embodiment of a heterojunction bipolar transistor that may be used in implementing the comparator of FIG. 41 in accordance with the present invention.

FIG. 44 illustrates a schematic of a cross-sectional view of another embodiment of a heterojunction bipolar transistor that may be used in implementing the comparator of FIG. 41 in accordance with the present invention.

FIG. 45 illustrates a flow chart of illustrative steps that may be involved in forming and operating a communications device that includes analog-to-digital data converter circuitry in accordance with the present invention.

FIG. 46 illustrates a functional block diagram of a composite semiconductor structure for an optical signal communications device that includes digital-to-analog data converter circuitry in accordance with the present invention.

FIG. 47 illustrates a functional block diagram of a composite semiconductor structure for an electrical signal communications device that includes digital-to-analog converter circuitry in accordance with the present invention.

FIG. 48 illustrates a functional block diagram of converter circuitry including a digital-to-analog data converter for the composite semiconductor structures of FIGs. 38, 46, and 47 in accordance with the present invention.

FIG. 49 illustrates a functional block diagram of a digital-to-analog data converter in accordance with the present invention.

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FIG. 50 illustrates a flow chart of illustrative steps that may be involved in forming and operating a communications device that includes digital-to-analog data converter circuitry in accordance with the present invention.

5 Skilled artisans will appreciate that in many cases elements in certain FIGs. are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in certain FIGs. may be exaggerated relative to other elements to help to improve understanding of what is being shown.

10 Detailed Description of the Drawings

The present invention involves semiconductor structures of particular types. For convenience herein, these semiconductor structures are sometimes referred to as "composite semiconductor structures" or "composite integrated circuits" because
15 they include two (or more) significantly different types of semiconductor devices in one integrated structure or circuit. For example, one of these two types of devices may be silicon-based devices such as CMOS devices, and the other of these two types of devices may be compound semiconductor devices such as GaAs devices.

20 FIG. 1 illustrates schematically, in cross section, a portion of a semiconductor structure 20 which may be relevant to or useful in connection with certain embodiments of the present invention. Semiconductor structure 20 includes a monocrystalline substrate 22, accommodating buffer layer 24 comprising a monocrystalline material, and a layer 26 of a monocrystalline
25 compound semiconductor material. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small number of defects such as dislocations and the like as are commonly found in substrates of
30 silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

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In accordance with one embodiment, structure 20 also includes an amorphous intermediate layer 28 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 30 between accommodating buffer layer 24 and compound semiconductor layer 26.

5 As will be explained more fully below, template layer 30 helps to initiate the growth of compound semiconductor layer 26 on accommodating buffer layer 24. Amorphous intermediate layer 28 helps to relieve the strain in accommodating buffer layer 24 and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer 24.

10 Substrate 22, in accordance with one embodiment, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of a material from Group IV of the periodic table. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Preferably
15 substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry. Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material epitaxially grown on the underlying substrate 22. In accordance with one embodiment, amorphous intermediate layer 28 is grown on substrate 22 at the
20 interface between substrate 22 and the growing accommodating buffer layer 24 by the oxidation of substrate 22 during the growth of layer 24. Amorphous intermediate layer 28 serves to relieve strain that might otherwise occur in monocrystalline accommodating buffer layer 24 as a result of differences in the lattice constants of substrate 22 and buffer layer 24. As used herein, lattice
25 constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by amorphous intermediate layer 28, the strain may cause defects in the crystalline structure of accommodating buffer layer 24. Defects in the crystalline structure of accommodating buffer layer 24, in turn, would make it difficult to achieve a high quality crystalline structure in
30 monocrystalline compound semiconductor layer 26.

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Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with underlying substrate 22 and with overlying compound semiconductor material 26. For example, the material could be an oxide or nitride having a lattice structure matched to substrate 22 and to the subsequently applied semiconductor material 26. Materials that are suitable for accommodating buffer layer 24 include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be used for accommodating buffer layer 24. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different metallic elements. In some specific applications, the metal oxides or nitride may include three or more different metallic elements.

Amorphous interface layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24. Typically, layer 28 has a thickness in the range of approximately 0.5-5 nm.

The compound semiconductor material of layer 26 can be selected, as needed for a particular semiconductor structure, from any of the Group IIIA and VA elements (III-V semiconductor compounds), mixed III-V compounds, Group II(A or B) and VIA elements (II-VI semiconductor compounds), and mixed II-VI compounds. Examples include gallium arsenide (GaAs), gallium indium arsenide (GaInAs), gallium aluminum arsenide (GaAlAs), indium phosphide (InP), cadmium sulfide (CdS), cadmium mercury telluride (CdHgTe), zinc selenide

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(ZnSe), zinc sulfur selenide (ZnSSe), and the like. Suitable template 30 materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for the nucleation of the epitaxial growth of the subsequent compound semiconductor layer 26. Appropriate materials for template 30 are
5 discussed below.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment. Structure 40 is similar to the previously described semiconductor structure 20 except that an additional buffer layer 32 is positioned between accommodating buffer layer 24 and layer of monocrystalline
10 compound semiconductor material 26. Specifically, additional buffer layer 32 is positioned between the template layer 30 and the overlying layer 26 of compound semiconductor material. Additional buffer layer 32, formed of a semiconductor or compound semiconductor material, serves to provide a lattice compensation when the lattice constant of accommodating buffer layer 24 cannot be adequately
15 matched to the overlying monocrystalline compound semiconductor material layer 26.

FIG. 3 schematically illustrates, in cross section, a portion of a semiconductor structure 34 in accordance with another exemplary embodiment of the invention. Structure 34 is similar to structure 20, except that structure 34
20 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28, and an additional semiconductor layer 38.

As explained in greater detail below, amorphous layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner to that described above. Monocrystalline semiconductor layer
25 26 is then formed (by epitaxial growth) overlying the monocrystalline accommodating buffer layer. The accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this manner comprises materials from both the accommodating buffer and interface layers, which amorphous layers
30 may or may not amalgamate. Thus, layer 36 may comprise one or two amorphous layers. Formation of amorphous layer 36 between substrate 22 and semiconductor

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layer 38 (subsequent to layer 38 formation) relieves stresses between layers 22 and 38 and provides a true compliant substrate for subsequent processing--*e.g.*, compound semiconductor layer 26 formation.

The processes previously described above in connection with FIGS. 1 and 2 are adequate for growing monocrystalline compound semiconductor layers over a monocrystalline substrate. However, the process described in connection with FIG. 3, which includes transforming a monocrystalline accommodating buffer layer to an amorphous oxide layer, may be better for growing monocrystalline compound semiconductor layers because it allows any strain in layer 26 to relax.

Semiconductor layer 38 may include any of the materials described throughout this application in connection with either of compound semiconductor material layer 26 or additional buffer layer 32. For example, layer 38 may include monocrystalline Group IV or monocrystalline compound semiconductor materials.

In accordance with one embodiment of the present invention, semiconductor layer 38 serves as an anneal cap during layer 36 formation and as a template for subsequent semiconductor layer 26 formation. Accordingly, layer 38 is preferably thick enough to provide a suitable template for layer 26 growth (at least one monolayer) and thin enough to allow layer 38 to form as a substantially defect free monocrystalline semiconductor compound.

In accordance with another embodiment of the invention, semiconductor layer 38 comprises compound semiconductor material (*e.g.*, a material discussed above in connection with compound semiconductor layer 26) that is thick enough to form devices within layer 38. In this case, a semiconductor structure in accordance with the present invention does not include compound semiconductor layer 26. In other words, the semiconductor structure in accordance with this embodiment only includes one compound semiconductor layer disposed above amorphous oxide layer 36.

The layer formed on substrate 22, whether it includes only accommodating buffer layer 24, accommodating buffer layer 24 with amorphous intermediate or interface layer 28, an amorphous layer such as layer 36 formed by annealing layers

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24 and 28 as described above in connection with FIG. 3, or template layer 30, may be referred to generically as an "accommodating layer."

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20, 40 and 34 in accordance with various alternative embodiments. These examples are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

10 In accordance with one embodiment, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. Silicon substrate 22 can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment, accommodating buffer layer 24 is a
15 monocrystalline layer of $\text{Sr}_z\text{Ba}_{1-z}\text{TiO}_3$ where z ranges from 0 to 1 and amorphous intermediate layer 28 is a layer of silicon oxide (SiO_x) formed at the interface between silicon substrate 22 and accommodating buffer layer 24. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. Accommodating buffer
20 layer 24 can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a thickness of about 5 nm. In general, it is desired to have an accommodating buffer layer 24 thick enough to isolate monocrystalline material layer 26 from substrate 22 to obtain the desired electrical and optical properties. Layers thicker than 100 nm usually provide little additional benefit while
25 increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer 28 of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1-2 nm.

In accordance with this embodiment, compound semiconductor material layer 26 is a layer of gallium arsenide (GaAs) or aluminum gallium arsenide
30 (AlGaAs) having a thickness of about 1 nm to about 100 micrometers (μm) and preferably a thickness of about 0.5 μm to 10 μm . The thickness generally depends

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on the application for which the layer is being prepared. To facilitate the epitaxial growth of the gallium arsenide or aluminum gallium arsenide on the monocrystalline oxide, a template layer 30 is formed by capping the oxide layer. Template layer 30 is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or
5 Sr-Al-O. By way of a preferred example, 1-2 monolayers 30 of Ti-As or Sr-Ga-O have been shown to successfully grow GaAs layers 26.

Example 2

10 In accordance with a further embodiment, monocrystalline substrate 22 is a silicon substrate as described above. Accommodating buffer layer 24 is a monocrystalline oxide of strontium or barium zirconate or hafnate in a cubic or orthorhombic phase with an amorphous intermediate layer 28 of silicon oxide formed at the interface between silicon substrate 22 and accommodating buffer
15 layer 24. Accommodating buffer layer 24 can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline SrZrO_3 , BaZrO_3 , SrHfO_3 , BaSnO_3 or BaHfO_3 . For example, a monocrystalline oxide layer of BaZrO_3 can grow at a temperature of about 700 degrees C. The lattice structure of the resulting
20 crystalline oxide exhibits a 45 degree rotation with respect to the substrate 22 silicon lattice structure.

An accommodating buffer layer 24 formed of these zirconate or hafnate materials is suitable for the growth of compound semiconductor materials 26 in the indium phosphide (InP) system. The compound semiconductor material 26 can be,
25 for example, indium phosphide (InP), indium gallium arsenide (InGaAs), aluminum indium arsenide, (AlInAs), or aluminum gallium indium arsenic phosphide (AlGaInAsP), having a thickness of about 1.0 nm to 10 μm . A suitable template 30 for this structure is 1-10 monolayers of zirconium-arsenic (Zr-As), zirconium-phosphorus (Zr-P), hafnium-arsenic (Hf-As), hafnium-phosphorus (Hf-
30 P), strontium-oxygen-arsenic (Sr-O-As), strontium-oxygen-phosphorus (Sr-O-P), barium-oxygen-arsenic (Ba-O-As), indium-strontium-oxygen (In-Sr-O), or barium-

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oxygen-phosphorus (Ba-O-P), and preferably 1-2 monolayers of one of these materials. By way of an example, for a barium zirconate accommodating buffer layer 24, the surface is terminated with 1-2 monolayers of zirconium followed by deposition of 1-2 monolayers of arsenic to form a Zr-As template 30. A
5 monocrystalline layer 26 of the compound semiconductor material from the indium phosphide system is then grown on template layer 30. The resulting lattice structure of the compound semiconductor material 26 exhibits a 45 degree rotation with respect to the accommodating buffer layer 24 lattice structure and a lattice mismatch to (100) InP of less than 2.5%, and preferably less than about 1.0%.

10

Example 3

In accordance with a further embodiment, a structure is provided that is suitable for the growth of an epitaxial film of a II-VI material overlying a silicon substrate 22. The substrate 22 is preferably a silicon wafer as described above. A
15 suitable accommodating buffer layer 24 material is $\text{Sr}_x\text{Ba}_{1-x}\text{TiO}_3$, where x ranges from 0 to 1, having a thickness of about 2-100 nm and preferably a thickness of about 5-15 nm. The II-VI compound semiconductor material 26 can be, for example, zinc selenide (ZnSe) or zinc sulfur selenide (ZnSSe). A suitable template 30 for this material system includes 1-10 monolayers of zinc-oxygen (Zn-
20 O) followed by 1-2 monolayers of an excess of zinc followed by the selenidation of zinc on the surface. Alternatively, a template 30 can be, for example, 1-10 monolayers of strontium-sulfur (Sr-S) followed by the ZnSeS.

25

Example 4

This embodiment of the invention is an example of structure 40 illustrated in FIG. 2. Substrate 22, monocrystalline oxide layer 24, and monocrystalline compound semiconductor material layer 26 can be similar to those described in example 1. In addition, an additional buffer layer 32 serves to alleviate any strains
30 that might result from a mismatch of the crystal lattice of the accommodating

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buffer layer and the lattice of the monocrystalline semiconductor material. The additional buffer layer 32 can be a layer of germanium or a GaAs, an aluminum gallium arsenide (AlGaAs), an indium gallium phosphide (InGaP), an aluminum gallium phosphide (AlGaP), an indium gallium arsenide (InGaAs), an aluminum indium phosphide (AlInP), a gallium arsenide phosphide (GaAsP), or an indium gallium phosphide (InGaP) strain compensated superlattice. In accordance with one aspect of this embodiment, buffer layer 32 includes a $\text{GaAs}_x\text{P}_{1-x}$ superlattice, wherein the value of x ranges from 0 to 1. In accordance with another aspect, buffer layer 32 includes an $\text{In}_y\text{Ga}_{1-y}\text{P}$ superlattice, wherein the value of y ranges from 0 to 1. By varying the value of x or y , as the case may be, the lattice constant is varied from bottom to top across the superlattice to create a match between lattice constants of the underlying oxide and the overlying compound semiconductor material. The compositions of other materials, such as those listed above, may also be similarly varied to manipulate the lattice constant of layer 32 in a like manner. The superlattice can have a thickness of about 50-500 nm and preferably has a thickness of about 100-200 nm. The template for this structure can be the same of that described in example 1. Alternatively, buffer layer 32 can be a layer of monocrystalline germanium having a thickness of 1-50 nm and preferably having a thickness of about 2-20 nm. In using a germanium buffer layer, a template layer of either germanium-strontium (Ge-Sr) or germanium-titanium (Ge-Ti) having a thickness of about one monolayer can be used as a nucleating site for the subsequent growth of the monocrystalline compound semiconductor material layer. The formation of the oxide layer is capped with either a monolayer of strontium or a monolayer of titanium to act as a nucleating site for the subsequent deposition of the monocrystalline germanium. The monolayer of strontium or titanium provides a nucleating site to which the first monolayer of germanium can bond.

Example 5

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This example also illustrates materials useful in a structure 40 as illustrated in FIG. 2. Substrate material 22, accommodating buffer layer 24, monocrystalline compound semiconductor material layer 26 and template layer 30 can be the same as those described above in example 2. In addition, a buffer layer 32 is inserted
5 between accommodating buffer layer 24 and overlying monocrystalline compound semiconductor material layer 26. Buffer layer 32, a further monocrystalline semiconductor material, can be, for example, a graded layer of indium gallium arsenide (InGaAs) or indium aluminum arsenide (InAlAs). In accordance with one aspect of this embodiment, buffer layer 32 includes InGaAs, in which the indium
10 composition varies from 0 to about 50%. The additional buffer layer 32 preferably has a thickness of about 10-30 nm. Varying the composition of buffer layer 32 from GaAs to InGaAs serves to provide a lattice match between the underlying monocrystalline oxide material 24 and the overlying layer 26 of monocrystalline compound semiconductor material. Such a buffer layer 32 is especially
15 advantageous if there is a lattice mismatch between accommodating buffer layer 24 and monocrystalline compound semiconductor material layer 26.

Example 6

20 This example provides exemplary materials useful in structure 34, as illustrated in FIG. 3. Substrate material 22, template layer 30, and monocrystalline compound semiconductor material layer 26 may be the same as those described above in connection with example 1.

Amorphous layer 36 is an amorphous oxide layer which is suitably formed
25 of a combination of amorphous intermediate layer materials (e.g., layer 28 materials as described above) and accommodating buffer layer materials (e.g., layer 24 materials as described above). For example, amorphous layer 36 may include a combination of SiO_x and $\text{Sr}_z\text{Ba}_{1-z}\text{TiO}_3$ (where z ranges from 0 to 1), which combine or mix, at least partially, during an anneal process to form
30 amorphous oxide layer 36.

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The thickness of amorphous layer 36 may vary from application to application and may depend on such factors as desired insulating properties of layer 36, type of semiconductor material comprising layer 26, and the like. In accordance with one exemplary aspect of the present embodiment, layer 36
5 thickness is about 2 nm to about 100 nm, preferably about 2-10 nm, and more preferably about 5-6 nm.

Layer 38 comprises a monocrystalline compound semiconductor material that can be grown epitaxially over a monocrystalline oxide material such as material used to form accommodating buffer layer 24. In accordance with one
10 embodiment of the invention, layer 38 includes the same materials as those comprising layer 26. For example, if layer 26 includes GaAs, layer 38 also includes GaAs. However, in accordance with other embodiments of the present invention, layer 38 may include materials different from those used to form layer 26. In accordance with one exemplary embodiment of the invention, layer 38 is
15 about 1 monolayer to about 100 nm thick.

Referring again to FIGS. 1-3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar manner, accommodating buffer layer 24 is also a
20 monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of accommodating buffer layer 24 and monocrystalline substrate 22 must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a substantial match in
25 lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 4 illustrates graphically the relationship of the achievable thickness of
30 a grown crystal layer of high crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 42

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illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that tend to be polycrystalline. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material 24 by 45° with respect to the crystal orientation of the silicon substrate wafer 22. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer 24 that might result from any mismatch in the lattice constants of the host silicon wafer 22 and the grown titanate layer 24. As a result, a high quality, thick, monocrystalline titanate layer 24 is achievable.

Still referring to FIGS. 1-3, layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, accommodating buffer layer 24 must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, monocrystalline accommodating buffer layer 24, and grown crystal 26 is desired. With properly selected materials this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of grown crystal 26 with respect to the orientation of host crystal 24. If grown crystal 26 is gallium arsenide, aluminum gallium arsenide, zinc selenide, or zinc sulfur selenide

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and accommodating buffer layer 24 is monocrystalline $\text{Sr}_x\text{Ba}_{1-x}\text{TiO}_3$, substantial matching of crystal lattice constants of the two materials is achieved, wherein the crystal orientation of grown layer 26 is rotated by 45° with respect to the orientation of the host monocrystalline oxide 24. Similarly, if host material 24 is a strontium or barium zirconate or a strontium or barium hafnate or barium tin oxide and compound semiconductor layer 26 is indium phosphide or gallium indium arsenide or aluminum indium arsenide, substantial matching of crystal lattice constants can be achieved by rotating the orientation of grown crystal layer 26 by 45° with respect to host oxide crystal 24. In some instances, a crystalline semiconductor buffer layer 32 between host oxide 24 and grown compound semiconductor layer 26 can be used to reduce strain in grown monocrystalline compound semiconductor layer 26 that might result from small differences in lattice constants. Better crystalline quality in grown monocrystalline compound semiconductor layer 26 can thereby be achieved.

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The following example illustrates a process, in accordance with one embodiment, for fabricating a semiconductor structure such as the structures depicted in FIGS. 1-3. The process starts by providing a monocrystalline semiconductor substrate 22 comprising silicon or germanium. In accordance with a preferred embodiment, semiconductor substrate 22 is a silicon wafer having a (100) orientation. Substrate 22 is preferably oriented on axis or, at most, about 4° off axis. At least a portion of semiconductor substrate 22 has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of substrate 22 has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate, although such a grown oxide is not essential to the process. In order to epitaxially grow a monocrystalline oxide layer 24 overlying monocrystalline substrate 22, the native oxide layer must first be removed to expose the crystalline structure of

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underlying substrate 22. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of
5 strontium and barium, or other alkaline earth metals or combinations of alkaline earth metals in an MBE apparatus. In the case where strontium is used, the substrate 22 is then heated to a temperature of about 750°C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which
10 exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer 24 of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer 24.

In accordance with an alternate embodiment, the native silicon oxide can be
15 converted and the surface of substrate 22 can be prepared for the growth of a monocrystalline oxide layer 24 by depositing an alkaline earth metal oxide, such as strontium oxide or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature a solid state reaction takes place between the strontium
20 oxide and the native silicon oxide causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate 22 surface. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer 24.

Following the removal of the silicon oxide from the surface of substrate 22,
25 the substrate is cooled to a temperature in the range of about 200-800°C and a layer 24 of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium, titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a
30 minimum value to grow stoichiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial

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pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer 28 at the interface between underlying substrate 22 and the growing strontium titanate layer 24. The growth of silicon oxide layer 28 results from the diffusion of oxygen through the growing strontium titanate layer 24 to the interface where the oxygen reacts with silicon at the surface of underlying substrate 22. The strontium titanate grows as an ordered (100) monocrystal 24 with the (100) crystalline orientation rotated by 45° with respect to the underlying substrate 22. Strain that otherwise might exist in strontium titanate layer 24 because of the small mismatch in lattice constant between silicon substrate 22 and the growing crystal 24 is relieved in amorphous silicon oxide intermediate layer 28.

After strontium titanate layer 24 has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer 30 that is conducive to the subsequent growth of an epitaxial layer of a desired compound semiconductor material 26. For the subsequent growth of a layer 26 of gallium arsenide, the MBE growth of strontium titanate monocrystalline layer 24 can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-2 monolayers of strontium-oxygen. Following the formation of this capping layer, arsenic is deposited to form a Ti-As bond, a Ti-O-As bond or a Sr-O-As. Any of these form an appropriate template 30 for deposition and formation of a gallium arsenide monocrystalline layer 26. Following the formation of template 30, gallium is subsequently introduced to the reaction with the arsenic and gallium arsenide 26 forms. Alternatively, gallium can be deposited on the capping layer to form a Sr-O-Ga bond, and arsenic is subsequently introduced with the gallium to form the GaAs.

FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the present invention. Single crystal SrTiO₃ accommodating buffer layer 24 was grown epitaxially on silicon substrate 22. During this growth process, amorphous interfacial layer 28 is formed which relieves strain due to lattice mismatch. GaAs compound semiconductor layer 26 was then grown epitaxially using template layer 30.

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FIG. 6 illustrates an x-ray diffraction spectrum taken on a structure including GaAs compound semiconductor layer 26 grown on silicon substrate 22 using accommodating buffer layer 24. The peaks in the spectrum indicate that both the accommodating buffer layer 24 and GaAs compound semiconductor layer 26 are single crystal and (100) orientated.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an additional buffer layer 32 deposition step. The additional buffer layer 32 is formed overlying template layer 30 before the deposition of monocrystalline compound semiconductor layer 26. If additional buffer layer 32 is a compound semiconductor superlattice, such a superlattice can be deposited, by MBE for example, on the template 30 described above. If instead additional buffer layer 32 is a layer of germanium, the process above is modified to cap strontium titanate monocrystalline layer 24 with a final layer of either strontium or titanium and then by depositing germanium to react with the strontium or titanium. The germanium buffer layer 32 can then be deposited directly on this template 30.

Structure 34, illustrated in FIG. 3, may be formed by growing an accommodating buffer layer, forming an amorphous oxide layer over substrate 22, and growing semiconductor layer 38 over the accommodating buffer layer, as described above. The accommodating buffer layer and the amorphous oxide layer are then exposed to an anneal process sufficient to change the crystalline structure of the accommodating buffer layer from monocrystalline to amorphous, thereby forming an amorphous layer such that the combination of the amorphous oxide layer and the now amorphous accommodating buffer layer form a single amorphous oxide layer 36. Layer 26 is then subsequently grown over layer 38. Alternatively, the anneal process may be carried out subsequent to growth of layer 26.

In accordance with one aspect of this embodiment, layer 36 is formed by exposing substrate 22, the accommodating buffer layer, the amorphous oxide layer, and semiconductor layer 38 to a rapid thermal anneal process with a peak temperature of about 700°C to about 1000°C and a process time of about 5 seconds

to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For example, laser annealing or "conventional" thermal annealing processes (in the proper environment) may be used to form layer 36.

5 When conventional thermal annealing is employed to form layer 36, an overpressure of one or more constituents of layer 30 may be required to prevent degradation of layer 38 during the anneal process. For example, when layer 38 includes GaAs, the anneal environment preferably includes an overpressure of arsenic to mitigate degradation of layer 38.

10 As noted above, layer 38 of structure 34 may include any materials suitable for either of layers 32 or 26. Accordingly, any deposition or growth methods described in connection with either layer 32 or 26, may be employed to deposit layer 38.

FIG. 7 is a high resolution Transmission Electron Micrograph (TEM) of
15 semiconductor material manufactured in accordance with the embodiment of the invention illustrated in FIG. 3. In accordance with this embodiment, a single crystal SrTiO₃ accommodating buffer layer was grown epitaxially on silicon substrate 22. During this growth process, an amorphous interfacial layer forms as described above. Next, GaAs layer 38 is formed above the accommodating buffer
20 layer and the accommodating buffer layer is exposed to an anneal process to form amorphous oxide layer 36.

FIG. 8 illustrates an x-ray diffraction spectrum taken on a structure including GaAs compound semiconductor layer 38 and amorphous oxide layer 36 formed on silicon substrate 22. The peaks in the spectrum indicate that GaAs
25 compound semiconductor layer 38 is single crystal and (100) orientated and the lack of peaks around 40 to 50 degrees indicates that layer 36 is amorphous.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate 22, an overlying oxide layer, and a monocrystalline gallium arsenide compound semiconductor layer 26 by the
30 process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor

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deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like. Further, by a similar process, other monocrystalline accommodating buffer layers 24 such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other III-V and II-VI monocrystalline compound semiconductor layers 26 can be deposited overlying monocrystalline oxide accommodating buffer layer 24.

Each of the variations of compound semiconductor materials 26 and monocrystalline oxide accommodating buffer layer 24 uses an appropriate template 30 for initiating the growth of the compound semiconductor layer. For example, if accommodating buffer layer 24 is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by the deposition of arsenic or phosphorus to react with the zirconium as a precursor to depositing indium gallium arsenide, indium aluminum arsenide, or indium phosphide respectively. Similarly, if monocrystalline oxide accommodating buffer layer 24 is an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium. The deposition of hafnium is followed by the deposition of arsenic or phosphorous to react with the hafnium as a precursor to the growth of an indium gallium arsenide, indium aluminum arsenide, or indium phosphide layer 26, respectively. In a similar manner, strontium titanate 24 can be capped with a layer of strontium or strontium and oxygen, and barium titanate 24 can be capped with a layer of barium or barium and oxygen. Each of these depositions can be followed by the deposition of arsenic or phosphorus to react with the capping material to form a template 30 for the deposition of a compound semiconductor material layer 26 comprising indium gallium arsenide, indium aluminum arsenide, or indium phosphide.

The formation of a device structure in accordance with another embodiment of the invention is illustrated schematically in cross-section in FIGs.

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9-12. Like the previously described embodiments referred to in FIGs. 1-3, this embodiment of the invention involves the process of forming a compliant substrate utilizing the epitaxial growth of single crystal oxides, such as the formation of accommodating buffer layer 24 previously described with reference to FIGs. 1 and 2 and amorphous layer 36 previously described with reference to FIG. 3, and the formation of a template layer 30. However, the embodiment illustrated in FIGs. 9-12 utilizes a template that includes a surfactant to facilitate layer-by-layer monocrystalline material growth.

Turning now to FIG. 9, an amorphous intermediate layer 58 is grown on substrate 52 at the interface between substrate 52 and a growing accommodating buffer layer 54, which is preferably a monocrystalline crystal oxide layer, by the oxidation of substrate 52 during the growth of layer 54. Layer 54 is preferably a monocrystalline oxide material such as a monocrystalline layer of $\text{Sr}_z\text{Ba}_{1-z}\text{TiO}_3$ where z ranges from 0 to 1. However, layer 54 may also comprise any of those compounds previously described with reference to layer 24 in FIGs. 1-2 and any of those compounds previously described with reference to layer 36 in FIG. 3 which is formed from layers 24 and 28 referenced in FIGs. 1 and 2.

Layer 54 is grown with a strontium (Sr) terminated surface represented in FIG. 9 by hatched line 55 which is followed by the addition of a template layer 60 which includes a surfactant layer 61 and capping layer 63 as illustrated in FIGs. 10 and 11. Surfactant layer 61 may comprise, but is not limited to, elements such as Al, In and Ga, but will be dependent upon the composition of layer 54 and the overlying layer of monocrystalline material for optimal results. In one exemplary embodiment, aluminum (Al) is used for surfactant layer 61 and functions to modify the surface and surface energy of layer 54. Preferably, surfactant layer 61 is epitaxially grown, to a thickness of one to two monolayers, over layer 54 as illustrated in FIG. 10 by way of molecular beam epitaxy (MBE), although other epitaxial processes may also be performed including chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the like.

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Surfactant layer 61 is then exposed to a Group V element such as arsenic, for example, to form capping layer 63 as illustrated in FIG. 11. Surfactant layer 61 may be exposed to a number of materials to create capping layer 63 such as elements which include, but are not limited to, As, P, Sb and N. Surfactant layer 61 and capping layer 63 combine to form template layer 60.

Monocrystalline material layer 66, which in this example is a compound semiconductor such as GaAs, is then deposited via MBE, CVD, MOCVD, MEE, ALE, PVD, CSD, PLD, or the like to form the final structure illustrated in FIG. 12.

FIGs. 13-16 illustrate possible molecular bond structures for a specific example of a compound semiconductor structure formed in accordance with the embodiment of the invention illustrated in FIGs. 9-12. More specifically, FIGs. 13-16 illustrate the growth of GaAs (layer 66) on the strontium terminated surface of a strontium titanate monocrystalline oxide (layer 54) using a surfactant containing template (layer 60).

The growth of a monocrystalline material layer 66 such as GaAs on an accommodating buffer layer 54 such as a strontium titanium oxide over amorphous interface layer 58 and substrate layer 52, both of which may comprise materials previously described with reference to layers 28 and 22, respectively in FIGs. 1 and 2, illustrates a critical thickness of about 1000 Angstroms where the two-dimensional (2D) and three-dimensional (3D) growth shifts because of the surface energies involved. In order to maintain a true layer by layer growth (Frank Van der Mere growth), the following relationship must be satisfied:

$$\delta_{\text{STO}} > (\delta_{\text{INT}} + \delta_{\text{GaAs}})$$

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where the surface energy of the monocrystalline oxide layer 54 must be greater than the surface energy of the amorphous interface layer 58 added to the surface energy of the GaAs layer 66. Since it is impracticable to satisfy this equation, a surfactant containing template was used, as described above with reference to FIGs. 10-12, to increase the surface energy of the monocrystalline

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oxide layer 54 and also to shift the crystalline structure of the template to a diamond-like structure that is in compliance with the original GaAs layer.

FIG. 13 illustrates the molecular bond structure of a strontium terminated surface of a strontium titanate monocrystalline oxide layer. An aluminum
5 surfactant layer is deposited on top of the strontium terminated surface and bonds with that surface as illustrated in FIG. 14, which reacts to form a capping layer comprising a monolayer of Al_2Sr having the molecular bond structure illustrated in FIG. 14 which forms a diamond-like structure with an sp^3 hybrid terminated surface that is compliant with compound semiconductors such as GaAs. The
10 structure is then exposed to As to form a layer of AlAs as shown in FIG. 15. GaAs is then deposited to complete the molecular bond structure illustrated in FIG. 16 which has been obtained by 2D growth. The GaAs can be grown to any thickness for forming other semiconductor structures, devices, or integrated circuits. Alkaline earth metals such as those in Group IIA are those elements preferably
15 used to form the capping surface of the monocrystalline oxide layer 54 because they are capable of forming a desired molecular structure with aluminum.

In this embodiment, a surfactant containing template layer aids in the formation of a compliant substrate for the monolithic integration of various material layers including those comprised of Group III-V compounds to form high
20 quality semiconductor structures, devices and integrated circuits. For example, a surfactant containing template may be used for the monolithic integration of a monocrystalline material layer such as a layer comprising Germanium (Ge), for example, to form high efficiency photocells.

Turning now to FIGs. 17-20, the formation of a device structure in
25 accordance with still another embodiment of the invention is illustrated in cross-section. This embodiment utilizes the formation of a compliant substrate which relies on the epitaxial growth of single crystal oxides on silicon followed by the epitaxial growth of single crystal silicon onto the oxide.

An accommodating buffer layer 74 such as a monocrystalline oxide layer is
30 first grown on a substrate layer 72, such as silicon, with an amorphous interface layer 78 as illustrated in FIG. 17. Monocrystalline oxide layer 74 may be

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comprised of any of those materials previously discussed with reference to layer 24 in FIGs. 1 and 2, while amorphous interface layer 78 is preferably comprised of any of those materials previously described with reference to the layer 28 illustrated in FIGs. 1 and 2. Substrate 72, although preferably silicon, may also
5 comprise any of those materials previously described with reference to substrate 22 in FIGs. 1-3.

Next, a silicon layer 81 is deposited over monocrystalline oxide layer 74 via MBE, CVD, MOCVD, MEE, ALE, PVD, CSD, PLD, and the like as illustrated in FIG. 18 with a thickness of a few hundred Angstroms but preferably with a
10 thickness of about 50 Angstroms. Monocrystalline oxide layer 74 preferably has a thickness of about 20 to 100 Angstroms.

Rapid thermal annealing is then conducted in the presence of a carbon source such as acetylene or methane, for example at a temperature within a range of about 800°C to 1000°C to form capping layer 82 and silicate amorphous layer
15 86. However, other suitable carbon sources may be used as long as the rapid thermal annealing step functions to amorphize the monocrystalline oxide layer 74 into a silicate amorphous layer 86 and carbonize the top silicon layer 81 to form capping layer 82 which in this example would be a silicon carbide (SiC) layer as illustrated in FIG. 19. The formation of amorphous layer 86 is similar to the
20 formation of layer 36 illustrated in FIG. 3 and may comprise any of those materials described with reference to layer 36 in FIG. 3 but the preferable material will be dependent upon the capping layer 82 used for silicon layer 81.

Finally, a compound semiconductor layer 96, shown in FIG. 20, such as gallium nitride (GaN) is grown over the SiC surface by way of MBE, CVD,
25 MOCVD, MEE, ALE, PVD, CSD, PLD, or the like to form a high quality compound semiconductor material for device formation. More specifically, the deposition of GaN and GaN based systems such as GaInN and AlGaIn will result in the formation of dislocation nets confined at the silicon/amorphous region. The resulting nitride containing compound semiconductor material may comprise
30 elements from groups III, IV and V of the periodic table and is defect free.

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Although GaN has been grown on SiC substrate in the past, this embodiment of the invention possesses a one step formation of the compliant substrate containing a SiC top surface and an amorphous layer on a Si surface. More specifically, this embodiment of the invention uses an intermediate single
5 crystal oxide layer that is amorphized to form a silicate layer which adsorbs the strain between the layers. Moreover, unlike past use of a SiC substrate, this embodiment of the invention is not limited by wafer size which is usually less than 50mm in diameter for prior art SiC substrates.

The monolithic integration of nitride containing semiconductor compounds
10 containing group III-V nitrides and silicon devices can be used for high temperature RF applications and optoelectronics. GaN systems have particular use in the photonic industry for the blue/green and UV light sources and detection. High brightness light emitting diodes (LEDs) and lasers may also be formed within the GaN system.

15 FIGs. 21-23 schematically illustrate, in cross-section, the formation of another embodiment of a device structure in accordance with the invention. This embodiment includes a compliant layer that functions as a transition layer that uses clathrate or Zintl type bonding. More specifically, this embodiment utilizes an intermetallic template layer to reduce the surface energy of the interface between
20 material layers thereby allowing for two dimensional layer by layer growth.

The structure illustrated in FIG. 21 includes a monocrystalline substrate 102, an amorphous interface layer 108 and an accommodating buffer layer 104. Amorphous interface layer 108 is formed on substrate 102 at the interface between substrate 102 and accommodating buffer layer 104 as previously described with
25 reference to FIGs. 1 and 2. Amorphous interface layer 108 may comprise any of those materials previously described with reference to amorphous interface layer 28 in FIGs. 1 and 2. Substrate 102 is preferably silicon but may also comprise any of those materials previously described with reference to substrate 22 in FIGs. 1-3.

A template layer 130 is deposited over accommodating buffer layer 104 as
30 illustrated in FIG. 22 and preferably comprises a thin layer of Zintl type phase material composed of metals and metalloids having a great deal of ionic character.

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As in previously described embodiments, template layer 130 is deposited by way of MBE, CVD, MOCVD, MEE, ALE, PVD, CSD, PLD, or the like to achieve a thickness of one monolayer. Template layer 130 functions as a "soft" layer with non-directional bonding but high crystallinity which absorbs stress build up
5 between layers having lattice mismatch. Materials for template 130 may include, but are not limited to, materials containing Si, Ga, In, and Sb such as, for example, AlSr_2 , $(\text{MgCaYb})\text{Ga}_2$, $(\text{Ca,Sr,Eu,Yb})\text{In}_2$, BaGe_2As , and SrSn_2As_2 .

A monocrystalline material layer 126 is epitaxially grown over template layer 130 to achieve the final structure illustrated in FIG. 23. As a specific
10 example, an SrAl_2 layer may be used as template layer 130 and an appropriate monocrystalline material layer 126 such as a compound semiconductor material GaAs is grown over the SrAl_2 . The Al-Ti (from the accommodating buffer layer of layer of $\text{Sr}_z\text{Ba}_{1-z}\text{TiO}_3$ where z ranges from 0 to 1) bond is mostly metallic while the Al-As (from the GaAs layer) bond is weakly covalent. The Sr participates in
15 two distinct types of bonding with part of its electric charge going to the oxygen atoms in the lower accommodating buffer layer 104 comprising $\text{Sr}_z\text{Ba}_{1-z}\text{TiO}_3$ to participate in ionic bonding and the other part of its valence charge being donated to Al in a way that is typically carried out with Zintl phase materials. The amount of the charge transfer depends on the relative electronegativity of elements
20 comprising the template layer 130 as well as on the interatomic distance. In this example, Al assumes an sp^3 hybridization and can readily form bonds with monocrystalline material layer 126, which in this example, comprises compound semiconductor material GaAs.

The compliant substrate produced by use of the Zintl type template layer
25 used in this embodiment can absorb a large strain without a significant energy cost. In the above example, the bond strength of the Al is adjusted by changing the volume of the SrAl_2 layer thereby making the device tunable for specific applications which include the monolithic integration of III-V and Si devices and the monolithic integration of high-k dielectric materials for CMOS technology.

30 Clearly, those embodiments specifically describing structures having compound semiconductor portions and Group IV semiconductor portions, are

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meant to illustrate embodiments of the present invention and not limit the present invention. There are a multiplicity of other combinations and other embodiments of the present invention. For example, the present invention includes structures and methods for fabricating material layers which form semiconductor structures, devices and integrated circuits including other layers such as metal and non-metal layers. More specifically, the invention includes structures and methods for forming a compliant substrate which is used in the fabrication of semiconductor structures, devices and integrated circuits and the material layers suitable for fabricating those structures, devices, and integrated circuits. By using embodiments of the present invention, it is now simpler to integrate devices that include monocrystalline layers comprising semiconductor and compound semiconductor materials as well as other material layers that are used to form those devices with other components that work better or are easily and/or inexpensively formed within semiconductor or compound semiconductor materials. This allows a device to be shrunk, the manufacturing costs to decrease, and yield and reliability to increase.

In accordance with one embodiment of this invention, a monocrystalline semiconductor or compound semiconductor wafer can be used in forming monocrystalline material layers over the wafer. In this manner, the wafer is essentially a "handle" wafer used during the fabrication of semiconductor electrical components within a monocrystalline layer overlying the wafer. Therefore, electrical components can be formed within semiconductor materials over a wafer of at least approximately 200 millimeters in diameter and possibly at least approximately 300 millimeters.

By the use of this type of substrate, a relatively inexpensive "handle" wafer overcomes the fragile nature of compound semiconductor or other monocrystalline material wafers by placing them over a relatively more durable and easy to fabricate base material. Therefore, an integrated circuit can be formed such that all electrical components, and particularly all active electronic devices, can be formed within or using the monocrystalline material layer even though the substrate itself may include a monocrystalline semiconductor material. Fabrication costs for

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compound semiconductor devices and other devices employing non-silicon monocrystalline materials should decrease because larger substrates can be processed more economically and more readily compared to the relatively smaller and more fragile substrates (e.g. conventional compound semiconductor wafers).

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FIG. 24 illustrates schematically, in cross section, a device structure 50 in accordance with a further embodiment. Device structure 50 includes a monocrystalline semiconductor substrate 52, preferably a monocrystalline silicon wafer. Monocrystalline semiconductor substrate 52 includes two regions, 53 and 57. An electrical semiconductor component generally indicated by the dashed line 56 is formed, at least partially, in region 53. Electrical component 56 can be a resistor, a capacitor, an active semiconductor component such as a diode or a transistor or an integrated circuit such as a CMOS integrated circuit. For example, electrical semiconductor component 56 can be a CMOS integrated circuit configured to perform digital signal processing or another function for which silicon integrated circuits are well suited. The electrical semiconductor component in region 53 can be formed by conventional semiconductor processing as well known and widely practiced in the semiconductor industry. A layer of insulating material 59 such as a layer of silicon dioxide or the like may overlie electrical semiconductor component 56.

Insulating material 59 and any other layers that may have been formed or deposited during the processing of semiconductor component 56 in region 53 are removed from the surface of region 57 to provide a bare silicon surface in that region. As is well known, bare silicon surfaces are highly reactive and a native silicon oxide layer can quickly form on the bare surface. A layer of barium or barium and oxygen is deposited onto the native oxide layer on the surface of region 57 and is reacted with the oxidized surface to form a first template layer (not shown). In accordance with one embodiment, a monocrystalline oxide layer is formed overlying the template layer by a process of molecular beam epitaxy. Reactants including barium, titanium and oxygen are deposited onto the template layer to form the monocrystalline oxide layer. Initially during the deposition the

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partial pressure of oxygen is kept near the minimum necessary to fully react with the barium and titanium to form monocrystalline barium titanate layer. The partial pressure of oxygen is then increased to provide an overpressure of oxygen and to allow oxygen to diffuse through the growing monocrystalline oxide layer. The oxygen diffusing through the barium titanate reacts with silicon at the surface of region 57 to form an amorphous layer of silicon oxide 62 on second region 57 and at the interface between silicon substrate 52 and the monocrystalline oxide layer 65. Layers 65 and 62 may be subject to an annealing process as described above in connection with FIG. 3 to form a single amorphous accommodating layer.

10 In accordance with an embodiment, the step of depositing the monocrystalline oxide layer 65 is terminated by depositing a second template layer 64, which can be 1-10 monolayers of titanium, barium, barium and oxygen, or titanium and oxygen. A layer 66 of a monocrystalline compound semiconductor material is then deposited overlying second template layer 64 by a process of molecular beam epitaxy. The deposition of layer 66 is initiated by depositing a layer of arsenic onto template 64. This initial step is followed by depositing gallium and arsenic to form monocrystalline gallium arsenide 66. Alternatively, strontium can be substituted for barium in the above example.

20 In accordance with a further embodiment, a semiconductor component, generally indicated by a dashed line 68 is formed in compound semiconductor layer 66. Semiconductor component 68 can be formed by processing steps conventionally used in the fabrication of gallium arsenide or other III-V compound semiconductor material devices. Semiconductor component 68 can be any active or passive component, and preferably is a semiconductor laser, light emitting diode, photodetector, heterojunction bipolar transistor (HBT), high frequency MESFET, or other component that utilizes and takes advantage of the physical properties of compound semiconductor materials. A metallic conductor schematically indicated by the line 70 can be formed to electrically couple device 68 and device 56, thus implementing an integrated device that includes at least one component formed in silicon substrate 52 and one device formed in monocrystalline compound semiconductor material layer 66. Although illustrative

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structure 50 has been described as a structure formed on a silicon substrate 52 and having a barium (or strontium) titanate layer 65 and a gallium arsenide layer 66, similar devices can be fabricated using other substrates, monocrystalline oxide layers and other compound semiconductor layers as described elsewhere in this disclosure.

FIG. 25 illustrates a semiconductor structure 71 in accordance with a further embodiment. Structure 71 includes a monocrystalline semiconductor substrate 73 such as a monocrystalline silicon wafer that includes a region 75 and a region 76. An electrical component schematically illustrated by the dashed line 79 is formed in region 75 using conventional silicon device processing techniques commonly used in the semiconductor industry. Using process steps similar to those described above, a monocrystalline oxide layer 80 and an intermediate amorphous silicon oxide layer 83 are formed overlying region 76 of substrate 73. A template layer 84 and subsequently a monocrystalline semiconductor layer 87 are formed overlying monocrystalline oxide layer 80. In accordance with a further embodiment, an additional monocrystalline oxide layer 88 is formed overlying layer 87 by process steps similar to those used to form layer 80, and an additional monocrystalline semiconductor layer 90 is formed overlying monocrystalline oxide layer 88 by process steps similar to those used to form layer 87. In accordance with one embodiment, at least one of layers 87 and 90 are formed from a compound semiconductor material. Layers 80 and 83 may be subject to an annealing process as described above in connection with FIG. 3 to form a single amorphous accommodating layer.

A semiconductor component generally indicated by a dashed line 92 is formed at least partially in monocrystalline semiconductor layer 87. In accordance with one embodiment, semiconductor component 92 may include a field effect transistor having a gate dielectric formed, in part, by monocrystalline oxide layer 88. In addition, monocrystalline semiconductor layer 90 can be used to implement the gate electrode of that field effect transistor. In accordance with one embodiment, monocrystalline semiconductor layer 87 is formed from a group III-V compound and semiconductor component 92 is a radio frequency amplifier that

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takes advantage of the high mobility characteristic of group III-V component materials. In accordance with yet a further embodiment, an electrical interconnection schematically illustrated by the line 94 electrically interconnects component 79 and component 92. Structure 71 thus integrates components that
5 take advantage of the unique properties of the two monocrystalline semiconductor materials.

Attention is now directed to a method for forming exemplary portions of illustrative composite semiconductor structures or composite integrated circuits like 50 or 71. In particular, the illustrative composite semiconductor
10 structure or integrated circuit 103 shown in FIGs. 26-30 includes a compound semiconductor portion 1022, a bipolar portion 1024, and a MOS portion 1026. In FIG. 26, a p-type doped, monocrystalline silicon substrate 110 is provided having a compound semiconductor portion 1022, a bipolar portion 1024, and an MOS
portion 1026. Within bipolar portion 1024, the monocrystalline
15 silicon substrate 110 is doped to form an N^+ buried region 1102. A lightly p-type doped epitaxial monocrystalline silicon layer 1104 is then formed over the buried region 1102 and the substrate 110. A doping step is then performed to create a lightly n-type doped drift region 1117 above the N^+ buried region 1102. The doping step converts the dopant type of the lightly p-type epitaxial layer within a
20 section of the bipolar region 1024 to a lightly n-type monocrystalline silicon region. A field isolation region 1106 is then formed between and around the bipolar portion 1024 and the MOS portion 1026. A gate dielectric layer 1110 is formed over a portion of the epitaxial layer 1104 within MOS portion 1026, and the gate electrode 1112 is then formed over the gate dielectric layer 1110.
25 Sidewall spacers 1115 are formed along vertical sides of the gate electrode 1112 and gate dielectric layer 1110.

A p-type dopant is introduced into the drift region 1117 to form an active or intrinsic base region 1114. An n-type, deep collector region 1108 is then formed within the bipolar portion 1024 to allow electrical connection to the buried region
30 1102. Selective n-type doping is performed to form N^+ doped regions 1116 and the emitter region 1120. N^+ doped regions 1116 are formed within layer 1104

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along adjacent sides of the gate electrode 1112 and are source, drain, or source/drain regions for the MOS transistor. The N⁺ doped regions 1116 and emitter region 1120 have a doping concentration of at least 1E19 atoms per cubic centimeter to allow ohmic contacts to be formed. A p-type doped region is formed
5 to create the inactive or extrinsic base region 1118 which is a P⁺ doped region (doping concentration of at least 1E19 atoms per cubic centimeter).

In the embodiment described, several processing steps have been performed but are not illustrated or further described, such as the formation of well regions, threshold adjusting implants, channel punchthrough prevention implants,
10 field punchthrough prevention implants, as well as a variety of masking layers. The formation of the device up to this point in the process is performed using conventional steps. As illustrated, a standard N-channel MOS transistor has been formed within the MOS region 1026, and a vertical NPN bipolar transistor has been formed within the bipolar portion 1024. Although illustrated with a NPN
15 bipolar transistor and a N-channel MOS transistor, device structures and circuits in accordance with various embodiments may additionally or alternatively include other electronic devices formed using the silicon substrate. As of this point, no circuitry has been formed within the compound semiconductor portion 1022.

After the silicon devices are formed in regions 1024 and 1026, a protective
20 layer 1122 is formed overlying devices in regions 1024 and 1026 to protect devices in regions 1024 and 1026 from potential damage resulting from device formation in region 1022. Layer 1122 may be formed of, for example, an insulating material such as silicon oxide or silicon nitride. All of the layers that have been formed during the processing of the bipolar and MOS portions of the integrated circuit,
25 except for epitaxial layer 1104 but including protective layer 1122, are now removed from the surface of compound semiconductor portion 1022. A bare silicon surface is thus provided for the subsequent processing of this portion, for example in the manner set forth above.

An accommodating buffer layer 124 is then formed over the substrate 110
30 as illustrated in FIG. 27. The accommodating buffer layer will form as a monocrystalline layer over the properly prepared (i.e., having the appropriate

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template layer) bare silicon surface in portion 1022. The portion of layer 124 that forms over portions 1024 and 1026, however, may be polycrystalline or amorphous because it is formed over a material that is not monocrystalline, and therefore, does not nucleate monocrystalline growth. The accommodating buffer layer 124

5 typically is a monocrystalline metal oxide or nitride layer and typically has a thickness in a range of approximately 2-100 nanometers. In one particular embodiment, the accommodating buffer layer is approximately 5-15 nm thick. During the formation of the accommodating buffer layer, an amorphous intermediate layer 122 is formed along the uppermost silicon surfaces of the

10 integrated circuit 103. This amorphous intermediate layer 122 typically includes an oxide of silicon and has a thickness and range of approximately 1-5 nm. In one particular embodiment, the thickness is approximately 2 nm. Following the formation of the accommodating buffer layer 124 and the amorphous intermediate layer 122, a template layer 125 is then formed and has a thickness in a range of

15 approximately one to ten monolayers of a material. In one particular embodiment, the material includes titanium-arsenic, strontium-oxygen-arsenic, or other similar materials as previously described with respect to FIGS. 1-5.

A monocrystalline compound semiconductor layer 132 is then epitaxially grown overlying the monocrystalline portion of accommodating

20 buffer layer 124 as shown in FIG. 28. The portion of layer 132 that is grown over portions of layer 124 that are not monocrystalline may be polycrystalline or amorphous. The compound semiconductor layer can be formed by a number of methods and typically includes a material such as gallium arsenide, aluminum gallium arsenide, indium phosphide, or other

25 compound semiconductor materials as previously mentioned. The thickness of the layer is in a range of approximately 1-5,000 nm, and more preferably 100-2000 nm. Furthermore, additional monocrystalline layers may be formed above layer 132, as discussed in more detail below in connection with FIGS. 31-32.

30 In this particular embodiment, each of the elements within the template layer are also present in the accommodating buffer layer 124, the monocrystalline

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compound semiconductor material 132, or both. Therefore, the delineation between the template layer 125 and its two immediately adjacent layers disappears during processing. Therefore, when a transmission electron microscopy (TEM) photograph is taken, an interface between the accommodating buffer layer 124 and the monocrystalline compound semiconductor layer 132 is seen.

After at least a portion of layer 132 is formed in region 1022, layers 122 and 124 may be subject to an annealing process as described above in connection with FIG. 3 to form a single amorphous accommodating layer. If only a portion of layer 132 is formed prior to the anneal process, the remaining portion may be deposited onto structure 103 prior to further processing.

At this point in time, sections of the compound semiconductor layer 132 and the accommodating buffer layer 124 (or of the amorphous accommodating layer if the annealing process described above has been carried out) are removed from portions overlying the bipolar portion 1024 and the MOS portion 1026 as shown in FIG. 29. After the section of the compound semiconductor layer and the accommodating buffer layer 124 are removed, an insulating layer 142 is formed overprotective layer 1122. The insulating layer 142 can include a number of materials such as oxides, nitrides, oxynitrides, low-k dielectrics, or the like. As used herein, low-k is a material having a dielectric constant no higher than approximately 3.5. After the insulating layer 142 has been deposited, it is then polished or etched to remove portions of the insulating layer 142 that overlie monocrystalline compound semiconductor layer 132.

A transistor 144 is then formed within the monocrystalline compound semiconductor portion 1022. A gate electrode 148 is then formed on the monocrystalline compound semiconductor layer 132. Doped regions 146 are then formed within the monocrystalline compound semiconductor layer 132. In this embodiment, the transistor 144 is a metal-semiconductor field-effect transistor (MESFET). If the MESFET is an n-type MESFET, the doped regions 146 and at least a portion of monocrystalline compound semiconductor layer 132 are also n-type doped. If a p-type MESFET were to be formed, then the doped regions 146 and at least a portion of monocrystalline compound semiconductor layer 132

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would have just the opposite doping type. The heavier doped (N^+) regions 146 allow ohmic contacts to be made to the monocrystalline compound semiconductor layer 132. At this point in time, the active devices within the integrated circuit have been formed. Although not illustrated in the drawing figures, additional processing steps such as formation of well regions, threshold adjusting implants, channel punchthrough prevention implants, field punchthrough prevention implants, and the like may be performed in accordance with the present invention. This particular embodiment includes an n-type MESFET, a vertical NPN bipolar transistor, and a planar n-channel MOS transistor. Many other types of transistors, including P-channel MOS transistors, p-type vertical bipolar transistors, p-type MESFETs, and combinations of vertical and planar transistors, can be used. Also, other electrical components, such as resistors, capacitors, diodes, and the like, may be formed in one or more of the portions 1022, 1024, and 1026.

Processing continues to form a substantially completed integrated circuit 103 as illustrated in FIG. 30. An insulating layer 152 is formed over the substrate 110. The insulating layer 152 may include an etch-stop or polish-stop region that is not illustrated in FIG. 30. A second insulating layer 154 is then formed over the first insulating layer 152. Portions of layers 154, 152, 142, 124, and 1122 are removed to define contact openings where the devices are to be interconnected. Interconnect trenches are formed within insulating layer 154 to provide the lateral connections between the contacts. As illustrated in FIG. 30, interconnect 1562 connects a source or drain region of the n-type MESFET within portion 1022 to the deep collector region 1108 of the NPN transistor within the bipolar portion 1024. The emitter region 1120 of the NPN transistor is connected to one of the doped regions 1116 of the n-channel MOS transistor within the MOS portion 1026. The other doped region 1116 is electrically connected to other portions of the integrated circuit that are not shown. Similar electrical connections are also formed to couple regions 1118 and 1112 to other regions of the integrated circuit.

A passivation layer 156 is formed over the interconnects 1562, 1564, and 1566 and insulating layer 154. Other electrical connections are made to the transistors as illustrated as well as to other electrical or electronic components

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within the integrated circuit 103 but are not illustrated in the FIGS. Further, additional insulating layers and interconnects may be formed as necessary to form the proper interconnections between the various components within the integrated circuit 103.

5 As can be seen from the previous embodiment, active devices for both compound semiconductor and Group IV semiconductor materials can be integrated into a single integrated circuit. Because there is some difficulty in incorporating both bipolar transistors and MOS transistors within a same integrated circuit, it may be possible to move some of the components within bipolar portion 1024 into
10 the compound semiconductor portion 1022 or the MOS portion 1026. Therefore, the requirement of special fabricating steps solely used for making a bipolar transistor can be eliminated. Therefore, there would only be a compound semiconductor portion and a MOS portion to the integrated circuit.

 In still another embodiment, an integrated circuit can be formed such that it
15 includes an optical laser in a compound semiconductor portion and an optical interconnect (waveguide) to a MOS transistor within a Group IV semiconductor region of the same integrated circuit. FIGs. 31-37 include illustrations of one embodiment.

 FIG. 31 includes an illustration of a cross-section view of a portion of an
20 integrated circuit 160 that includes a monocrystalline silicon wafer 161. An amorphous intermediate layer 162 and an accommodating buffer layer 164, similar to those previously described, have been formed over wafer 161. Layers 162 and 164 may be subject to an annealing process as described above in connection with FIG. 3 to form a single amorphous accommodating layer. In this specific
25 embodiment, the layers needed to form the optical laser will be formed first, followed by the layers needed for the MOS transistor. In FIG. 31, the lower mirror layer 166 includes alternating layers of compound semiconductor materials. For example, the first, third, and fifth films within the optical laser may include a material such as gallium arsenide, and the second, fourth, and sixth films within
30 the lower mirror layer 166 may include aluminum gallium arsenide or vice versa. Layer 168 includes the active region that will be used for photon generation.

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Upper mirror layer 170 is formed in a similar manner to the lower mirror layer 166 and includes alternating films of compound semiconductor materials. In one particular embodiment, the upper mirror layer 170 may be p-type doped compound semiconductor materials, and the lower mirror layer 166 may be n-type doped compound semiconductor materials.

Another accommodating buffer layer 172, similar to the accommodating buffer layer 164, is formed over the upper mirror layer 170. In an alternative embodiment, the accommodating buffer layers 164 and 172 may include different materials. However, their function is essentially the same in that each is used for making a transition between a compound semiconductor layer and a monocrystalline Group IV semiconductor layer. Layer 172 may be subject to an annealing process as described above in connection with FIG. 3 to form an amorphous accommodating layer. A monocrystalline Group IV semiconductor layer 174 is formed over the accommodating buffer layer 172. In one particular embodiment, the monocrystalline Group IV semiconductor layer 174 includes germanium, silicon germanium, silicon germanium carbide, or the like.

In FIG. 32, the MOS portion is processed to form electrical components within this upper monocrystalline Group IV semiconductor layer 174. As illustrated in FIG. 32, a field isolation region 171 is formed from a portion of layer 174. A gate dielectric layer 173 is formed over the layer 174, and a gate electrode 175 is formed over the gate dielectric layer 173. Doped regions 177 are source, drain, or source/drain regions for the transistor 181, as shown. Sidewall spacers 179 are formed adjacent to the vertical sides of the gate electrode 175. Other components can be made within at least a part of layer 174. These other components include other transistors (n-channel or p-channel), capacitors, transistors, diodes, and the like.

A monocrystalline Group IV semiconductor layer is epitaxially grown over one of the doped regions 177. An upper portion 184 is P+ doped, and a lower portion 182 remains substantially intrinsic (undoped) as illustrated in FIG. 32. The layer can be formed using a selective epitaxial process. In one embodiment, an insulating layer (not shown) is formed over the transistor 181 and the field

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isolation region 171. The insulating layer is patterned to define an opening that exposes one of the doped regions 177. At least initially, the selective epitaxial layer is formed without dopants. The entire selective epitaxial layer may be intrinsic, or a p-type dopant can be added near the end of the formation of the selective epitaxial layer. If the selective epitaxial layer is intrinsic, as formed, a
5 doping step may be formed by implantation or by furnace doping. Regardless how the P+ upper portion 184 is formed, the insulating layer is then removed to form the resulting structure shown in FIG. 32.

 The next set of steps is performed to define the optical laser 180 as
10 illustrated in FIG. 33. The field isolation region 171 and the accommodating buffer layer 172 are removed over the compound semiconductor portion of the integrated circuit. Additional steps are performed to define the upper mirror layer 170 and active layer 168 of the optical laser 180. The sides of the upper mirror layer 170 and active layer 168 are substantially coterminous.

15 Contacts 186 and 188 are formed for making electrical contact to the upper mirror layer 170 and the lower mirror layer 166, respectively, as shown in FIG. 33. Contact 186 has an annular shape to allow light (photons) to pass out of the upper mirror layer 170 into a subsequently formed optical waveguide.

 An insulating layer 190 is then formed and patterned to define optical
20 openings extending to the contact layer 186 and one of the doped regions 177 as shown in FIG. 34. The insulating material can be any number of different materials, including an oxide, nitride, oxynitride, low-k dielectric, or any combination thereof. After defining the openings 192, a higher refractive index material 202 is then formed within the openings to fill them and to deposit the
25 layer over the insulating layer 190 as illustrated in FIG. 35. With respect to the higher refractive index material 202, "higher" is in relation to the material of the insulating layer 190 (i.e., material 202 has a higher refractive index compared to the insulating layer 190). Optionally, a relatively thin lower refractive index film (not shown) could be formed before forming the higher refractive index material
30 202. A hard mask layer 204 is then formed over the high refractive index layer 202. Portions of the hard mask layer 204, and high refractive index layer 202 are

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removed from portions overlying the opening and to areas closer to the sides of FIG. 35.

The balance of the formation of the optical waveguide, which is an optical interconnect, is completed as illustrated in FIG. 36. A deposition procedure
5 (possibly a dep-etch process) is performed to effectively create sidewall sections 212. In this embodiment, the sidewall sections 212 are made of the same material as material 202. The hard mask layer 204 is then removed, and a low refractive index layer 214 (low relative to material 202 and layer 212) is formed over the higher refractive index material 212 and 202 and exposed portions of the insulating
10 layer 190. The dash lines in FIG. 36 illustrate the border between the high refractive index materials 202 and 212. This designation is used to identify that both are made of the same material but are formed at different times.

Processing is continued to form a substantially completed integrated circuit as illustrated in FIG. 37. A passivation layer 220 is then formed over the optical
15 laser 180 and MOSFET transistor 181. Although not shown, other electrical or optical connections are made to the components within the integrated circuit but are not illustrated in FIG. 37. These interconnects can include other optical waveguides or may include metallic interconnects.

In other embodiments, other types of lasers can be formed. For example,
20 another type of laser can emit light (photons) horizontally instead of vertically. If light is emitted horizontally, the MOSFET transistor could be formed within the substrate 161, and the optical waveguide would be reconfigured, so that the laser is properly coupled (optically connected) to the transistor. In one specific embodiment, the optical waveguide can include at least a portion of the
25 accommodating buffer layer. Other configurations are possible.

Clearly, these embodiments of integrated circuits having compound semiconductor portions and Group IV semiconductor portions, are meant to illustrate what can be done and are not intended to be exhaustive of all possibilities or to limit what can be done. There is a multiplicity of other possible
30 combinations and embodiments. For example, the compound semiconductor portion may include light emitting diodes, photodetectors, diodes, or the like, and

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the Group IV semiconductor can include digital logic, memory arrays, and most structures that can be formed in conventional MOS integrated circuits. By using what is shown and described herein, it is now simpler to integrate devices that work better in compound semiconductor materials with other components that work better in Group IV semiconductor materials. This allows a device to be shrunk, the manufacturing costs to decrease, and yield and reliability to increase.

Although not illustrated, a monocrystalline Group IV wafer can be used in forming only compound semiconductor electrical components over the wafer. In this manner, the wafer is essentially a "handle" wafer used during the fabrication of the compound semiconductor electrical components within a monocrystalline compound semiconductor layer overlying the wafer. Therefore, electrical components can be formed within III-V or II-VI semiconductor materials over a wafer of at least approximately 200 millimeters in diameter and possibly at least approximately 300 millimeters.

By the use of this type of substrate, a relatively inexpensive "handle" wafer overcomes the fragile nature of the compound semiconductor wafers by placing them over a relatively more durable and easy to fabricate base material. Therefore, an integrated circuit can be formed such that all electrical components, and particularly all active electronic devices, can be formed within the compound semiconductor material even though the substrate itself may include a Group IV semiconductor material. Fabrication costs for compound semiconductor devices should decrease because larger substrates can be processed more economically and more readily, compared to the relatively smaller and more fragile, conventional compound semiconductor wafers.

A composite integrated circuit may include components that provide electrical isolation when electrical signals are applied to the composite integrated circuit. The composite integrated circuit may include a pair of optical components, such as an optical source component and an optical detector component. An optical source component may be a light generating semiconductor device, such as an optical laser (e.g., the optical laser illustrated in FIG. 33), a photo emitter, a diode, etc. An optical detector component may be a light-sensitive semiconductor

junction device, such as a photodetector, a photodiode, a bipolar junction, a transistor, etc.

A composite integrated circuit may include processing circuitry that is formed at least partly in the Group IV semiconductor portion of the composite integrated circuit. The processing circuitry is configured to communicate with
5 circuitry external to the composite integrated circuit. The processing circuitry may be electronic circuitry, such as a microprocessor, RAM, logic device, decoder, etc.

For the processing circuitry to communicate with external electronic circuitry, the composite integrated circuit may be provided with electrical signal
10 connections to the external electronic circuitry. The composite integrated circuit may also have internal optical communications connections for connecting the processing circuitry in the composite integrated circuit to the electrical connections with the external circuitry. Optical components in the composite integrated circuit may provide the optical communications connections which may electrically
15 isolate the electrical signals in the communications connections from the processing circuitry. Together, the electrical and optical communications connections may be for communicating information, such as data, control, timing, etc.

A pair of optical components (an optical source component and an optical
20 detector component) in the composite integrated circuit may be configured to pass information. Information that is received or transmitted between the optical pair may be from or for the electrical communications connection between the processing circuitry and the external circuitry while providing electrical isolation for the processing circuitry. If desired, a plurality of optical component pairs may
25 be included in the composite integrated circuit for providing a plurality of communications connections and for providing isolation. For example, a composite integrated circuit receiving a plurality of data bits may include a pair of optical components for communication of each data bit.

In operation, for example, an optical source component in a pair of
30 components may be configured to generate light (e.g., photons) based on receiving electrical signals from an electrical signal connection with the external circuitry.

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An optical detector component in the pair of components may be optically connected to the source component to generate electrical signals based on detecting light generated by the optical source component. Information that is communicated between the source and detector components may be digital or
5 analog.

If desired the reverse of this configuration may be used. An optical source component that is responsive to the on-board processing circuitry may be coupled to an optical detector component to have the optical source component generate an electrical signal for use in communications with external circuitry. A plurality of
10 such optical component pair structures may be used for providing two-way connections. In some applications where synchronization is desired, a first pair of optical components may be coupled to provide data communications and a second pair may be coupled for communications synchronization information.

For clarity and brevity, optical detector components that are discussed
15 below are discussed primarily in the context of optical detector components that have been formed in a compound semiconductor portion of a composite integrated circuit. In application, the optical detector component may be formed in many suitable ways (e.g., formed from silicon, etc.).

A composite integrated circuit will typically have an electric connection for
20 a power supply and a ground connection. The power and ground connections are in addition to the communications connections that are discussed above.

Processing circuitry in a composite integrated circuit may include electrically isolated communications connections and include electrical connections for power and ground. In most known applications, power supply and ground connections
25 are usually well-protected by circuitry to prevent harmful external signals from reaching the composite integrated circuit. A communications ground may be isolated from the ground signal in communications connections that use a ground communications signal.

An integrated communications device that includes differing types of
30 semiconductors, which are suitable for different communications functions, is provided based on the processes and structures discussed herein in combination

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with processes and structures that are known to those skilled in the art. Non-compound semiconductor devices that are suitable for functions such as digital signal processing are preferably integrated in a single integrated circuit or die with compound semiconductors that are suitable for functions such as data conversion or optical signal handling. For example, a compound semiconductor analog-to-digital or digital-to-analog data converter is integrated with a silicon processor in a composite semiconductor structure in providing an integrated communications circuit.

With reference now to FIG. 38, an electrical block diagram shows composite semiconductor structure 302 that is for providing an integrated communications circuit in accordance with an embodiment. Composite semiconductor structure 302 has a monolithic structure that preferably includes communications transceiver circuitry 304, data converter circuitry 306, and processor circuitry 308. Composite semiconductor structure 302 includes compound semiconductor regions and non-compound semiconductor regions that are integrated together in the composite semiconductor structure 302. Communications transceiver circuitry 304, data converter circuitry 306, and processor circuitry 308 are formed using both compound semiconductor regions and non-compound semiconductor regions in composite semiconductor structure 302 in a way that best suits the functions of individual circuit components or groups of circuit components. In communications transceiver circuitry 304, functions such as the transmission or reception of optical communications signals or high frequency (e.g., 1-100Ghz) radio frequency signals are implemented using compound semiconductors such as monocrystalline Group III-V semiconductor materials. In communications transceiver circuitry 304, non-compound semiconductor materials such as monocrystalline Group IV semiconductors (e.g., silicon) are preferably used in providing low frequency transmission or reception functionality. Data converter circuitry 306 of composite semiconductor structure 302 includes compound semiconductor circuitry that is suitable for high frequency operation and has close matching of threshold voltages or transient responses.

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Other circuitry may be included in composite semiconductor structure 302 for providing additional functionality.

Communications transceiver circuitry 304 may be a receiver that substantially comprises compound semiconductor circuit components, non-compound semiconductor circuit components, or a combination of compound and non-compound semiconductor circuit components. Communications transceiver circuitry 304 as a receiver preferably receives and operates on a transmitted signal to deliver an analog domain signal for data converter circuitry 306. Communications transceiver circuitry 304 as a receiver preferably includes a demodulator, an amplifier, a filter, a phase locked loop, and other elements of a receiver as needed or desired. Communications transceiver circuitry 304 as a receiver preferably receives a transmitted signal that is directly representative of information that is sought to be conveyed (e.g., information that is transmitted in an electrical or optical signal with modulation, coding, or other signal transmission processing techniques).

Communications transceiver circuitry 304 may be a transmitter that substantially comprises compound semiconductor circuit components, non-compound semiconductor circuit components, or a combination of compound and non-compound semiconductor circuit components. Communications transceiver circuitry 304 as a transmitter may operate on analog domain signals to transmit communications signals that are based on the analog domain signals. Communications transceiver circuitry 304 as a transmitter preferably includes a modulator, an oscillator, an amplifier, a filter, or other elements of a transmitter as needed or desired. In one embodiment, communications transceiver circuitry 304 comprises both a transmitter and a receiver.

Data converter circuitry 306 of composite semiconductor structure 302 may receive an analog domain signal from communications transceiver circuitry 304. In this embodiment, data converter circuitry 306 preferably includes an analog-to-digital data converter that converts the analog domain signal to a digital domain signal. The analog-to-digital data converter preferably includes one or more comparators used in performing a comparison to determine a signal level of the

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analog domain signal. The comparators are preferably compound semiconductor comparators that are implemented to perform the comparison using compound semiconductor transistors such as heterojunction bipolar transistors that have properties such as closely matched threshold voltage and high frequency cutoff.

5 Data converter circuitry 306 of composite semiconductor structure 302 may receive a digital domain signal from processing circuitry 308. Data converter circuitry 306 preferably includes a digital-to-analog data converter that converts the digital domain signal to an analog domain signal. In this embodiment, the digital-to-analog data converter preferably includes one or more switches used in
10 selecting an appropriate voltage or current level for the analog domain signal. The level is selected to be representative of the information in the digital domain signal. The level is selected from a range of differing levels that are available for the analog domain signal. The switches are preferably compound semiconductor switches that are implemented to perform the selection using compound
15 semiconductor transistors such as heterojunction bipolar transistors that have properties such as matched transient characteristics and high frequency cutoff. In one embodiment, data converter circuitry 306 includes both an analog-to-digital converter and a digital-to-analog converter.

 In one embodiment, composite semiconductor structure 302 is a single
20 structure that includes data converter circuitry 306 and processor circuitry 308, but does not include communications transceiver circuitry 304. In another embodiment, composite semiconductor structure 302 is a single structure that includes data converter circuitry 306 and communications transceiver circuitry 304, but does not include processor circuitry 308. In yet another embodiment,
25 composite semiconductor structure 302 is a single structure that includes data converter circuitry 306, but does not include communications transceiver circuitry 304 and processor circuitry 308.

 Processor circuitry 308 of composite semiconductor structure 302 receives digital domain signals from data converter circuitry 306 when data converter
30 circuitry is serving as an analog-to-digital converter. Processor circuitry 308 of composite semiconductor structure 302 generates digital domain signals for data

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converter circuitry 306 when data converter circuitry is serving as a digital-to-analog converter. Processor circuitry 308 preferably includes a processor and/or other processing devices that are formed from a non-compound semiconductor, which are better suited for operating on information in a digital domain than
5 processors or processing devices that are made from compound semiconductors.

Advantages of such composite semiconductor structures that combine processing circuitry formed substantially from compound semiconductors and data converter circuitry formed substantially from compound semiconductors may include the appropriate matching of communications circuit functions with suitable
10 semiconductor technologies. The advantages may also include a reduction in packaging parasitics and a reduction in manufacturing costs that is due to the essentially monolithic characteristic of the composite semiconductor structure.

As described above, composite semiconductor structure 302 includes a semiconductor layer that may comprise a plurality of layers that are formed to
15 integrate compound semiconductor regions with non-compound semiconductor regions in the same structure (e.g., see FIGs. 1-3, 9-12, and 17-23). For example, in FIG. 23 the semiconductor layer includes a template layer, an accommodating buffer layer, and an amorphous layer.

Communications transceiver circuitry 304 in one embodiment is
20 communications circuitry that is to provide optical signal communications. For example, with reference now to FIG. 39, composite semiconductor structure 310 is for providing optical signal communications. Composite semiconductor structure 310 includes optical receiver circuitry 312, analog-to-digital data converter circuitry 314, and processing circuitry 316. Optical receiver circuitry
25 312 comprises compound semiconductor circuit elements for receiving and processing optical signals. Optical receiver circuitry 312 converts a received optical signal to an analog domain signal for use in composite semiconductor structure 310.

The analog domain signal is provided to analog-to-digital data converter
30 314, which may include compound semiconductor comparators, to convert the analog domain signal to a digital domain signal. The digital domain signal is

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provided to processor circuitry 316, which may include a non-compound semiconductor processor, to operate on information that is carried in the digital domain signal in digital format. As mentioned above, processors formed from non-compound semiconductor materials are particularly suitable for processing or
5 operating on information in digital form.

Communications transceiver circuitry in a composite semiconductor structure, such as communications circuitry 304 of composite semiconductor structure of FIG. 38, is, in another embodiment, for providing electrical signal communications. For example, with reference now to FIG. 40, composite
10 semiconductor structure 318 may include communications circuitry for electrical signal communications. Composite semiconductor structure 318 preferably includes electrical receiver circuitry 320, analog-to-digital data converter circuitry 322, and processor circuitry 324. Electrical receiver circuitry 320 may include compound semiconductor devices when electrical receiver circuitry 320 is to
15 receive and handle high frequency electrical input signals such as radio frequency electrical input signals. For low frequency electrical signal communications, electrical receiver circuitry 320 preferably includes non-compound semiconductor circuit elements, which are more suitable for low frequency electrical signal applications than compound semiconductor circuit elements. Electrical receiver
20 circuitry 320 receives a transmitted electrical signal on which electrical receiver circuitry 320 may operate to provide an analog domain signal.

Analog-to-digital data converter circuitry 322 receives the analog domain signal from electrical receiver circuitry 320. Analog-to-digital data converter circuitry 322 converts the analog domain signal to a digital domain signal.
25 Analog-to-digital data converter circuitry 322 includes an analog-to-digital data converter. The analog-to-digital data converter is preferably formed substantially or entirely from compound semiconductors. For example, the analog-to-digital data converter comprises compound semiconductor heterojunction bipolar transistors for implementing comparators in the analog-to-digital data converter.

30 Processor circuitry 324 receives the digital domain signal from analog-to-digital data converter circuitry 322 to process the information that is carried by the

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digital domain signal. Processor circuitry 324 includes circuit elements that are formed from non-compound semiconductor materials, which are materials that are better suited for digital signal processing than compound semiconductor materials. Processor circuitry 324 may include a processor, a microprocessor, or other
5 processing circuitry suitable for implementing digital algorithms.

The data converter circuitry for converting information between analog and digital domains is included in a composite semiconductor structure that is used for providing a communications device. The data converter circuitry is preferably formed to have a high sampling rate by forming the data converter circuitry from
10 compound semiconductor components. For example, with reference now to FIG. 41, data converter circuitry 326 includes analog-to-digital data converter 328 and data-converter-related circuitry 334. At a high level of design, analog-to-digital data converter 328 is preferably a conventional analog-to-digital data converter. However, at a lower level (at which transistor material types are determined) the
15 design technique in accordance with the present invention uniquely selects transistors fabricated in a semiconductor material selected for optimization of circuit performance and cost. For example, analog-to-digital data converter 328 can be a conventional high-speed flash analog-to-digital data converter. Analog-to-digital data converter 328 may include one or more compound semiconductor
20 comparators 330. The performance of analog-to-digital data converter 328 is typically substantially tied to the performance of compound semiconductor comparators 330 that are used in the analog-to-digital data converter 328 to compare the signal level of analog domain signals to a reference signal level. Compound semiconductor comparators can typically operate at high frequencies.
25 Thus, compound semiconductor data converter 330 may be formed substantially from compound semiconductor materials and may include some components that are formed from non-compound semiconductor materials.

Analog-to-digital data converter 328 typically includes other data converter circuitry 332 such as encoders, counters, gated clocks, resistors, capacitors,
30 conductors, etc. Other data converter circuitry 332 may be formed from compound semiconductor materials, non-compound semiconductor materials, or a

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combination thereof. Data-converter-related circuitry 334 is circuitry external to analog-to-digital data converter 328 that is used in implementing analog-to-digital data converter 328.

Data converter circuitry 326 preferably includes a comparator such as compound semiconductor comparator 336 of FIG. 42. With reference now to FIG. 42, comparator 336 has an analog voltage input 338 and a reference voltage input 342. The reference voltage input 342 is preferably set to a constant level but may vary over time depending on the design of the data converter in which comparator 336 is implemented. Comparator 336 has a comparator output 340 that is an output signal that is based on a comparison of analog voltage input 338 and reference voltage input 342. Comparator 336 may include compound semiconductor transistors that are used to perform a comparison between analog voltage input 338 and reference voltage input 342. Some or all of the compound semiconductor transistors in comparator 336 may be heterojunction bipolar transistors. If desired, other compound semiconductor transistors may also be used. Techniques and structures for forming comparators by coupling transistors are known to those skilled in the art. However, as described above, the semiconductor materials used for each transistor are selected in accordance with the present invention to optimize circuit performance and cost.

As mentioned above, a comparator may include compound semiconductor heterojunction bipolar transistors such as compound semiconductor heterojunction bipolar transistor 344 of FIG. 43 to implement a comparison function. With reference now to FIG. 43, compound semiconductor heterojunction bipolar transistor 344 includes emitter 346, base 348, and collector 350. Compound semiconductor heterojunction bipolar transistor 344 is formed from two types of compound semiconductors. For example, compound semiconductor heterojunction bipolar transistor 344 is formed from gallium arsenide and aluminum gallium arsenide (AlGaAs). Base 348 and collector 350 are formed from gallium arsenide. Emitter 346 is formed from gallium arsenide and aluminum gallium arsenide (e.g., aluminum gallium arsenide region 352 of emitter 346). Emitter 346, collector 350, and base 348 include contacts as shown in FIG. 43. Compound semiconductor

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heterojunction bipolar transistor 344 may include implant damage regions 354 and oxygen-implanted regions 356.

Other compound semiconductor heterojunction bipolar transistor structures may also be used. For example, with reference now to FIG. 44, compound
5 semiconductor heterojunction bipolar transistor 358 includes buffer layer 360 formed over supporting layer 362, subcollector layer 364, collector layer 378, base layer 368, emitter layer 372, and emitter cap layer 374. Compound semiconductor heterojunction bipolar transistor 358 further includes collector electrode 366, base
electrode 370, and emitter electrode 376. Collector electrode 366 is preferably
10 made of a material different from that of emitter electrode 376 and base electrode 370.

Structures such as compound semiconductor transistors, comparators that include compound semiconductor transistors, data converters that include such comparators, and integrated communications circuits that use such data converters
15 may be formed using techniques illustratively described herein, using techniques known to those skilled in the art, or using a combination thereof.

Illustrative steps involved in providing and operating integrated communications circuits are shown in FIG. 45. At step 380, a composite semiconductor structure (e.g., a single composite semiconductor structure) is
20 formed that includes, among other things, a layer that is used in integrating compound and non-compound semiconductor devices in the structure. The layer relieves strains that may be caused due to a mismatch in the crystalline structure of the compound and non-compound semiconductors. Step 380 preferably includes steps 388, 390, and 392. At step 388, receiver circuitry is formed in forming the
25 composite semiconductor structure. As mentioned above, the receiver circuitry may be formed to include compound semiconductor circuitry (e.g., circuitry for handling optical signals or high frequency electrical signals), non-compound semiconductor circuitry (e.g., circuitry for handling low frequency electrical signals), or both.

30 At step 390, data converter circuitry is formed in forming the composite semiconductor structure. For example, as described above, data converter circuitry

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may be formed that includes compound semiconductor circuitry that allows for a high sampling rate and high speed operation. Data converter circuitry may be formed to include one or more compound semiconductor comparators, one or more comparators that are formed from compound semiconductor transistors (e.g.,
5 compound semiconductor heterojunction bipolar transistors) or combinations thereof. At step 392, processor circuitry is formed in forming the composite semiconductor structure. The processor circuitry may include non-compound semiconductor circuitry that is suitable for operating on digital information signals (e.g., low frequency digital signals). For example, non-compound semiconductor
10 circuitry may include a non-compound semiconductor processor (e.g., a silicon processor).

At step 382, analog domain signals are received. The receiver circuitry may receive the analog domain signals in a transmitted signal (e.g., electrical or optical signals). The receiver circuitry operates on the transmitted signal to
15 provide the analog domain signals. The analog domain signals are preferably received directly at the data converter circuitry. The analog domain signals embody information. At step 384, the analog domain signals are converted to digital domain signals. The conversion is performed by the data converter circuitry. At step 386, the digital domain signal is operated on using non-
20 compound semiconductor devices that are part of the processor circuitry. The combination of using compound semiconductor devices (e.g., a compound semiconductor heterojunction bipolar transistor) in converting data from analog to digital form and using non-compound semiconductor devices (e.g., a non-
25 compound semiconductor processor) in processing transmitted information that is converted from analog to digital allows for high speed operation of a communications device.

As mentioned above, communications transceiver circuitry (e.g., communications transceiver circuitry 304 of FIG. 38) may include a transmitter. The communications transceiver circuitry can be communications circuitry that is
30 to provide optical signal communications. For example, with reference now to FIG. 46, composite semiconductor structure 410 is for providing optical signal

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communications. Composite semiconductor structure 410 includes optical transmitter circuitry 412, digital-to-analog data converter circuitry 414, and processing circuitry 416. Optical transmitter circuitry 412 preferably comprises compound semiconductor circuit elements for transmitting optical signals, which
5 may include circuit elements for generating optical signals. Optical transmitter circuitry 412 transmits an optical signal that is generated from an analog domain signal from digital-to-analog data converter circuitry 414.

The analog domain signal is preferably provided to optical transmitter circuitry 412 by digital-to-analog data converter 414, which may include
10 compound semiconductor switches, to convert a digital domain signal to an analog domain signal. The digital domain signal is provided to digital-to-analog data converter 414 by processor circuitry 316, which may include a non-compound semiconductor processor, to generate a digital domain signal of information in digital format. As mentioned above, processors formed from non-compound
15 semiconductor materials are particularly suitable for processing or operating on information in digital form.

Communications transceiver circuitry in a composite semiconductor structure, such as communications circuitry 304 of composite semiconductor structure of FIG. 38, may be for transmitting electrical signal communications. For
20 example, with reference now to FIG. 47, composite semiconductor structure 418 includes communications circuitry for electrical signal communications.

Composite semiconductor structure 418 includes electrical transmitter circuitry 420, digital-to-analog data converter circuitry 422, and processor circuitry 424. Electrical transmitter circuitry 420 includes compound semiconductor devices
25 when electrical transmitter circuitry 420 is to transmit and handle high frequency electrical input signals such as radio frequency electrical input signals. For low frequency electrical signal communications, electrical transmitter circuitry 420 may include non-compound semiconductor circuit elements, which are more suitable for low frequency electrical signal applications than compound
30 semiconductor circuit elements. Electrical transmitter circuitry 420 operates on an

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analog domain signal from digital-to-analog data converter circuitry 422 to transmit a communications signal that is based on the analog domain signal.

Digital-to-analog data converter circuitry 422 provides the analog domain signal to electrical transmitter circuitry 420. Digital-to-analog data converter circuitry 422 converts a digital domain signal to provide the analog domain signal.

Digital-to-analog data converter circuitry 422 includes a digital-to-analog data converter. The digital-to-analog data converter may be formed substantially or entirely from compound semiconductors. For example, the digital-to-analog data converter may comprise compound semiconductor heterojunction bipolar transistors for implementing switches in the digital-to-analog data converter.

Processor circuitry 424 provides the digital domain signal to digital-to-analog data converter circuitry 422. Processor circuitry 424 may include circuit elements that are formed from non-compound semiconductor materials, which are materials that are better suited for digital signal processing than compound semiconductor materials. Processor circuitry 424 may include a processor, a microprocessor, or other processing circuitry suitable for implementing digital algorithms.

The data converter circuitry for converting information between analog and digital domains are included in a composite semiconductor structure that is used for providing a communications device. The data converter circuitry is preferably formed to have a high sampling rate or high switching rate by forming the data converter circuitry from compound semiconductor components. For example, with reference now to FIG. 48, data converter circuitry 426 includes digital-to-analog data converter 428 and data-converter-related circuitry 434.

At a high level of design, digital-to-analog data converter 428 is preferably a conventional digital-to-analog data converter. However, at a lower level (at which transistor material types are determined) the design technique in accordance with the present invention uniquely selects transistors fabricated in a semiconductor material selected for optimization of circuit performance and cost. Digital-to-analog data converter 428 may include one or more compound semiconductor switches 430. The performance of digital-to-analog data converter

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428 is typically substantially tied to the performance of compound semiconductor switches 430 that are used in the digital-to-analog data converter 428 to switch between differing analog domain signal levels. Compound semiconductor switches can typically operate at high frequencies and typically operate with a better transient response than non-compound semiconductor switches. Thus, compound semiconductor data converter 428 may be formed substantially from compound semiconductor materials and may include some components that are formed from non-compound semiconductor materials.

Digital-to-analog data converter 428 typically includes other data converter circuitry 432 such as decoders, amplifiers, clocks, resistors, capacitors, conductors, etc. Other data converter circuitry 432 may be formed from compound semiconductor materials, non-compound semiconductor materials, or a combination thereof. Data-converter-related circuitry 434 is circuitry external to digital-to-analog data converter 428 that is used in implementing digital-to-analog data converter 428.

With reference now to FIG. 49, digital-to-analog data converter 442 may include compound semiconductor switches 440. Compound semiconductor switches 440 may be heterojunction bipolar transistors. If desired, other compound semiconductor transistors may also be used. Digital-to-analog data converter 442 receives digital domain signals 438 that are a plurality of bits (e.g., a digital word) that approximately represent analog information in digital format. Digital-to-analog data converter 442 has a voltage or current reference 436. Digital-to-analog data converter 442 has an output 441 comprising an analog domain signal (e.g., a voltage or current) that is generated based on the bits received on input 438. Compound semiconductor switches 440 are selectively activated based on the bits received on input 438 to generate the analog domain signal. Compound semiconductor switches 440 may be implemented to generate a stepwise variable signal. The high speed operating capabilities of compound semiconductor switches and the transient response characteristics of compound semiconductor switches are particularly suitable for digital-to-analog data conversion functions.

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Techniques and structures for forming switches and for forming digital-to-analog data converters using transistors are known to those skilled in the art.

As mentioned above, compound semiconductor switches 440 may include compound semiconductor heterojunction bipolar transistors such as compound
5 semiconductor heterojunction bipolar transistor 344 of FIG. 43 to implement a switching function. Other compound semiconductor heterojunction bipolar transistor structures may also be used.

Structures such as compound semiconductor transistors, switches that
include compound semiconductor transistors, data converters that include such
10 switches, and integrated communications circuits that use such data converters are formed using techniques illustratively described herein, using techniques known to those skilled in the art, or using a combination thereof.

Illustrative steps involved in providing and operating integrated communications circuits are shown in FIG. 50. At step 480, a composite
15 semiconductor structure (e.g., a single composite semiconductor structure) is formed that includes, among other things, a layer that is used in integrating compound and non-compound semiconductor devices in the structure. The layer relieves strains that may be caused due to a mismatch in the crystalline structure of the compound and non-compound semiconductors. Step 480 preferably includes
20 steps 488, 490, and 492. At step 488, transmitter circuitry is formed in forming the composite semiconductor structure. As mentioned above, the transmitter circuitry may be formed to include compound semiconductor circuitry (e.g., circuitry for handling optical signals or high frequency electrical signals), non-compound semiconductor circuitry (e.g., circuitry for handling low frequency electrical
25 signals), or both.

At step 490, data converter circuitry is formed in forming the composite semiconductor structure. For example, as described above, data converter circuitry may be formed that includes compound semiconductor circuitry that allows for a high sampling rate and high speed operation. Data converter circuitry may be
30 formed to include one or more compound semiconductor switches, one or more switches that are formed from compound semiconductor transistors (e.g.,

compound semiconductor heterojunction bipolar transistors), or combinations thereof. At step 492, processor circuitry is formed in forming the composite semiconductor structure. The processor circuitry may include non-compound semiconductor circuitry that is suitable for operating on digital information signals
5 (e.g., low frequency digital signals). For example, non-compound semiconductor circuitry may include a non-compound semiconductor processor (e.g., a silicon processor).

At step 482, digital domain signals are generated. The digital domain signals may be generated using the processor circuitry (e.g., using non-compound
10 semiconductor devices in the processor circuitry). At step 484, the digital domain signals may be converted to analog domain signals. The conversion may be performed by the data converter circuitry. The analog domain signal may be provided to transmitter circuitry. The transmitter circuitry operates on the analog domain signal and transmits communications signals based on the analog domain
15 signal. The combination of using compound semiconductor devices (e.g., a compound semiconductor heterojunction bipolar transistor) in converting data from digital to analog form and using non-compound semiconductor devices (e.g., a non-compound semiconductor processor) in processing transmitted information that is converted from analog to digital allows for high speed operation of a
20 communications device.

As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements includes not only those elements but may also include other elements not expressly listed or inherent
25 to such process, method, article, or apparatus.

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WHAT IS CLAIMED IS

1. A composite semiconductor structure comprising:
data converter circuitry that converts analog domain signals
carrying information into digital domain signals using compound semiconductor
5 comparator circuitry;
signal processor circuitry that includes non-compound
semiconductor devices that are to operate on the information carried by the digital
domain signals; and
an accommodating layer for integrating together the
10 compound semiconductor comparator circuitry and the non-compound
semiconductor devices in a single die.
2. The composite semiconductor structure of claim 1 wherein the
compound semiconductor comparator circuitry comprises a compound
15 semiconductor comparator.
3. The composite semiconductor structure of claim 2 wherein the
compound semiconductor comparator comprises compound semiconductor
heterojunction bipolar transistors that implement the comparator.
20
4. The composite semiconductor structure of claim 3 wherein the
compound semiconductor heterojunction bipolar transistors are gallium arsenide
heterojunction bipolar transistors.
- 25 5. The composite semiconductor structure of claim 1 wherein the non-
compound semiconductor devices are Group IV monocrystalline semiconductor
devices.
6. The composite semiconductor structure of claim 1 wherein the non-
30 compound semiconductor devices are silicon semiconductor devices.

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7. The composite semiconductor structure of claim 1 further comprising receiver circuitry that receives transmitted signals and uses the transmitted signals that are received to provide the analog domain signals.

5 8. The composite semiconductor structure of claim 7 wherein the receiver circuitry receives the transmitted signals comprising optical signals and provides the analog domain signals based on the optical signals.

9. The composite semiconductor structure of claim 7 wherein the
10 receiver circuitry receives the transmitted signals comprising an electrical signal and provides the analog domain signals based on the electrical signal.

10. A method comprising:
forming a composite semiconductor structure comprising
15 data converter circuitry that includes compound semiconductor comparator circuitry, signal processor circuitry that includes non-compound semiconductor devices, and an accommodating layer that is for integrating together the compound semiconductor comparator circuitry and the non-compound semiconductor devices in that single die;
20 converting analog domain signals carrying information into digital domain signals using the compound semiconductor comparator circuitry;
and
operating on the information carried by the digital domain signals using the non-compound semiconductor devices.

25

11. The method of claim 10 wherein the forming comprises forming the compound semiconductor comparator circuitry to include a compound semiconductor comparator.

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12. The method of claim 11 further comprising implementing the compound semiconductor comparator using compound semiconductor heterojunction bipolar transistors.

5 13. The method of claim 12 wherein the forming comprises forming the compound semiconductor heterojunction bipolar transistors from gallium arsenide.

14. The method of claim 10 wherein the forming comprises forming the non-compound semiconductor devices from a Group IV monocrystalline
10 semiconductor material.

15. The method of claim 10 wherein the forming comprises forming the non-compound semiconductor devices from silicon.

15 16. The method of claim 10 wherein the forming comprises forming receiver circuitry that is to receive transmitted signals and provide the analog domain signals based on the transmitted signals.

17. The method of claim 16 further comprising:
20 using the receiver circuitry to receive the transmitted signals comprising optical signals; and
 providing the analog domain signals based on the optical signals.

25 18. The method of claim 16 further comprising:
 using the receiver circuitry to receive the transmitted signals that comprises electrical signals; and
 providing the analog domain signals based on the electrical signals.

30

19. A semiconductor structure comprising:

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a monocrystalline silicon substrate;
an amorphous oxide material overlying the monocrystalline silicon substrate;
a monocrystalline perovskite oxide material overlying the
5 amorphous oxide material;
a monocrystalline compound semiconductor material overlying the monocrystalline perovskite oxide material;
data converter circuitry that converts an analog domain signal carrying information into a digital domain signal, wherein the data converter
10 circuitry comprises compound semiconductor comparator circuitry formed from the monocrystalline compound semiconductor material for comparing the analog domain signal in providing the digital domain signal; and
signal processor circuitry that includes silicon devices formed from the monocrystalline silicon substrate that are to operate on the
15 information in the digital domain signal.

20. The semiconductor structure of claim 19 wherein the monocrystalline compound semiconductor material is gallium arsenide.

20 21. The semiconductor structure of claim 19 wherein the compound semiconductor comparator circuitry comprises a compound semiconductor comparator.

22. The semiconductor structure of claim 19 wherein the compound
25 semiconductor comparator circuitry comprises a compound semiconductor comparator comprising compound semiconductor heterojunction bipolar transistors for implementing the compound semiconductor comparator.

23. The semiconductor structure of claim 19 further comprising
30 receiver circuitry.

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24. A process for fabricating a semiconductor structure comprising:
providing a monocrystalline silicon substrate;
depositing a monocrystalline perovskite oxide film
overlying the monocrystalline silicon substrate, the film having a thickness less
5 than a thickness of the material that would result in strain-induced defects;
forming an amorphous oxide interface layer containing at
least silicon and oxygen at an interface between the monocrystalline perovskite
oxide film and the monocrystalline silicon substrate;
epitaxially forming a monocrystalline compound
10 semiconductor layer overlying the monocrystalline perovskite oxide film;
forming data converter circuitry that converts an analog
domain signal carrying information into a digital domain signal, wherein the data
converter circuitry comprises compound semiconductor comparator circuitry
formed from the monocrystalline compound semiconductor material for comparing
15 the analog domain signal in providing the digital domain signal; and
forming signal processor circuitry that includes silicon
devices formed from the monocrystalline silicon substrate that are to operate on the
information in the digital domain signal.
- 20 25. The process of claim 24 wherein the epitaxially forming comprises
epitaxially forming a gallium arsenide layer overlying the monocrystalline
perovskite oxide film.
26. The process of claim 24 wherein the forming the data converter
25 circuitry comprises forming the compound semiconductor comparator circuitry to
include a compound semiconductor comparator.
27. The process of claim 24 wherein the forming the data converter
circuitry comprises forming the compound semiconductor comparator circuitry to
30 include a compound semiconductor comparator that comprises compound

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semiconductor heterojunction bipolar transistors for implementing the compound semiconductor comparator.

28. The process of claim 24 further comprising forming receiver
5 circuitry in the semiconductor structure.

29. A composite semiconductor structure comprising:
signal processor circuitry that includes non-compound
semiconductor devices that are to generate digital domain signals representing
10 information;
data converter circuitry that converts the digital domain
signals into an analog domain signal using compound semiconductor switching
circuitry;
and
15 an accommodating layer for integrating together the
compound semiconductor switching circuitry and the non-compound
semiconductor devices in a single die.

30. The composite semiconductor structure of claim 29 wherein the
20 compound semiconductor switching circuitry comprises one or more compound
semiconductor switches.

31. The composite semiconductor structure of claim 30 wherein the
compound semiconductor switches comprising compound semiconductor
25 heterojunction bipolar transistors that implement the compound semiconductor
switches.

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32. The composite semiconductor structure of claim 31 wherein the compound semiconductor heterojunction bipolar transistors are gallium arsenide heterojunction bipolar transistors.

5 33. The composite semiconductor structure of claim 29 wherein the non-compound semiconductor devices are Group IV monocrystalline semiconductor devices.

34. The composite semiconductor structure of claim 29 wherein the
10 non-compound semiconductor devices are silicon semiconductor devices.

35. The composite semiconductor structure of claim 29 further comprising transmitter circuitry that transmits communications signals and uses the analog domain signals to provide the communications signals.

15

36. The composite semiconductor structure of claim 35 wherein the transmitter circuitry transmits the communications signals comprising optical signals that are based on the analog domain signals.

20 37. The composite semiconductor structure of claim 35 wherein the transmitter circuitry transmits the communications signals comprising electrical signals that are based on the analog domain signals.

38. A method comprising:
25 forming a composite semiconductor structure comprising data converter circuitry that includes compound semiconductor switching circuitry, signal processor circuitry that includes non-compound semiconductor devices, and a semiconductor layer that is for integrating together the compound semiconductor switching circuitry and the non-compound semiconductor devices in that single
30 die;

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generating digital domain signals representing information
by using the non-compound semiconductor devices; and
converting the digital domain signals of information into
analog domain signals using the compound semiconductor switching circuitry.

5

39. The method of claim 38 wherein the forming comprises forming the
compound semiconductor switching circuitry to include a plurality of compound
semiconductor switches.

10

40. The method of claim 39 further comprising implementing the
compound semiconductor switches using compound semiconductor heterojunction
bipolar transistors.

15

41. The method of claim 40 wherein the forming comprises forming the
compound semiconductor heterojunction bipolar transistors from gallium arsenide.

20

42. The method of claim 38 wherein the forming comprises forming the
non-compound semiconductor devices from a Group IV monocrystalline
semiconductor material.

43. The method of claim 38 wherein the forming comprises forming the
non-compound semiconductor devices from silicon.

25

44. The method of claim 38 wherein the forming comprises forming
transmitter circuitry that is to transmit communications signals based on the analog
domain signals.

30

45. The method of claim 44 further comprising:
providing the analog domain signals to the transmitter
circuitry; and

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using the transmitter circuitry to transmit the communications signals comprising an optical signal that is based on the analog domain signals.

- 5 46. The method of claim 44 further comprising:
 providing the analog domain signals to the transmitter
 circuitry; and
 using the transmitter circuitry to transmit the
communications signals comprising electrical signals that are based on the analog
10 domain signals.

47. A semiconductor structure comprising:
 a monocrystalline silicon substrate;
 an amorphous oxide material overlying the monocrystalline
15 silicon substrate;
 a monocrystalline perovskite oxide material overlying the
amorphous oxide material;
 a monocrystalline compound semiconductor material
overlying the monocrystalline perovskite oxide material;
20 signal processor circuitry that includes silicon devices
formed from the monocrystalline silicon substrate that are to generate digital
domain signals representing information; and
 data converter circuitry that converts the digital domain
signals of information into analog domain signals, wherein the data converter
25 circuitry comprises compound semiconductor switching circuitry formed from the
monocrystalline compound semiconductor material for switching between different
analog domain signal levels based on the digital domain signals.

48. The semiconductor structure of claim 47 wherein the
30 monocrystalline compound semiconductor material is gallium arsenide.

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49. The semiconductor structure of claim 47 wherein the compound semiconductor switching circuitry comprises a compound semiconductor switch.

50. The semiconductor structure of claim 47 wherein the compound semiconductor switching circuitry comprises a compound semiconductor switch comprising a compound semiconductor heterojunction bipolar transistor for implementing the compound semiconductor switch.

51. The semiconductor structure of claim 47 further comprising transmitter circuitry.

52. A process for fabricating a semiconductor structure comprising:
providing a monocrystalline silicon substrate;
depositing a monocrystalline perovskite oxide film
overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;
forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate;
epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film;
forming signal processor circuitry that includes silicon devices formed from the monocrystalline silicon substrate that are to generate digital domain signals of information; and
forming data converter circuitry that converts the digital domain signals representing information into an analog domain signal, wherein the data converter circuitry comprises compound semiconductor switching circuitry formed from the monocrystalline compound semiconductor material for switching between different analog domain signal levels based on the digital domain signals.

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53. The process of claim 52 wherein the epitaxially forming comprises epitaxially forming a gallium arsenide layer overlying the monocrystalline perovskite oxide film.

5 54. The process of claim 52 wherein the forming a data converter circuitry comprises forming the compound semiconductor switching circuitry to include a compound semiconductor switch.

10 55. The process of claim 52 wherein the forming a data converter circuitry comprises forming the compound semiconductor switching circuitry to include a compound semiconductor switch that comprises a compound semiconductor heterojunction bipolar transistor for implementing the compound semiconductor switch.

15 56. The process of claim 52 further comprising forming transmitter circuitry in the semiconductor structure.

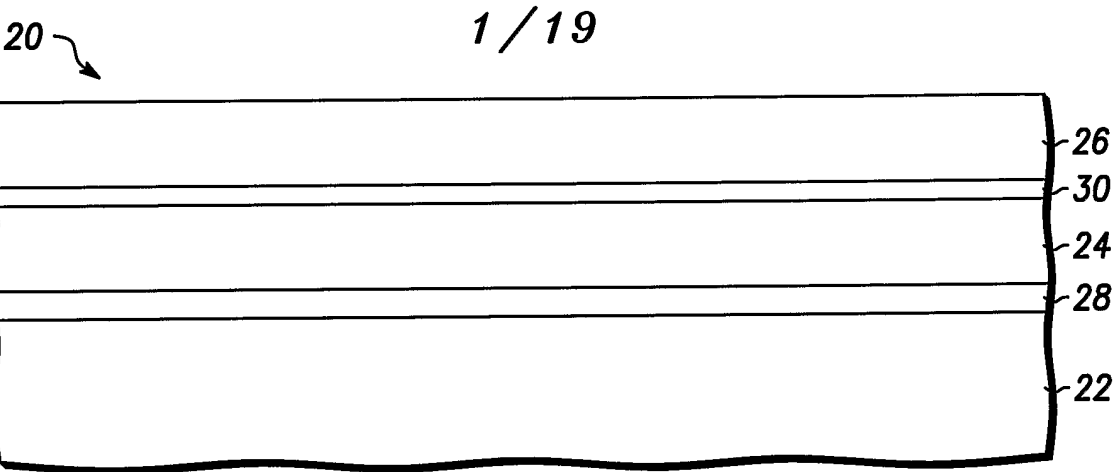


FIG. 1

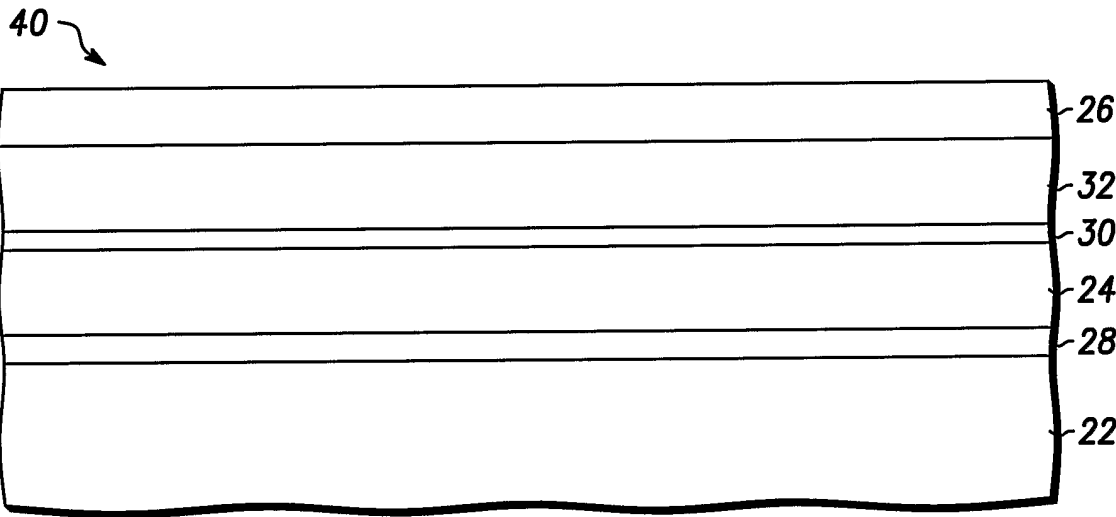


FIG. 2

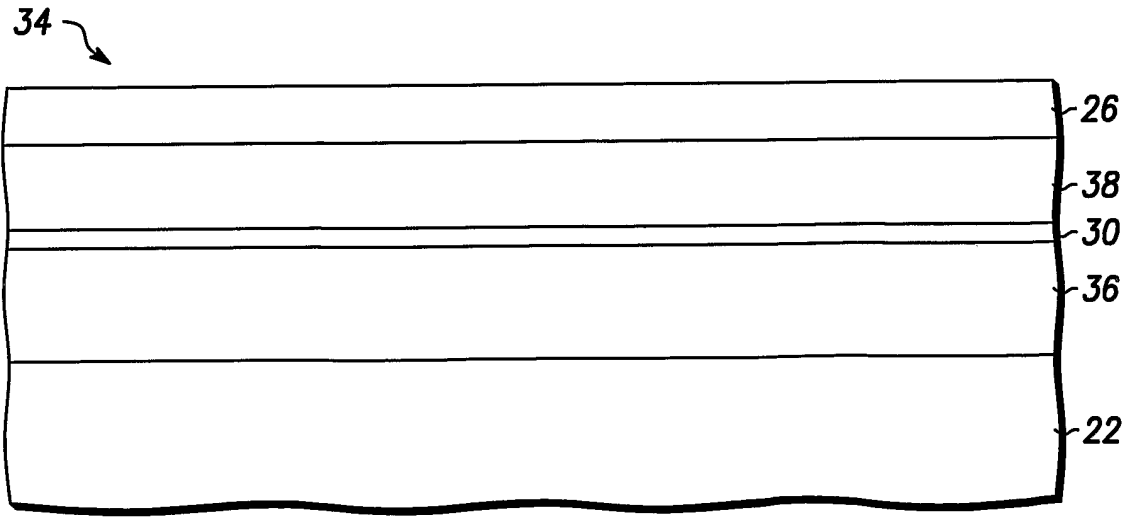


FIG. 3

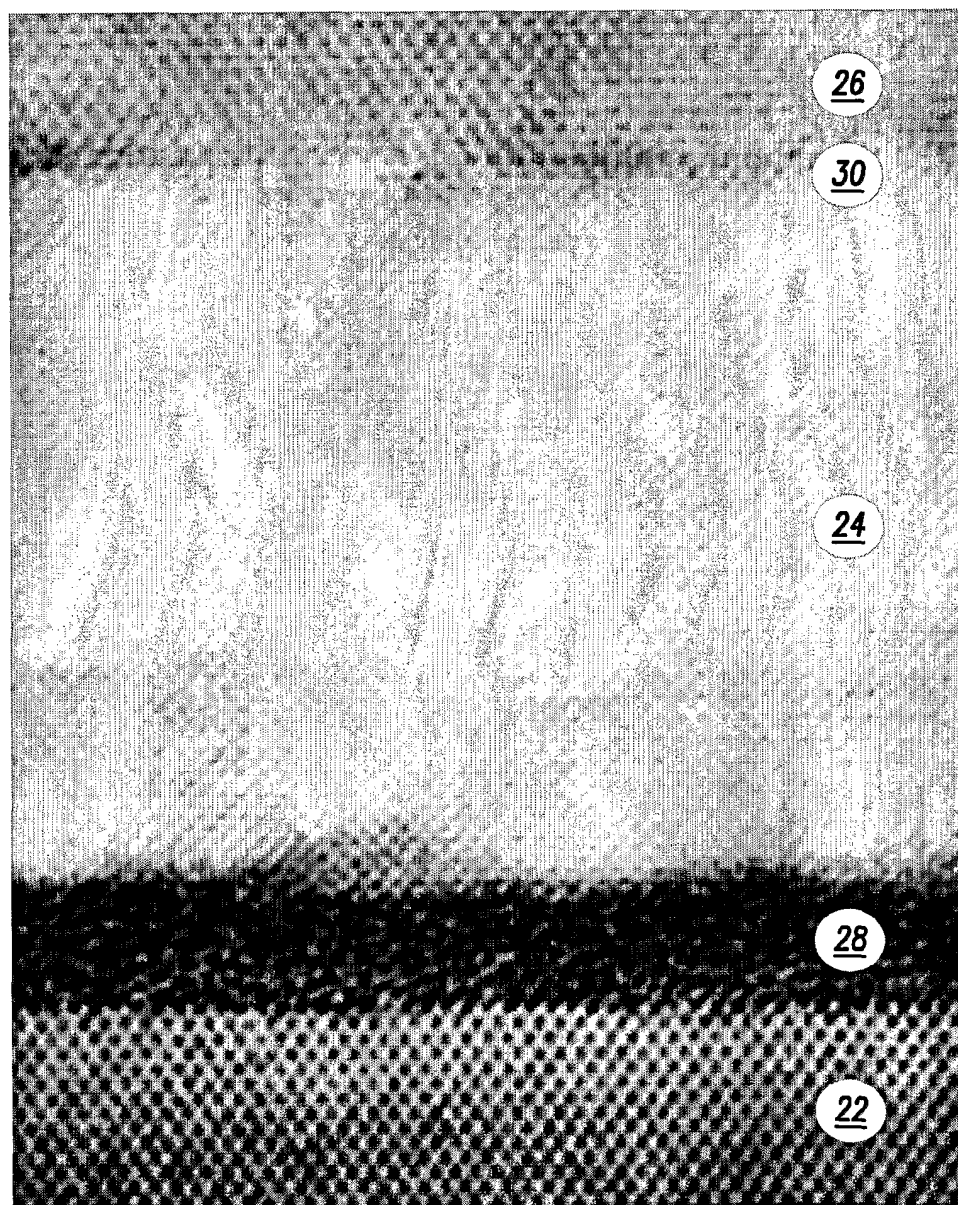
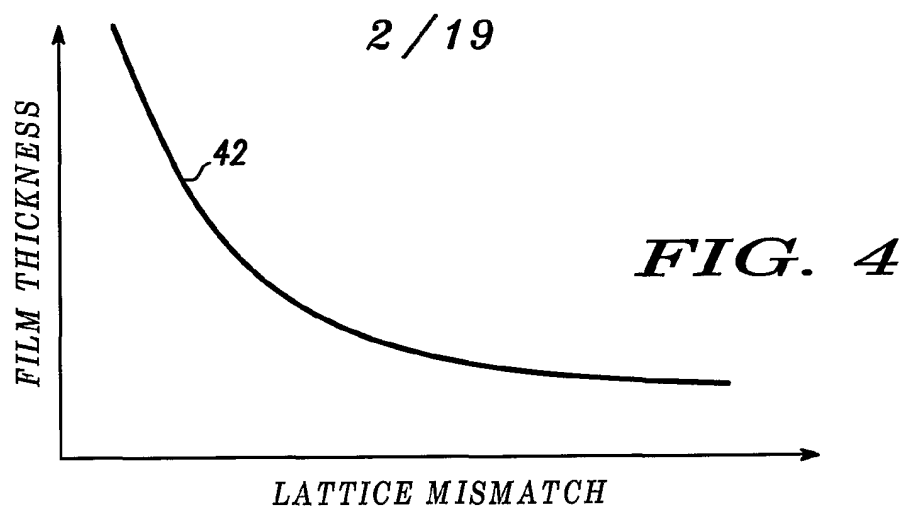
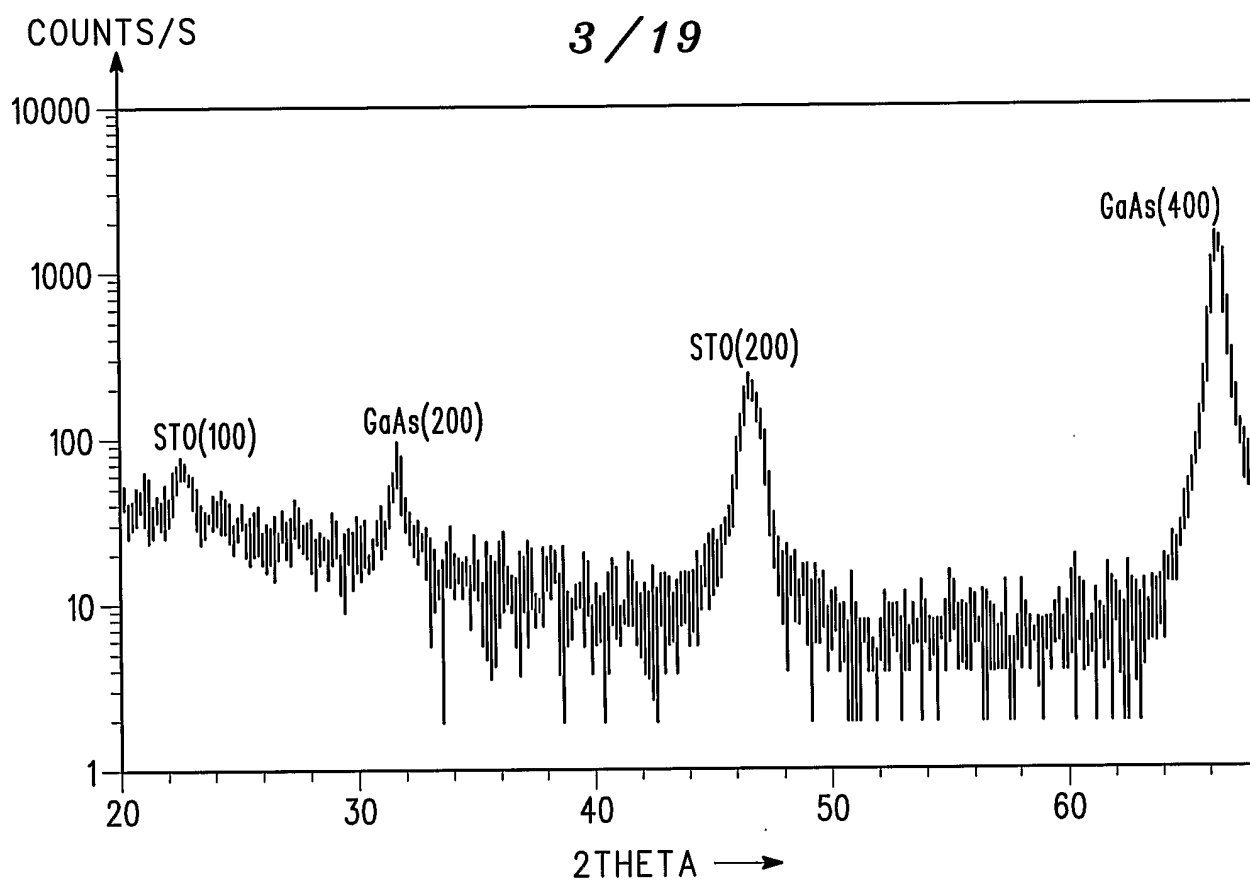
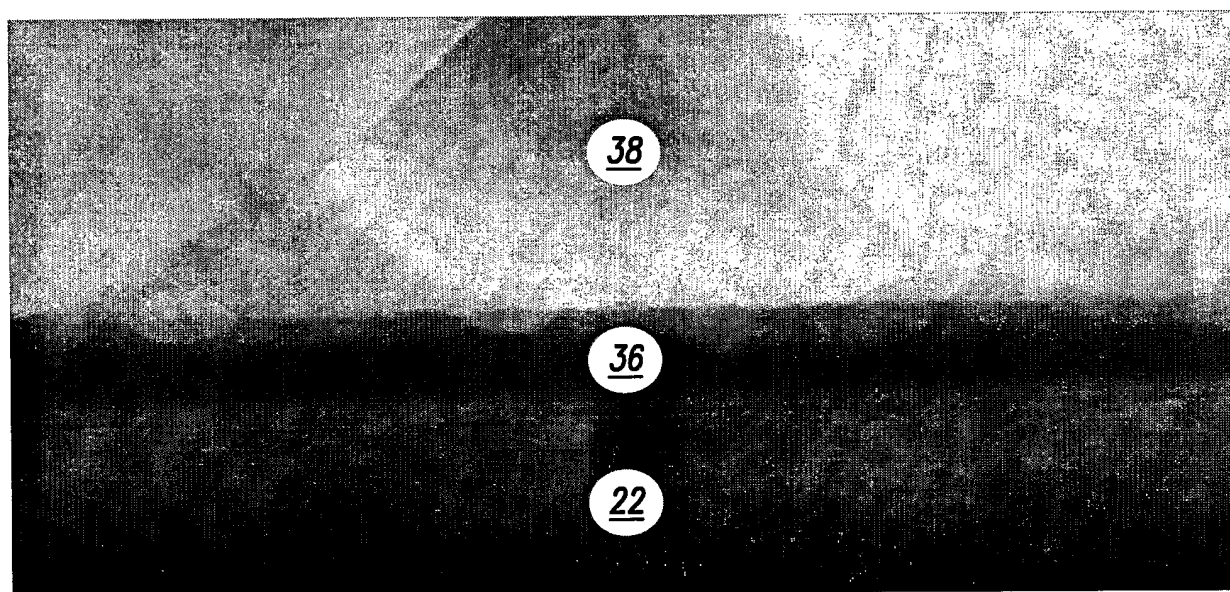
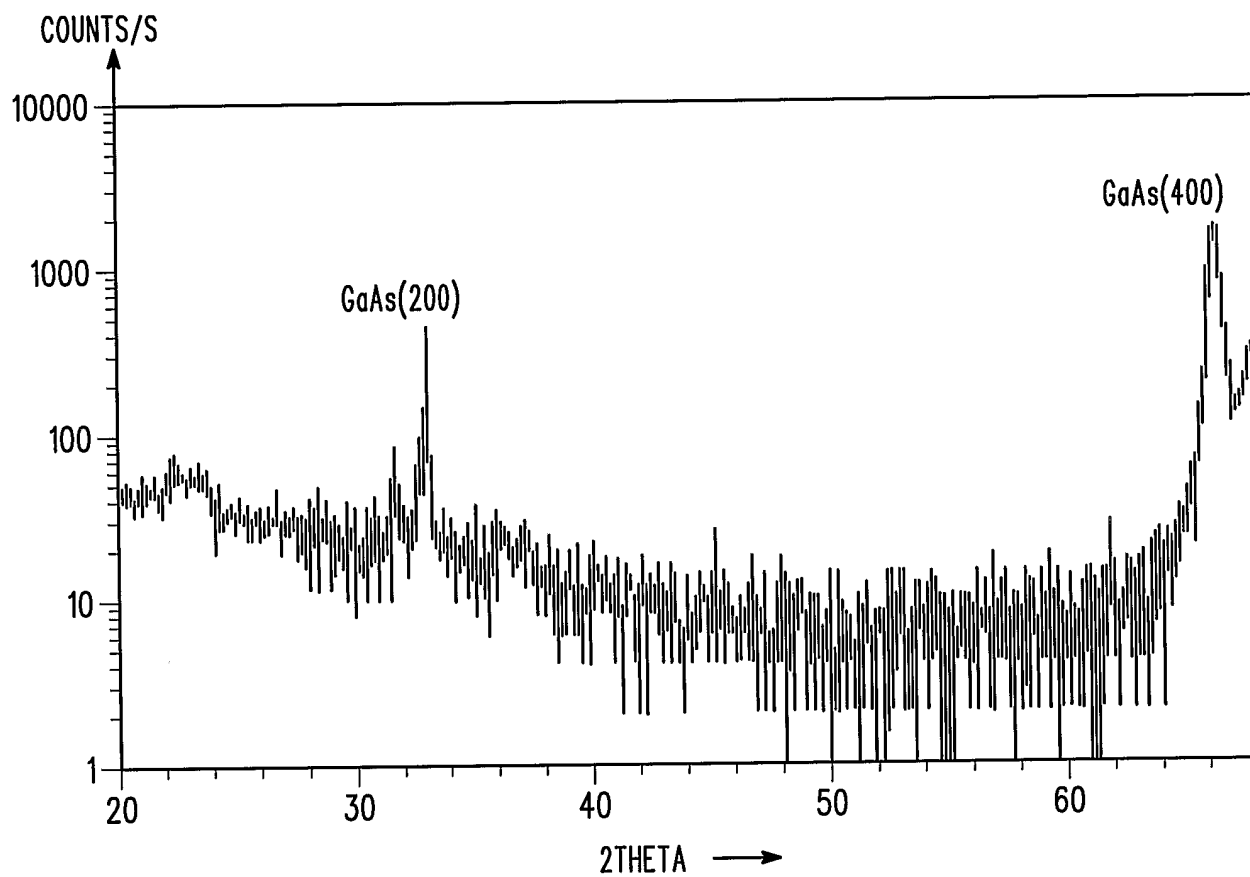


FIG. 5

**FIG. 6****FIG. 7**

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**FIG. 8**

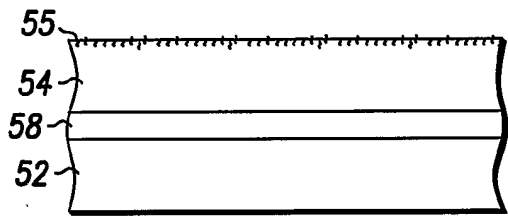


FIG. 9

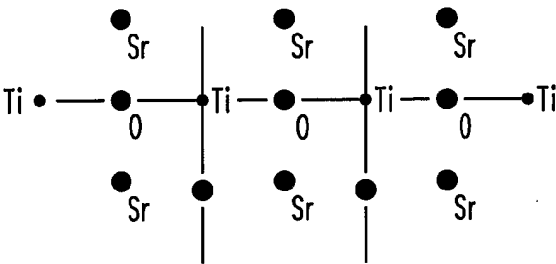


FIG. 13

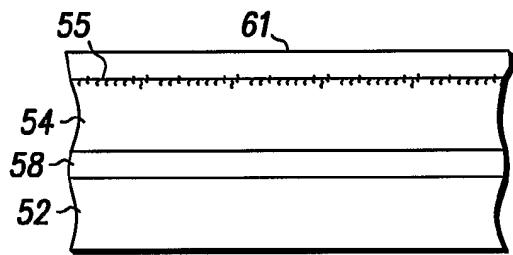


FIG. 10

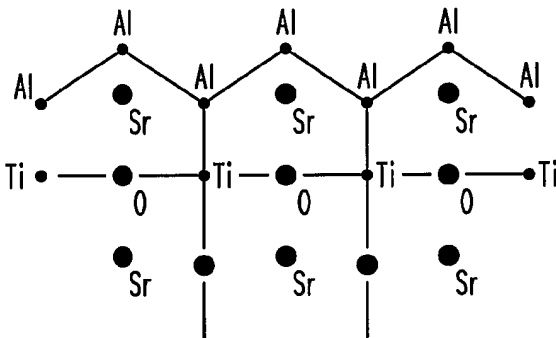


FIG. 14

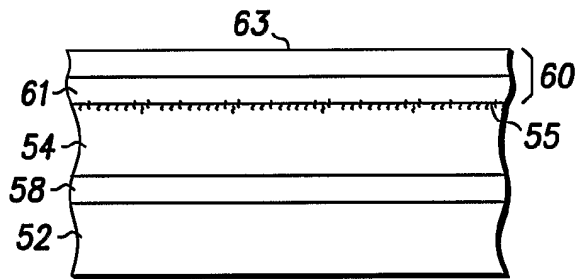


FIG. 11

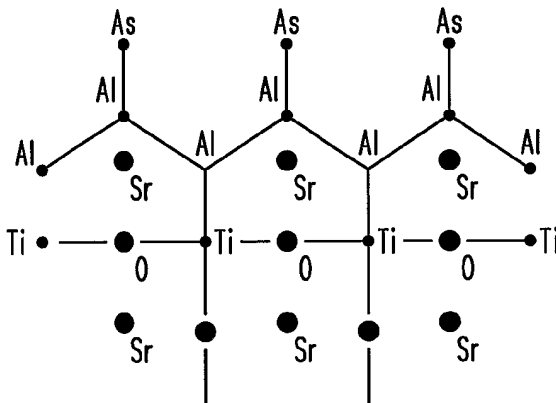


FIG. 15

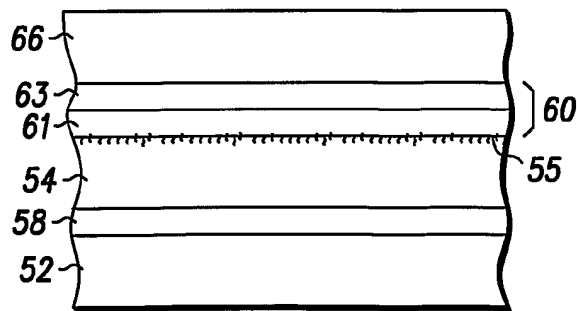


FIG. 12

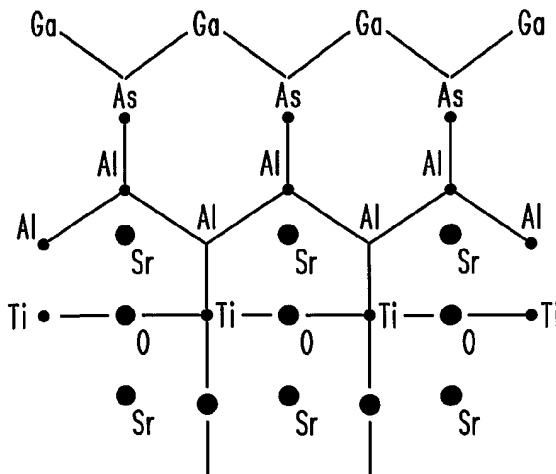


FIG. 16

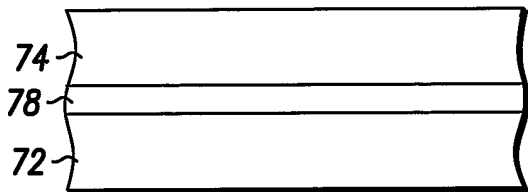


FIG. 17

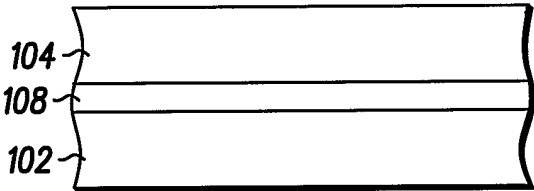


FIG. 21

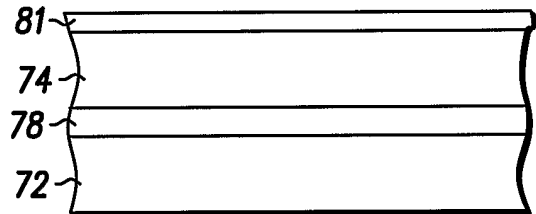


FIG. 18

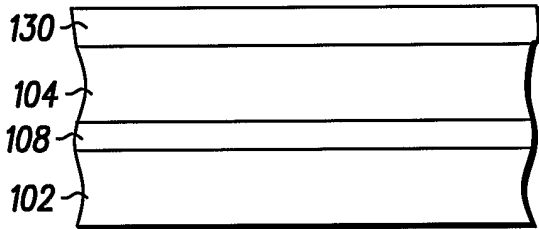


FIG. 22

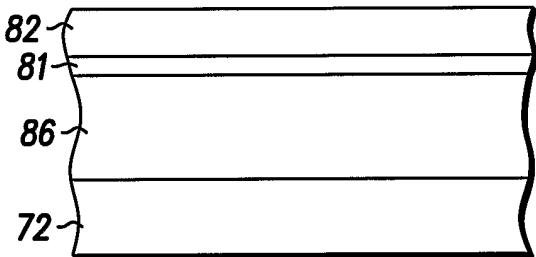


FIG. 19

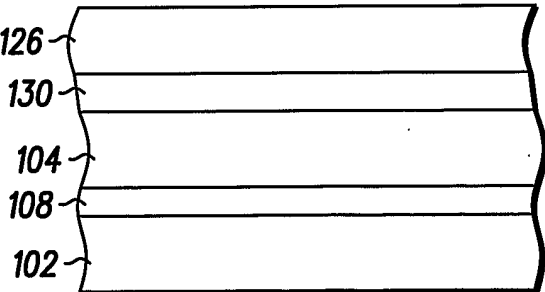


FIG. 23

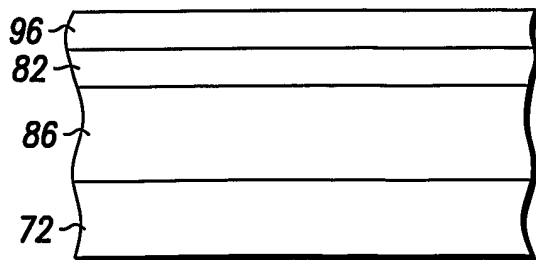


FIG. 20

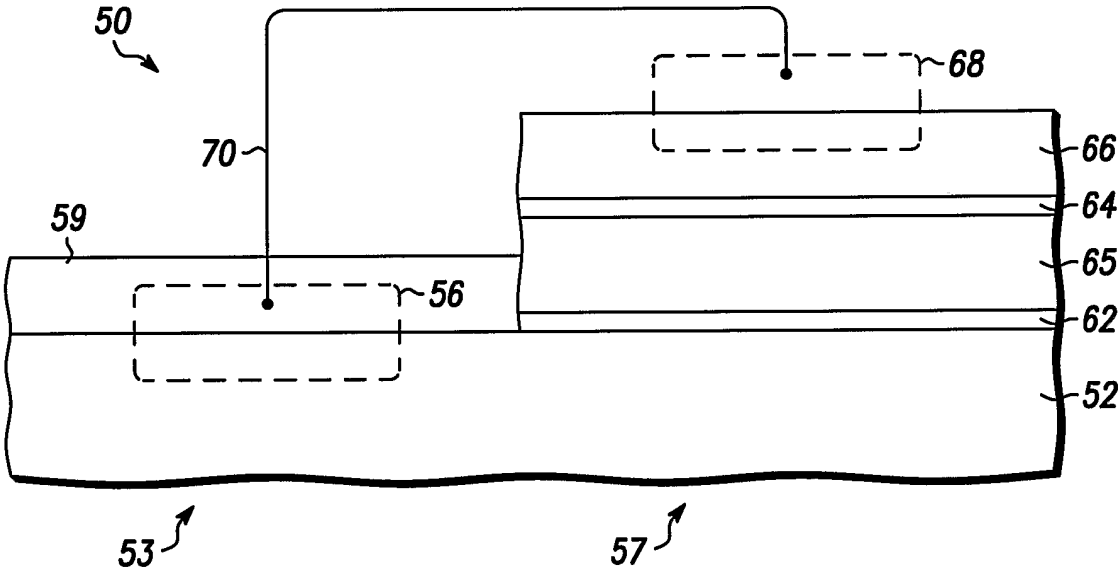


FIG. 24

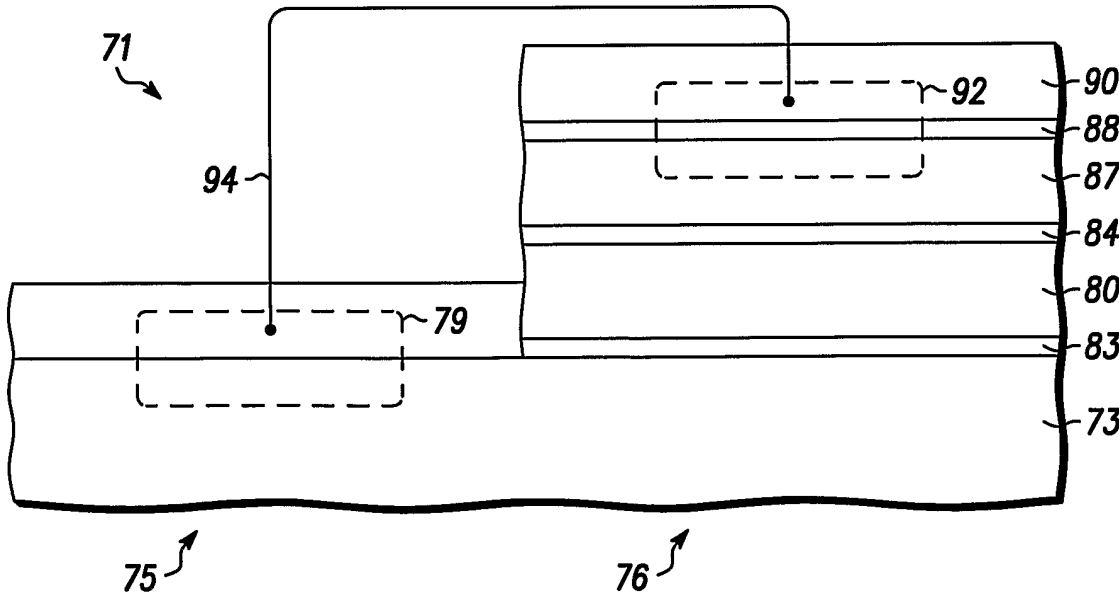
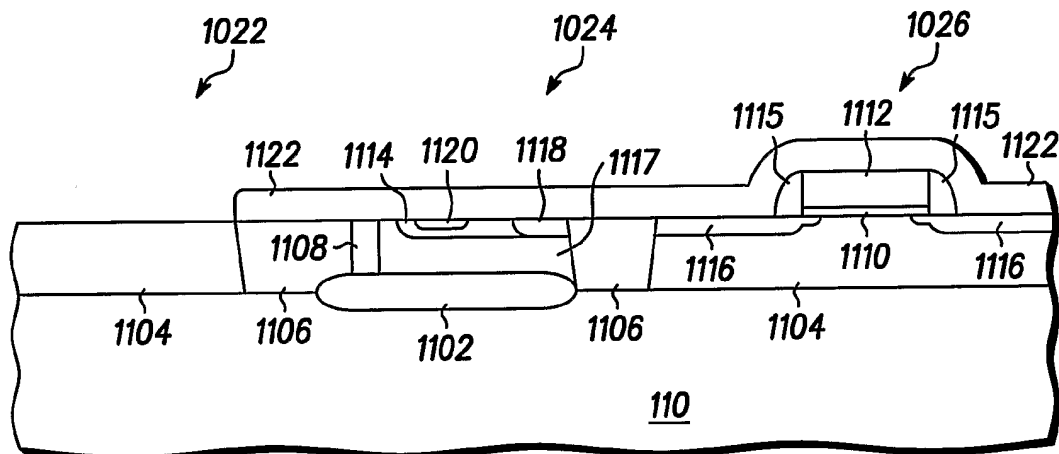
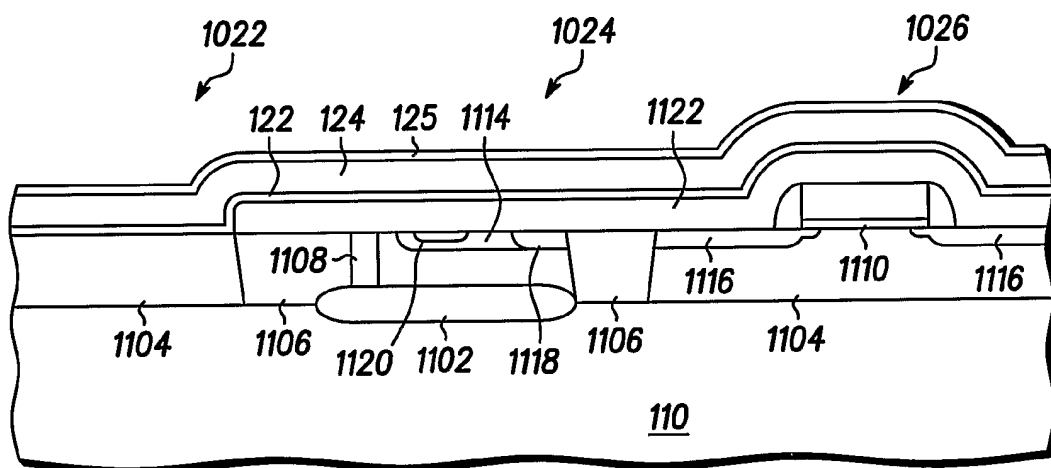


FIG. 25

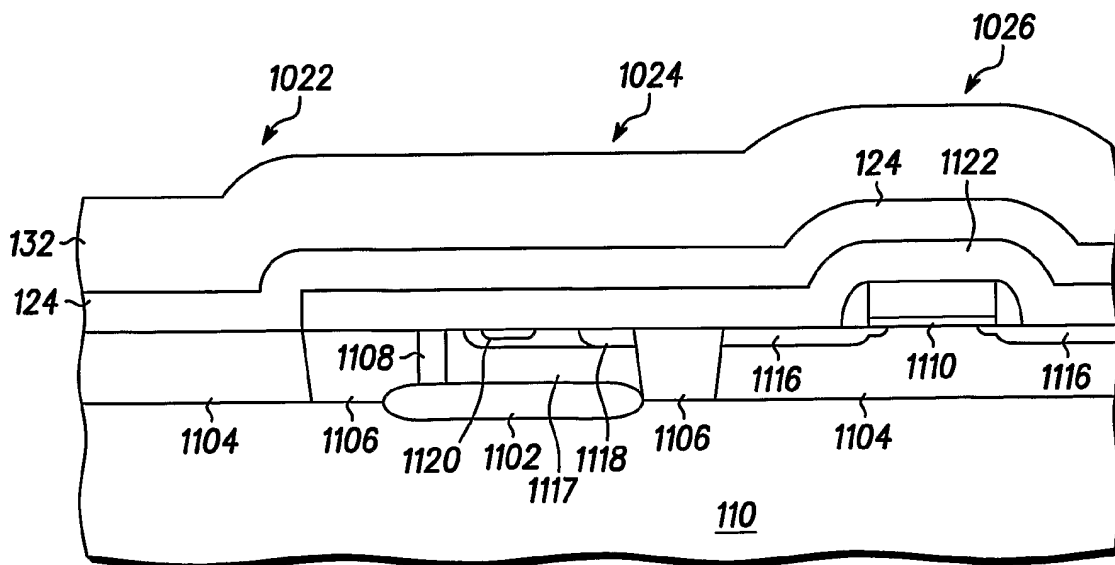
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103 **FIG. 26**

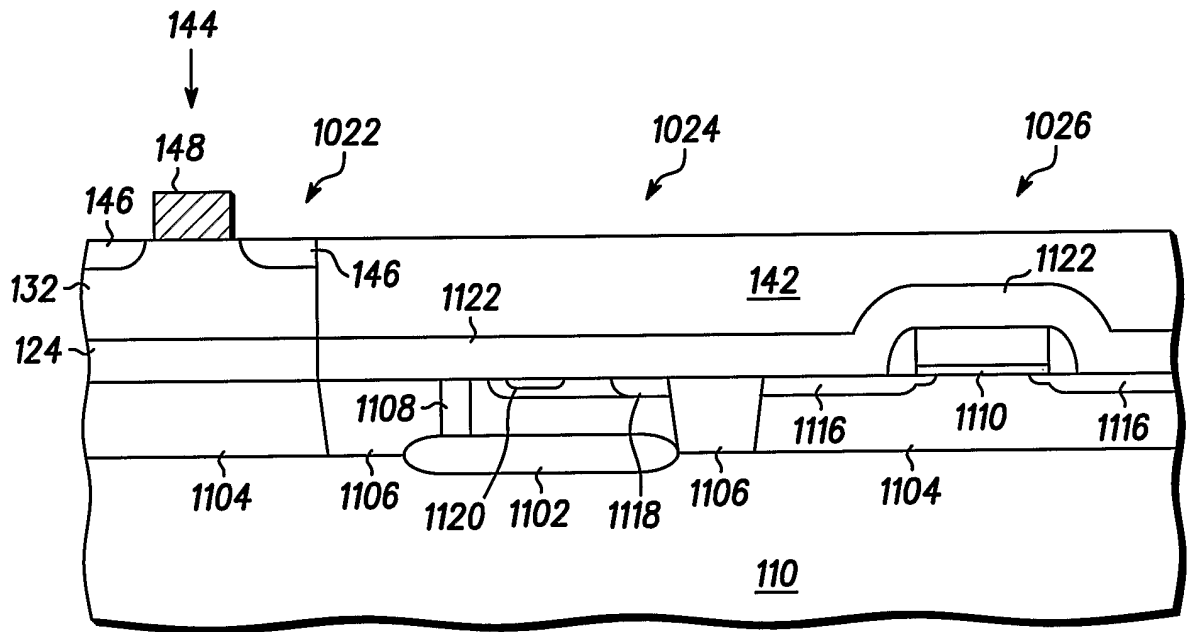


103 **FIG. 27**

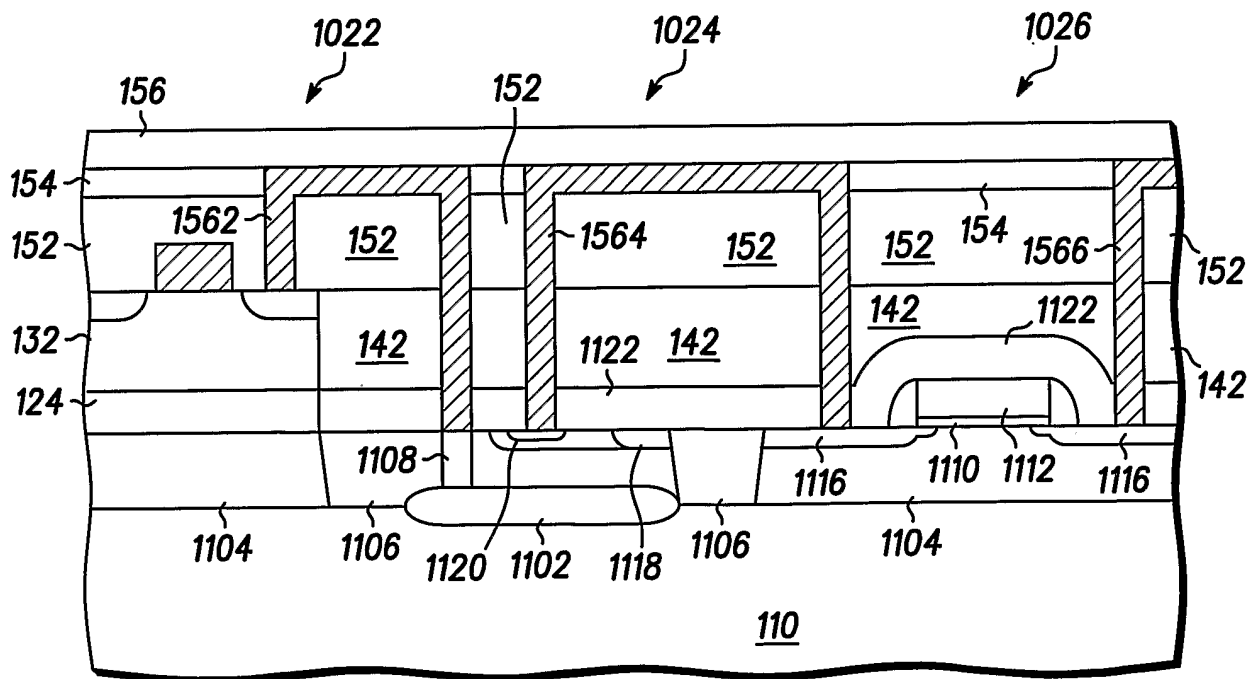


103 **FIG. 28**

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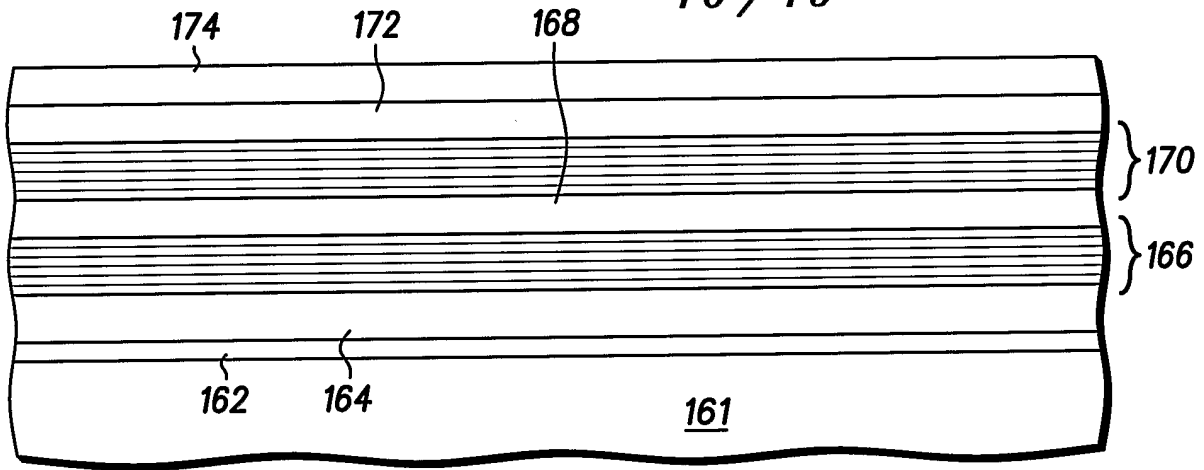


103 **FIG. 29**

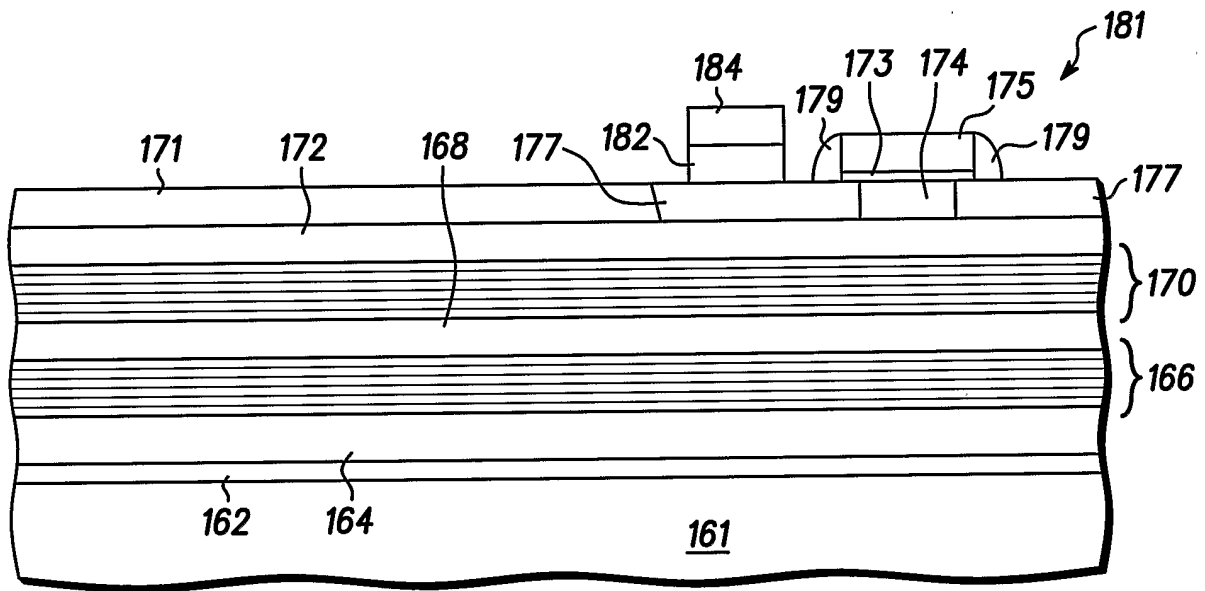


103 **FIG. 30**

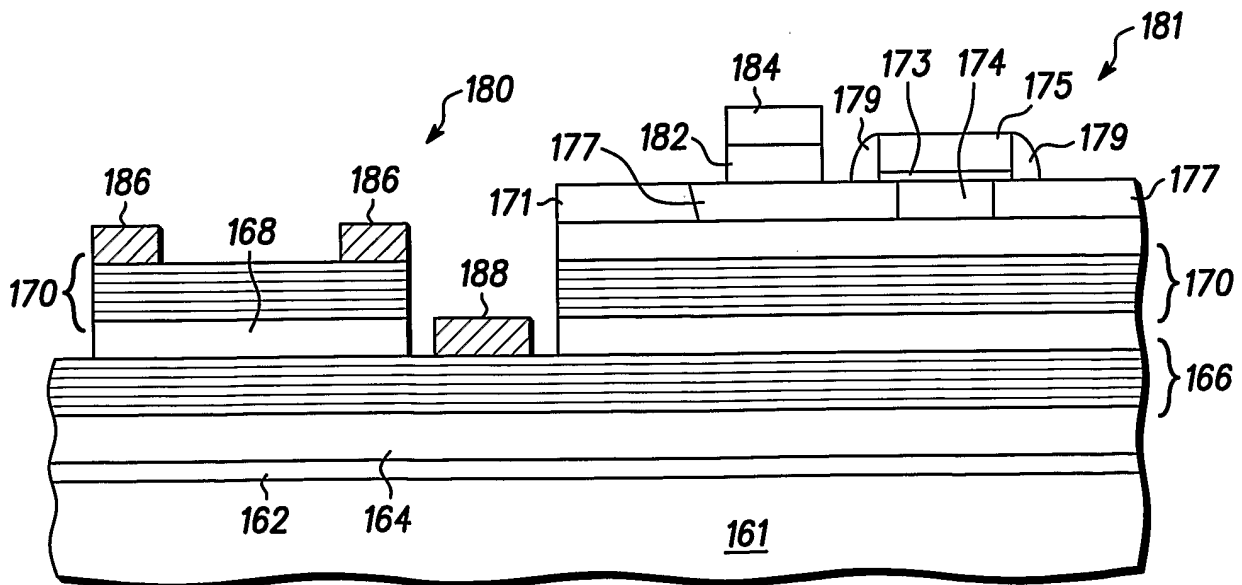
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160 **FIG. 31**

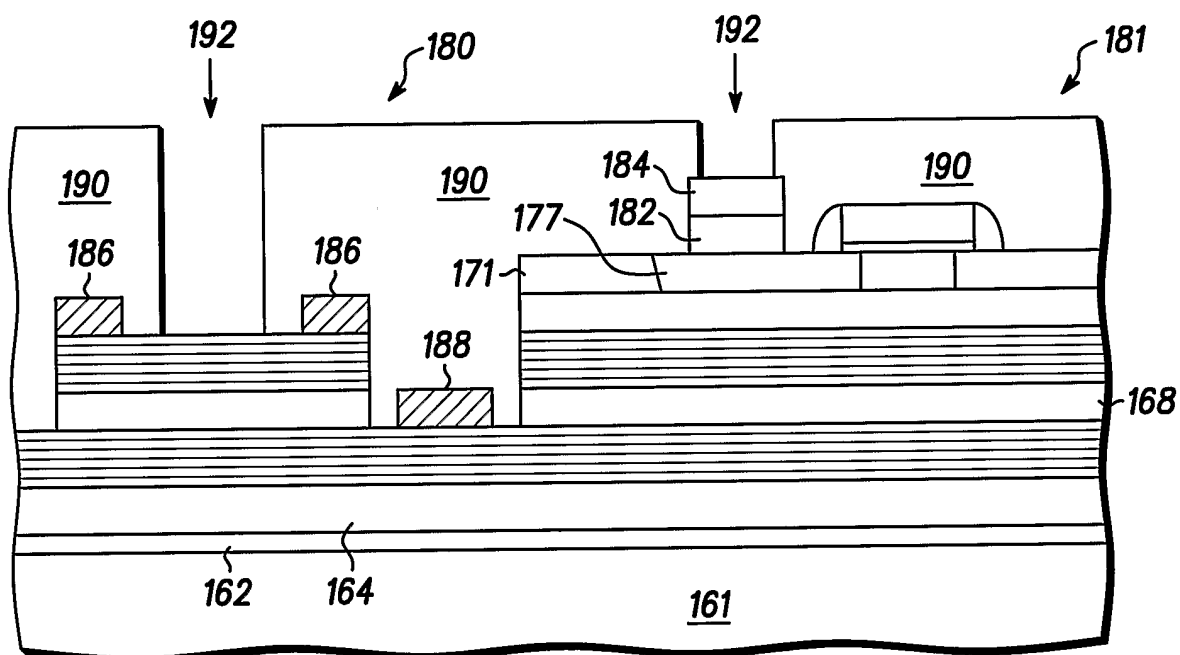
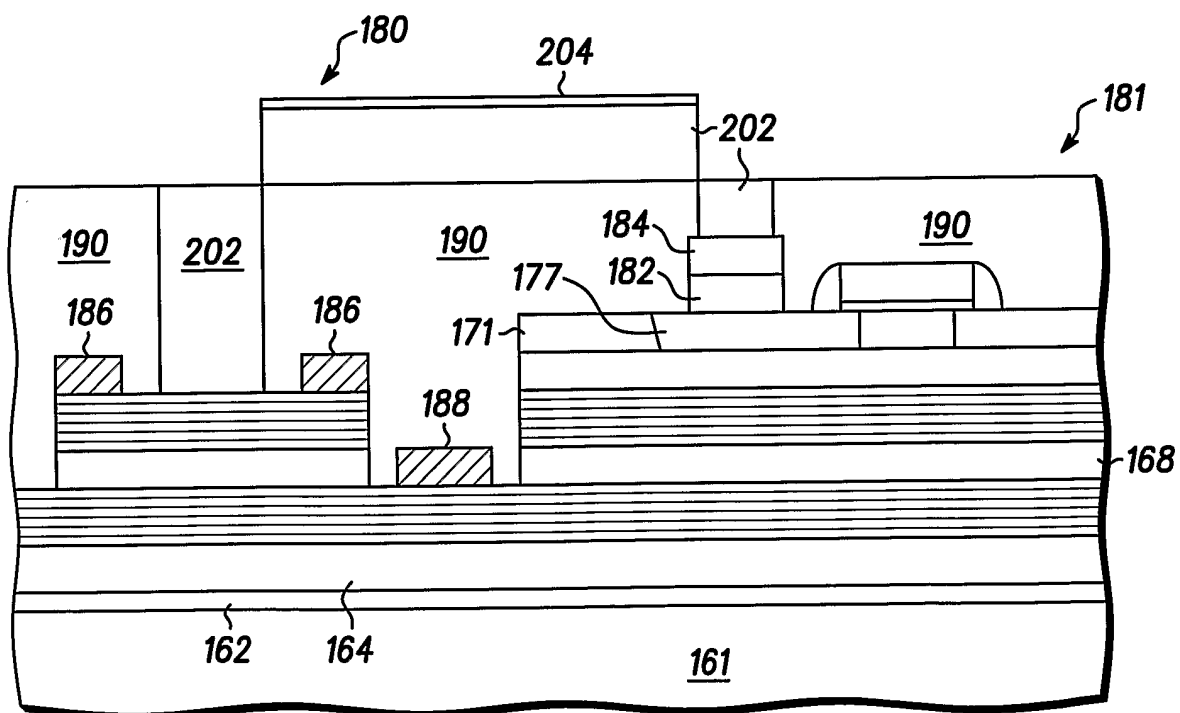


160 **FIG. 32**



160 **FIG. 33**

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**FIG. 34****FIG. 35**

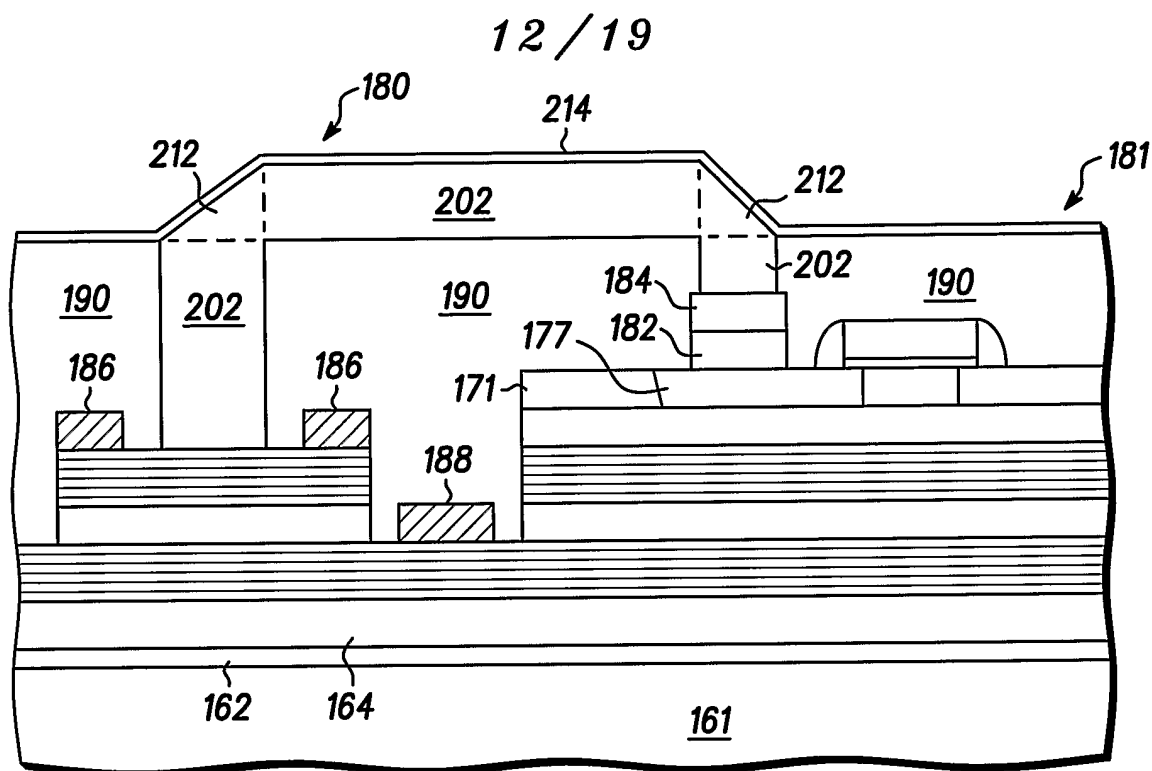


FIG. 36

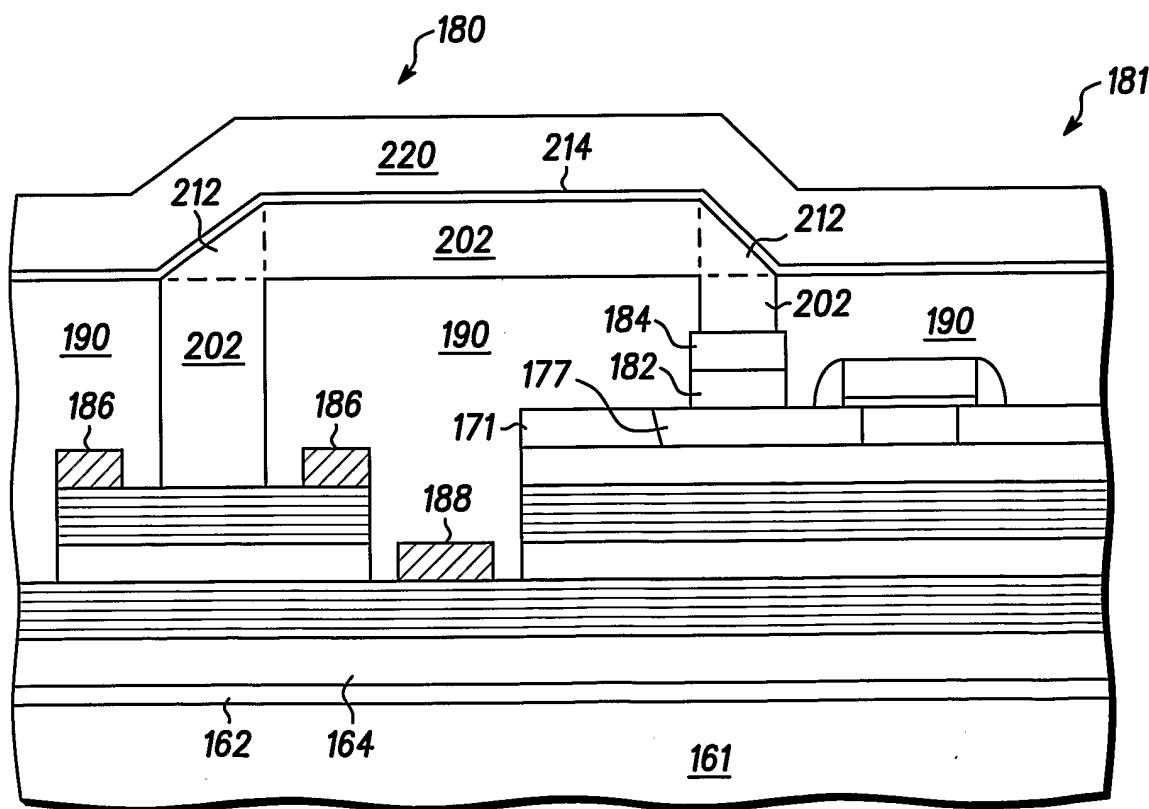
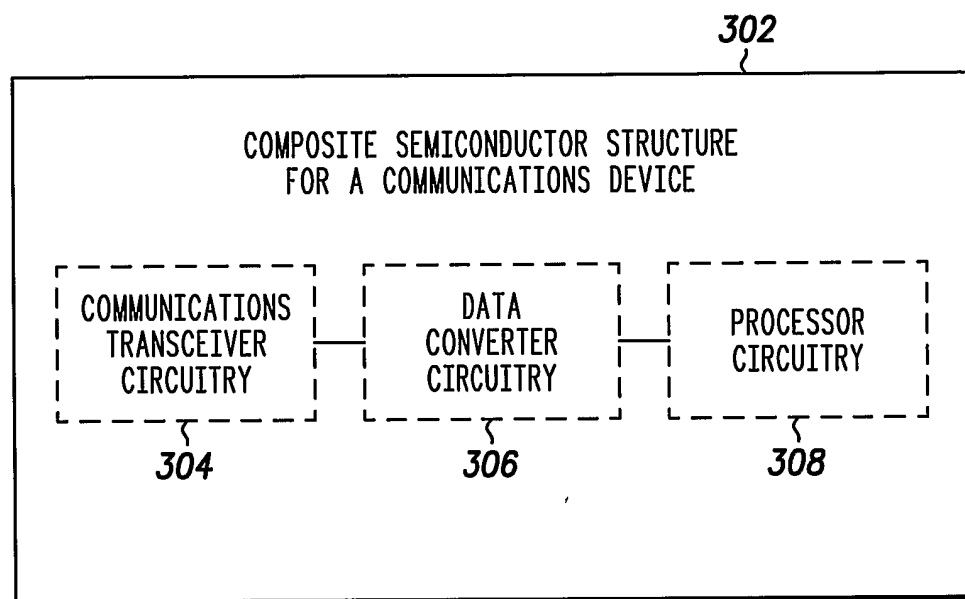
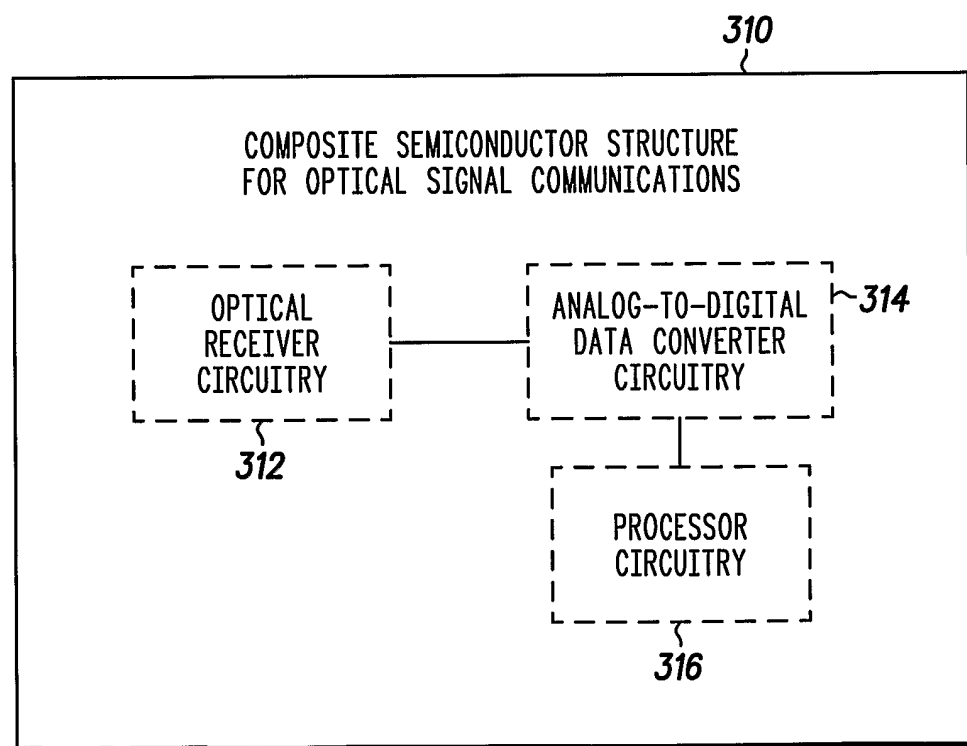
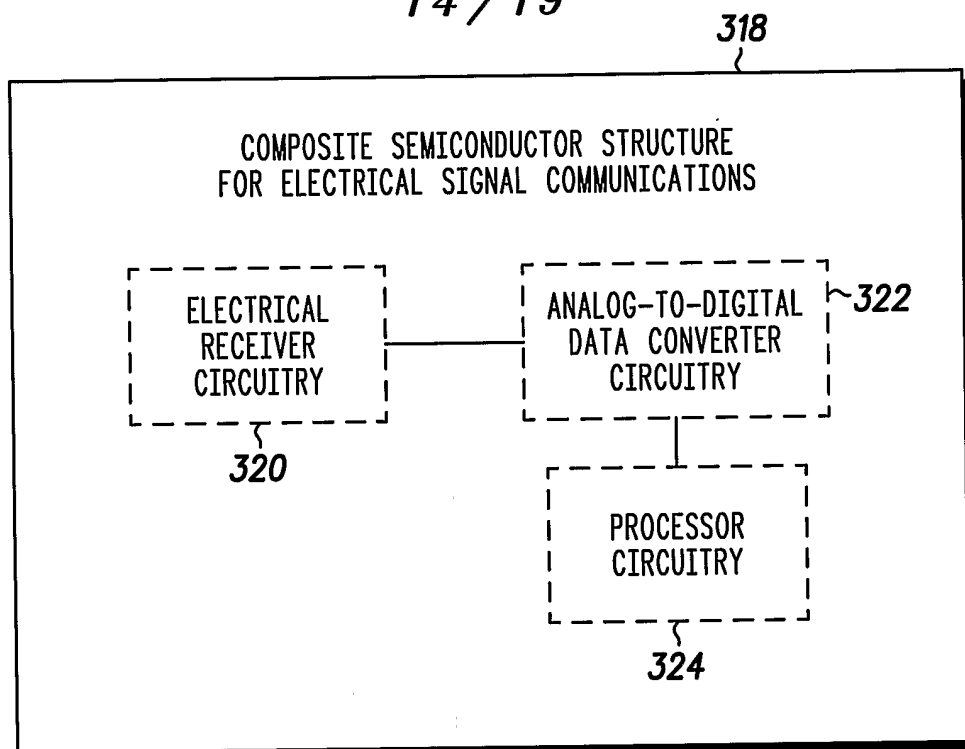
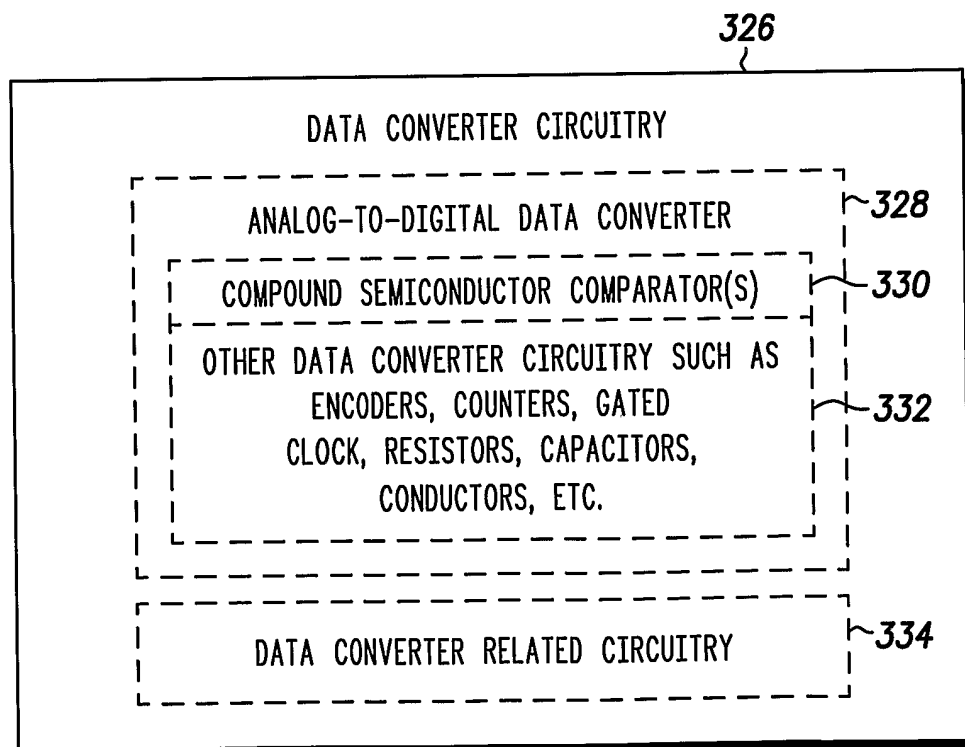


FIG. 37

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*FIG. 38**FIG. 39*

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**FIG. 40****FIG. 41**

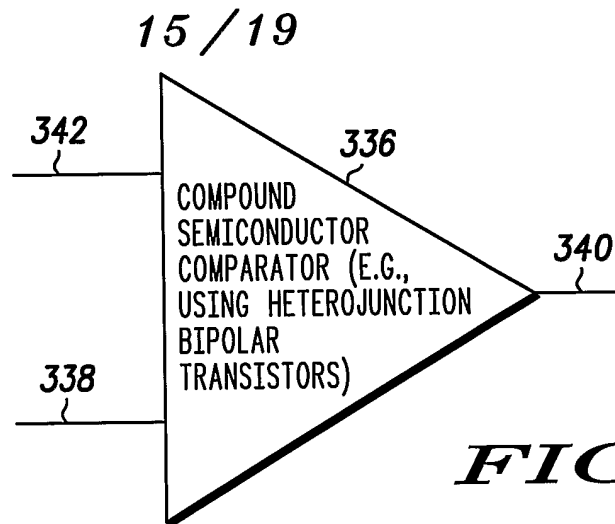


FIG. 42

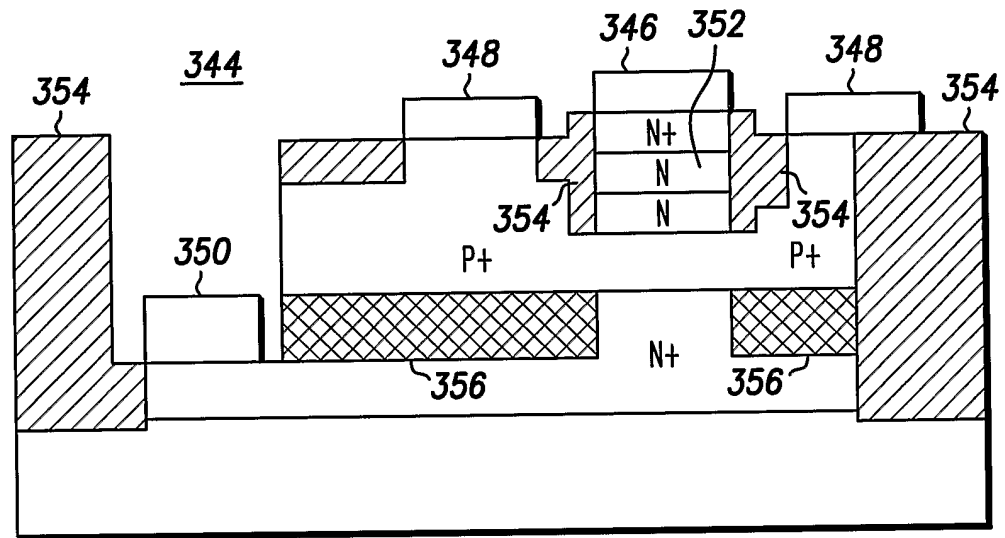


FIG. 43

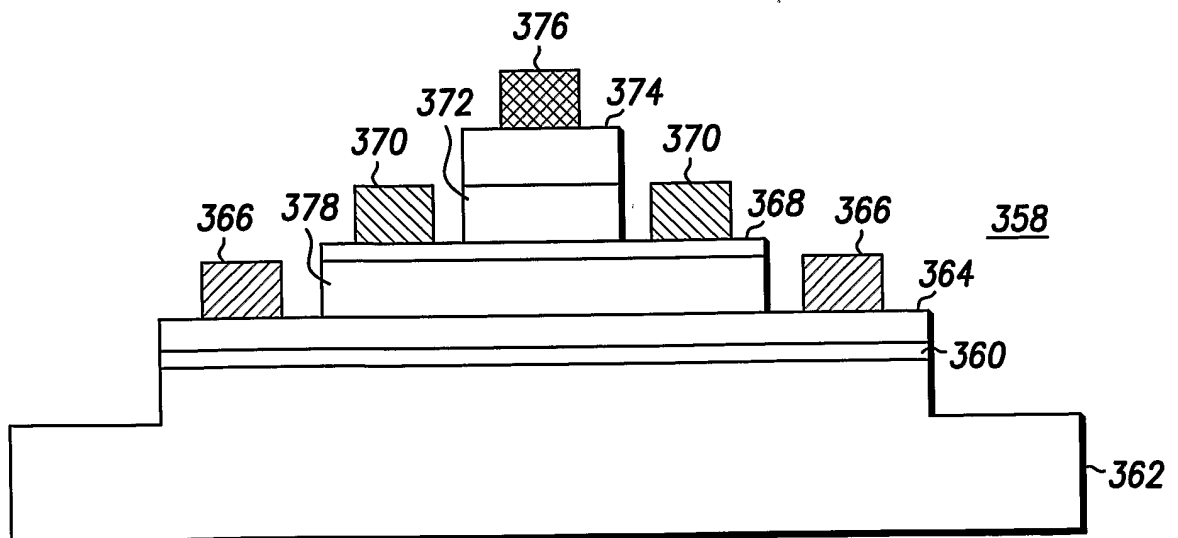
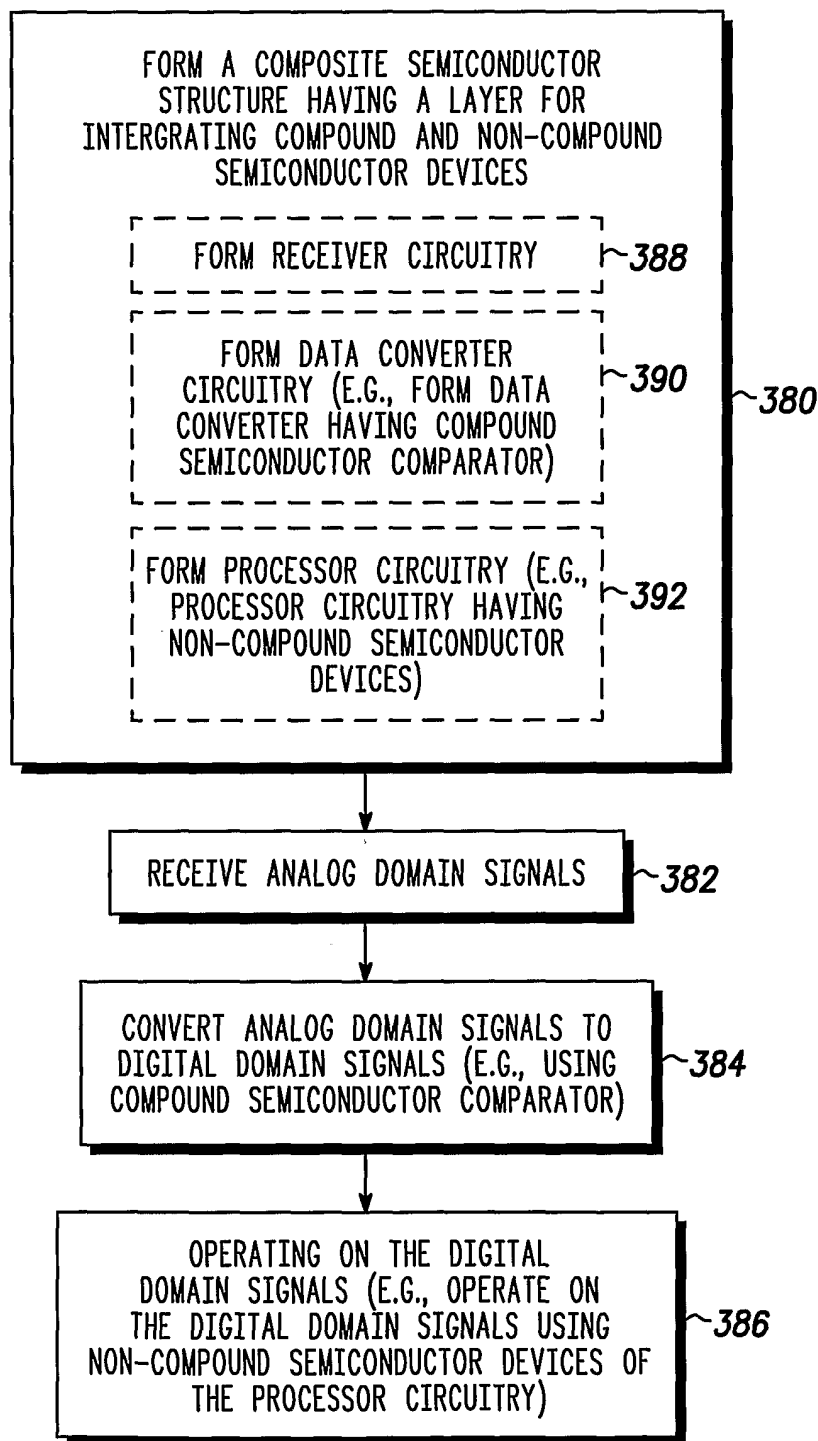
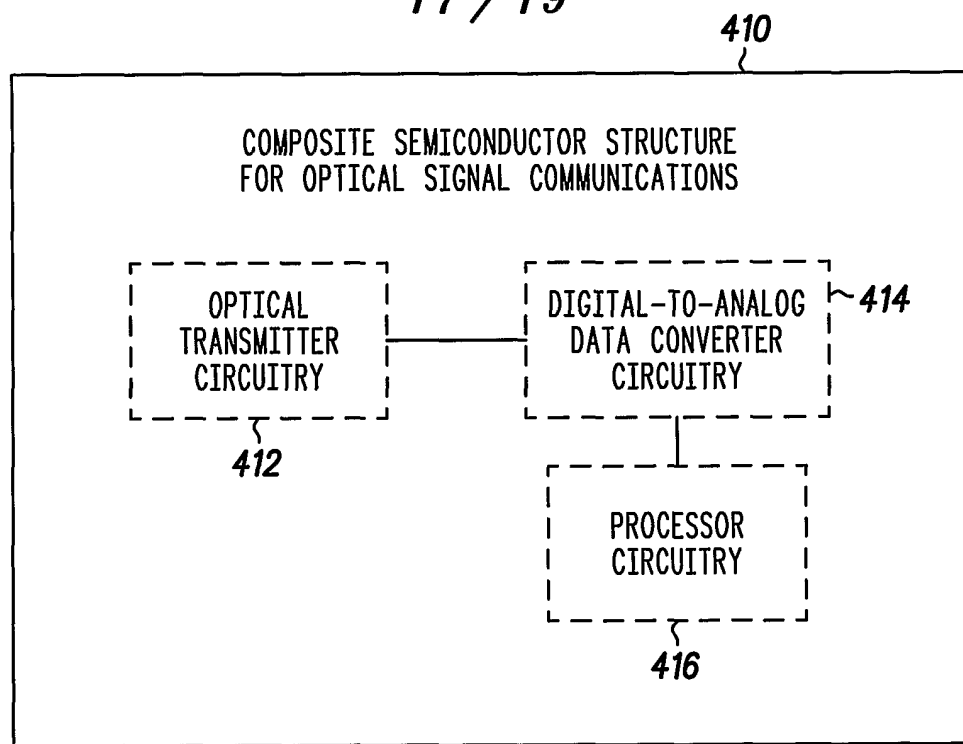
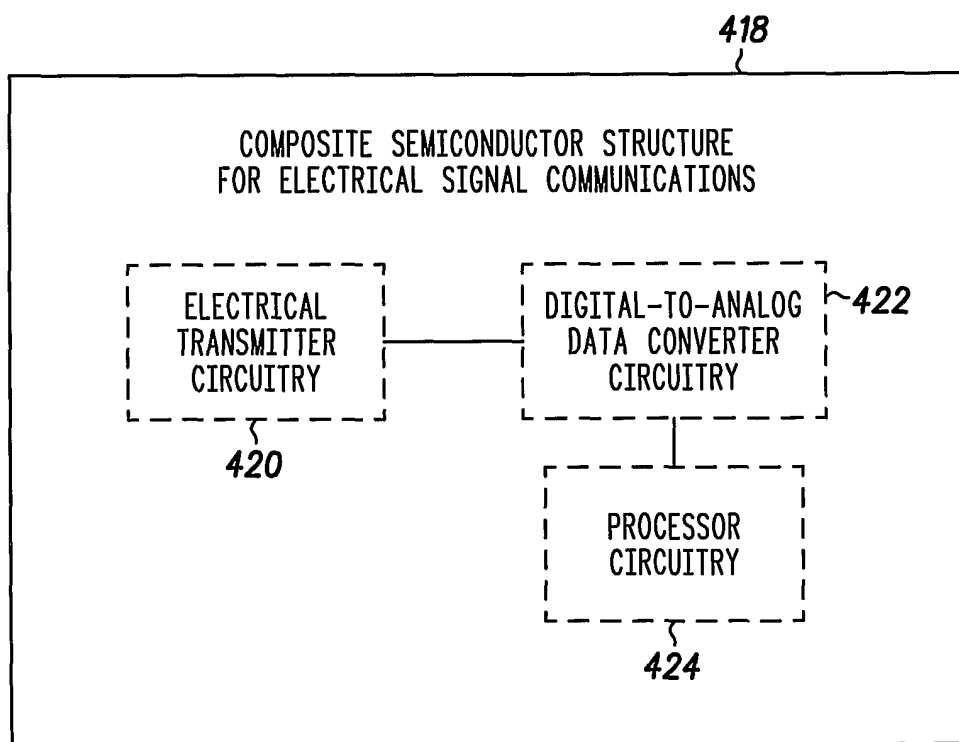


FIG. 44

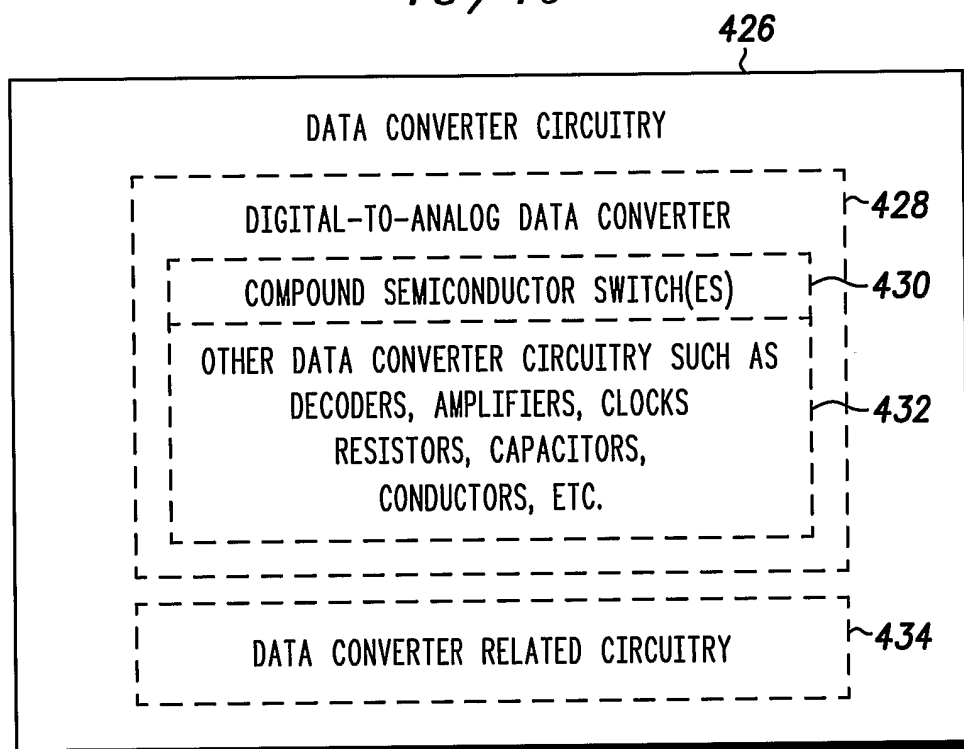
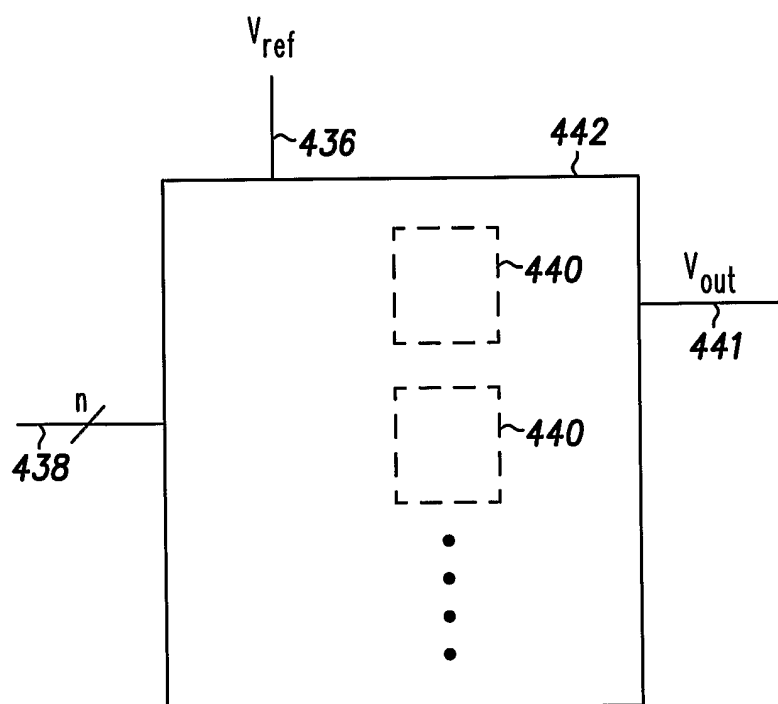
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**FIG. 45**

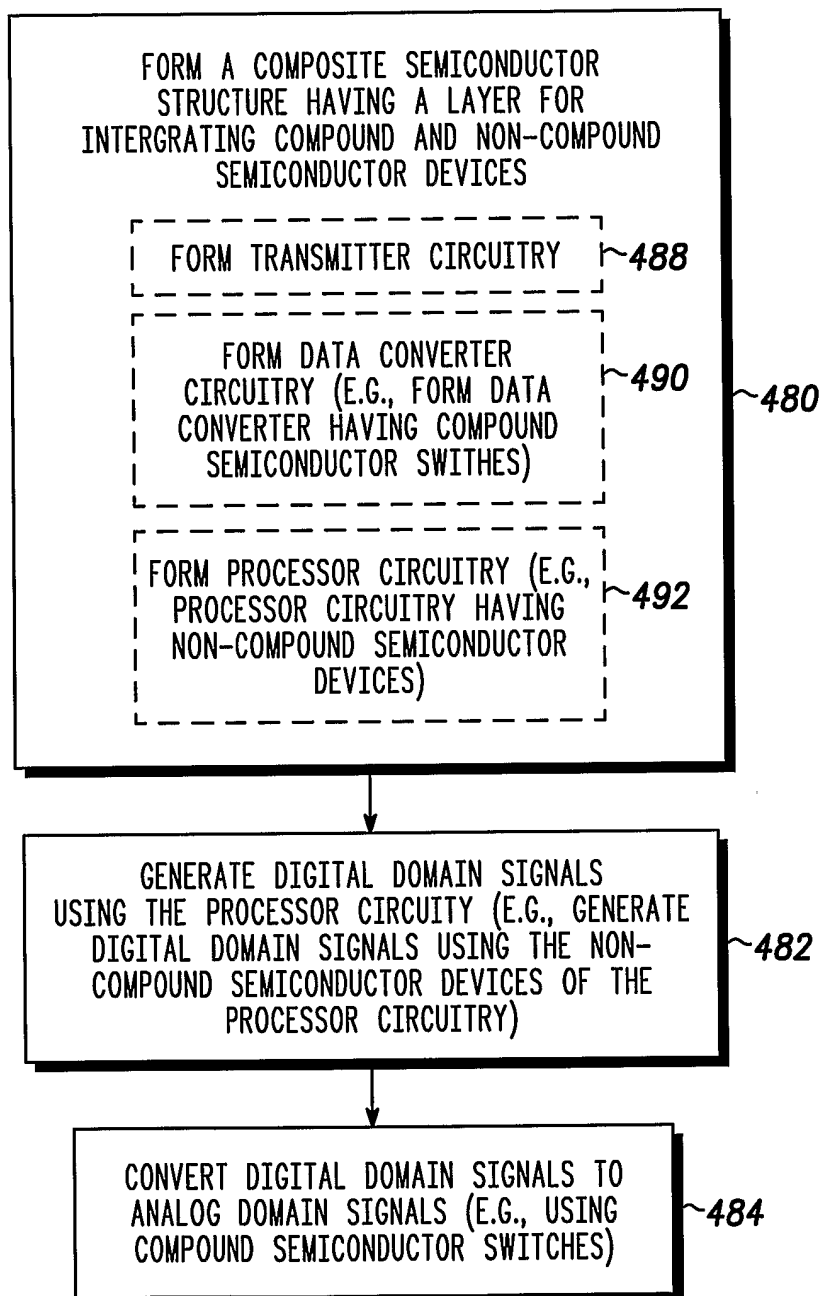
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**FIG. 46****FIG. 47**

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**FIG. 48****FIG. 49**

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**FIG. 50**