

- [54] **DIGITAL GATED DEPTH OF FIELD INTENSITY EQUALIZER**
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- [73] Assignee: The United States of America as represented by the Secretary of the Army, Washington, D.C.
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- [51] Int. Cl.: G01c 3/08
- [58] Field of Search: 356/5; 343/13 R, 5 SM, 343/7.3

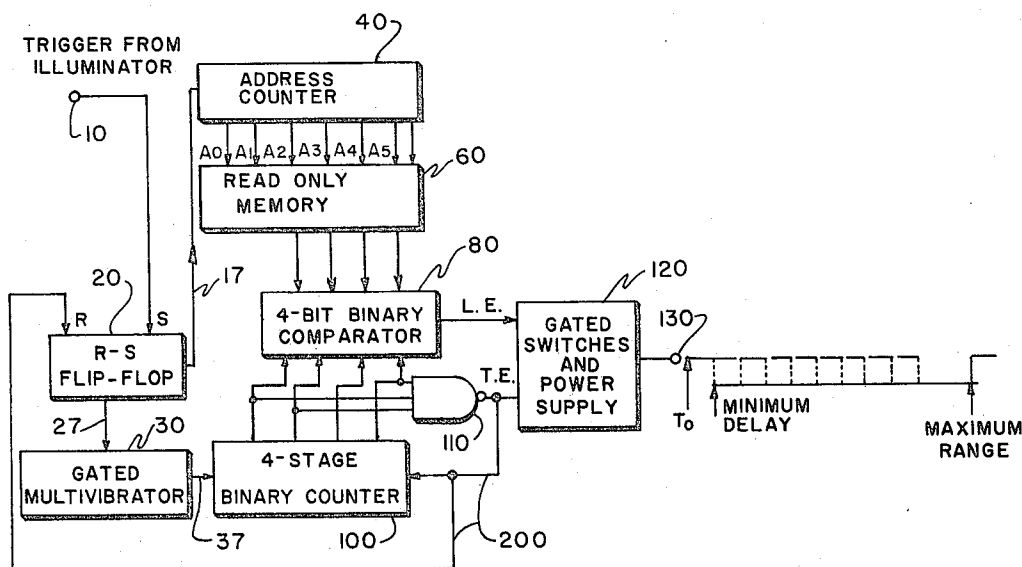
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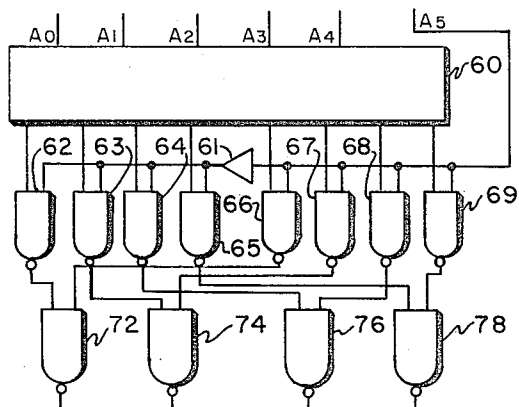
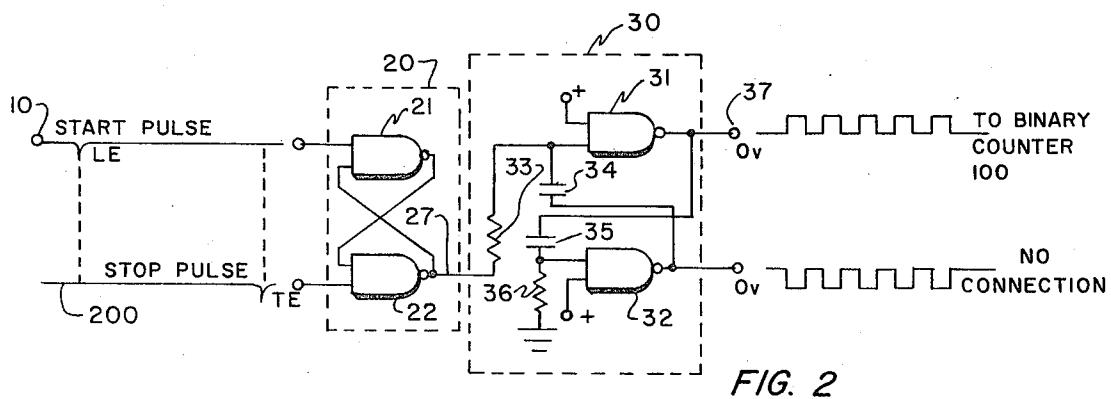
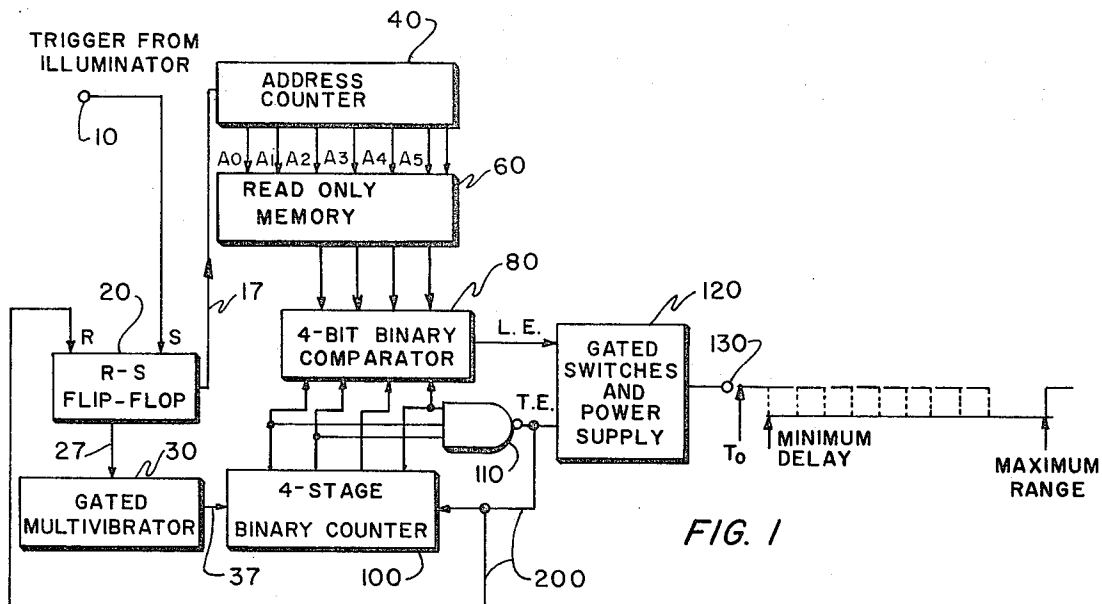
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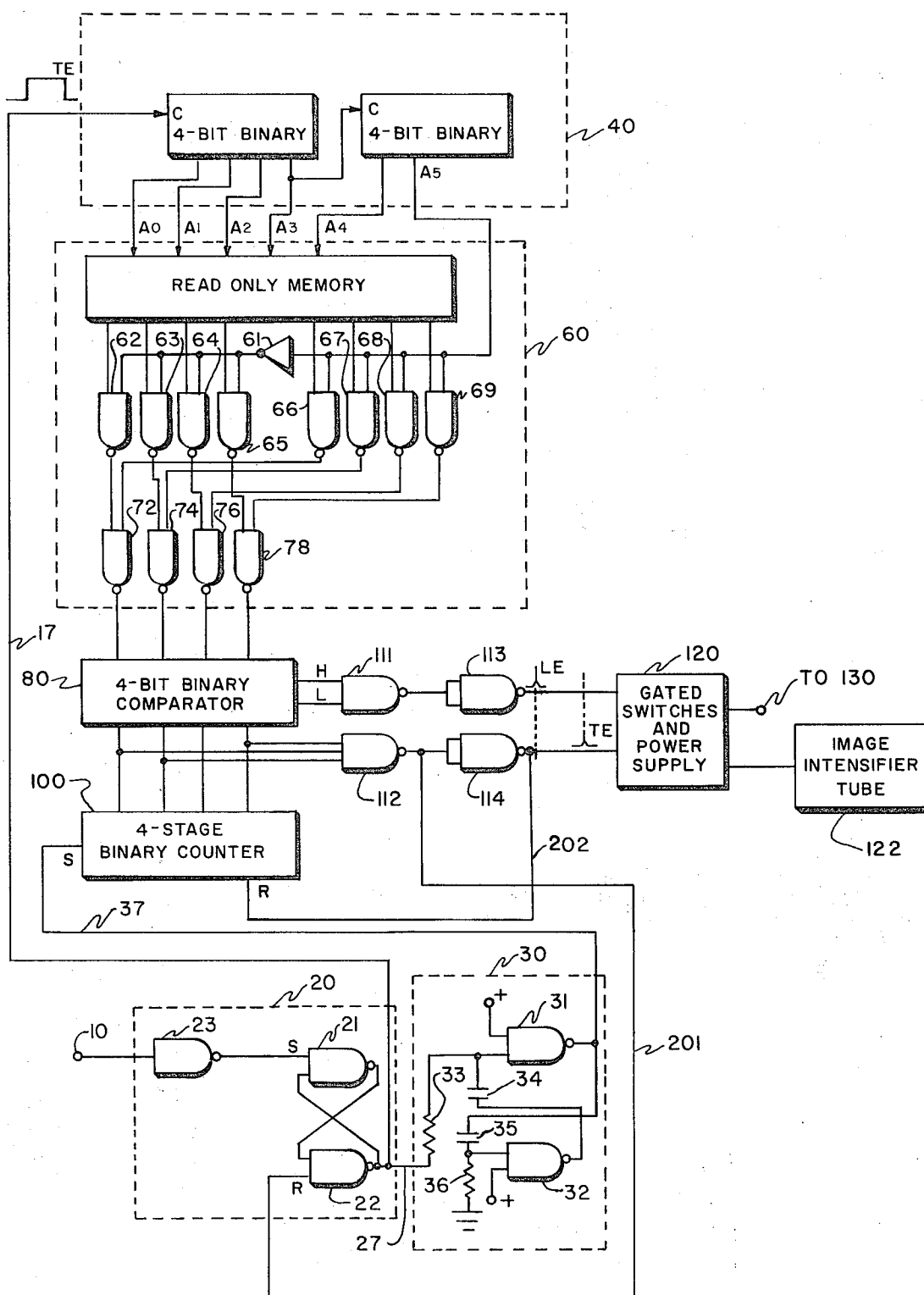
[57] **ABSTRACT**

A digital gating system for an image intensifier that has a built in read only memory weighted to duty cycle the power supply of an image intensifier in accordance with the inverse square law for returned illumination. A pulsing illuminator, which is generally an integral part of the image intensifier system, projects a train of illumination pulses outward which strikes targets and is reflected and returned to the image intensifier. Returned illumination from these targets is reduced according to the inverse square law. The present invention discloses a digital method of controlling a programmed read only memory that switches an image intensifier "on" more often in time as each illumination pulse travels through both the distances to and return from targets at increasing distances away from the image intensifier. Reflections from close targets are looked at less often by the image intensifier than reflections from targets at the maximum range. The number of looks, or activations, of the image intensifier are weighted commensurate with the inverse square law.

7 Claims, 7 Drawing Figures







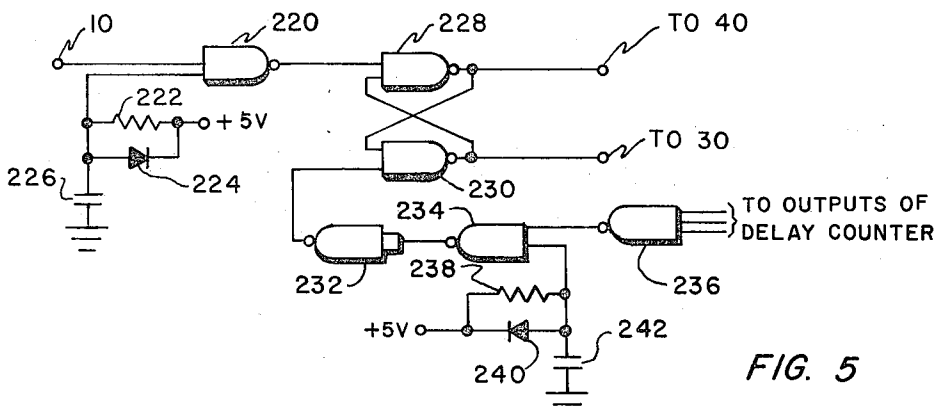


FIG. 5

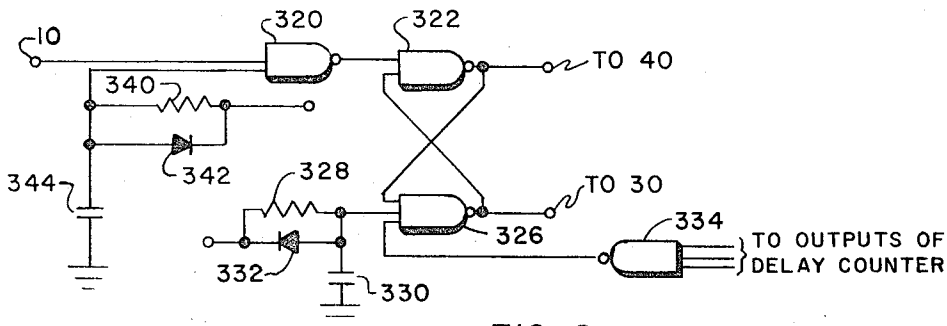


FIG. 6

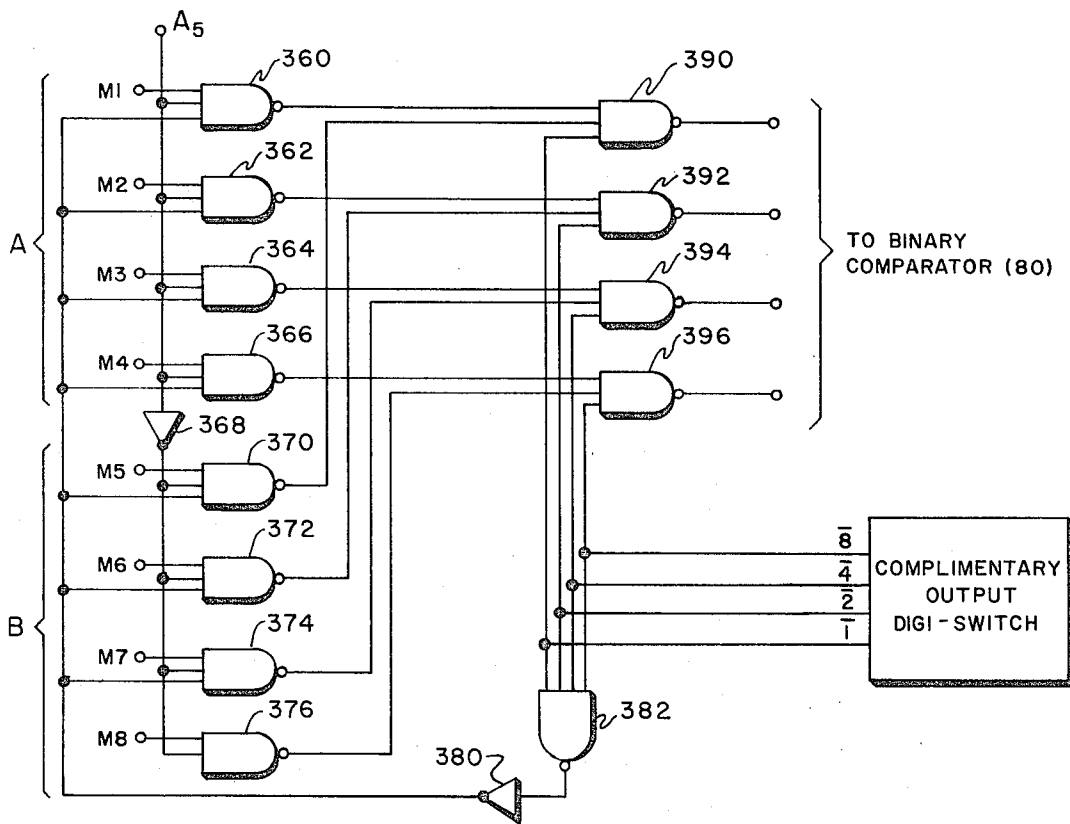


FIG. 7

DIGITAL GATED DEPTH OF FIELD INTENSITY EQUALIZER

The invention described herein may be manufactured, used, and licensed by or for the Government for governmental purposes without the payment to me of any royalty thereon.

BACKGROUND OF INVENTION

Prior art gating systems for image intensifiers use manual methods of accentuating the returned illumination at specific ranges. Returned illumination may be accentuated at all ranges in the manual method by varying the on-of time of the image intensifier such that each pulse of illumination is reflected back into the image intensifier for targets at specific ranges. The disadvantage of the manual method is obvious in that an operator of the image intensifier needs as little distraction as possible in observation of returned illumination. Obviously, an automatic means for amplifying the returned illumination evenly over the entire useable range is needed so that the operator can devote his time to observing returned illumination.

SUMMARY OF INVENTION

The present invention relates to a digital gating system for an image intensifier in which an address binary counter provides inputs to a programmed read only memory. The four outputs from the read only memory are compared with outputs from a four stage binary counter in a comparator circuit wherein the output from the comparator provides a leading edge pulse to a gated switch and power supply circuit. The starting time of the leading edge varies according to the program built in the read only memory. The program has various delay times built therein for sampling returned reflections in range during those delay times. At each delay time the number of samples per system cycle is increased as the square of the ratio of delay time to the minimum delay time. By increasing the number of samples at each increment of delay time, the decreased illumination from reflected targets appears as an evenly illuminated scene at all ranges. The present invention may further comprise a circuit for providing accentuated illumination at a specific range by programming more samples in the read only memory at the specific range desired.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates the digital binary switching circuits of the present invention in block diagram form;

FIG. 2 illustrates the logic circuit diagram of a flip-flop and multivibrator of the present invention showing the output pulses therefrom;

FIG. 3 illustrates a schematic block and logic diagram of the memory circuit;

FIG. 4 shows the digital binary switching circuit of the present invention in block-logic diagram form;

FIG. 5 illustrates a second embodiment of a flip-flop circuit;

FIG. 6 illustrates a third embodiment of a flip-flop circuit; and

FIG. 7 illustrates a logic circuit control for selecting returned illumination exclusively at various distinct ranges.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 shows, in block diagram form, the components used in the operation of a digital gating system that causes pulsed illumination returned from all useable ranges back into an image intensifier (not shown) to appear at equal intensity at the output of the image intensifier. The actual intensity of returned illumination from a target diminishes with the distance of the target from the image intensifier in accordance with the inverse square law. When a pulse from the pulsed illuminator (not shown) is directed parallel to the optical axis of the image intensifier, the same pulse is present at terminal 10 and is simultaneously applied to flip-flop 20 to set the flip-flop. With flip-flop 20 in the set condition, two outputs are produced therefrom. One output is the leading edge of a pulse that is applied to address binary counter 40 by lead 17. The other output is applied to gated astable multivibrator 30 by lead 27 and starts 30 to free run until a reset signal (explained hereinbelow) is applied to flip-flop 20. Multivibrator 30, therefore, starts free running in time relationship with initiation of the pulse from the pulse illuminator. The multivibrator 30 may be constructed from standard TTL logic. The reset pulse is not received on flip-flop 20 until multivibrator 30 free runs through a four stage binary counter 100 whose outputs are simultaneously applied to a steering gate NAND circuit 110, that provides the reset pulse, and to a four bit binary comparator 80, that compares the outputs of 100 with signals from a read only memory 60. A reset pulse is produced at the output of circuit 110 when the 1, 2, and 8 outputs are all generated from the four stage binary counter 100. The reset pulse is applied back to both 20 and 100. Counter 100 and flip-flop 20 are stopped by the reset pulse. Multivibrator 30 ceases operation until it is again activated by flip-flop 20 and starts counter 100 through another cycle of operation. When the reset pulse is produced, the flip-flop flops over to the reset position and remains there until the illuminator again sets the flip-flop. When the flip-flop is reset, a trailing edge from flip-flop 20 is produced on lead line 17 to advance counter 40 for the next cycle of operation. This pulse is shown in FIG. 4.

Refer now to FIGS. 2, 3 and 4 along with FIG. 1 for a more detailed explanation of the digital gating system. Major components are shown in FIG. 1 with these components further elaborated on in FIGS. 2, 3, and 4. The address counter 40 outputs are applied to a read only memory 60. The read only memory 60 has a program therein which controls the number of times that the image intensifier is activated as time increases from one pulse to the occurrence of a subsequent pulse with the program repeated over and over again. The number of times that the image intensifier is turned on is increased as time elapses from the instant of each pulse until the occurrence of a subsequent pulse, with the total turn on time at any given range corresponding to the inverse square law. Thus, as the intensity of returned illuminations from a more distant target is decreased according to the inverse square law, the apparent brightness is equalized by squaring the number of turn on times of the image intensifier. Table I shows pertinent figures for either nine or ten delay steps of the entire range sweep.

The number of delay steps are self explanatory since they indicate the number of steps that are programmed in the read only memory 60. Even though both the results of the ten delay step and the nine delay step programs are shown, applicant believes that the nine delay step program is the best program since the program is a little simpler and no noticeable flicker occurs with the one less delay step, yet the apparatus brightness of returned illumination appears to be the same. The nine delay step program will be used in explaining the operation of the system. The ninth delay is the last delay step per sweep and represents the maximum useable range of the image intensifier. The integral number represents the number of times that the image intensifier gate is on out of a total of 64. The read only memory 60 has a 64 word and 4 bit output which is available as a total of 64 samples or returned illumination per system cycle.

TABLE I

NO. OF DELAY STEPS	CALC. NO.	ADJ NO.	INTEGRAL NO.	NO. OF DELAY STEPS	CALC. NO.	ADJ NO.	INTEGRAL NO.	NO. OF TURN- ONS
1	1	.64	1	1	1	.79	1	1
2	4	2.56	3	2	4	3.16	3	2
3	9	5.76	6	3	9	7.11	7	4
4	16	10.24	10	4	16	12.64	13	6
5	25	16.0	16	5	25	19.75	20	7
6	36	23.04	23	6	36	28.44	28	8
7	49	31.36	31	7	49	38.72	39	11
8	64	40.96	41	8	64	50.51	51	12
9	81	51.84	52	9	81	64.0	64	13
10	100	64.0	64					

The samples are shown in Table I as integral numbers. The number of turn-ons at each delay time is shown in the right most column of the nine delay steps and represents the turn-ons at each of the nine selected range limits with the total turn-ons being 64. The number of samples at a given delay step are the sum of the turn-ons at that step plus all those at lower numbered delay steps. For example, at delay step 4 there are six turn-ons plus four at step 3 plus 2 at step 2 plus one at step 1, for a total of 13, the number of samples at that delay. The calculated (calc) numbers show the square of the number of each delay step. The adjusted (adj) numbers represent a proportionate reduction of the numbers in the calculated column to adjust the largest number to match the number of words available in the memory.

The read only memory 60 has a 32 word and 8 bit-per-word output further broken down into a 64 word and 4 bit output. The output is hypothetically chosen as binary contents A and binary contents B. The programmed read only memory for a binary address of 2⁴, or 16, from address counter 40 is shown in Table II. The contents of the programmed read only memory are in a scrambled sequence designed to reduce flicker of returned illumination through the image intensifier.

TABLE II

Half of Contents of Programmed Read Only Memory at a Scrambled Sequence to Minimize Flicker of Image																		
Address No.		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Contents:	A -	9	2	8	4	7	9	6	8	5	7	3	9	6	8	4	7	9
	B -	9	2	8	4	7	9	6	8	5	7	3	9	6	8	4	7	1
Binary Address:	A ₄ -	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
{	A ₃ -	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
	A ₂ -	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1	0
	A ₁ -	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
	A ₀ -	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

TABLE II—Continued

Half of Contents of Programmed Read Only Memory at a Scrambled Sequence to Minimize Flicker of Image																		
Binary Contents:		{	0 ₁ -	1	0	1	0	0	1	0	0	0	1	0	1	0	0	1
A		{	0 ₂ -	0	0	0	1	1	0	1	0	1	1	0	1	1	0	0
		{	0 ₃ -	0	1	0	0	1	0	1	0	0	1	0	0	1	0	0
		{	0 ₄ -	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1
		{	0 ₅ -	1	0	1	0	0	1	0	0	0	1	0	0	0	0	0
B		{	0 ₆ -	0	0	0	1	1	0	1	0	1	0	1	1	0	0	1
		{	0 ₇ -	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0
		{	0 ₈ -	1	0	0	0	1	1	1	0	1	0	0	0	0	1	1
		{	0 ₉ -	1	0	0	0	1	1	1	0	0	0	0	0	1	1	0

FIG. 2 illustrates one embodiment of flip-flop 20 and multivibrator 30 circuits showing their inputs and outputs. A negative going leading edge start pulse from terminal 10 sets the flip-flop 20 which produces an output pulse therefrom by lead 27 that starts 30 to free running for producing two trains of output pulses that

are 180 degrees phase shifted from each other. The train of pulses at the output of NAND gate 31, present on lead 37, are applied to binary counter 100. The output pulses from NAND gate 32 is not connected to any useable circuit. A negative going trailing edge pulse on lead 200, produced at the output of NAND gate 110 after binary counter 100 has cycled through its entire count, resets flip-flop 20.

FIG. 3 shows a schematic block and logic diagram of the memory circuit illustrating the binary inputs A₀ through A₄ into the read only memory from address counter and binary input A₅ that is directly applied to NAND gates 66-69 and is inverted by inverter 61 and applied to NAND gates 62-65. The other inputs to NAND gates 62-69 are applied directly from the read only memory 60. Outputs from 62-65 and 66-69 are applied to four NAND gates 72, 74, 76, and 78 thus giving the read only memory 60 a total of 64 word and 4 bit outputs therefrom. The various 4 bit outputs are applied to 4-bit comparator 80 and are compared with the four outputs from 4-stage binary counter 100. The output from comparator 80 produces a leading edge pulse into the gated switches and power supply 120, with the timing of one of a total of nine leading edges being determined by the sequence of programs that are being cycled through the read only memory 60. For each of the bit inputs to address counter 40, the 4-stage binary counter 100 has cycled through one complete sweep and produced an output to comparator 80 to compare one of the 64 possible outputs from the read only memory 60 that is present at the other inputs to comparator 80. The total time that the power supply is applied to the image intensifier is illustrated by curves at output terminal 130. The minimum delay represents power supply application at the nearest target ranges with the power supply application increasing toward the maximum range of the image intensifier as the read

only memory program is cycled through its program of nine delay steps.

FIG. 4 illustrates the digital binary switching circuit in block-logic diagram form with slight variations of some circuits as shown in FIGS. 1 and 2. Flip-flop 20 has an additional NAND gate 23 connected between terminal 10 and the set portion of the flip-flop. NAND gate 23 presents the proper pulse phase to the flip-flop. The address counter 40 is shown as two 4-bit binary counters, even though one 6-bit binary counter is sufficient when the program in 60 is for only 64 word output. The output of comparator 80 is also different in the embodiment shown in FIG. 4. Both a high and a low signal from comparator 80 will cause NAND gate 111 to operate and produce a signal at the input of NAND gate 113, which produces a leading edge pulse that is applied to 120. Further, NAND gates 112 and 114 are substituted for the single NAND gate 110 for producing a trailing edge to 120 and reset pulses to both 20 and 100.

FIGS. 5 and 6 show two different embodiments of flip-flop circuits that may be used in the digital gating system. In FIG. 5, NAND gate 236 receives the three outputs from delay binary counter 100. A first voltage holding network, comprising a +5 volts d.c. power supply connected in parallel with resistor 238 and diode 240, and capacitor 242 connected to ground on one side and on the other side to the junction of the resistor and diode that is opposite the d.c. power supply, is connected to a first input of NAND gate 234. A second input to 234 comes from 236. The first voltage holding network keeps a regulated 5 d.c. volts on the first input to 234 so that NAND gate 234 will only trigger when a positive pulse of about 5 d.c. volts is received from 236. NAND gate 232 isolates NAND gate 234 from the flip-flop circuit, comprising NAND gates 228 and 230. The first voltage holding network and accompanying NAND gates 232, 234, and 236 keeps the flip-flop from false triggering into the reset mode. A second voltage holding network, comprising capacitor 226, parallel connected resistor 222 and diode 224, and 5 d.c. volt power supply, holds 5 d.c. volts on one input to NAND gate 220. Another input to NAND gate 220 is from the illuminator trigger at terminal 10. The second voltage holding network holds the timing start-stop flip-flop 20 in the reset, or stop, mode until the logic power has risen to a level sufficient for stable operation. The function of this voltage holding network is to force the logic to predictable states at the first application of power to the system, thus preventing possible lock-up which could occur with a system power supply that came on slowly. The nature of this lock-up is as follows. The flip-flop 20 can just as easily go into the set mode as the reset mode during turn-on. A slow rise of voltage to the multivibrator 30 can result in the multivibrator not oscillating even though it is receiving an enable signal from flip-flop 20. The capacitor 226 and 242 hold the inputs to their gates of 220 and 234 at a low level for a finite time after application of power supply voltage, thus forcing flip-flop 20 (gates 228 and 230) to initially assume a reset condition. The capacitors then charge through resistors 222 and 238 to allow normal operation until the power is removed from the system. Capacitors 226 and 242 are then discharged through diodes 224 and 240. The function and operation of FIG. 6 is similar. The +5 volts points shown in FIG. 6 is the supply voltage to the entire logic system.

In the flip-flop circuit of FIG. 6, the outputs from binary delay counter 100 are applied to NAND gate 334. The output from NAND gate 334 is applied directly to one input of a three input NAND gate 326 of the flip-flop circuit comprising NAND gates 322 and 326. A second input to 326 is applied from a third voltage holding network, comprising capacitor 330, resistor 328, diode 332 and 5 d.c. volt power supply, with this voltage holding network operating the same as the other voltage holding networks. A fourth voltage holding network is connected to one input to NAND gate 320, with a second input thereto being applied from the trigger illuminator at terminal 10. The fourth voltage holding network comprises capacitor 344, resistor 340, diode 342, and 5 d.c. volt power supply.

FIG. 7 shows an embodiment wherein memory steering logic is modified to allow selection of a single range by using a complimentary output digi-switch. Eight, three input NAND gates 360 through 376 are substituted for the eight, two input NAND gates 62 through 69 shown in FIGS. 1 and 3. One input is from address counter 40, shown as A_5 and functioning the same as A_5 in FIG. 4. The address A_5 is connected directly to the four NAND gates 360-366, and is inverted by inverter 368 before being applied to the four NAND gates 370-376. Eight outputs from the read only memory, designated as M1 through M8, are shown as the third inputs to NAND gates 360-376. These eight outputs, or bit numbers in the memory output word, are separated into four binary contents A and four binary contents B. The binary contents A and B that correspond to their related binary addresses from address counter 40 are shown in Table II. If the complimentary output digi-switch is at 0 output, then the outputs from NAND gates 390 through 396 to the binary comparator 80 follows the bit numbers M1 through M8 in the memory output word. However, if the digi-switch is at any of its other binary output settings, these settings will be reflected at the outputs of 390 through 396 into the binary comparator. By having the complimentary output digi-switch inserted into the memory steering logic as shown in FIG. 7, a single range may be selected for viewing to the exclusion of the other ranges.

It is to be understood that although the invention has been described with specific reference to particular embodiments thereof, it is not to be so limited since changes and alterations therein may be made which are within the full intended scope of this invention as defined by the appended claims.

I claim:

1. A digital gating system for an image intensifier in which the image intensifier is gated on in accordance with the inverse square law in range, the system comprising:

- a pulsed illuminator source producing output trigger pulses therefrom;
- a switching circuit having a first and a second input and a first and a second output therefrom with first of said inputs being connected to and operating simultaneously with said pulsed illuminator;
- a pulsing circuit having an input connected to said first output from said switching circuit;
- a four stage binary counter having a first and a second input and four outputs therefrom;
- an address counter having an input connected to said second output from said switching circuit and having multiple outputs therefrom;

a read only memory having multiple inputs that are connected to said multiple outputs from said address counter and having four outputs therefrom, said read only memory having stored therein an assigned number of switching pulses in a total cycle of sixty four switching pulses at each delay on said multiple outputs from said address counter to the input of said read only memory;

a four bit binary comparator having four inputs from said read only memory and four inputs from said four stage binary counter and two outputs therefrom;

a logic circuit having three inputs from three of said four outputs from said four stage binary counter and having an output therefrom; and

gates switches and power supply having a first and a second input and an output therefrom wherein said output from said logic circuit produce a trailing edge pulse when said four stage binary counter has cycled through all four outputs wherein said trailing edge pulse is simultaneously applied to said first input of said gated switches and power supply and to said second input of said switching circuit for stopping said switching circuit and to said four stage binary counter for resetting said four stage binary to receive the next output trigger pulse from said pulsed illuminator source for triggering said switching and pulsing circuits and wherein said output from said four bit binary comparator produces a leading edge that is applied to said second input to said gated switches and power supply whereby said leading edge is varied in time commensurate with the inverse square law of returned illumination and said leading edge activates switches within said gated switches and power supply that applies said power supply to an image intensifier tube and said trailing edge deactivates said switches to remove said power supply from said image intensifier.

2. A digital gating system as set forth in claim 1 wherein said address counter has six outputs with five of said outputs applied directly to said read only memory to apply binary counts thereto and said sixth output is applied directly to four of eight outputs from said read only memory and through an inverter to the other four of said eight outputs for producing a total 64 word and 4 bit outputs from said read only memory in which

a programmed number of the 64 words are used at each binary count delay representing range.

3. A digital gating system as set forth in claim 2 wherein said binary count delay representing range is a total of nine delays through the entire useable range of the image intensifier.

4. A digital gating system as set forth in claim 2 wherein said binary count delay representing range is a total of ten delays through the entire useable range of the image intensifier.

5. A digital gating system as set forth in claim 3 wherein read only memory comprises steering logic having eight outputs connected to first inputs of eight NAND logic circuits in parallel with the first four of said eight NAND logic circuits having a second input thereto directly from said sixth input from said address counter and the second four of said eight NAND logic circuits having a second input thereto which is an inverted said sixth output from said address counter wherein the four outputs from each of said first and second four NAND logic circuits are respectively cross connected as first and second inputs to a third four NAND logic circuits providing said 64 word and 4 bit output therefrom to said four binary comparator.

6. A digital gating system as set forth in claim 5 wherein said two outputs from said comparator have either a high voltage on one of said outputs or a low voltage on the other of said outputs in which the two outputs are applied to an NAND logic circuit that produces multiple output leading edge pulses according to the time lapsed with respect to the inverse square law from each illumination pulse wherein the multiple output leading edge pulses switch on said gate switches and power supply for providing power to the image intensifier over a longer period of time as the time lapse increases from the time of the illumination pulse.

7. A digital gating system as set forth in claim 6 wherein said read only memory further comprises a complimentary output digi-switch having four binary outputs therefrom that are sequentially connected to said third four NAND logic circuits and is serially connected to an NAND logic circuit and inverter as a third input to all of said first and second four of said eight NAND logic circuits to allow for selection of a single range by selecting the output of said digi-switch.

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