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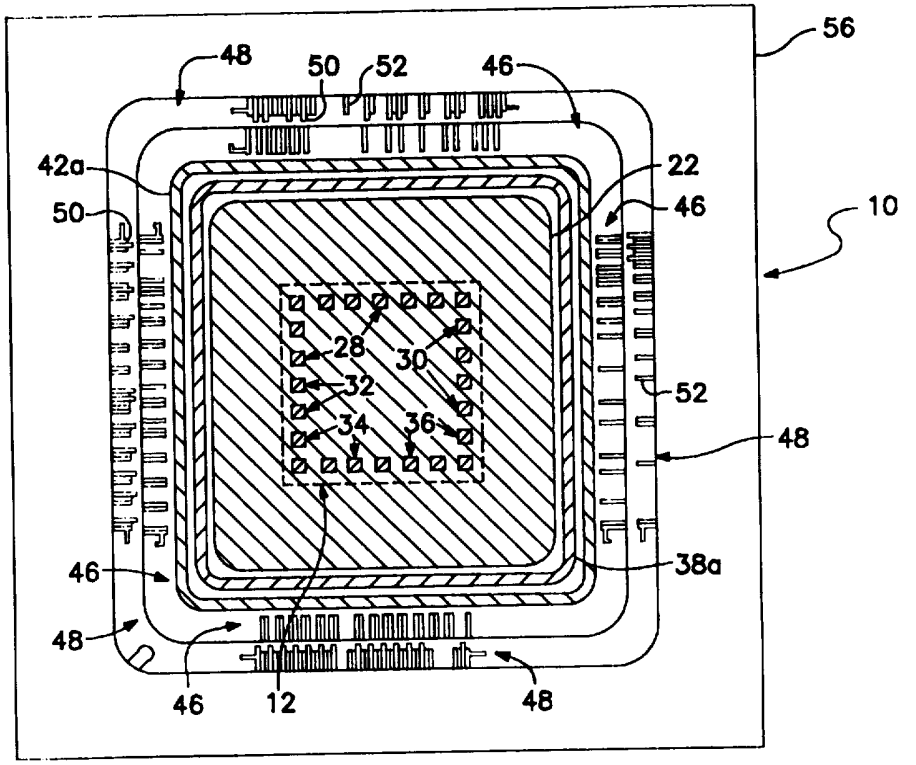
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(54) Title: HIGH PERFORMANCE INTEGRATED CIRCUIT PACKAGE

(57) Abstract

A high performance integrated circuit package (10) placed on a printed circuit (PC) board (56) and having a first dielectric layer. On top of this first dielectric layer a metallized die pad (22) and a first metal ring (38a), surrounding this metallized die pad, are positioned. The metallized die pad and the first metal ring electrically couple to the PC board to receive respectively a first power supply signal and a second power supply signal. An integrated circuit die (12) is then affixed to the metallized die pad. This integrated circuit die (12) has a first power supply signal bond pad (28, 30) and a second power supply signal bond pad (33, 34), which respectively are coupled to the metallized die pad and the first metal ring. Consequently, the metallized die pad and the first metal ring operate as a first power supply plane and a second power supply plane coupling the first and second power supply signals coming from the PC board to the first and second power supply signal bond pads on the integrated circuit die.



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HIGH PERFORMANCE INTEGRATED CIRCUIT PACKAGE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of high performance integrated circuit packaging.

2. Art Background

Traditionally, microprocessors have been packaged in ceramic pin grid array packages because of electrical and thermal performance requirements. More specifically, the high instruction execution speed of microprocessors places two limitations on the design of packaging for microprocessors. First, since power consumption is a function of the instruction execution speed and since microprocessors operate at high instruction execution speeds, the conservation of energy is one limitation placed on the design of packaging for microprocessors. Second, the high instruction execution speed of microprocessors requires the packaging to minimize the time for removing and supplying the transient power supply currents (e.g., the transient ground and the transient V_{CC} supply currents) to the microprocessor die, in order to allow the circuit nodes to charge and discharge as quickly as possible.

The conservation of energy and time constraints can both be satisfied by providing the shortest paths from the printed circuit (PC) board to the die for the power supply signals (e.g. the ground supply signal and the V_{CC} supply signal). In other words, energy is conserved by minimizing the distance that the power supply signals have to traverse from the PC board to

the die, because the power supply signals encounter less obstructions (i.e., resistance and inductance) in the path. Furthermore, the time for supplying and removing the transient power supply currents from the PC board to the die is also minimized by minimizing the distance that the power supply signals have to traverse from the PC board to the die.

In the past, microprocessors have been packaged mostly in ceramic pin grid array packages, because the prior art solutions for shortening the power supply signal paths (from the PC board to the die) often cannot be successfully implemented in other types of packaging. One prior art method for shortening the power signal paths is the placement of capacitive electrical planes within the package. These capacitive electrical planes (which are also called thin layer capacitors) are connected to the power supply signals, and thus provide a local on-chip power source that can be quickly accessed by the die.

Unfortunately, capacitive electrical planes can only be implemented in a few types of materials. The feasibility of implementing capacitive electrical planes depends on the minimum separation distance that can be achieved between each power and ground plane and the dielectric constant of the package. Thus, since ceramic packages have high dielectric constants and provide for small separation distances, capacitive electrical planes can be implemented in ceramic packages. However, as mentioned above, capacitive electrical planes cannot be implemented in all types of packages. For example, the cheaper plastic package technology cannot use capacitive electrical planes to shorten the power supply signal paths, because plastic packages have a low dielectric constant and cannot provide small separation distances between adjacent electrical planes.

Another prior art solution for shortening the paths of the power supply signals is to mount chip capacitors on the package, and to couple these capacitors to the power supply signals so that these capacitors act as local sources of power. However, as the chip capacitors are expensive, this prior art solution increases the processing cost of the microprocessors.

Consequently, it would be desirable to provide a packaging method and apparatus for microprocessors that would cost effectively conserve energy and time in delivering the power supply signals from the PC board to the die. More specifically, a packaging method and apparatus for microprocessors is needed that would provide the shortest power signal paths from the PC board to the die without the use of capacitive electrical planes (which cannot be implemented in all types of packaging) and without the use of chip capacitors (which are expensive).

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a packaging method and apparatus for microprocessors that would cost effectively conserve energy and time in delivering power supply signals from the PC board to the die. More specifically, it is an object of the present invention to provide a packaging method and apparatus for microprocessors that would provide for the shortest power signal paths from the PC board to the die without the use of capacitive electrical planes and without the use of chip capacitors.

These and other objects of the present invention are accomplished by a high performance integrated circuit package which is placed on a printed circuit (PC) board. This high performance package has a first dielectric layer, on top of which a metallized die pad and a first metal ring, surrounding this metallized die pad, are positioned. The metallized die pad and the first metal ring electrically couple to the PC board to receive respectively a first power supply signal and a second power supply signal. An integrated circuit die is then affixed to the metallized die pad. This integrated circuit die has a first power supply signal bond pad and a second power supply signal bond pad, which respectively are coupled to the metallized die pad and the first metal ring. Consequently, the metallized die pad and the first metal ring operate as a first power supply plane and a second power supply plane coupling the first and the second power supply signals coming from the PC board to the first and the second power supply signal bond pads on the integrated circuit die.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, wherein:

Figure 1 presents a top view of a ball grid array package for one embodiment of the present invention;

Figure 2 presents a side cross-sectional view of the ball grid array package of **Figure 1**;

Figure 3 presents an enlarged cross-sectional view of the ball grid array package of **Figure 1**.

Figure 4 presents the high performance integrated circuit package of the present invention housing a microprocessor of a general purpose computer system.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides an integrated circuit packaging method and apparatus that takes advantage of the high performance qualities of ball grid array (BGA) packages. More specifically, since solder balls can be affixed to integrated circuit packages with relatively small distances (e.g., 50 mils) between adjacent balls, BGA packages have a high solder ball density. In turn, the high solder ball density of BGA packages allow them to have a relatively small size. As described below, the package design of the present invention then utilizes the high solder ball density and small size of BGA packages to provide the shortest power supply signal paths.

In the following description, for purposes of explanation numerous details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the invention. For example, although the following description of the invention is with respect to BGA packages, it will be understood by one skilled in the art that pin grid array (PGA) packages can be used to implement the present invention if their pin density and adjacent pin spacing are comparable to the ball density and adjacent ball spacing of BGA packages.

Figures 1-3 present one embodiment of the packaging method and apparatus of the present invention. As shown in these figures, plastic package 10 houses an integrated circuit 12, which in one embodiment of the present invention is a microprocessor. In addition, although a plastic package is described for the embodiment of the present invention that is set forth in **Figures 1-3**, it is to be understood that package 10 may be composed

of other types of material. Package 10 has a plurality of connectors 14 which are affixed to the bottom surface of the package. These connectors form contacts with metal pads on a PC board, and thereby couple package 10 to the PC board. For the embodiment of the present invention that is set forth in **Figures 1-3**, the connectors are solder balls. However, as mentioned before, other types of connectors (e.g., pins) can be used if their density and adjacent spacing are comparable to the ball density and adjacent ball spacing of BGA packages.

For the embodiment of the present invention that **Figures 1-3** set forth, package 10 has the following three layers of dielectric material: first dielectric layer 16, second dielectric layer 18, and third dielectric layer 20. On the top surface of the first dielectric layer of package 10, first metallized die pad 22 is affixed to package 10. In one embodiment of the present invention, first metallized die pad 22 is affixed to package 10 through a lamination process. This die pad is electrically and thermally connected through plated vias 24 to second metallized pad 26, which is attached to the bottom surface of first dielectric layer 16. In turn, through solder balls 14a coupled to second metallized pad 26, first metallized die pad 22 couples to a first power supply signal on the PC board. In the embodiment of the present invention that is set forth in **Figures 1-3**, the first power supply signal is the core ground supply signal V_{SS}. However, it is to be understood that the first power supply signal can be any one of a number of different types of power supply signals.

Microprocessor die 12 is then attached to first metallized die pad 22 by an electrically and thermally conductive adhesive. Microprocessor die 12 contains a plurality of bond pads including core ground bond pads 28, peripheral ground bond pads 30, core V_{CC} bond pads 32, peripheral V_{CC}

bond pads 34, and individual signal bond pads 36. The core ground bond pads are all shorted together by wire bonding them to die pad 22. Thus, a shortest electrical (i.e., lowest inductance) path from the core ground bond pads on the die to the core ground supply signal on the PC board is established through first metallized die pad 22, vias 24, second metallized pad 26, and solder balls 14a. This shortest path is independent of the die size and package size.

Package 10 also includes a first set of metal rings 38 that surround the metallized pads on both the top and bottom sides of first dielectric layer 16. Top side ring 38a and bottom side ring 38b of the first set of metal rings are electrically and thermally connected together through plated vias 40. Through solder balls 14b, the bottom side first metal ring couples to a second power supply signal on the PC board. In the embodiment of the present invention that is set forth in **Figures 1-3**, the second power supply signal is the core V_{CC} supply signal. However, it is to be understood that the second power supply signal can be any one of a number of different types of power supply signals. The core V_{CC} bond pads on the microprocessor die are all shorted together by wire bonding them to the top first metal ring. Thus, a short electrical (i.e., a low inductance) path from the core V_{CC} bond pads on the die to the core V_{CC} supply signal on the PC board is established through top first metal ring 38a, vias 40, bottom first metal ring 38b, and the solder balls 14b.

As further shown in the figures, package 10 also includes second set of metal rings 42 that surround the metallized pads and first set of metal rings on both the top and bottom surfaces of the first dielectric layer 16. Top side ring 42a and bottom side ring 42b of the second set of metal rings are electrically and thermally connected together through plated vias 44. The

bottom side second metal ring is coupled to a third power supply signal on the PC board through solder balls 14c that are attached to it. In the embodiment of the present invention that is set forth in **Figures 1-3**, the third power supply signal is the peripheral ground supply signal V_{SSP}. However, it is to be understood that the third power supply signal can be any one of a number of different types of power supply signals.

The peripheral ground bond pads on the microprocessor die are all shorted together by wire bonding them to the top second metal ring. In this manner, the second set of metal rings is used to couple the peripheral ground bond pads on the die to the peripheral ground supply signal on the PC board. This embodiment of the present invention provides peripheral power supply connections in order to isolate the power supplies that are used by the microprocessor's core activities (e.g., instruction executions) from the "noisier" power supplies that are used for the microprocessor's peripheral activities (e.g., communication with other devices).

As further shown in the figures, package 10 also has two rows of bond fingers. The first row of bond fingers 46 is placed on the top surface of the first dielectric layer 16 (which constitutes a first lower bonding shelf) along with the metallized die pad 22, first top metal ring 38a, and second top metal ring 42a. The first row of bond fingers 46 has a number of individual signal bond fingers which are used for individual signal connections. More specifically, a specific signal bond pad on the microprocessor die can be coupled to a specific signal coming from the PC board through wire bonding the specific signal bond pad to a specific signal finger; in turn, the specific signal finger couples to an individual trace that traverses along the length or width of the package (i.e., traverses along either a portion of the length or width of the package or the entire length or width of the package) to an

individual via and an individual solder ball that receive the specific signal on the PC board.

Second row of bond fingers 48 is placed on the top surface of the third dielectric layer 20 (constituting a second higher bonding shelf), which itself is positioned on top of the second dielectric layer 18. As shown in **Figures 1-3**, the second and third dielectric layers surround first metallized die pad 22, first top metal ring 38a, second top metal ring 42a, and first row of bond fingers 46. In addition, the second and third dielectric layers are offset from the central axis of the package by a predetermined amount so as to allow the die pad, top metal rays, and first row of bond fingers to be exposed.

The second row of bond fingers includes two types of bond fingers. The first type of bond fingers are fourth power supply bond fingers 50, which are shown in **Figure 1** as the longer bond fingers. These fourth power supply bond fingers traverse the edge of the cavity formed by first, second, and third dielectric layers and couple to metallized plane 54 which is positioned in between the top surface of the second dielectric layer and the bottom surface of the third dielectric layer. This metallized plane through at least one via couples to at least one solder ball, which in turn couples to a fourth power supply signal on the PC board. In this manner, metallized plane 54 shorts all fourth power supply fingers to the fourth power supply signal.

In the embodiment of the present invention that is set forth in **Figures 1-3**, the fourth power supply signal is the peripheral V_{CC} supply signal (V_{CCP}). However, it is to be understood that the fourth power supply signal can be any one of a number of different types of power supply signals. In addition, as mentioned before, this embodiment of the present invention provides peripheral V_{CC} supply signal connections in order to

separate the V_{CC} supply signal used for the core activities of the microprocessor from the "noisier" V_{CC} supply signal used for the peripheral activities of the microprocessor.

In the embodiment of the present invention that is set forth in **Figures 1-3**, the second row of bond fingers also include a second type of bond fingers. However, it is to be understood that in alternative embodiments of the present invention, the second row of bond fingers could include only the fourth power supply bond fingers. In the embodiment set forth in **Figures 1-3**, the second type of bond fingers on the second row are additional individual signal bond fingers 52, whereby each specific signal finger couples a specific signal bond pad on the microprocessor die to a specific signal coming from the PC board through a wire interconnect, a particular trace (traversing the length or width of the package), a particular via, and a particular solder ball. In this embodiment, the second row of individual signal bond fingers are provided in order to allow adjacent individual signal bond pads on the die to couple to individual signal bond fingers. More specifically, since currently the minimum spacing that can be achieved between individual bond fingers is 200 microns, while the minimum separation that can be achieved between individual bond pads is 100 microns, this embodiment of the present invention provides a second row of signal fingers so as to allow adjacent individual signal bond pads to couple to individual signal bond fingers. Finally, package 10 has plastic top 56 that further forms (along with the first, second, and third dielectric layers) the cavity in which a molding compound encapsulent is poured in order to enclose the top of the BGA package.

Figure 4 presents the high performance integrated circuit package of the present invention housing a microprocessor of a general purpose

computer system. As shown in this figure, computer system 60 is housed on printed circuit (PC) board 62 and includes bus 64, microprocessor 66, high performance microprocessor package 68, power supply signal generator 70, and memory 72. High performance microprocessor package 68 couples microprocessor 66 to bus 64 in order to communicate power supply signals and non-power supply signals between microprocessor 66 and devices coupled to bus 64. For the embodiment of the present invention shown in **Figure 4**, bus 64 couples microprocessor 66 to memory 72 and power supply signal generator 70. However, it is to be understood that in alternative embodiments of the present invention, microprocessor 66 can be coupled to memory 72 and power supply signal generator 70 through two different buses. In addition, in alternative embodiments of the present invention, power supply signal generator 70 is not positioned on PC board 62 in order to couple to bus 64.

Thus, the present invention has numerous advantages. For example, by using the shortest paths from the die to the PC board as the power supply signal paths (i.e., by using the balls near the center of the package for V_{CC} and ground connections), the present invention lowers the power loop inductance without using on-chip capacitors and capacitive electrical planes. In addition, since this design uses the balls near the center of the package for power supply connections and the balls from the outer rows of the package for the signal connections, the signal routing on the PC board is simplified (i.e., additional routing layers are not needed to route the balls near the center of the package). Furthermore, the method and apparatus of the present invention minimizes the multiple metal and substrate layers by placing the die pad, and first and second top metal rings on one bonding shelf (i.e., the first bonding shelf), which thereby makes

areas outside the metal rings on the top side of the package available for signal connections.

It will be recognized that the above described invention may be embodied in other specific forms without departing from the spirit or essential characteristics of the disclosure. For example, although the description above is with respect to a package having two bonding shelves, it will be understood by one skilled in the art that alternative embodiments of the invention include integrated circuit packages having only one bonding shelf. For instance, one embodiment of the present invention has only one bonding shelf (1) because, instead of fourth power supply bond fingers 50 and metallized plane 54, it uses a third set of metal rings surrounding second set of metal rings 42 to couple fourth power supply bond pads 34 to the fourth power supply on the PC board, and (2) because it uses only one row of signal bond fingers (i.e., first row of signal bond fingers 46), surrounding metallized die pad 22, first top metal ring 36a, second top metal ring 42a, and the third top metal ring, to couple individual signal bond pads on the die to individual signals on the PC board. Thus, while certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that the invention is not to be limited by the foregoing illustrative details, but rather is to be defined by the appended claims.

CLAIMS

I claim:

1. A high performance integrated circuit package for coupling to a printed circuit (PC) board and for housing an integrated circuit die, the integrated circuit die having a first power supply signal bond pad and a second power supply signal bond pad, the package comprising:

a) a first dielectric layer;

b) a metallized die pad for electrically coupling to the PC board to receive a first power supply signal, said metallized die pad affixed to the first dielectric layer, said metallized die pad for housing said integrated circuit die and for coupling to said first power supply signal bond pad; and

c) a first metal ring surrounding the metallized die pad, said first metal ring for electrically coupling to the PC board to receive a second power supply signal and for coupling to said second power supply signal bond pad.

2. The high performance integrated circuit package of claim 1, wherein the integrated circuit die further has a third power supply signal bond pad, the package further comprising a second metal ring surrounding the first metal ring, said second metal ring for electrically coupling to the PC board to receive a third power supply signal and for coupling to said third power supply signal bond pad.

3. The high performance integrated circuit package of claim 2, wherein the integrated circuit die further has a first non-power supply signal bond pad, the package further comprising a first row of bond fingers surrounding the second metal ring, said first row of bond fingers having a first bond finger for receiving a first non-power supply signal from the PC board and for coupling to said first non-power supply signal bond pad.

4. The high performance integrated circuit package of claim 3, wherein the integrated circuit die further has a fourth power supply signal bond pad, the package further comprising:

a) a second dielectric layer positioned on top of the first dielectric layer so as to expose the metallized die pad, the metal rings, and the first row of bond fingers; and

b) a second row of bond fingers positioned on the second dielectric layer, the second row of bond finger having a second bond finger for receiving a fourth power supply signal from the PC board and for coupling to said fourth power supply signal bond pad.

5. The high performance integrated circuit package of claim 4 further comprising:

a) a third dielectric layer positioned in between the first and the second dielectric layers; and

b) a metallized plane positioned in between the second and the third dielectric layers, said metallized plane for coupling said fourth power supply signal to said second bond finger.

6. The high performance integrated circuit package of claim 5, wherein the integrated circuit die further has a second non-power supply signal bond pad, the second row of bond fingers further having a third bond finger for receiving a second non-power supply signal from the PC board and for coupling to said second non-power supply signal bond pad.

7. The high performance integrated circuit package of claim 5, wherein said integrated circuit is a microprocessor.

8. The high performance integrated circuit package of claim 5, wherein said package is a ball grid array package.

9. A high performance integrated circuit package for coupling to a printed circuit (PC) board, the package comprising:

a) a first dielectric layer;

b) a metallized die pad for electrically coupling to the PC board to receive a first power supply signal, said metallized die pad affixed to the first dielectric layer;

c) an integrated circuit die positioned on top of said metallized die pad so as to expose a portion of the metallized die pad, said integrated circuit die having a first power supply signal bond pad and a second power supply signal bond pad, said first power supply signal bond pad coupled to the exposed portion of said metallized die pad; and

d) a first metal ring surrounding the metallized die pad, said first metal ring for electrically coupling to the PC board to receive a second power supply signal, said second power supply signal bond pad coupled to the first metal ring.

10. The high performance integrated circuit package of claim 9, wherein the integrated circuit die further has a third power supply signal bond pad, the package further comprising a second metal ring surrounding the first metal ring, said second metal ring for electrically coupling to the PC board to receive a third power supply signal, said third power supply signal bond pad coupled to the second metal ring.

11. The high performance integrated circuit package of claim 10, wherein the integrated circuit die further has a first non-power supply signal bond pad, the package further comprising a first row of bond fingers surrounding the second metal ring, said first row of bond fingers having a first bond finger for receiving a first non-power supply signal from the PC board, said first non-power supply signal bond pad coupled to said first bond finger.

12. The high performance integrated circuit package of claim 11, wherein the integrated circuit die further has a fourth power supply signal bond pad, the package further comprising:

a) a second dielectric layer positioned on top of the first dielectric layer so as to expose the metallized die pad, the metal rings, and the first row of bond fingers;

b) a third dielectric layer positioned on top of the second dielectric layer so as to expose the metallized die pad, the metal rings, and the first row of bond fingers; and

c) a second row of bond fingers positioned on the third dielectric layer, the second row of bond finger having a second bond finger for receiving a fourth power supply signal, said second bond finger coupled to said fourth power supply signal bond pad.

13. The high performance integrated circuit package of claim 12 further comprising a metallized plane positioned in between the second and third dielectric layers, said metallized plane for coupling said fourth power supply signal to said second bond finger.

14. The high performance integrated circuit package of claim 13, wherein the integrated circuit die further has a second non-power supply signal bond pad, the second row of bond fingers further having a third bond finger for receiving a second non-power supply signal from the PC board, said third bond finger coupled to said second non-power supply signal bond pad.

15. The high performance integrated circuit package of claim 13, wherein said integrated circuit is a microprocessor.

16. The high performance integrated circuit package of claim 13, wherein said package is a ball grid array package.

17. A high performance integrated circuit package for coupling to a printed circuit (PC) board, the package comprising:

a) a first dielectric layer having a top and a bottom surface;

b) a top metallized die pad affixed to the top surface of the first dielectric layer;

c) a bottom metallized pad for electrically coupling to the PC board to receive a first power supply signal, said bottom metallized pad affixed to the bottom surface of the first dielectric layer and electrically coupled to the top metallized die pad;

d) an integrated circuit die positioned on top of said top metallized die pad so as to expose a portion of the top metallized die pad, said integrated circuit die having a first power supply signal bond pad and a second power supply signal bond pad, said first power supply signal bond pad coupled to the exposed portion of said top metallized die pad;

e) a top first metal ring surrounding the top metallized die pad, the second power supply signal bond pad coupled to the top first metal ring; and

f) a bottom first metal ring for electrically coupling to the PC board to receive a second power supply signal, said bottom first metal ring surrounding the bottom metallized pad and electrically coupled to the top first metal ring.

18. The high performance integrated circuit package of claim 17, wherein the integrated circuit die further has a third power supply signal bond pad, the package further comprising:

a) a top second metal ring surrounding the top first metal ring, the third power supply signal bond pad coupled to the top second metal ring; and

b) a bottom second metal ring for electrically coupling to the PC board to receive a third power supply signal, said bottom second metal ring surrounding the bottom first metal ring and coupled to the top second metal ring.

19. The high performance integrated circuit package of claim 18, wherein the integrated circuit die further has a first non-power supply signal bond pad, the package further comprising a first row of bond fingers surrounding the top second metal ring, said first row of bond fingers having a first bond finger for receiving a first non-power supply signal from the PC board, said first non-power supply signal bond pad coupled to said first bond finger.

20. The high performance integrated circuit package of claim 19, wherein the integrated circuit die further has a fourth power supply signal bond pad, the package further comprising:

a) a second dielectric layer positioned on top of the top surface of the first dielectric layer so as to expose the top metallized die pad, the top metal rings, and the first row of bond fingers;

b) a third dielectric layer positioned on top of the second dielectric layer so as to expose the top metallized die pad, the top metal rings, and the first row of bond fingers; and

c) a second row of bond fingers positioned on top of the third dielectric layer, the second row of bond finger having a second bond finger for receiving a fourth power supply signal, said second bond finger coupled to said fourth power supply signal bond pad.

21. The high performance integrated circuit package of claim 20 further comprising a metallized plane positioned in between the second and third dielectric layers, said metallized plane for coupling said fourth power supply signal to said second bond finger.

22. The high performance integrated circuit package of claim 21, wherein the integrated circuit die further has a second non-power supply signal bond pad, the second row of bond fingers further having a third bond finger for

receiving a second non-power supply signal from the PC board, said third bond finger coupled to said second non-power supply signal bond pad.

23. The high performance integrated circuit package of claim 21, wherein said integrated circuit is a microprocessor.

24. The high performance integrated circuit package of claim 21, wherein said package is a ball grid array package.

25. A computer system positioned on a printed circuit (PC) board, said computer system comprising:

a) a bus;

b) a memory coupled to said bus; and

c) a high performance integrated circuit package coupled to said bus and to said PC board, said package including:

a first dielectric layer having a top and a bottom surface;

a top metallized die pad affixed to the top surface of the first dielectric layer;

a bottom metallized pad for electrically coupling to the PC board to receive a first power supply signal, said bottom metallized pad affixed to the bottom surface of the first dielectric layer and electrically coupled to the top metallized die pad;

an integrated circuit die positioned on top of said top metallized die pad so as to expose a portion of the top metallized die pad, said integrated circuit die having a first power supply signal bond pad and a second power supply signal bond pad, said first power supply signal bond pad coupled to the exposed portion of said top metallized die pad;

a top first metal ring surrounding the top metallized die pad, the second power supply signal bond pad coupled to the top first metal ring; and

a bottom first metal ring for electrically coupling to the PC board to receive a second power supply signal, said bottom first metal ring surrounding the bottom metallized pad and electrically coupled to the top first metal ring.

26. The computer system of claim 25, wherein the integrated circuit die further has a third power supply signal bond pad, the package further comprising:

a) a top second metal ring surrounding the top first metal ring, the third power supply signal bond pad coupled to the top second metal ring; and

b) a bottom second metal ring for electrically coupling to the PC board to receive a third power supply signal, said bottom second metal ring surrounding the bottom first metal ring and coupled to the top second metal ring.

27. The computer system of claim 26, wherein the integrated circuit die further has a first non-power supply signal bond pad, the package further comprising a first row of bond fingers surrounding the top second metal ring, said first row of bond fingers having a first bond finger for receiving a first non-power supply signal from the PC board, said first non-power supply signal bond pad coupled to said first bond finger.

28. The computer system of claim 27, wherein the integrated circuit die further has a fourth power supply signal bond pad, the package further comprising:

a) a second dielectric layer positioned on top of the top surface of the first dielectric layer so as to expose the top metallized die pad, the top metal rings, and the first row of bond fingers;

b) a third dielectric layer positioned on top of the second dielectric layer so as to expose the top metallized die pad, the top metal rings, and the first row of bond fingers; and

c) a second row of bond fingers positioned on top of the third dielectric layer, the second row of bond finger having a second bond finger for receiving a fourth power supply signal, said second bond finger coupled to said fourth power supply signal bond pad.

29. The computer system of claim 28 wherein the package further comprises a metallized plane positioned in between the second and third dielectric layers, said metallized plane for coupling said fourth power supply signal to said second bond finger.

30. The computer system of claim 29, wherein the integrated circuit die further has a second non-power supply signal bond pad, the second row of bond fingers further having a third bond finger for receiving a second non-power supply signal from the PC board, said third bond finger coupled to said second non-power supply signal bond pad.

31. The computer system of claim 30, wherein said integrated circuit is a microprocessor.

32. The computer system of claim 31, wherein said package is a ball grid array package.

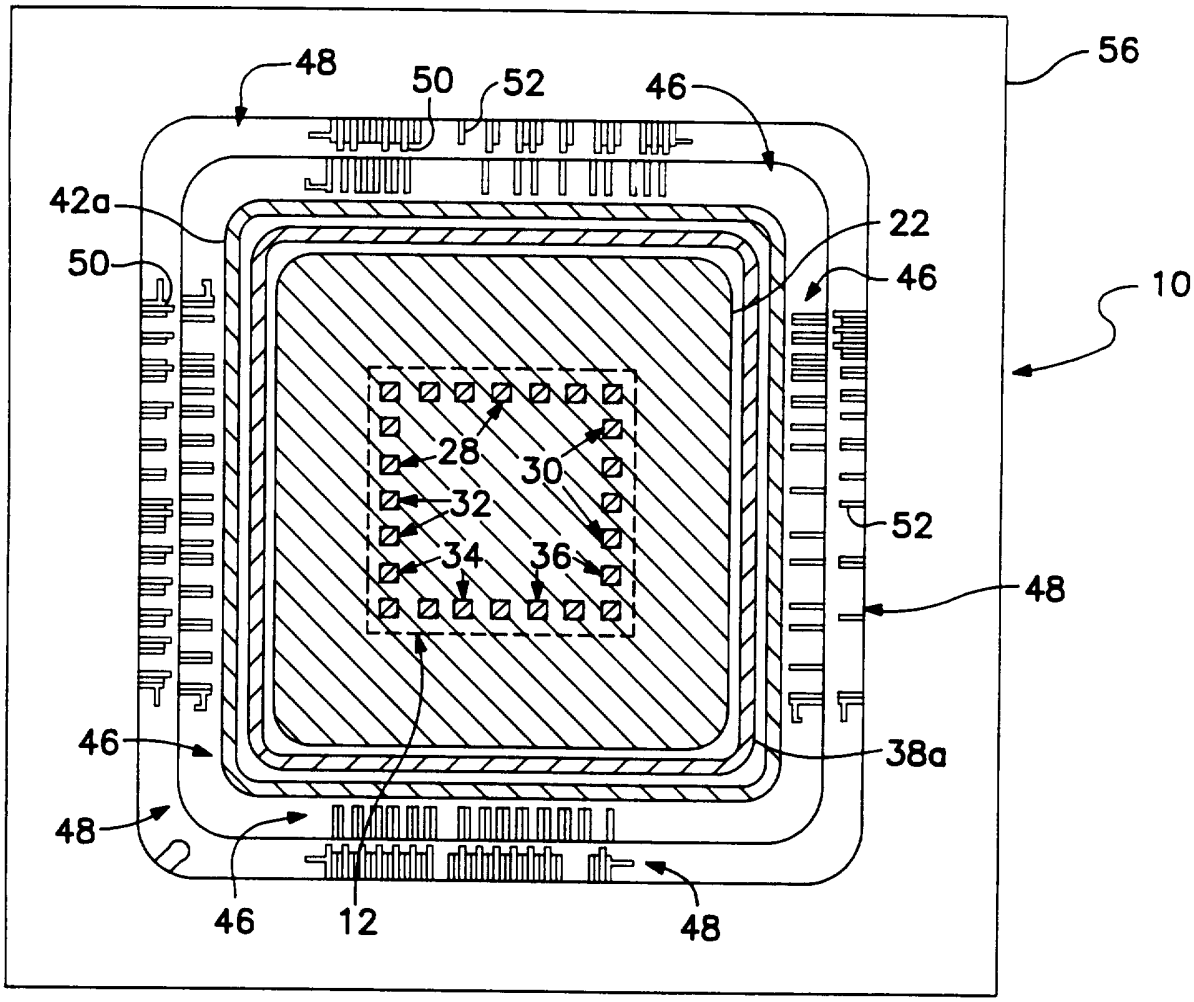

48
50
52
46
56
42a
22
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32
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36
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38a
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12
48

FIG. 1

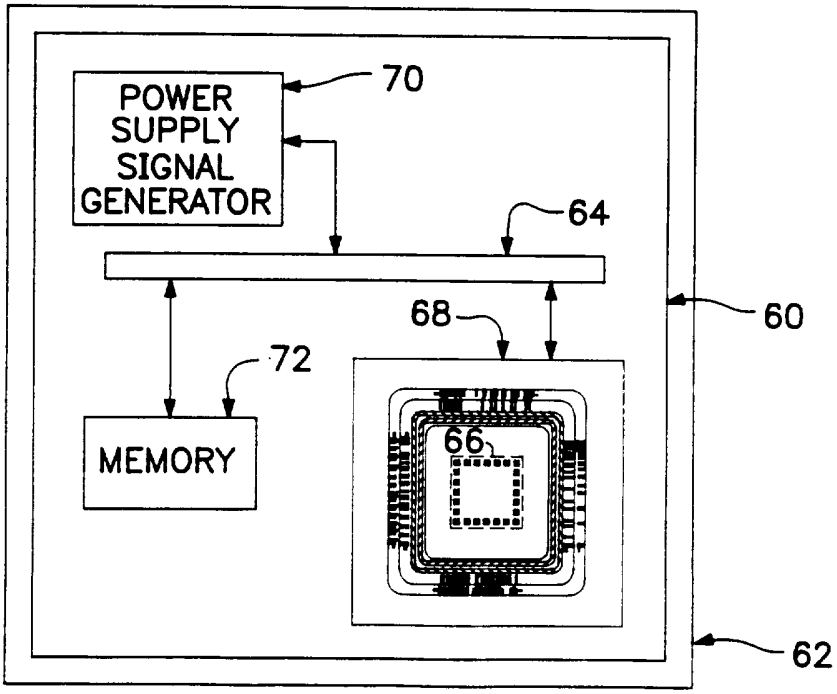

POWER SUPPLY SIGNAL GENERATOR
70
64
68
60
72
MEMORY
66
62

FIG. 4

FIG. 2

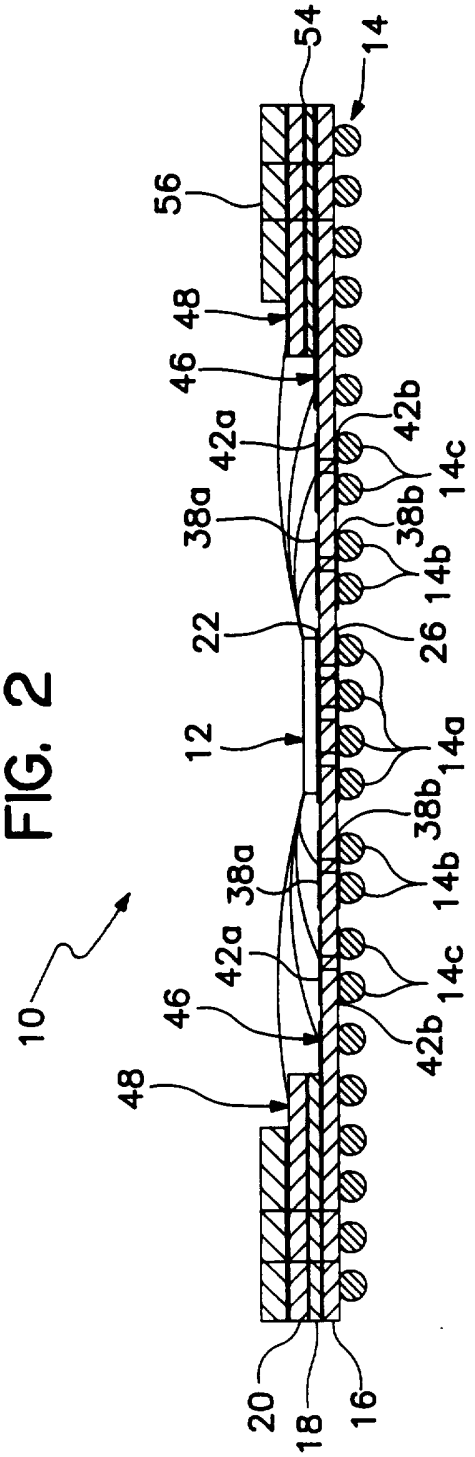
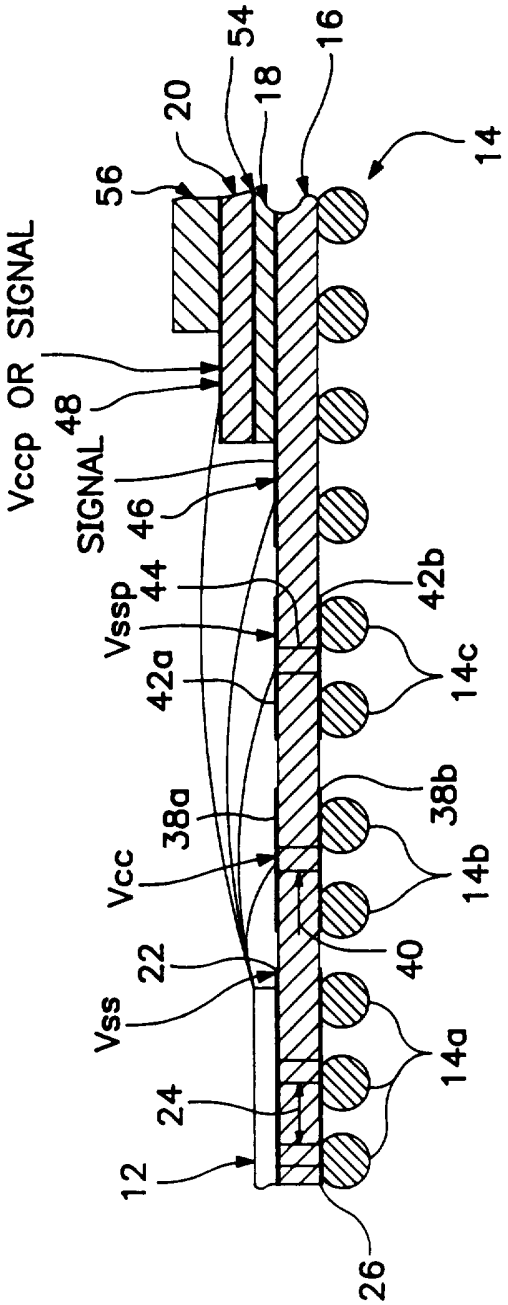

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12
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16
18
20
22
26
38a
38b
42a
42b
46
48
54
56
14a
14b
14c

FIG. 3


Vccp OR SIGNAL
SIGNAL
Vssp
Vcc
Vss
12
14
16
18
20
22
24
26
38a
38b
40
42a
42b
44
46
48
54
56
14a
14b
14c

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/00400

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 23/02; H05K 1/18, 7/02, 9/09
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 174/52.1, 52.4; 257/678; 361/728,760,761-764,775,777,780,783,820; 439/68,70-72

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 5,036,163 (SPIELBERGER ET AL.) 30 JULY 1991, See figure 3.	1-32
X ----- Y	US A, 4,560,826 (BURNS ET AL.) 24 DECEMBER 1985, See figure 1A.	1-3 and 9-11 ---------- 17-19
X	WIPO WO90/15439 (MABBOUX) 13 DECEMBER 1990, See figures 2-4.	1-16 and 32

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 31 MARCH 1996	Date of mailing of the international search report 22 APR 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DONALD A. SPARKS Telephone No. (703) 308-1756

Form PCT/ISA/210 (second sheet)(July 1992)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/00400

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

174/52.1, 52.4; 257/678; 361/728,760,761-764,775,777,780,783,820; 439/68,70-72