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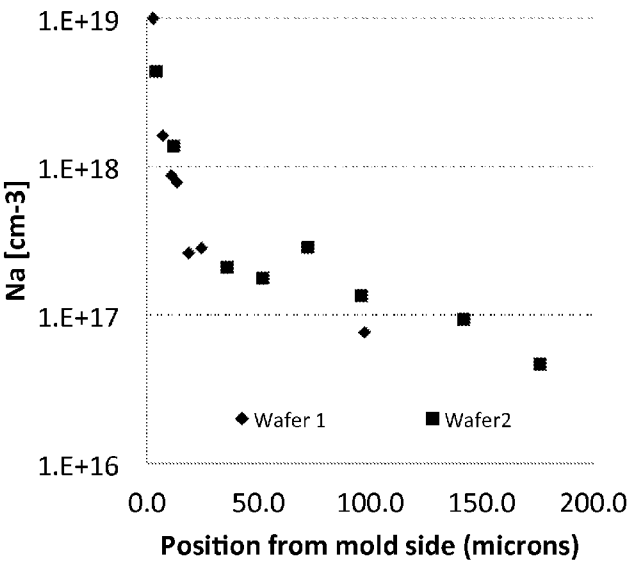

Fig. 5

(57) Abstract: A semiconductor wafer forms on a mold containing a dopant. The dopant dopes a melt region adjacent the mold. There, dopant concentration is higher than in the melt bulk. A wafer starts solidifying. Dopant diffuses poorly in solid semiconductor. After a wafer starts solidifying, dopant can not enter the melt. Afterwards, the concentration of dopant in the melt adjacent the wafer surface is less than what was present where the wafer began to form. New wafer regions grow from a melt region whose dopant concentration lessens over time. This establishes a dopant gradient in the wafer, with higher concentration adjacent the mold. The gradient can be tailored. A gradient gives rise to a field that can function as a drift or back surface field. Solar collectors can have open grid conductors and better optical reflectors on the back surface, made possible by the intrinsic back surface field.

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METHODS FOR CREATING A SEMICONDUCTOR WAFER HAVING PROFILED DOPING AND WAFERS AND SOLAR CELL COMPONENTS HAVING A PROFILED FIELD, SUCH AS DRIFT AND BACK SURFACE

RELATED DOCUMENTS

[0001] Priority is hereby claimed to U.S. Provisional application, no. 62/107,711, filed on January 26, 2015, Entitled METHODS OF CREATING A SEMICONDUCTOR WAFER HAVING A DRIFT FIELD WITH PROFILED DOPING AND WAFERS HAVING A PROFILED DRIFT FIELD, inventors Ralf Jonczyk, et al., Applicant 1366 Technologies, Inc., of Bedford, MA, the complete disclosure of which is hereby incorporated by reference. Priority is hereby also claimed to U.S. Provisional application, no. 62/239,115 filed on October 8, 2015, entitled METHODS FOR CREATING A SEMICONDUCTOR WAFER HAVING PROFILED DOPING AND WAFERS AND SOLAR CELL COMPONENTS HAVING A PROFILED FIELD, SUCH AS DRIFT AND BACK SURFACE, inventors Ralf Jonczyk, et al., Applicant 1366 Technologies, Inc., of Bedford, MA, the complete disclosure of which is also hereby incorporated by reference.

[0002] A semiconductor wafer can be formed directly from a semiconductor melt, generally using techniques disclosed in U.S. Patent No. 8,293,009, issued on Oct. 23, 2012, entitled METHODS FOR EFFICIENTLY MAKING THIN SEMICONDUCTOR BODIES FROM MOLTEN MATERIAL FOR SOLAR CELLS AND THE LIKE, by Sachs, et al., which is fully incorporated herein by reference).

[0003] Conventional solar collectors are composed of semiconductor wafers that have a relatively thicker portion, in which there are majority carriers, for instance lattice holes, and a much thinner section in which the opposite type of carrier, in that case, electrons, are the majority carriers. The two portions meet at what is called the p/n junction. In an industry standard wafer of 180 microns thick, the p-type potion would be 180 microns thick, and the n-type portion would be about 0.5 micron thick. In such conventional wafers, doping is uniform throughout the thicker portion of the wafer, such as the p-type portion, doped with acceptors (holes) in a p-type wafer, such as a silicon wafer doped with boron. In such a collector, the minority charge carriers are free to move in an essentially random fashion, diffusing randomly from their point of generation (in each portion, but here primary concern is with the thicker portion). Some minority carriers may go toward the p/n-junction collection region, some, in other directions. Such a situation lacks efficiency. It is known that establishing an electric field that would urge the minority charge carriers toward the p/n-junction collection region could, other things being equal increase efficiency. Such an electric field is said to point towards the p/n-junction and would cause generated minority charge carriers to preferentially move toward the collection p/n-junction. This directional preference would increase the collection efficiency of the solar cell. It is believed that this effect cannot be achieved by any conventional melt solidification method used for slicing wafers from thick ingots or bricks. Such a field is sometimes referred to as a drift field.

[0004] A known attempt to create such an electric drift field in a wafer established a gradient of doping, which established an electric field pointing towards the collecting p/n-junction. This known work is described in PCT patent

application no PCT/NL2005/000422, published as WO2005122287A1, entitled, Method for the production of crystalline silicon foils. This patent application was assigned to Stichting Energie, and the work is referred to below as the Stichting work. The Stichting work had significant negative effects. The main semiconductor material was silicon, and the dopant was gallium. A profile of doping level was created by rapid cooling of a molten body, where the initial rapid cooling resulted in impaired segregation at the initially solidified surface and as the cooling slowed, the gallium would preferentially segregate away from the subsequently later solidified surface, due to gallium's significant equilibrium segregation coefficient (approximately 0.008). Impaired segregation implies that the cooling happens sufficiently fast such that the actual segregation coefficient of the gallium impurity is more than 10 times higher than the equilibrium segregation coefficient. A segregation coefficient of 1 signifies no preference of segregation between liquid and solid phases, representing the maximum value for segregation coefficient. For a weakly segregating dopant such as boron, which as an equilibrium coefficient of 0.8, the maximum increase from the impairment mechanism would be only 1.25 times.

[0005] A necessary consequence of this rapid cooling is not mentioned in the Stichting patent application, but it is evident to a skilled practitioner. Metallic impurities within the molten material would necessarily also be incorporated into the solid of the initially rapidly cooled and solidified semiconductor crystal to a large and unacceptable degree. The Stichting work method takes advantage of the relatively significant, (numerically very small), segregation coefficient of gallium to achieve the gradient in concentration. But the metallic impurities also have a relatively significant (numerically very small) segregation coefficients, and for the

gallium to be present to a degree sufficient to provide a useable doping profile, it would also necessarily be that any metallic impurities would also be present in the solidified crystal to a high, and thus, unacceptable degree. Thus, although a doping profile would be created by the Stichting method, any formed body would not be practically useful for solar collection, having impurities to a degree of at least one order of magnitude higher metal content relative to equilibrium segregation.

[0006] Stated slightly differently, to achieve a 10 times difference (an order of magnitude) in doping from one portion of a wafer to another, the Stichting method would inherently have this same factor, i.e., 10 times more metal in the region of higher doping, than would be present in the region of lower doping. Practitioners in the art understand that such high metal content (and also such varied metal content (or other impurities)) has serious deleterious effects. For instance, the minority carrier lifetimes would be lower than it otherwise would be in the absence of these impurities. Such lower lifetime results in a cell that performs less well than one with higher lifetimes.

[0007] A hypothetical but reasonable case illustrates the problems. Consider a case where there is 1ppm of metal in the melt, with an equilibrium segregation coefficient of $k = 10^{-6}$, for example iron (Fe). With the Stichting method, this would result in $5x10^{11}$atoms/cm^3 of metal in the wafer. This would result in minority carrier lifetime of about 7 microseconds, which leads to 16.4% efficiency.

[0008] Another sort of field imposed upon wafers used in known solar collectors is called a back surface field (BSF). Conventional cells often have a back surface field. This field lowers effective back-surface recombination velocity and improves collection probability of minority carriers. A

typical way to achieve this is to provide a thin layer of aluminum or aluminum alloy on the back surface during processing. The application of aluminum has drawbacks. First, it is a separate step in the processing, thereby adding a complication that would be absent if no such aluminum layer were required. Second, aluminum is a rather poor reflector of long wavelength light. Thus, when an aluminum back surface layer is present, a relatively high amount of such long wavelength light is not reflected, and is lost. It would be beneficial to be able to reflect and thus capture some or all of such long wavelength light. (As a point of clarification, it should be noted that the BSF discussion entails the repulsion, or reflection of two totally different entities- minority carriers are urged away from the back surface by the BSF. Certain photons are not adequately reflected from the back surface, because they are absorbed or at least, not reflected, by the aluminum layer that gives rise to the BSF.)

[0009] Thus, there is a need for semiconductor wafers that have a means for establishing an electric field in a direction to urge the minority charge carriers (principally in the thicker portion of the wafer) to the collection p/n junction. There is a further need for such wafers that have excellent electrical properties and acceptably low levels of impurities. There is also a need for such wafers doped by dopants that do not have a significant segregation coefficient. There is also a need for such dopant-profiled wafers of p-type semiconductor, and also of n-type semiconductor. There is further a need for a method of fabricating such wafers. There is also a need for solar collectors and solar panels incorporating such wafers.

[0010] There is also a need for wafers for use in solar cells in which a BSF can be established without requiring a processing step dedicated to that purpose, and also without requiring a layer of optically poorly reflective aluminum at

the back surface. There is a further need for such a wafer that can be constructed to enable reflection of a relatively high amount of long wave-length light and thus its capture within the wafer and cell.

[0011] Thus, objects of inventions hereof include, semiconductor wafers that have a means for establishing an electric field in a direction to urge the minority charge carriers to the collection p/n junction. A further object includes such wafers with excellent electrical properties and relatively low levels of impurities. Another object are such wafers doped by dopants that do not have a significant segregation coefficient. Yet another object includes such dopant profiled wafers of p-type semiconductor, and also of n-type semiconductor. Still another object is a wafer having a BSF, which has no aluminum back surface. Still other objects are methods of making any and all such wafers. Still another object is a solar cell incorporating wafers having such drift fields or BSF or both. Yet another object is a solar cell that has higher efficiency for collecting long wave-length light, than do cells with aluminum BSF planes.

[0012] These objects and others are achieved by inventions hereof, which are shown more fully in the several Figures of the Drawing, which are:

SUMMARY OF FIGURES

[0013] Fig. 1A, which shows, schematically, in cross-section, a mold that is treated with a doping agent approaching a melt of semiconductor material;

[0014] Fig. 1B, which shows, schematically, in cross-section, the treated mold of Fig. 1A contacting the melt, with the upper portion of the melt having some of the treating material entering the melt;

[0015] Fig. 1C, which shows, schematically, in cross-section, the treated mold of Fig. 1B still contacting the melt, with a wafer solidifying upon the mold, and with a larger portion of the melt than that shown in Fig. 1B having some of the treating material entering the larger portion of the melt;

[0016] Fig. 1D, which shows, schematically, in cross-section, the treated mold of Fig. 1C still contacting the melt, with a thicker amount of wafer solidifying upon the mold, and with an even larger portion of the melt than that shown in Fig. 1C having some of the treating material entering the larger portion of the melt;

[0017] Fig. 2A, which shows schematically in cross-section, a wafer formed upon the mold as shown in Fig. 1D, with a gradient profile of doping;

[0018] Fig. 2B, which shows schematically in cross-section, the wafer of Fig. 2A after a doping of n-type material has been added to one side, thereby forming a p/n junction, and a region of higher doping has been formed on the opposite side from the n-type material, which will give rise to a BSF;

[0019] Fig. 3, which shows, schematically, in cross section, a mold of an invention hereof, which is treated with doping material throughout its volume;

[0020] Fig. 4, which shows, schematically, in cross section, a mold of an invention hereof, which is treated with doping material in a pair of layers or coatings on and near one surface;

[0021] Fig. 5, which shows, in graphical form, a relationship between the number of acceptors (Na/cm^3) and position from the mold side, of representative wafers made according to inventions hereof;

[0022] Fig. 6A, which shows, schematically in cross-section, a prior art wafer for use in a solar collector, with an Aluminum alloy back surface electrode;

[0023] Fig. 6B, which shows, schematically in cross-section, a wafer of an invention hereof, for use in a solar collector, with a highly doped rear surface due to a doping profile, without an Aluminum alloy back surface electrode, but with an open grid electrode and a high efficiency optical reflector;

[0024] Fig. 7, which shows, in graphical form the relationship between the Quantum Efficiency, as compared to incident light wavelength, for two different configurations, including those shown in Figs. 6A and 6B;

[0025] Fig. 8A is a schematic representation of a wafer of an invention hereof, showing segregation of donor compensating dopant atoms at the grain boundaries; and

[0026] Fig. 8B is a schematic representation of a wafer of an invention hereof shown in Fig. 8A, also showing segregation of acceptor counter compensating dopant atoms at the grain boundaries.

SUMMARY

[0027] A wafer is formed on a mold, which is in some manner provided with a dopant. For instance, the mold can have a coating that contains a dopant. To create a p-type wafer using silicon, a dopant can be boron, which provides extra electron acceptors. When the mold heats up, the dopant enters the melt (by several possible modalities), thereby doping a region of the melt directly adjacent the mold, so that in that adjacent region, the concentration of the dopant (such as boron), is relatively higher, as compared to the concentration of dopant in the bulk of the melt. Within a very short time a

semiconductor wafer starts solidifying on the surface of the mold. The dopant, such as boron, does not significantly diffuse in solid silicon. Thus, after a solid wafer is formed, the dopant can no longer enter the melt from the mold, because, solid silicon on the mold surface acts as a boron dopant diffusion barrier. At that time and afterwards, the concentration of boron dopant in the region of the melt adjacent the growing surface of the wafer will be less than the concentration that was present in the region of the melt where the wafer first began to form. As the wafer continues to grow, the new, additional regions of the wafer are formed from a new growth region of the melt, which has a boron dopant concentration, which, over time, becomes continuously less and less. This continuing diminishment of dopant in each successive new growth region establishes a concentration gradient or profile of boron dopant, with a higher concentration being present at the wafer adjacent the mold, which had solidified first, and a lower concentration of boron at the melt side of the solidified wafer, which solidified last. The gradient can be tailored by various means. A gradient in doping would give rise to an electric field that points in a specific direction, and whose strength at any location is related to the degree of gradient at that location and adjacent locations. Such an electric field can have an influence on minority charge carriers in a wafer used for a solar collector.

[0028] One gradient concentration profile can be useful to create a drift field within the wafer. Another profile can be useful to create a back surface field within the wafer. Wafers of inventions hereof can be used in solar cells. Higher efficiency is promoted due to the drift field, which promotes the collection of carriers within the cell. Higher efficiency also arises due to the provision of better reflectors on the back surface, made possible by the intrinsic back surface

field arising from the doping profile, which enables elimination of industry standard poor reflectors of Aluminum alloy back surface elements.

[0029] A characteristic that relates to local doping concentration in a deterministic manner is local resistivity. A gradient in resistivity is also present, and by measuring the resistivity at different locations, the concentration can be determined. Thus, an equivalent way of thinking about and analyzing a gradient in dopant concentration and thus a generated gradient of electric field is to consider the profile of resistivity, from one surface of a wafer to the other.

[0030] Method inventions include methods of making one such wafer from a melt. Method inventions also include making a plurality of such wafers from the same melt, including steps to compensate within the melt for accumulation of primary dopant within the melt that would otherwise be too high to use for wafers to be made at a target net dopant concentration to achieve target bulk resistivity for use in solar cells. Compensation is achieved by providing the melt with a compensating dopant of the opposite acceptor/donor type (for instance, to compensate for the acceptor dopant of boron, a donor dopant of phosphorous can be used), periodically as more and more wafers are formed. In some cases, the compensating dopant might segregate disproportionately to the grain boundaries, which could be disadvantageous. In such cases, a method invention hereof is to add a counter compensating dopant (in the case of the boron (acceptor) and phosphorous (donor) system, a counter compensating dopant would be an acceptor, such as gallium, with a suitably significant segregation constant, to minimize the electrical effects of the concentration of the compensating dopant at the grain boundaries.

DESCRIPTION

[0031] As is discussed above, a typical semiconductor wafer for use with a solar collector has a relatively thicker portion, in which the majority carriers are of one donor/acceptor type, for instance typically p-type. Such wafers are formed, and subsequently treated so that one face is doped to have majority carriers of the opposite donor/acceptor type, thus, n-type, in the case of a principally p-type wafer. For a typical wafer the first portion would be essentially the full thickness of 180 microns, and the other type portion would be only about 0.5 micron thick. The junction between the two portions is known as the p/n junction. The following discussion deals primarily with a new method to make the relatively thicker portion, which is typically a p-type portion. The methods discussed below would typically be used to create such a wafer. The p/n junction and opposite carrier type portion would be created on one surface after conducting the method steps discussed herein. These methods could also be used to create a thick, primarily n-type wafer. In such a wafer of an invention hereof, there will be a gradient profile of doping from one face of the grown wafer to the other. This doping gradient profile will give rise to an electric field in the finished grown wafer, which field can act as a drift field, and also or alternatively as a back surface field (BSF).

[0032] Figs. 1A, 1B, 1C and 1D show a mold 110 (also sometimes called a substrate), which is in some manner provided with a dopant, upon which will be formed a wafer 100 (Fig. 2A). For instance, the mold 110 can have a coating 112 that contains a dopant 114. To create a p-type wafer using molten silicon, the dopant can be boron (which is a charge carrier acceptor). An alternate embodiment, shown schematically in Fig. 3 has a mold 310 with a dopant 314 distributed either evenly or in some other mode throughout its

body. Several different embodiments of mold dopant treatment are discussed below. The principal typical use for inventions hereof would be with p-type semiconductor wafers and thus, acceptor dopants. Thus, the discussion will focus primarily on such combinations. However, inventions hereof also may be used with n-type semiconductors, and charge carrier donor dopants. (An example of such a system would be a phosphorous-doped substrate, with boron melt compensation.) Yet another, more involved combination is also possible, and is discussed below.

[0033] The primary dopant, such as boron, can be anywhere on the surface of such a mold 110, or within the body of such a mold 310. However, it is believed that if it is present in a region of the mold nearest the melt, such as a coating 112 or a region within the body 310 immediately adjacent the surface, that this provides the most advantage, as discussed below. Many different semiconductors can be used as the primary melt component. Silicon is very commonly used, and will be used as a representative example in the following discussion. Likewise, other dopants are possible. Boron will be used as a representative dopant example in the following discussion. The generality of this disclosure is not, however, intended to be limited to silicon as the semiconductor, or boron as the dopant. All reasonable alternatives are considered as aspects of inventions hereof. For instance, for Silicon as the semiconductor, examples of dopants include, but are not limited to: boron (B), aluminum (Al), gallium (Ga) and indium (In). For n-type wafers, dopants include but are not limited to: Phosphorous (P), Arsenic (As), lead (Sb) and Bismuth (Bi).

[0034] When the mold 110 heats up, such as when it contacts the hot semiconductor melt 116, for instance of molten silicon, the dopant, such as boron 314 within the mold (Fig. 3) or boron 114 of the mold coating 112 enters the melt 116, thereby doping a region 118b of the melt 116 directly adjacent

the mold 110, so that adjacent the mold, the concentration of the boron 114b, is relatively higher, as compared to the concentration of boron in the bulk (remaining regions) 120 of the melt 116. An embodiment as shown in Figs. 1A, 1B, 1C and 1D, using a coating 112, will be discussed first. As shown in Fig. 1C, within a very short time (e.g., a few milliseconds to several seconds) a semiconductor (e.g. silicon) wafer 100, starts solidifying on the surface 122 of the mold 110.

[0035] The mold could be heated other ways (for instance it can be pre-heated before contacting the melt). It is typically advantageous that the mold be cooler than the melt when it touches the liquid silicon to best allow extraction of heat and therefore solidification of the molten silicon. This solidification process will heat up the mold from its starting temperature.

[0036] Boron does not significantly diffuse in solid silicon. Thus, as shown in Fig. 1C, after a solid wafer 100 is formed, the boron 114 can no longer enter the melt 116 from the mold/substrate 110, because, solid silicon 100 has formed on the mold surface 122 and the solid silicon acts as a boron diffusion barrier. (This is also typically the case with other dopants and semiconductor wafer systems discussed herein.) Typically, a thickness of a few microns of solid material is sufficient to prevent further diffusion. This thickness may appear initially at spaced apart locations on the mold surface, but relatively quickly, the solidified thickness everywhere on the mold is sufficient to prevent further diffusion. At that time, the concentration of boron 114c in the region 118c of the melt 116 adjacent the growing surface 111 of the wafer 100 will be less than the concentration 114b that was present in the region 118b where the wafer 100 first began to form, immediately after the mold surface 122 contacted the melt 116, as shown in Fig. 1B, because boron 114c atoms have diffused and moved by convection

away from the mold 110 and the growing wafer 100 and away from the region 118c adjacent the mold 110 and the growing surface 111 of the wafer 100, into the melt 116.

[0037] As the wafer 100 continues to grow (i.e., to thicken) during a time scale of the next few seconds, the new, additional regions of the forming wafer 100 are formed at the surface 111, from a new growth region 118c, 18d of the melt adjacent the growing surface 111, which new growth region 118d has a boron concentration 114d which, over time, becomes continuously less and less. For each successive quantity of growing wafer, the new growth region 118, is ever so slightly progressively further away from the mold, the original source of the dopant. The dopant has rapidly diffused into the bulk 120 of the melt 116, distant from the mold 110.

[0038] Fig. 2A, shows the grown silicon wafer 100. The continuing diminishment of dopant in each successive new growth region 118 establishes a gradient of dopant boron in the grown wafer 100, as shown in Fig. 2A, with a higher concentration of boron being present at the portion 132 of the wafer that was adjacent the mold 110 and its surface 122 when the wafer completed its formation, which surface 132 had solidified first, from the region 118 of the melt 116, when it had a relatively higher concentration of boron. There is a lower concentration of boron at the surface 136 of the solidified wafer 100, which solidified last, from the region 118 of the melt (relatively distant from the mold surface 122, with the boron content at that location) at a time when and a location where the melt had a relatively lower concentration of boron.

[0039] The foregoing discussion is cast in terms of successive regions of grown wafer 100 and successive new growth regions 118 of the melt, as if these growth regions are discrete, layer-wise, such as sheets of paper. In actuality,

the growing of the wafer is continuous, atom-by-atom, and the diffusion of the dopant into the melt is also continuous, atom-by-atom. The amount of dopant that is incorporated into the growing wafer depends on the relative rates of diffusion of dopant into the melt, away from and out of the continuously successive new growth regions of the melt, and the rate of growth of the semiconductor wafer. These two rates are affected by the diffusion propensities of the dopant in the melt, the temperature, the crystal growth speeds, etc. Thus, the concentration of boron in the wafer varies smoothly, from the surface 132, which formed nearest the mold, to the surface 136, which formed more distantly from the mold, deeper within the melt. (Fig. 2A shows three different regions of the formed wafer, with three different, discrete concentrations of dopant, concentration being indicated by closeness of the horizontal hatching lines, closer hatching indicating greater dopant concentration. This is not meant to realistically represent the formed wafer, but is merely a limitation of the drawings, which must show in black and white a physical situation that might better be shown in a segue of grey scales from the surface 132, which formed adjacent to the mold, to the surface 136, which formed more distant from the mold.)

[0040] Fig. 5 shows the p-type doping concentration for two different wafers (designated wafer 1 and wafer 2), each showing a concentration of about 1 x 10^{19} N_a/cm^3 at the portion of the wafer that formed first, immediately adjacent the mold, descending in a smooth curve with a roughly exponential decay shape, with N_a/cm^3 concentrations of between about 1 x 10^{17} and 1.5 x 10^{17} over a range of positions from about 25 to about 150 microns from the portion of the wafer that formed first, immediately adjacent the mold. N_a as high as 1 x 10^{20} N_a/cm^3 are believed to be possible, and also at the location of the wafer that formed last, farthest from the mold, it is believed that concentrations as low as low as 1 x 10^{15} N_a/cm^3 are possible.

The unit N_a stands for the number of acceptors, as in electron acceptors. For an n-type dopant, a corresponding unit would be N_d, which stands for the number of donors, as in electron donors. (In some cases below, and in the claims, the expression N_x, is used to denote either N_a or N_d, as the case may be, depending on whether electron donors or acceptors are intended.) As can be seen, the transition from relatively higher concentration to relatively lower concentration is smooth and continuous.

[0041] Semiconductor wafers having such a doping gradient are not known to have been produced before, other than in the very limited type mentioned above, using the Stichting method. As discussed above, that method created semiconductors having very poor electrical properties.

[0042] Recalling the hypothetical example outlined above regarding impurities and the Sticting method, having a factor of ten difference in doping, and thus the same difference in impurities, and $5x10^{11}$ atoms/cm^3 of metal in the wafer, resulting in a minority carrier lifetime of about 7 microsecond, leading to a 16.4% efficiency, wafers made according to inventions hereof would have significantly better properties. Such a wafer would have $5x10^{10}$ atoms/cm^3 of metal in the wafer, resulting in a minority carrier lifetime of about 70 microseconds, leading to an 18.4% efficiency. This example is hypothetical, and other factors will enter into any actual physical case, but the comparison is apt.

[0043] In a dopant profiled wafer of an invention hereof, if formed from a melt doped with p-type material, the wafer is first formed, and then the opposite type material, in this case n-type, will be created on one surface, thereby creating a p/n junction. Fig. 2B shows, schematically, the relationship between the p/n junction and the doping profile of an invention hereof. For a p-type wafer formed from a melt

as discussed above, with a doping profile, the p-side of the wafer 100 (the more positively doped side) will be the side 242, with the higher p-type dopant of boron concentration, which formed closer to the mold surface 122. The n-side of the wafer (the less positively doped side, or, the more negative side) will be formed on the side 246, with an initially lower p-type dopant boron concentration, which formed more distant from the mold surface 122. Formation of the n-type (or oppositely doped) portion 250 can be done by any conventional, or yet to be developed method. Typically, the depth of such a section would be only about 0.5 micron thick. In a typical application, the boron p-type doping provides N_a of about 1 x $10^{16}/cm^3$. The n-type doping provides N_d of approximately 1 x $10^{19}/cm^3$. Thus, at the side 246, the n-type doping predominates. The p/n junction 252 is between the n-type portion 250 and the side 246 with an initially lower p-type dopant concentration. The sun-facing side of this wafer would have the n-type portion 250 facing the sun. A back surface field portion 254 (discussed in more detail below) is also shown, which is adjacent the side 242 having initially higher p-type dopant concentration, on the side opposite from where the sun would be.

[0044] As discussed above, such a dopant gradient is beneficial because it establishes an electric field pointing towards the collecting p/n-junction with regard to the minority carriers. The electric field causes generated minority charge carriers to preferentially move toward the p/n-junction. This directional preference increases the collection efficiency of the solar cell. It is believed that this effect cannot be achieved by any conventional melt doping method. (In a p-type semiconductor, the minority carriers are electrons).

[0045] It should be noted that considering the dopant concentration at different locations within the body of the

wafer is only one way to describe its structure and properties. Another way is to consider the resistivity of the material at the same different locations throughout its body. It is also true that, due to the different net doping concentration, there will be a corresponding and related difference in the resistivity of the wafer at different locations throughout the body. Thus, there is also a gradient in resistivity of the body, which gradient is generally inverse that of the net doping gradient. By that, it is meant that resistivity is higher in regions of lower dopant concentration, and it is lower in regions of higher dopant concentration. It is also to be noted that although these gradients in concentration and resistivity are generated by the phenomena described above of melt solidification and segregation, it is relatively difficult to measure material concentrations at different locations within a wafer. However, it is much easier to measure resistivity at such locations through the body. (This can be done by measuring the resistivity of a body, removing a layer of material, and measuring the resistivity of the remaining body, whereby it is possible to determine, from the difference, the resistivity of the portion that has been removed.) From this determined resistivity, it is also possible to determine the material concentration, i.e., the doping concentration, of the layer that has been removed. Layer by layer, the resistivity profile, and thus also the doping concentration profile through the entire body, can be measured and thus determined.

[0046] The relationship between resistivity and dopant, or carrier concentration is deterministic and non-linear. Table 1 below shows a representative set of values relating resistivity (ohm-cm) on the one hand to acceptor carrier concentration (atoms/c^3) and also to donor carrier concentration.

Resistivity (ohm-cm)	Acceptor Conc. (atoms/cc^3) P-type dopant	Donor Conc. (atoms/cc^3) N-type dopant
0.001	1.15×10^{20}	7.36×10^{19}
0.01	7.98×10^{18}	4.38×10^{18}
0.1	2.40×10^{17}	7.77×10^{16}
0.3	5.83×10^{16}	1.87×10^{16}
0.5	3.19×10^{16}	1.04×10^{16}
1	1.47×10^{16}	4.83×10^{15}
2	6.97×10^{15}	2.31×10^{15}
4	3.38×10^{15}	1.13×10^{15}
6	2.23×10^{15}	7.43×10^{14}
10	1.32×10^{15}	4.41×10^{14}

TABLE 1- RELATION BETWEEN RESISTIVITY AND CARRIER CONCENTRATION

[0047] The relationship can also be characterized graphically, such as in a log-log plot. Such a graph is shown at www.solecon.com/pdf/converting resitivity to carrier concentration graph sige.pdf. This is a website showing work of Solecon Laboratories of Trademark Dr., Reno, NV. The graph shown there is hereby incorporated fully herein by reference. The vertical scale denotes carrier concentration/cm^3, with the horizontal scale denoting resistivity (ohm-cm). The relationship between carrier concentration and resistivity shows generally higher concentration correlates with lower resistivity, and vice-versa. On the log-log scale, the slope

is generally negative. Graphs for n-type and p-type doping of the same semiconductor, for instance, germanium, are generally congruent and spaced apart, with that of p-type being displaced toward the right, generally such that in the p-type semiconductor, there will be higher resistivity for the same carrier concentration in an n-type semiconductor. The relationship between carrier concentration and resistivity for silicon semiconductors is generally the same as described for the germanium semiconductor. The values were determined using Spreading Resistance Analysis (SRA). The authors explain that to calculate carrier concentration values for silicon, they used mobility values derived from Thurber, Mattis, Liu, and Filliben, National Bureau of Standards Special Publication 400-64, *The Relationship Between Resistivity and Dopant Density for Phosphorus- and Boron-Doped Silicon* (May 1981), Table 10, Page 34 and Table 14, Page 40. To calculate germanium carrier concentration values, they used carrier mobility values derived from D.B. Cuttriss, Bell System Technical Journal (March 1961), p. 509.

[0048] The process described above works very well without modification for creating one, or a small number of wafers from a single melt without adjusting the melt composition.

[0049] One challenge presented by this process is that without modification, it will result, over time, as more and more wafers are made, in an increase in the concentration of the dopant, such as boron, in the melt. That is because less than all of the boron that had moved from the mold during the time of the production of a single wafer, will be incorporated into the wafer being formed during that time interval. This concentration build-up in the melt limits the number of wafers that can be grown, before the melt becomes too rich in dopant, e.g., boron, for the baseline doping level. To be precise, the melt has become too rich in whatever it is that the dopant provides, either electron donors or acceptors. Eventually,

equilibrium is reached, at which point, the amount of boron removed from the melt with the formation of each wafer is equal to the amount of boron added from the mold to the melt with each wafer growth cycle. The boron concentration at which this equilibrium is reached is typically too high to make a quality conventional solar cell wafer from the dopant rich melt.

[0050] To compensate for such a buildup of boron in the melt, an amount (specified below) of a different material, referred to herein as a compensating dopant, for instance in the case of a boron primary dopant, a compensating dopant of phosphorous can be added directly to the melt. (As explained below, there is reason in some cases for yet another compensating dopant (for different reasons), and so, in some cases, this compensating dopant about to be described may be referred to as a first compensating dopant.)

[0051] Boron is a member of Group III of the periodic table of elements, and has a propensity to accept, or to receive one electron. Thus, boron is an electron acceptor. Phosphorous is a member of Group V of the periodic table of elements, and thus, it has an excess electron that can be donated to the melt. Thus, phosphorous is an electron donor. Thus, Phosphorous compensates for the excess electron acceptors of boron, because phosphorous provides the electrons that the excess boron tends to accept, thus compensating for the excessive boron acceptors. A single atom of phosphorous donates a single electron, and a single atom of boron accepts a single electron.

[0052] Phosphorous added in the proper amount will compensate for excess boron and maintain the wafer formation process indefinitely at desirable boron dopant levels. The amount (as measured by the number of atoms) of phosphorous (compensating, donor dopant) to compensate is approximately

equal to the amount (as measured by the number of atoms) of boron (excess, primary, accepting dopant) in the melt, multiplied with the segregation coefficient k of boron and divided with the segregation coefficient of phosphorous (specifically k=0.8 for boron and k=0.3 for phosphorous).

[0053] Stated differently, melt doping (the concentration of acceptors, or donors, as the case may be, depending on whether a p-type or n-type semiconductor) should ideally be kept at or close to conditions under which a wafer grown on a mold with no doping material contained in any part of the mold or mold coating will be of high resistivity, such as typically for n-type, greater than 1 Ohm-cm, and for p-type, greater than 2 Ohm-cm. To achieve this, the amount of compensating doping material of the opposite type to the primary type present in the mold or coating, should preferably be present in the melt in a concentration described by the following relation:

$$C_{cd} \text{ approximately equals } C_{md}*(k_{md}/k_{cd})$$

where:

C_{md} is the melt concentration of the mold primary dopant (boron for example);

C_{cd} is the melt concentration of the compensating-dopant (phosphorous for the above example of a boron primary dopant);

k_{md} is the effective segregation coefficient of the mold primary dopant; and

k_{cd} is the effective segregation coefficient of the compensating dopant.

[0054] The resulting wafer will have a measurable gradient in boron concentration (see Fig. 5), from, for instance about

1 x 10^{19} N_a/cm^3 to about 1 x 10^{17} N_a/cm^3. Thus, one aspect of an invention disclosed herein is an article of manufacture, which is a wafer that has a measurable gradient in a primary dopant, such as boron, concentration, as measured from one surface to the opposite surface. In fact, a reasonable minimum difference between the doping at the melt side and the doping at the substrate side is factor of three times. This yields a 0.1% increase in efficiency over a flat doping profile containing the same number of acceptors. The size of the gain is dependent on many factors, such as cell architecture, minority carrier lifetime of the wafer, surface passivation, etc. The example above (0.1% gain, front to back doping difference of 1/3, is achieved with a PERC architecture. The gain may be different with an aluminum BSF architecture. As mentioned above, it is difficult to directly measure dopant, such as boron, concentration within the body of the wafer. Thus, by measurable dopant concentration, what is meant is a dopant concentration that can be determined by either measuring dopant concentration directly, either by present or yet to be developed means, or by measuring resistivity, layer by layer, as discussed above, and then from the resistivity, calculating or determining in some other way, such as by reference to a table such as Table 1 or graph, the dopant concentration that correlates with that resistivity, and thus compiling a resistivity gradient profile and also a dopant gradient profile.

[0055] The compensating dopant should be added periodically, or continuously, to match the rate of addition of dopant from the mold.

[0056] Thus another aspect of an invention disclosed herein is a method of fabricating a wafer, and a more specific aspect of a method invention disclosed herein is a method of fabricating a wafer having a measurable gradient in dopant, such as boron, concentration, or resistivity, as described

above, and a particular method invention hereof is a method of producing a plurality of such a wafers from a melt over time, while maintaining relatively similar doping and resistivity profile, even as more and more wafers are made, and more primary dopant enters the melt.

[0057] Turning now to a discussion of the location of the dopant source that will be incorporated into the wafer, a typical location is shown in Fig. 1A, as a coating on the forming surface 122 of the mold 110, or as shown in Fig. 3 and Fig. 4, somewhere within the body of the mold 110, in a location where, upon heating of the mold, the dopant can move through the body of the mold, to exit the mold and dope the melt 116. Thus, as shown at 114 in Fig. 1A, the dopant 114 may be in an outermost layer 112 of a coating on the mold 110, such as a release layer. Or, as shown in Fig. 3, it may be located within the body 314 of the mold 310, either evenly distributed, or in more concentrated regions, such as more concentrated closer to the forming surface 322. Or, as shown in Fig. 4, it may be located in a submerged layer 414 of a coating on the mold, with another layer, 424, such as a release layer, at the surface.

[0058] More specifically, the mold 310 itself, can contain volatile boron-containing compounds 314, such as: boron oxide, boron nitride, boron, boric acid and boro-silicate glass. Alternatively, or in addition, the mold coating 112 that is in immediate contact with the melt can contain volatile boron compounds and boron compounds soluble in silicon (in the case of a silicon wafer being formed, otherwise, soluble in the semiconductor being formed) including: boron oxide, boron nitride, boron, boric acid, boro-silicate glass, boron carbide, boron silicide. Yet further in alternative, or in addition, the mold coating region 414 that is not in immediate contact with the melt can contain volatile boron compounds,

including: boron oxide, boron nitride, boron, boric acid, boro-silicate glass.

[0059] Another matter to consider, related to the location of the dopant, is the modality by which it passes or migrates from the mold to the molten material. It is believed that three different major possible modalities exist. One would be dissolution of dopant into the molten silicon, followed by diffusion further into the melt. This dissolution and diffusion modality is believed to confer many benefits. A second would be diffusion from the mold into the liquid of the melt. The third, and presently least preferred, is vaporization from the mold to the melt.

[0060] Turning to each of these in turn, the most preferred would be where the dopant from the mold, such as in the form of B_4C (boron carbide) or B_4Si (boron silicide) would dissolve from the mold, such as from the coating, into the melt. Within the melt, the dopant would decompose into its constituents, and the dopant, such as boron, would diffuse further into the body of molten material. The other components, such as C or Si, to the extent the melt were not already saturated with them, such as is likely the case, would diffuse also. Advantages that follow from this modality are that each wafer made on the same mold receives the same amount of dopant, unlike other modalities, such as the third mentioned below, where more dopant is released for the earlier wafers made.

[0061] The second modality, in which the dopant diffuses directly into the liquid from the mold, would diffuse from a coating, or from the mold itself into the melt, is thought to be least likely because most, if not all materials would enter the melt by some mode other than diffusion only, such as by dissolution or vaporization. In any case, for all modes in which dopant is in actual contact with the melt, diffusion will take place to some degree.

[0062] The third modality, direct vaporization, is not preferred. For example, B_2O_3 (boron Oxide) or BN (boron nitride) might be heated to a degree that it vaporizes directly from its location on the mold (e.g. in a coating) or in the mold, to pass directly into the molten semiconductor material as a gas. This is not preferred because it is expected to be difficult to control the degree to which the dopant is released into the melt. The entire source for dopant gets hot all at once, and will release boron by vaporization, not just the portion of dopant source in contact with the melt . Thus, the first time the mold is heated, more dopant will be released, for instance small particles could disappear after just one heat cycle. Or the process is limited by diffusion to the surface of the mold of the dopant particles.

[0063] Relating to both the location of the dopant, and the modality, some examples are instructive. For doping from a coating of the mold, such as a release coating, that contacts the melt directly, such as shown in Fig. 4 at layer 424, or Fig. 1B, at layer 112, when minimal vapor transport is desired, a suitable dopant source would be a coating material of Si_3N_4 or SiO_2, and dopant of B_4C or SiB_4. For doping from any layer of a mold coating that is not in direct contact with the melt, such as shown in Fig. 4, at layer 414, a suitable dopant source would be a coating material of Si_3N_4 or SiC, and dopant of B_sO_3 or BN. For doping from the mold, but not a coating, such as shown at 314 in Fig. 3, a suitable mold material would be SiC, and dopant of B_2O_3 or BN.

[0064] The basic method described above will also work with any other p-type primary dopant instead of Boron (such as Aluminum (Al), Gallium (Ga), Indium (In)) and using any suitable n-type dopant to compensate the melt (Phosphorus (P), Arsenic (As), antimony (Sb), Bismuth (Bi)), respectively. However, the pair of B and P is thought to be extremely advantageous for use with growing silicon wafers, because they

have the numerically highest segregation coefficients of all effective dopants in silicon. (An element with a relatively higher segregation coefficient segregates during solidification relatively less than others, and as such, those with the highest segregation coefficient segregate during solidification the least.) Thus, upon solidification, the dopant B and compensating dopant P would be distributed relatively uniformly within the crystal, as compared to the case that would arise if elements were used that had numerically smaller segregation coefficients (with greater propensity to segregate). A similar, but correlative process could also be used to make primarily n-type doped wafers. In that case, the primary dopant provided by the mold or a coating thereon would be an n-type dopant (such as P, As, Sb, Bi) and the melt compensating dopant would be a p-type dopant (such as B, Al, Ga, In).

[0065] Table A below shows representative primary dopants and compensating dopants for p-type and n-type semiconductors and their respective segregation coefficients.

P-Type		N-type	
Primary dopant	compensating dopant	Primary dopant	compensating dopant
B (0.8)	P (0.3)	P	B
Al (.002)	As (0.3)	As	Al
Ga (0.008)	Sb (0.023) (antimony)	Sb (antimony)	Ga
In (0.004)	Bi (0.0007)	Bi	In

TABLE A- Dopants and Equilibrium Segregations Constants

[0066] This method of doping a semiconductor material could be applied to any semiconductor that can be grown from a melt, including Silicon (Si), Germanium, (Ge), Gallium arsenide (GaAs), etc. Growing semiconductor wafers/bodies from semiconductor materials other than silicon would require using different dopants (for example silicon as a primary dopant for GaAs wafers) and different compensating dopant materials.

[0067] Table B below shows compounds of doping elements that could be used as source. An x mark means that compound exists, e.g. boron carbide, boron oxide, etc. (In contrast, there are no silicides for P, As, Sb, Bi.) Pure elements could also be used and any compound of Si, C, O, N, could be doped with any of the elements and then used as source for dopant. Some of the compounds listed exist but are not practical, due to low stability, reactivity with moisture, toxicity, etc.

Element	B	Al	Ga	In	P	As	Sb	Bi
Carbide	x	x	x	x	x	x	x	x
Oxide	x	x	x	x	x	x	x	x
Nitride	x	x	x	x	x	x	x	
Silicide	x	x	x	x				

TABLE B- compounds of doping elements

[0068] Inventions disclosed herein confer many benefits. One is a beneficial electric field that improves minority carrier collection and thus efficiency of a solar cell. Another is higher efficiency at lower resistivity, which implies that a higher fill factor is possible. There are also possible synergies with PERC-like processes (lower resistivity

is beneficial for PERC like cell architectures). (PERC stands for Passivated Emitter Rear Contact.)

[0069] Yet another benefit relates to the fact that the gradient of dopant (or its correlate, resistivity) can give rise to a passivating field automatically. (This is evidenced by the very high doping concentration in the portion of the wafer that was formed nearest to the mold, as shown on the left hand side of the curve, as shown in Fig. 5.) A passivating field will reduce recombinations at the rear surface. The benefit is that a conventional Aluminum BSF (Back Surface Field), which would conventionally be applied during cell processing, is not necessary, and could be eliminated. This would then reduce the number of steps in the formation of a typical cell.

[0070] Another advantage grows from this. If the Al BSF need not be present, then an open grid contact can be used at the back of the wafer, allowing long wavelength light to pass through the cell and be reflected at an efficiently reflective sheet at the module back and then passed back through the cell again. This is discussed in more detail below.

[0071] The gradient of doping (and its correlate, resistivity) through the thickness of the wafer can also provide what is called a Back Surface Field (BSF). Fig. 6A shows schematically in cross-section a known solar cell 600 incorporating a BSF. A BSF is created by a region 662 of particularly high concentration of dopant at the back (surface facing away from the sun) of the solar cell, which creates a strong electric field within the semiconductor material at the back of the cell. This electric field repels the minority carriers that approach the back of the cell and prevents the vast majority of them from reaching the very back surface 664 of the semiconductor material. This is important because if they were to reach this back surface 664, there is a high

probability that they would re-combine at this surface and therefore no longer be available to create current in an external circuit.

[0072] Drift fields and back surface fields both rely on spatial variation of the doping density through the thickness of the wafer, with a higher doping density toward the back of the cell and a lower doping density toward the front of the cell. However, they differ in several important regards. First, a drift field is most effective when it extends through the thickness of the wafer, because as such, it will keep gently pushing the minority carriers toward the collecting junction (and not let them be subject exclusively to diffusion). Conversely, a BSF is confined to the back portion of a cell wafer. For example, in a cell wafer of 180-200 micron thickness, a BSF region of the cell wafer might be 1-10 microns thick, with a typical thickness of approximately 5 microns. Further, the doping level in a BSF is very high, to create a high electric field, which then effectively repels the minority carriers toward the front. In fact, this doping level is so high that it can negatively impact the minority carrier diffusion length (or lifetime) in this rear portion of the cell. The net impact on the device performance is still very positive, because the reduction in diffusion length is localized only to the very back of the cell and because the BSF itself minimizes the number of carriers that enter this region. In contrast, the lower doping levels in a drift field have relatively little negative impact on the minority carrier diffusion length. Such a BSF cell is shown in Fig. 6A.

[0073] The most common way to create a BSF is to screen print aluminum paste onto the back of the wafer and fire it in a belt furnace. This results in a region 662 of silicon with a very high doping density of aluminum – a p-type dopant. In addition there is a layer 668 of aluminum-silicon alloy (much of it at the eutectic composition) behind this. This aluminum

alloy region 668 acts as the rear contact/conductor for the cell. Unfortunately, for the operation of such a conventional BSF cell, the aluminum-silicon alloy is not a particularly good optical reflector, having a reflection coefficient of approximately 60%. Thus, 40% of the infra-red light that is not absorbed in its first pass through the cell body 652 is absorbed by this rear contact and is no longer available to travel back through the cell body 652 in a second pass. This limits the current generated by the cell significantly and the voltage a small amount. The sun-facing surface of the cell may be provided with a textured surface 650, and with electrical contact fingers 670.

[0074] As shown in Fig. 6B, the grown-in doping of an invention hereof can provide a region 682 with a doping profile, which functions as a BSF, without the drawbacks mentioned above. In certain embodiments, this region 682 of particularly high doping (for the back surface) can be created together with a more extensive region 692 of profiled drift-field doping through the thickness of the cell wafer. (As shown in Fig. 6B, the region 692 does not have any graphical representation of a doping profile, in order to simplify the figure. However, it should be understood that there can be a gradual or less gradual doping profile similar to that as shown in Figs. 2A and 2B, discussed above.) In other embodiments, the flux of dopant coming from the mold or mold coating can be designed to be confined more narrowly to the back of the cell wafer. This could then be used to create a significantly doped BSF region 682, and also to create a drift field region 692 that is only very mildly doped, so that although there would be a drift field, it's gradient would be very gradual, or less abrupt. Or, both effects can be achieved with the same doping, or, with different doping patterns.

[0075] Several methods exist to create a grown-in doping, which functions as a BSF. A typical BSF would have about 1 x

$10^{18}/cm^3$ acceptors. To achieve this, a large amount of an acceptor dopant, such as boron, would be provided within the mold. To enhance the back side doping, as compared to the front side doping, the semiconductor crystal could be grown relatively slowly, after initial nucleation, which would provide more time for acceptors already in the melt to diffuse deeper into the melt, away from the solidifying crystal, thus allowing a much lower concentration of acceptors (boron) in the majority of the crystal compared to the initial layer grown immediately adjacent to the mold. The strength of the BSF is proportional to the ratio of doping at the back over doping in the bulk of the wafer. In addition, or alternatively, nucleation could be enhanced by providing higher vacuum (or pressure differential), as discussed below, during earlier portions of solidification. This would cause the crystal solidification and growth to start earlier, while the dopant concentration near to the mold in the portion of the melt from which the body will solidify, will form. The technique of varying the vacuum (or differential pressure regime) over time, or in different locations, is described in the above referenced Patent No. 8,293,009, by Sachs et al. Wafers have been made with a carrier concentration of 1 x $10^{18}/cm^3$ acceptors at the surface of the wafer that was formed adjacent the mold face.

[0076] The foregoing mentions adjusting vacuum pressure or differential pressure regime during solidification. This refers to a method disclosed in the 8,293,009 patent. It is beneficial for the mold described therein to be porous (as discussed below). A pressure differential is provided between the surface of the mold that contacts the surface of the molten material, and a back surface of the mold, so that upon contact, molten material is drawn toward the mold face. The porosity of the mold is such that molten material is not drawn into the porosities. This is accomplished by the porosities

being small enough so that surface tension and other phenomena prevent the molten material from entering the porosities before the material solidifies. They are also numerous enough so that the pressure differential can be established, despite their small individual sizes. The pressure differential can be established by providing a vacuum, or by providing the surface of the molten material at a pressure above atmospheric pressure, with the opposite surface of the mold at a lesser pressure, so that the pressure differential provides a force that forces the molten material and then the solidified body toward the mold face. By providing this pressure differential, the force of contact between the molten material and the mold face is enhanced as compared to a case with no pressure differential, which provides for more rapid solidification. Enhanced pressure differential can also be provided at individual locations across the mold face, as opposed to other, un-enhanced locations, by various means, such as thermal inserts or voids at specific locations in the mold face. By porous, it is meant a body that is full of very small holes and passageways, such that continuous paths exist for gas to flow from one surface of the mold to the other. The porosities are very small. They are typically micron scale, such as ten microns in diameter, up to perhaps thirty or forty microns diameter. They are numerous, covering the surface of the mold and passing through a large volume of its body. The pathways are tortuous, such as in a natural sponge. As defined herein, porous does not include macroscopic simple holes that pass from one surface to the other, such as holes drilled through the mold body.

[0077] Fig. 6B shows a cell wafer 601 with a BSF region 682 and with a rear electrode 698 in the form of fingers 671 similar to the fingers 673 of the front, sun facing electrode 699, which also shows fingers. An optical (typically white) reflector 695 (which may be specular or diffuse) is behind

(relative to the sun) the rear electrode 698. This reflector may be the back sheet used during the encapsulation of the module. There can be a physical space 687 between the back of the cell wafer and the reflector or there can be no space. In this way, photons that are not absorbed in their first pass through the main body of silicon 693 will exit the cell wafer, be reflected by the optical reflector 695 and re-enter the cell wafer from the back surface, for a second pass through the silicon body 693 and an additional chance to be absorbed. The optical reflectivity of most of the back contact is in that case governed by the reflectivity of the material 695 placed behind the cell wafer, which can be greater than 90% and in many cases, greater than 95%. The sun-facing surface of the cell wafer may be provided with a textured surface 651 similar to the prior art embodiment shown in Fig. 6A.

[0078] Fig. 7 shows, graphically, the quantum efficiency (QE) measurements for the two types of cells. The photo-response for the structure shown in Fig. 6A is shown in dashed line and is generally inside of the other curve. The photo-response for the structure of an invention hereof, with a grown-in BSF and reflective back sheet, shown in Fig. 6B, is shown in solid line, and is generally outside of the other curve. Thus, as can be seen, the photo-response of the cell is higher for the structure of an invention hereof, shown in Fig. 6B. The increased QE is in the infra-red region of the spectrum wavelengths on the graph 900nm-1200nm, as expected – because it is these longer wavelengths which can penetrate to the back of the cell. The result is a higher efficiency cell.

[0079] A basic cell structure of a wafer, and some form of BSF, for instance provided by alloying aluminum during the contact firing step, backed by an open region, a grid-like electrode, and a reflector is known in the art. An example is a PASHA cell structure. It is also known to provide a BSF by a separate doping step to provide heavier doping near the back

surface of the cell. To create such a structure requires this separate doping step. It is considered to be an invention hereof to create such a doped BSF without a separate step for same, namely by creating the BSF during the growing phase of the wafer, along with the drift field, as explained above. Thus another invention hereof concerns a novel and non-obvious method of manufacturing such a structure, wherein the doping required to create the BSF is created during the wafer growth process according to the methods of discussed above.

[0080] It has been determined that in any particular system, such as using Silicon as the semiconductor, Boron as primary dopant, and Phosphorous as compensating dopant, an undesirable condition may arise. Recall that the compensating dopant is added to the bulk of the melt over time as many runs of wafers are made from the same vessel and melt, to keep the resistivity of each newly made wafer in a series of wafers made from this same melt, to be the same. This must be done despite the fact that there is increasing accumulation of the primary dopant (for instance the boron) in the melt over time.

[0081] The undesirable phenomenon is that the compensating dopant, having a lower segregation coefficient than the primary dopant, segregates more strongly to the grain boundaries. See for instance Fig. 8A, showing, schematically, a Si crystal 800, and accumulated low segregation coefficient compensating dopant D at the grain boundaries 860. This is generally undesirable, because the higher concentration of compensating dopant D near the grain boundaries 860 results in there being a higher concentration near the grain boundaries of the carrier type D that the compensating dopant entails (in the case of P, these are donors, and thus, the letter D is used to represent them). As such, there will be an electric field established within the grains directed toward the grain boundaries, and thus, minority carriers will be drawn to the boundaries. Such a condition is undesirable, because that is

not where it is desired to direct these carriers. They are to be directed away from the surface 242 of the wafer with the higher concentration of the acceptor dopant A, toward the p/n junction (not yet formed, and thus not shown in Fig. 8A), which will be formed adjacent the surface 246, which has the lower concentration of the acceptor dopant A.

[0082] It has been determined that this undesirable effect can be overcome by the counter intuitive step of providing a 2nd compensating dopant, which is referred to herein as a counter-compensating dopant, for example in the case of a Si/B/Ph system, a counter-compensating dopant of Aluminum (Al). The aluminum is the same type of carrier donor/acceptor as the primary dopant. Thus, aluminum is an acceptor, as is boron. It is most beneficial that the segregation coefficient of the counter compensating dopant be numerically smaller than that of the 1st compensating dopant, and numerically, as close as possible to the value of the coefficient of the 1st compensating dopant. Having a numerically smaller segregation coefficient, the counter compensating dopant migrates to the grain boundaries even more strongly than does the compensating dopant. Thus, it's acceptor/donor character cancels out, compensates, for the excess degree of donor/acceptors present from the relatively high concentration of compensating dopant at these boundaries.

[0083] In cases in which the segregation coefficient of the primary dopant is numerically lower than that of the 1st compensating dopant, it is not necessary to use a 2nd, counter compensating dopant (and thus, the compensating dopant is simply a compensating dopant, not a first compensating dopant). A very useful combination for a Silicon semiconductor uses Boron for the primary dopant, Phosphorous for the compensating dopant, and Ga (Gallium) for the 2nd counter compensating dopant. B has the largest (least segregating)

segregation coefficient, at 0.8 followed by P at 0.3 and Ga at 0.008.

[0084] Table C shows different combinations of Primary (substrate) dopant, compensating dopant and 2nd counter compensating dopant, for both P-type semiconductor crystals, such as Silicon, and N-type semiconductors, as shown in Table A, but with the further information relating to the counter compensating dopants. The segregation coefficient for each element is also provided at the first mention of the element.

P-Type			N-type		
Primary dopant	comp dopant	counter comp dopant	Primary dopant	comp dopant	counter comp dopant
B (0.8)	P (0.3)	Al	P	B	As
Al (.002)	As (0.3)	Ga	As	Al	Sb
Ga (0.008)	Sb (0.023)	In	Sb	Ga	Bi
In (0.004)	Bi (0.0007)		Bi	In	
B (0.8)	P (0.3)	Ga			

TABLE C - Combinations of Primary, Compensating and Counter Compensating Dopant, for P-type and N-type Semiconductors

[0085] The compounds listed in Table C above can be used for providing the counter compensating dopant as well as the primary and compensating dopants. In the case where both an n-

type and p—type dopant is added to the melt, a compound semiconductor could be used to add the 2nd, counter compensating dopant. For example with a Boron primary dopant, InP (Indium phosphide) could be used. The phosphorous would provide compensating doping, and the Indium would provide counter compensation, in the same manner as would Ga, in the table above. But the P and In would be provided as a compound agent, rather as individual additives.

EXAMPLES

[0086] Wafers have been grown and solar cells have been made. Solar cells show high efficiency at very low resistivity. For example solar cells made on wafers using this method having an average bulk resistivity of only 0.3Ohm-cm had 2% higher efficiency than control wafers having a resistivity of 2.2Ohm-cm. The doping profile shown schematically in Fig. 5 was measured by selectively removing layer after layer of silicon and measuring resistivity of the remaining wafer. In general, lower resistivity is present in regions with higher dopant concentration, and vice versa. (Doping was inferred by measuring resistivity, because measuring concentrations of material in a formed wafer is difficult, however, measuring resistivity, layer by layer, is not particularly difficult. Thus when considering infringement of claims herein, presence of a profile in resistivity, from one surface to another, may be considered to be evidence of a corresponding profile in dopant concentration. Furthermore, wafers exhibiting a profile in resistivity, with lesser resistivity at one surface (typically the back surface, not facing the sun, where there is a higher dopant concentration in p-type wafers), and higher resistivity at the other surface, which would be the sun facing surface, in that case, are considered to be an invention hereof, as are solar cells including such wafers, and methods of making such wafers.

[0087] The average net acceptor concentration was about $5x10^{15}/cm^3$ with about 10 times more doping at the back (formed on mold facing side) surface. The cell had an aluminum back surface field, not a grown in BSF, as also discussed above. The boron dopant was about $1X10^{18}$atoms/cm^3. Impurity content was minimal, and, in any case, less than ten times the amount that would be present at equilibrium segregation. There was a range of compensating dopant from none (at the very beginning of the run) to about 1 X 10^{18} atoms/cm^3 at the end of the run (in which approximately 2,000 wafers were made.

[0088] Inventions disclosed herein solve numerous problems. An invention hereof allows the low cost establishment of a dopant gradient from one surface of the formed wafer to the other. To date, methods known to establish a gradient in dopants in silicon wafers result in low quality silicon (such as gallium doped RGS (ribbon growth on substrate) or are very costly (epitaxial grown silicon).

[0089] It should be noted that many/any of the foregoing techniques to provide a wafer with a profile of doping level can be used with any others. For instance, the any of the modalities of providing dopant to the mold, for instance in a coating, in the body of the mold or near the surface of the mold, can be used with any of the methods of compensating for excessive dopant in the melt over time, and also any method of counter compensating for excessive segregation of the compensating dopant to the grain boundaries can be used with any other method of providing a doping profile. Provision of dopant to a degree and in locations to create a BSF can be used with any of the techniques for dopant compensation, and also for countering the accumulation of compensating dopant at the grain boundaries. Techniques for forming a dopant profile of any curve, or shape, can be used with the compensating and counter compensating techniques, and also with methods of forming a BSF.

[0090] This disclosure describes and discloses more than one invention. The inventions are set forth in the claims of this and related documents, not only as filed, but also as developed during prosecution of any patent application based on this disclosure. The inventors intend to claim all of the various inventions to the limits permitted by the prior art, as it is subsequently determined to be. No feature described herein is essential to each invention disclosed herein. Thus, the inventors intend that no features described herein, but not claimed in any particular claim of any patent based on this disclosure, should be incorporated into any such claim.

[0091] For instance, the invention of a drift field is not essential to the invention of a BSF, and vice versa. A drift field can be established that is gradual, and which does not have an extremely highly doped BSF. A BSF can be provided with a relatively highly doped region, and the rest of the wafer can be relatively uniform, essentially with no drift field, or with only a drift field of mild degree. It is not necessary to provide compensating dopant in a melt, either for single wafer formation, or even for a run of wafers, so long as the concentration of primary dopant in the melt does not become too large to form quality wafers. Other methods of dopant compensation can be used. Likewise, the method of counter compensating, to prevent excessive accumulation of the compensating dopant at grain boundaries, which is disclosed herein of providing a counter dopant with an even smaller segregation coefficient, need not be used. Such accumulation may be tolerated for some applications, or other methods of countering the accumulation could be used.

[0092] Some assemblies of hardware, or groups of steps, are referred to herein as an invention. However, this is not an admission that any such assemblies or groups are necessarily patentably distinct inventions, particularly as contemplated by laws and regulations regarding the number of inventions

that will be examined in one patent application, or unity of invention. It is intended to be a short way of saying an embodiment of an invention.

[0093] An abstract is submitted herewith. It is emphasized that this abstract is being provided to comply with the rule requiring an abstract that will allow examiners and other searchers to quickly ascertain the subject matter of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims, as promised by the Patent Office's rule.

[0094] The foregoing discussion should be understood as illustrative and should not be considered to be limiting in any sense. While the inventions have been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the inventions as defined by the claims.

[0095] The corresponding structures, materials, acts and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or acts for performing the functions in combination with other claimed elements as specifically claimed.

ASPECTS OF INVENTIONS

[0096] The following aspects of inventions hereof are intended to be described herein, and this section is to ensure that they are mentioned. They are named aspects, and although they appear similar to claims, they are not claims. However, at some point in the future, the applicants reserve the right to claim any and all of these aspects in this and any related applications.

[0097] A1. A method for fabricating a semiconductor wafer for use as a solar collector, the method comprising the steps of:

a. providing a molten semiconductor material, having a surface;

b. providing a mold, comprising a forming surface, the mold also comprising a primary dopant relative to the semiconductor material;

c. contacting the forming surface to the molten material such that dopant migrates from the mold into the molten semiconductor material; and

d. maintaining conditions such that a body of semiconductor material in the form of a wafer solidifies upon the forming surface, with a first surface contacting the forming surface, the wafer having a profile of dopant concentration, there being a larger concentration of dopant at the first surface of the wafer, and a lesser concentration of dopant at a second surface of the wafer.

[0098] A2. A method for fabricating a semiconductor wafer for use as a solar collector, the method comprising the steps of:

a. providing a molten semiconductor material, having a surface;

b. providing a mold, comprising a forming surface, the mold also comprising a dopant relative to the semiconductor material;

c. contacting the forming surface to the molten material for a contact duration such that for at least a portion of the contact duration dopant migrates from the mold into the molten semiconductor material; and

d. maintaining conditions such that a body of semiconductor material in the form of a wafer solidifies

upon the forming surface, the wafer having a profile of resistivity, there being a relatively lesser resistivity at a first surface of the wafer, and a relatively larger resistivity at a second surface of the wafer.

[0099] A3. The method of any one of aspects 1 and 2, further comprising the step of detaching the solidified wafer from the forming surface.

[00100] A4. The method of any one of aspects 1 - 3, the mold comprising a coating on one surface, which coating contains the primary dopant.

[00101] A5. The method of any one of aspects 1 - 3, the mold further comprising a body, wherein the primary dopant is distributed within the mold body.

[00102] A6. The method of any one of aspects 1 - 3, the mold further comprising a body, wherein the primary dopant is within the mold body at a higher concentration near one surface.

[00103] A7. The method of any one of aspects 1 - 6, the step of maintaining conditions comprising providing the primary dopant at the mold in a form for which the solidifying body of semiconductor acts as a diffusion barrier, such that as the solidifying body grows, initially primary dopant migrates at a first rate into the molten material, and the solidifying body, and subsequently, primary dopant migrates at lesser and lesser rates into the molten material and the solidifying body, so that portions of the body that solidify earlier have relatively more primary dopant per unit volume, as compared to portions of the body that solidify later.

[00104] A8. The method of any one of aspects 1-7, the primary dopant comprising a charge carrier of one type only of a donor and an acceptor type, further comprising;

conducting steps a, b, c, and d (of aspect 1 or 2, as appropriate) at least two times;

providing in the molten material, a quantity of compensating dopant of an opposite charge carrier donor/acceptor type to the primary dopant.

[00105] A9. The method of aspect 8, further comprising, the step of providing in the molten material, a quantity of counter compensating dopant of an opposite charge carrier donor/acceptor type to the compensating dopant.

[00106] A10. The method of aspect 9, the compensating and the counter compensating dopants each having an equilibrium segregation coefficient, the equilibrium segregation coefficient of the counter compensating dopant being equal to or less than the equilibrium segregation coefficient of the compensating dopant.

[00107] A11. The method of aspect 8 where the step of providing a quantity of compensating dopant is accomplished by providing the compensating dopant in the melt at a concentration C_{cd} according to the following relation:

$$C_{cd} \text{ approximately equals } C_{md}*(k_{md}/k_{cd})$$

C_{md} is the melt concentration of the primary dopant;

C_{cd} is the melt concentration of the compensating dopant;

k_{md} is the effective segregation coefficient of the primary dopant; and

k_{cd} is the effective segregation coefficient of the compensating dopant.

[00108] A12. The method of aspect 1, the primary dopant concentration being less than or equal to 1×10^{20} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1×10^{15} N_x/cm^3 at the second surface of the wafer, where N_x

means for a charge carrier acceptor dopant, the number of charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

[00109] A13. The method of aspect 2 the primary dopant being a charge carrier acceptor, the resistivity being greater than or equal to 0.001 ohm-cm at the first surface of the wafer and less than or equal to about 10 ohm-cm at the second surface of the wafer.

[00110] A14. The method of aspect 1, the primary dopant concentration being less than or equal to 1 x 10^{19} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1 x 10^{17} N_x/cm^3 at the second surface of the wafer, where N_x means for a charge carrier acceptor dopant, the number of charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

[00111] A15. The method of aspect 2, the primary dopant being a charge carrier donor, the resistivity being greater than or equal to 0.001 ohm-cm at the first surface of the wafer and less than or equal to about 0.1 ohm-cm at the second surface of the wafer.

[00112] A16. The method of any one of aspects 1 and 2, the semiconductor comprising a p-type semiconductor, the primary dopant being chosen from the group consisting of: boron, aluminum, gallium and indium.

[00113] A17. The method of any one of aspects 1 and 2, the semiconductor comprising an n-type semiconductor, the primary dopant being chosen from the group consisting of: phosphorous, arsenic, Antimony (Sb) and bismuth.

[00114] A18. The method of aspect 8, the semiconductor comprising a p-type semiconductor, the compensating dopant

being chosen from the group consisting of: phosphorous, arsenic, antimony (Sb) and Bismuth.

[00115] A19. The method of aspect 8, the semiconductor comprising an n-type semiconductor, the compensating dopant being chosen from the group consisting of boron, aluminum, gallium and indium.

[00116] A20. The method of aspect 18, further comprising the step of providing in the molten material a counter compensating dopant selected from the group consisting of: aluminum, gallium and Indium.

[00117] A21. The method of aspect 19, further comprising the step of providing in the molten material, a counter compensating dopant selected from the group consisting of: arsenic, antimony and bismuth.

[00118] A22. The method of aspect 4, the molten material comprising silicon, the coating comprising a dopant selected from the group consisting of: B_4C (boron carbide) and B_4Si (boron silicide).

[00119] A23. The method of any one of aspects 1 and 2, the primary dopant comprising a compound selected from the group consisting of a carbide, an oxide, a nitride and a silicide, or an element selected from the group consisting of: boron, aluminum, gallium, indium, phosphorous, arsenic, antimony and bismuth.

[00120] A24. The method of any one of aspects 1 and 2, the step of maintaining being conducted so as to provide a concentration of primary dopant at the first surface of the wafer sufficiently high so as to establish a back surface field in a wafer used as a solar collector.

[00121] A25. The method of aspect 24, further comprising the steps of providing:

a. coupled to the wafer, a metallic conductor in the form of an open grid, contacting the first surface of the wafer; and

b. spaced from the first surface, an optical reflector, arranged such that the metallic conductor is between the first surface and the optical reflector.

[00122] A26. The method of aspect 1, the profile of dopant concentration having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

[00123] A27. The method of aspect 2, the profile of resistivity having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

[00124] A28. A semiconductor wafer for use as a solar collector, the wafer comprising a body having a first and a second surface, the body having a dopant concentration profile, there being a larger concentration of dopant at a first surface of the wafer, and a continuous transition to a lesser concentration of dopant at a second surface of the wafer, the larger concentration being at least three times the lesser concentration, further, where any metallic impurities that are present in the body are present at the first surface to a degree less than ten times the degree of metallic impurities that are present at the second surface.

[00125] A29. A semiconductor wafer for use as a solar collector, the wafer comprising a body having a first and a second surface, the body having a resistivity profile, there being a smaller resistivity at a first surface of the wafer, and a continuous transition to a larger resistivity at a second surface of the wafer, the larger resistivity being at least three times the smaller resistivity, further, where any metallic impurities that are present in the body are present

at the first surface to a degree less than ten times the degree of metallic impurities that are present at the second surface.

[00126] A30. The semiconductor wafer of any one of aspects 28 and 29, the semiconductor comprising silicon, and the dopant comprising boron.

[00127] A31. The semiconductor wafer of any one of aspects 28 and 29, the semiconductor comprising silicon and the dopant being selected from the group consisting of: boron, aluminum, gallium and indium.

[00128] A32. The semiconductor wafer of any one of aspects 28 and 29, the semiconductor comprising a p-type semiconductor and the dopant being selected from the group consisting of: boron, aluminum, gallium and indium.

[00129] A33. The semiconductor wafer of any one of aspects 28 and 29, the semiconductor comprising an n-type semiconductor and the dopant being selected from the group consisting of: phosphorous, arsenic, Antimony (Sb) and bismuth.

[00130] A34. The semiconductor wafer of aspect 28, the dopant concentration being less than or equal to 1 x 10^{20} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1 x 10^{15} N_x/cm^3 at the second surface of the wafer, where N_x means, for a charge carrier acceptor dopant, the number of charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

[00131] A35. The semiconductor wafer of aspect 29, the resistivity being greater than or equal to 0.001 ohm-cm at the first surface of the wafer and less than or equal to about 10 ohm-cm at the second surface of the wafer.

[00132] A36. The semiconductor wafer aspect 28, the concentration of primary dopant at the first surface of the wafer being sufficiently high so as to establish a back surface field in a wafer used as a solar collector.

[00133] A37. The semiconductor wafer aspect 29, the resistivity at the first surface of the wafer being sufficiently low so as to establish a back surface field in a wafer used as a solar collector.

[00134] A38. The semiconductor wafer of any one of aspects 36 and 37, further comprising:

a. coupled to the wafer, a metallic conductor in the form of an open grid, contacting the first surface of the wafer; and

b. spaced from the first surface, an optical reflector, arranged such that the metallic conductor is between the first surface and the optical reflector.

[00135] A39. The semiconductor wafer of aspect 28, the profile of dopant concentration having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

[00136] A40. The semiconductor wafer of aspect 29, the profile of resistivity having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

[00137] A41. A solar collector comprising a plurality of semiconductor wafers, each wafer comprising a body having a first and a second surface, the body having a dopant concentration profile, there being a larger concentration of dopant at a first surface of the wafer, and a continuous transition to a lesser concentration of dopant at a second surface of the wafer, the larger concentration being at least

three times the lesser concentration, further, where any metallic impurities that are present in the body are present at the first surface to a degree less than ten times the degree of metallic impurities that are present at the second surface.

[00138] A42. A solar collector comprising a plurality of semiconductor wafers, each wafer comprising a body having a first and a second surface, the body having a profile of resistivity, there being a relatively lesser resistivity at a first surface of the wafer, and a continuous transition to a relatively larger resistivity at a second surface of the wafer, further, where any metallic impurities that are present in the body are present at the first surface to a degree less than ten times the degree of metallic impurities that are present at the second surface.

[00139] A43. The solar collector of any one of aspects 41 and 42, the semiconductor comprising silicon, and the dopant comprising boron.

[00140] A44. The solar collector of any one of aspects 41 and 42, the semiconductor comprising silicon and the dopant being selected from the group consisting of: boron, aluminum, gallium and indium.

[00141] A45. The solar collector of any one of aspects 41 and 42, the semiconductor comprising a p-type semiconductor and the dopant being selected from the group consisting of: boron, aluminum, gallium and indium.

[00142] A46. The solar collector of any one of aspects 41 and 42, the semiconductor comprising an n-type semiconductor and the dopant being selected from the group consisting of: phosphorous, arsenic, Antimony (Sb) and bismuth.

[00143] A47. The solar collector of aspect 41, the dopant concentration being less than or equal to 1 x 10^{20} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1 x 10^{15} N_x/cm^3 at the second surface of the wafer, where N_x means, for a charge carrier acceptor dopant, the number of charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

[00144] A48. The solar collector of aspect 42, the resistivity being greater than or equal to 0.001 ohm-cm at the first surface of the wafer and less than or equal to about 10 ohm-cm at the second surface of the wafer.

[00145] A49. The solar collector of aspect 41, the concentration of primary dopant at the first surface of the wafer being sufficiently high so as to establish a back surface field in a wafer used as a solar collector.

[00146] A50. The solar collector aspect 42, the resistivity at the first surface of the wafer being sufficiently low so as to establish a back surface field in a wafer used as a solar collector.

[00147] A51. The solar collector of any one of aspects 49 and 50, further comprising:

a. coupled to the wafer, a metallic conductor in the form of an open grid, contacting the first surface of the wafer; and

b. spaced from the first surface, an optical reflector, arranged such that the metallic conductor is between the first surface and the optical reflector.

[00148] A52. The solar collector of aspect 41, the profile of dopant concentration having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

[00149] A53. The solar collector of aspect 42, the profile of resistivity having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

[00150] Having described the invention, what is claimed is:

CLAIMS

1. A method for fabricating a semiconductor wafer for use as a solar collector, the method comprising the steps of:

a. providing a molten semiconductor material, having a surface;

b. providing a mold, comprising a forming surface, the mold also comprising a primary dopant relative to the semiconductor material;

c. contacting the forming surface to the molten material such that dopant migrates from the mold into the molten semiconductor material; and

d. maintaining conditions such that a body of semiconductor material in the form of a wafer solidifies upon the forming surface, with a first surface contacting the forming surface, the wafer having a profile of dopant concentration, there being a larger concentration of dopant at the first surface of the wafer, and a lesser concentration of dopant at a second surface of the wafer.

2. A method for fabricating a semiconductor wafer for use as a solar collector, the method comprising the steps of:

a. providing a molten semiconductor material, having a surface;

b. providing a mold, comprising a forming surface, the mold also comprising a dopant relative to the semiconductor material;

c. contacting the forming surface to the molten material for a contact duration such that for at least a portion of the contact duration dopant migrates from the mold into the molten semiconductor material; and

d. maintaining conditions such that a body of semiconductor material in the form of a wafer solidifies upon the forming surface, the wafer having a profile of resistivity, there being a relatively lesser resistivity at a first surface of the wafer, and a relatively larger resistivity at a second surface of the wafer.

3. The method of any one of claims 1 and 2, further comprising the step of detaching the solidified wafer from the forming surface.

4. The method of any one of claims 1 and 2, the mold comprising a coating on one surface, which coating contains the primary dopant.

5. The method of any one of claims 1 and 2, the mold further comprising a body, wherein the primary dopant is distributed within the mold body.

6. The method of any one of claims 1 and 2, the mold further comprising a body, wherein the primary dopant is within the mold body at a higher concentration near one surface.

7. The method of any one of claims 1 and 2, the step of maintaining conditions comprising providing the primary dopant at the mold in a form for which the solidifying body of semiconductor acts as a diffusion barrier, such that as the solidifying body grows, initially primary dopant migrates at a first rate into the molten material, and the solidifying body, and subsequently, primary dopant migrates at lesser and lesser rates into the molten material and the solidifying body, so that portions of the body that solidify earlier have relatively more primary dopant per unit volume, as compared to portions of the body that solidify later.

8. The method of claim 3, the primary dopant comprising a charge carrier of one type only of a donor and an acceptor type, further comprising;

conducting steps a, b, c, and d (of claim 1 or 2, as appropriate) at least two times;

providing in the molten material, a quantity of compensating dopant of an opposite charge carrier donor/acceptor type to the primary dopant.

9. The method of claim 8, further comprising, the step of providing in the molten material, a quantity of counter compensating dopant of an opposite charge carrier donor/acceptor type to the compensating dopant.

10. The method of claim 9, the compensating and the counter compensating dopants each having an equilibrium segregation coefficient, the equilibrium segregation coefficient of the counter compensating dopant being equal to or less than the equilibrium segregation coefficient of the compensating dopant.

11. The method of claim 8 where the step of providing a quantity of compensating dopant is accomplished by providing the compensating dopant in the melt at a concentration C_{cd} according to the following relation:

C_{cd} approximately equals $C_{md}*(k_{md}/k_{cd})$ where:

C_{md} is the melt concentration of the primary dopant;

C_{cd} is the melt concentration of the compensating dopant;

k_{md} is the effective segregation coefficient of the primary dopant; and

k_{cd} is the effective segregation coefficient of the compensating dopant.

12. The method of claim 1, the primary dopant concentration being less than or equal to 1×10^{20} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1×10^{15} N_x/cm^3 at the second surface of the wafer, where N_x means for a charge carrier acceptor dopant, the number of

charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

13. The method of claim 2 the primary dopant being a charge carrier acceptor, the resistivity being greater than or equal to 0.001 ohm-cm at the first surface of the wafer and less than or equal to about 10 ohm-cm at the second surface of the wafer.

14. The method of claim 1, the primary dopant concentration being less than or equal to 1 x 10^{19} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1 x 10^{17} N_x/cm^3 at the second surface of the wafer, where N_x means for a charge carrier acceptor dopant, the number of charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

15. The method of claim 1, the primary dopant being a charge carrier donor, the resistivity being greater than or equal to 0.001 ohm-cm at the first surface of the wafer and less than or equal to about 0.1 ohm-cm at the second surface of the wafer.

16. The method of any one of claims 1 and 2, the semiconductor comprising a p-type semiconductor, the primary dopant being chosen from the group consisting of: boron, aluminum, gallium and indium.

17. The method of any one of claims 1 and 2, the semiconductor comprising an n-type semiconductor, the primary dopant being chosen from the group consisting of: phosphorous, arsenic, Antimony (Sb) and bismuth.

18. The method of claim 8, the semiconductor comprising a p-type semiconductor, the compensating dopant being chosen from the group consisting of: phosphorous, arsenic, antimony (Sb) and Bismuth.

19. The method of claim 8, the semiconductor comprising an n-type semiconductor, the compensating dopant being chosen

from the group consisting of boron, aluminum, gallium and indium.

20. The method of claim 18, further comprising the step of providing in the molten material, a counter compensating dopant selected from the group consisting of: aluminum, gallium and Indium.

21. The method of claim 19, further comprising the step of providing in the molten material, a counter compensating dopant selected from the group consisting of: arsenic, antimony and bismuth.

22. The method of claim 4, the molten material comprising silicon, the coating comprising a dopant selected from the group consisting of: B_4C (boron carbide) and B_4Si (boron silicide).

23. The method of any one of claims 1 and 2, the primary dopant comprising a compound selected from the group consisting of a carbide, an oxide, a nitride and a silicide, or an element selected from the group consisting of: boron, aluminum, gallium, indium, phosphorous, arsenic, antimony and bismuth.

24. The method of any one of claims 1 and 2, the step of maintaining being conducted so as to provide a concentration of primary dopant at the first surface of the wafer sufficiently high so as to establish a back surface field in a wafer used as a solar collector.

25. The method of claim 24, further comprising the steps of providing:

a. coupled to the wafer, a metallic conductor in the form of an open grid, contacting the first surface of the wafer; and

b. spaced from the first surface, an optical reflector, arranged such that the metallic conductor is between the first surface and the optical reflector.

26. The method of claim 1, the profile of dopant concentration having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

27. The method of claim 2, the profile of resistivity having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

28. A semiconductor wafer for use as a solar collector, the wafer comprising a body having a first and a second surface, the body having a dopant concentration profile, there being a larger concentration of dopant at a first surface of the wafer, and a continuous transition to a lesser concentration of dopant at a second surface of the wafer, the larger concentration being at least three times the lesser concentration, further, where any metallic impurities that are present in the body are present at the first surface to a degree less than ten times the degree of metallic impurities that are present at the second surface.

29. A semiconductor wafer for use as a solar collector, the wafer comprising a body having a first and a second surface, the body having a resistivity profile, there being a smaller resistivity at a first surface of the wafer, and a continuous transition to a larger resistivity at a second surface of the wafer, the larger resistivity being at least three times the smaller resistivity, further, where any metallic impurities that are present in the body are present at the first surface to a degree less than ten times the degree of metallic impurities that are present at the second surface.

30. The semiconductor wafer of any one of claims 28 and 29, the semiconductor comprising silicon, and the dopant comprising boron.

31. The semiconductor wafer of any one of claims 28 and 29, the semiconductor comprising silicon and the dopant being

selected from the group consisting of: boron, aluminum, gallium and indium.

32. The semiconductor wafer of any one of claims 28 and 29, the semiconductor comprising a p-type semiconductor and the dopant being selected from the group consisting of: boron, aluminum, gallium and indium.

33. The semiconductor wafer of any one of claims 28 and 29, the semiconductor comprising an n-type semiconductor and the dopant being selected from the group consisting of: phosphorous, arsenic, Antimony (Sb) and bismuth.

34. The semiconductor wafer of claim 28, the dopant concentration being less than or equal to 1×10^{20} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1×10^{15} N_x/cm^3 at the second surface of the wafer, where N_x means, for a charge carrier acceptor dopant, the number of charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

35. The semiconductor wafer of claim 29, the resistivity being greater than or equal to 0.001 ohm-cm at the first surface of the wafer and less than or equal to about 10 ohm-cm at the second surface of the wafer.

36. The semiconductor wafer claim 28, the concentration of primary dopant at the first surface of the wafer being sufficiently high so as to establish a back surface field in a wafer used as a solar collector.

37. The semiconductor wafer claim 29, the resistivity at the first surface of the wafer being sufficiently low so as to establish a back surface field in a wafer used as a solar collector.

38. The semiconductor wafer of any one of claims 36 and 37, further comprising:

a. coupled to the wafer, a metallic conductor in the form of an open grid, contacting the first surface of the wafer; and

b. spaced from the first surface, an optical reflector, arranged such that the metallic conductor is between the first surface and the optical reflector.

39. The semiconductor wafer of claim 28, the profile of dopant concentration having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

40. The semiconductor wafer of claim 29, the profile of resistivity having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

41. A solar collector comprising a plurality of semiconductor wafers, each wafer comprising a body having a first and a second surface, the body having a dopant concentration profile, there being a larger concentration of dopant at a first surface of the wafer, and a continuous transition to a lesser concentration of dopant at a second surface of the wafer, the larger concentration being at least three times the lesser concentration, further, where any metallic impurities that are present in the body are present at the first surface to a degree less than ten times the degree of metallic impurities that are present at the second surface.

42. A solar collector comprising a plurality of semiconductor wafers, each wafer comprising a body having a first and a second surface, the body having a profile of resistivity, there being a relatively lesser resistivity at a first surface of the wafer, and a continuous transition to a relatively larger resistivity at a second surface of the wafer, further, where any metallic impurities that are present in the body are present at the first surface to a degree less

than ten times the degree of metallic impurities that are present at the second surface.

43. The solar collector of any one of claims 41 and 42, the semiconductor comprising silicon, and the dopant comprising boron.

44. The solar collector of any one of claims 41 and 42, the semiconductor comprising silicon and the dopant being selected from the group consisting of: boron, aluminum, gallium and indium.

45. The solar collector of any one of claims 41 and 42, the semiconductor comprising a p-type semiconductor and the dopant being selected from the group consisting of: boron, aluminum, gallium and indium.

46. The solar collector of any one of claims 41 and 42, the semiconductor comprising an n-type semiconductor and the dopant being selected from the group consisting of: phosphorous, arsenic, Antimony (Sb) and bismuth.

47. The solar collector of claim 41, the dopant concentration being less than or equal to 1 x 10^{20} N_x/cm^3 at the first surface of the wafer and greater than or equal to about 1 x 10^{15} N_x/cm^3 at the second surface of the wafer, where N_x means, for a charge carrier acceptor dopant, the number of charge carrier acceptors N_a and, for a charge carrier donor dopant, the number of charge carrier donors N_d.

48. The solar collector of claim 42, the resistivity being greater than or equal to 0.001 ohm-cm at the first surface of the wafer and less than or equal to about 10 ohm-cm at the second surface of the wafer.

49. The solar collector of claim 41, the concentration of primary dopant at the first surface of the wafer being sufficiently high so as to establish a back surface field in a wafer used as a solar collector.

50. The solar collector claim 42, the resistivity at the first surface of the wafer being sufficiently low so as to establish a back surface field in a wafer used as a solar collector.

51. The solar collector of any one of claims 49 and 50, further comprising:

a. coupled to the wafer, a metallic conductor in the form of an open grid, contacting the first surface of the wafer; and

b. spaced from the first surface, an optical reflector, arranged such that the metallic conductor is between the first surface and the optical reflector.

52. The solar collector of claim 41, the profile of dopant concentration having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

53. The solar collector of claim 42, the profile of resistivity having a shape that will give rise to a drift electric field within the wafer body directed to urge charge carriers in a preferred direction.

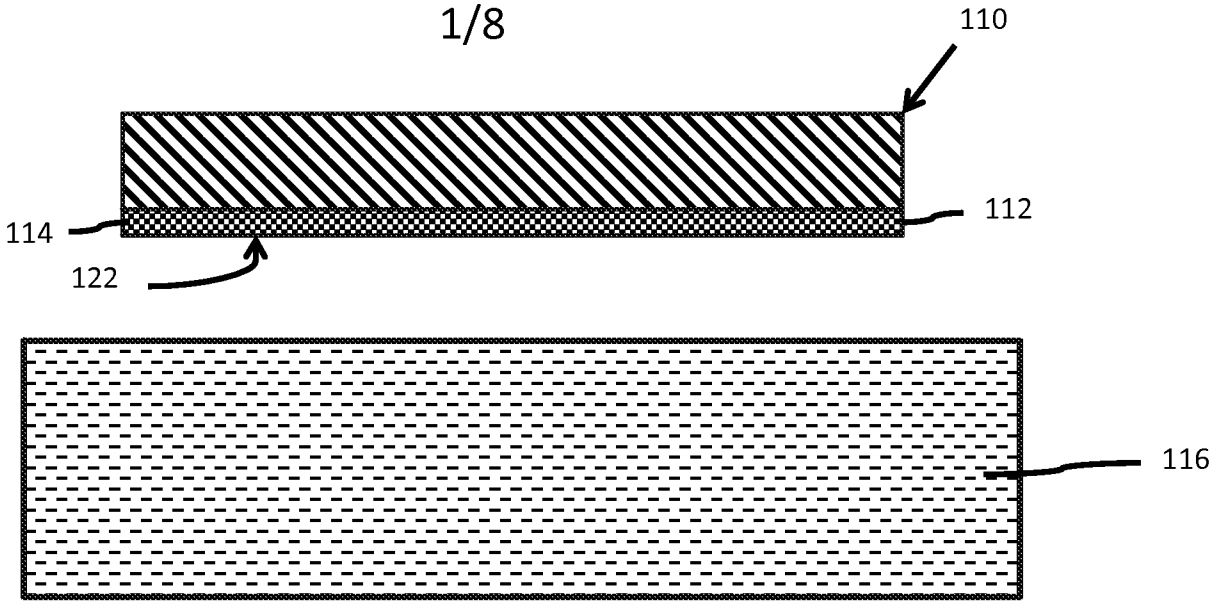

Fig. 1A

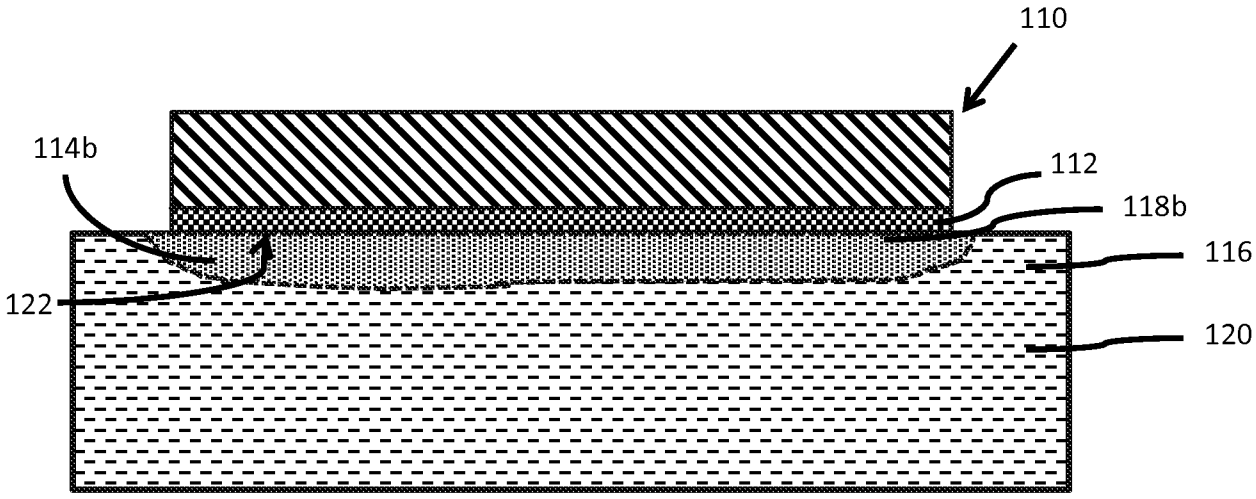

Fig. 1B

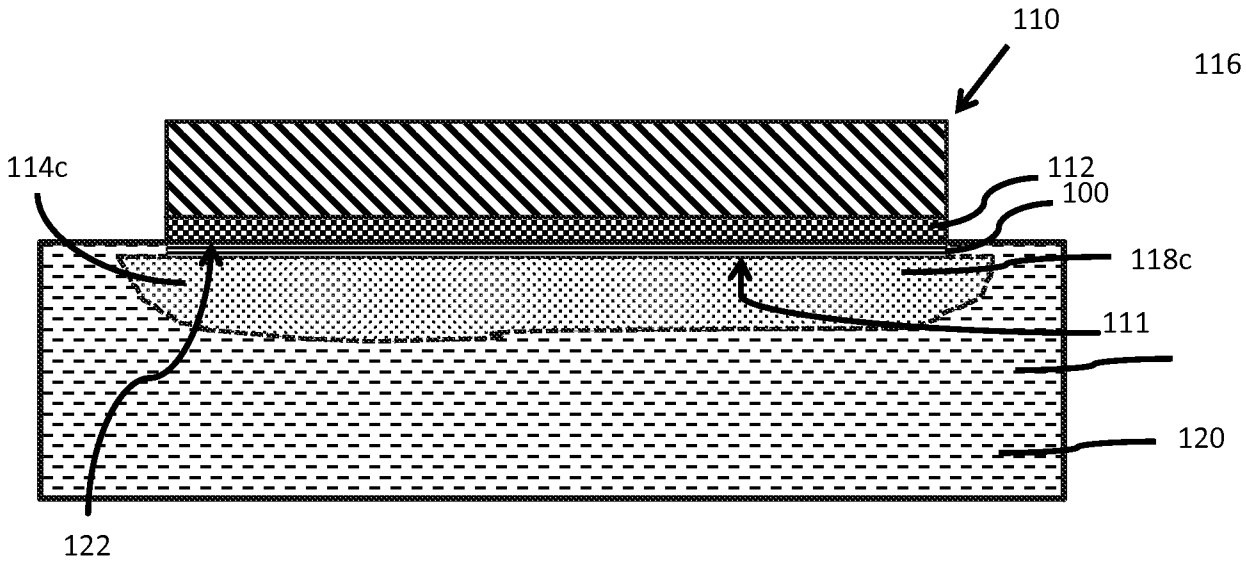
110
116
114c
112
100
118c
111
120
122

Fig. 1C

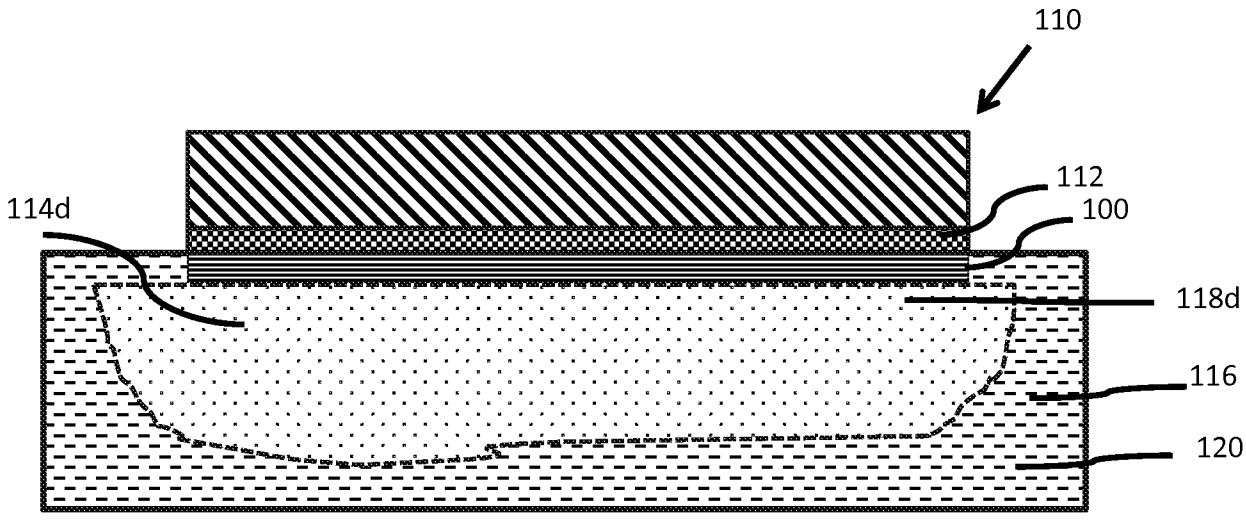
110
114d
112
100
118d
116
120

Fig. 1D

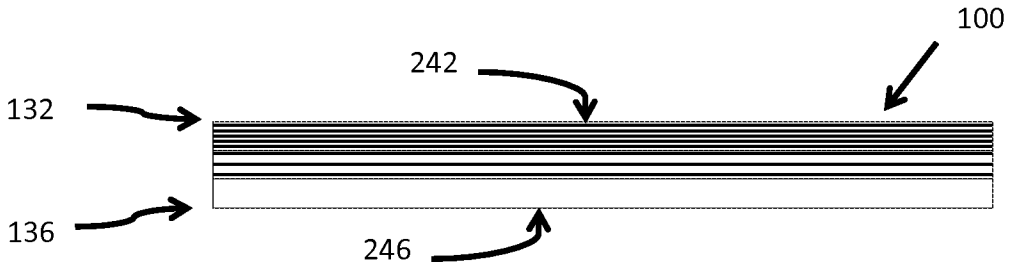

Fig. 2A

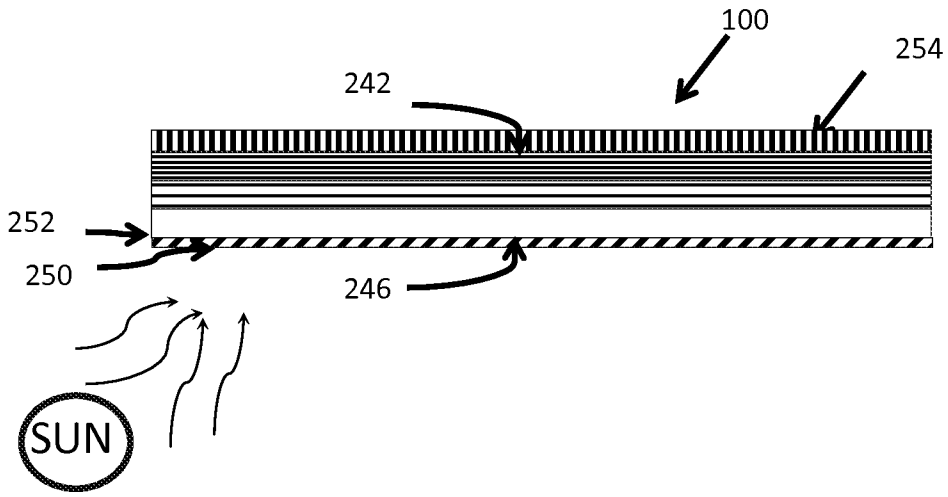

Fig. 2B

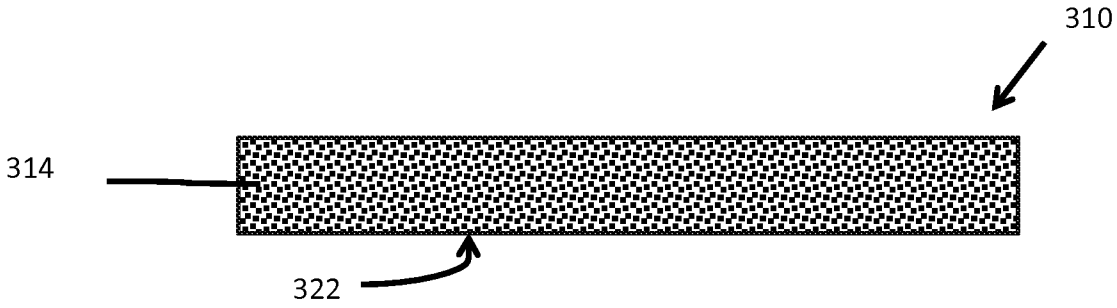

Fig. 3

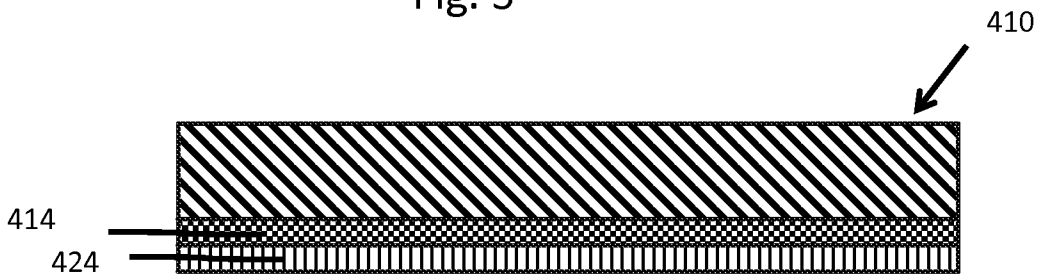

Fig. 4

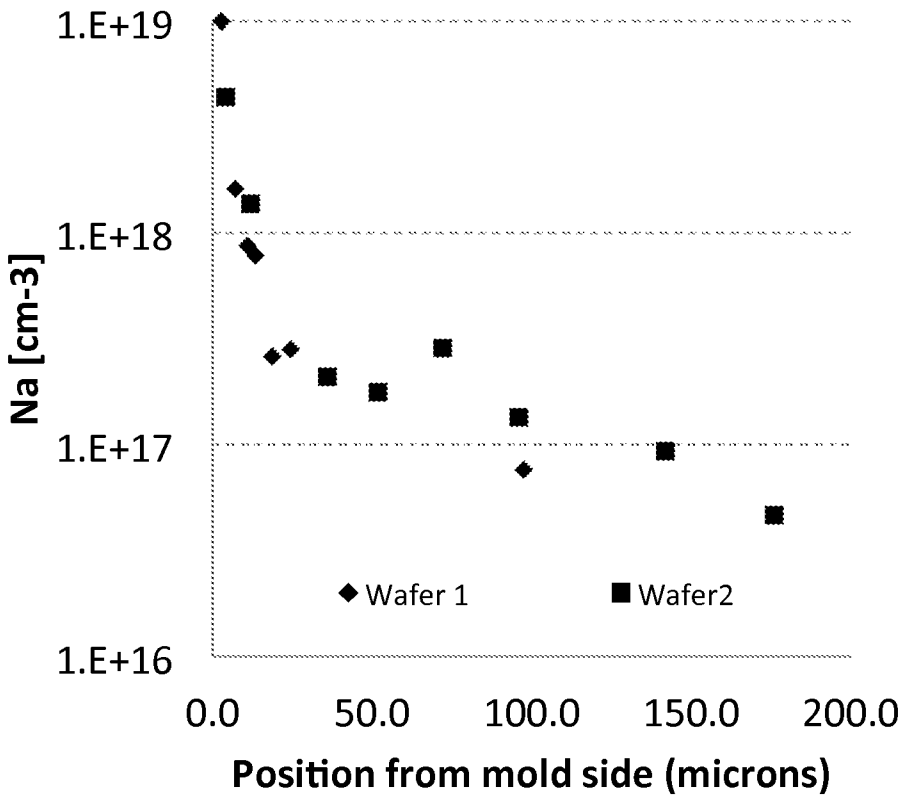
1.E+19
1.E+18
1.E+17
1.E+16
Na [cm-3]
Wafer 1
Wafer2
0.0
50.0
100.0
150.0
200.0
Position from mold side (microns)

Fig. 5

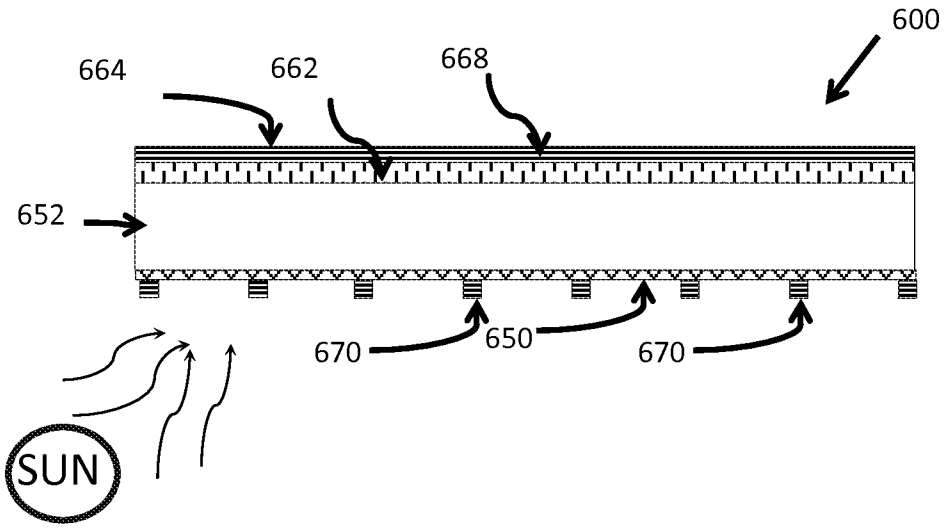

Fig. 6A
(PRIOR ART)

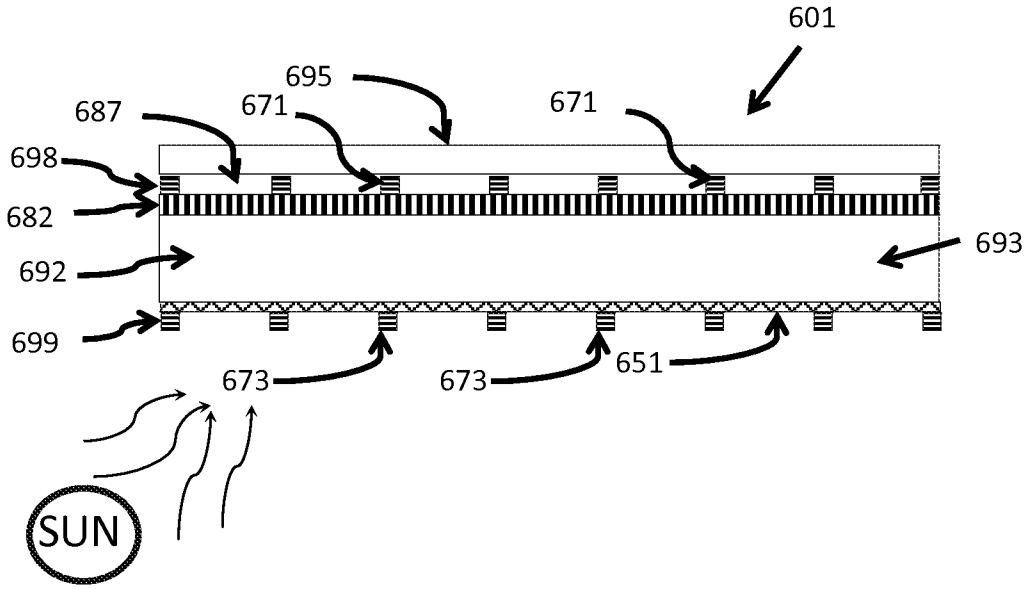

Fig. 6B

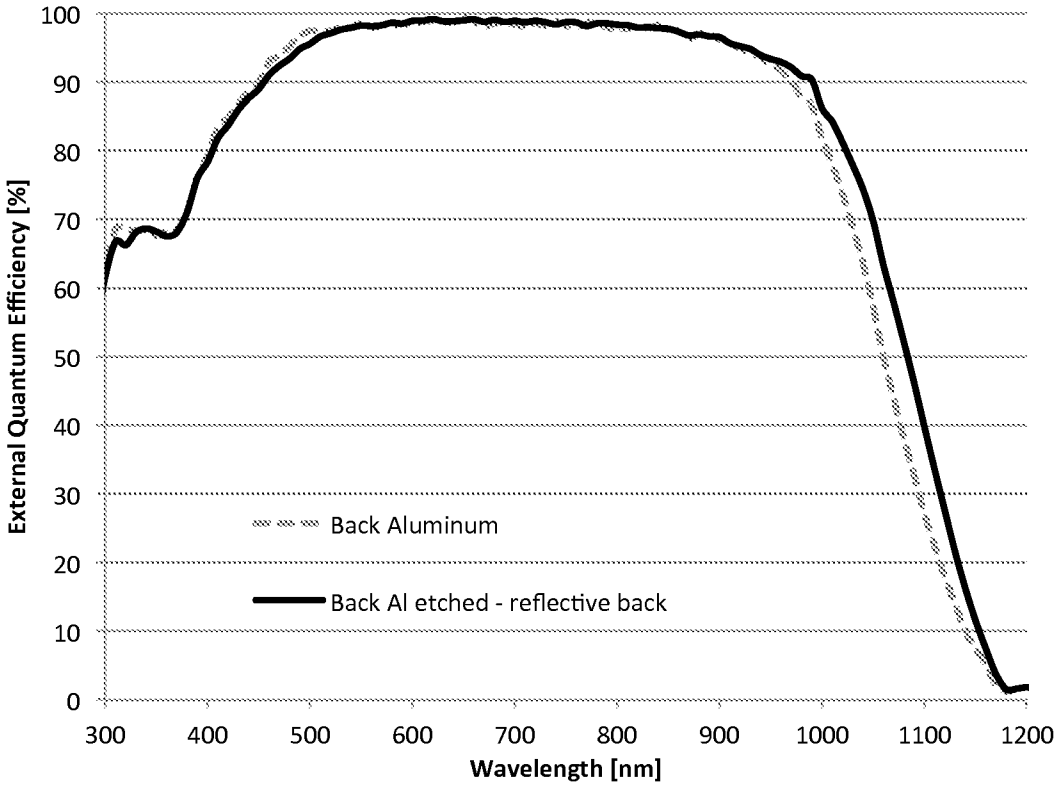
External Quantum Efficiency [%]
100
90
80
70
60
50
40
30
20
10
0
300
400
500
600
700
800
900
1000
1100
1200
Wavelength [nm]
Back Aluminum
Back Al etched - reflective back

Fig. 7

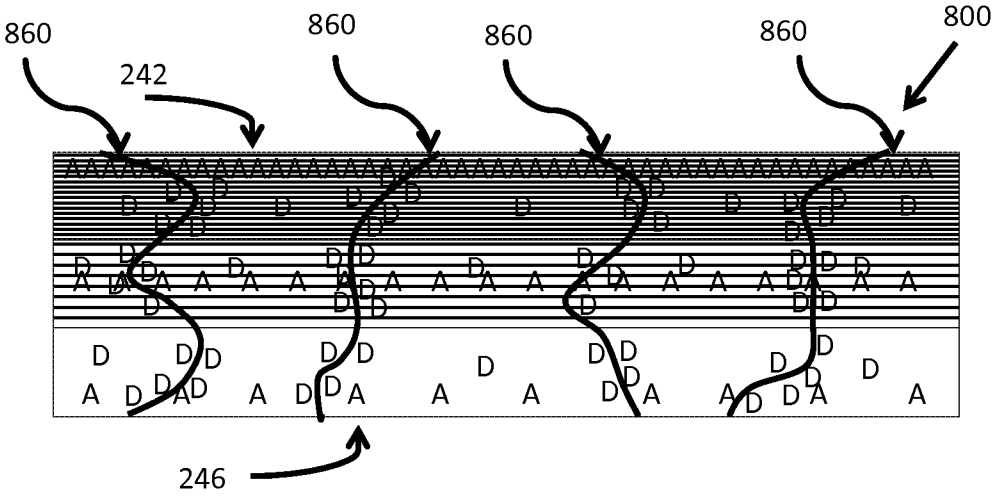

Fig. 8A

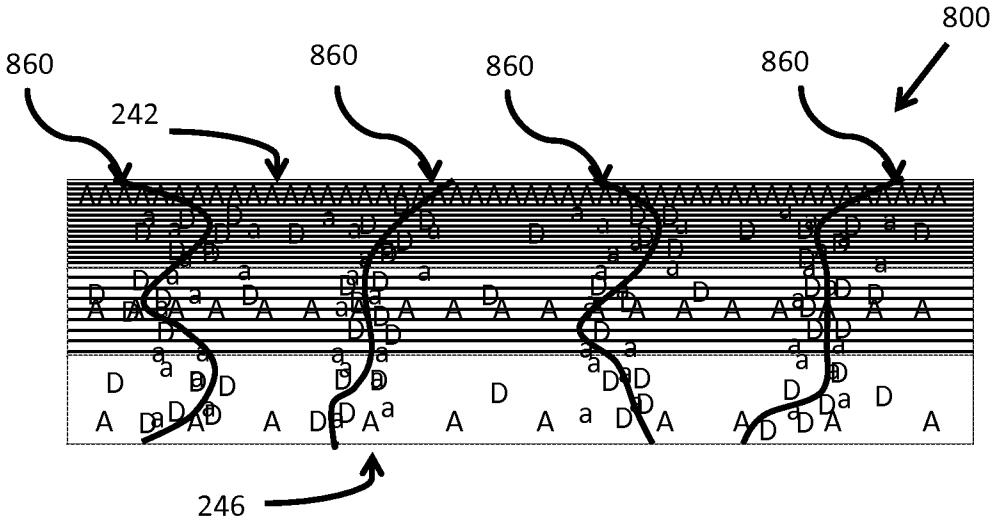

Fig. 8B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/055460

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/00 (2015.01)
CPC - H01L 31/068 (2015.12)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 21/00, 21/66, 31/00 (2015.01)
CPC - H01L 27/14689, 31/068, 31/075 (2015.12)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC- 136/252, 255, 258, 261; 438/57, 61, 72 (Keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Orbit, Google Patents, ProQuest
Search terms used: solar collector, dopant, molten, concentration profile, melt, segregation coefficient, wafer, doped

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013/0157401 A1 (JAGER et al) 20 June 2013 (20.06.2013) entire document	1-3, 5, 6, 12-15, 17, 23, 24
---		---
Y		4, 7-11, 16, 18-22, 25-27
Y	US 2012/0125424 A1 (WENHAM et al) 24 May 2012 (24.05.2012) entire document	4, 22
Y	WO 2013/142892 A1 (NEWSOUTH INNOVATIONS PTY LIMITED et al) 03 October 2013 (03.10.2013) entire document	7
Y	US 2008/0220544 A1 (BUCHER et al) 11 September 2008 (11.09.2008) entire document	8-11, 16, 18-21
Y	US 2014/0065764 A1 (SCARDERA et al) 06 March 2014 (06.03.2014) entire document	22
Y	US 2010/0275995 A1 (KAES et al) 04 November 2010 (04.11.2010) entire document	25
Y	US 2010/0006138 A1 (RAO) 14 January 2010 (14.01.2010) entire document	26, 27
A	US 2009/0050204 A1 (HABIB) 26 February 2009 (26.02.2009) entire document	1-27
A	US 2008/0138456 A1 (FORK et al) 12 June 2008 (12.06.2008) entire document	1-27

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 January 2016	02 MAR 2016
Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	Authorized officer Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/055460

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See supplemental page

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-27

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/055460

Continued from Box No. III Observations where unity of invention is lacking

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claims 1-27, drawn to a method for fabricating a semiconductor wafer for use as a solar collector.
Group II, claims 28-53, drawn to a solar collector.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the special technical feature of the Group I invention: the mold also comprising a primary dopant relative to the semiconductor material; c. contacting the forming surface to the molten material such that dopant migrates from the mold into the molten semiconductor material; and d. maintaining conditions such that a body of semiconductor material in the form of a wafer solidifies upon the forming surface, with a first surface contacting the forming surface as claimed therein is not present in the invention of Group II. The special technical feature of the Group II invention: where any metallic impurities that are present in the body are present at the first surface to a degree less than ten times the degree of metallic impurities that are present at the second surface as claimed therein is not present in the invention of Group I.

Groups I and II lack unity of invention because even though the inventions of these groups require the technical feature of a semiconductor wafer for use as a solar collector; the wafer having a profile of dopant concentration, there being a larger concentration of dopant at the first surface of the wafer, and a lesser concentration of dopant at a second surface of the wafer; the wafer having a profile of resistivity, there being a relatively lesser resistivity at a first surface of the wafer, and a relatively larger resistivity at a second surface of the wafer, this technical feature is not a special technical feature as it does not make a contribution over the prior art.

Specifically, US 2009/0050204 A1 (HABIB) 26 February 2009 (26.02.2009) teaches a semiconductor wafer for use as a solar collector (Paras. 68-69); the wafer having a profile of dopant concentration, there being a larger concentration of dopant at the first surface of the wafer, and a lesser concentration of dopant at a second surface of the wafer (By properly engineering size and dopant concentration of the nanorod devices, calculations show that gains in efficiency of 1.5-13% can be attained compared to planar silicon solar cells, Para. 30); the wafer having a profile of resistivity, there being a relatively lesser resistivity at a first surface of the wafer, and a relatively larger resistivity at a second surface of the wafer (Previous work has shown that nanowire resistivity decreases with the addition of both boron and phosphorus dopants (FIG. 14 (a)), however, it is possible to obtain significantly lower resistivities in the n-type silicon nanowires compared to the p-type, Para. 58).

Since none of the special technical features of the Group I or II inventions are found in more than one of the inventions, unity of invention is lacking.

(19)中华人民共和国国家知识产权局

(12)发明专利申请

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2017.09.26

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PCT/US2015/055460 2015.10.14

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WO2016/122731 EN 2016.08.04

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(51)Int.Cl.
H01L 21/00(2006.01)

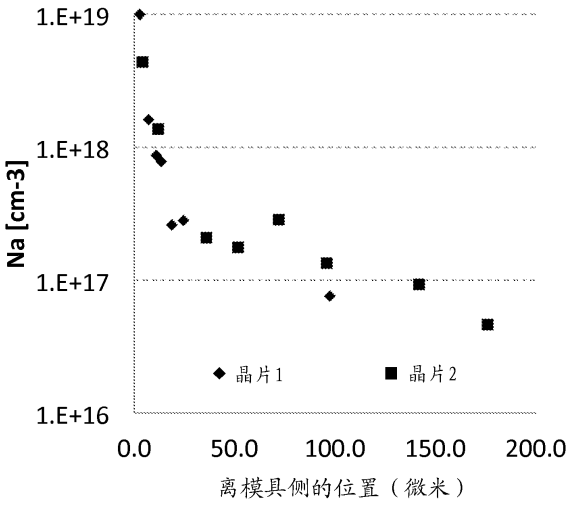
权利要求书5页 说明书21页 附图6页

(54)发明名称

用于创建具有分布掺杂的半导体晶片的方法以及具有分布场诸如漂移场和背表面场的晶片和太阳能电池组件

(57)摘要

半导体晶片在包含掺杂剂的模具上形成。掺杂剂对邻近模具的熔体区域进行掺杂。在那里，掺杂剂浓度高于熔体块体中的掺杂剂浓度。晶片开始凝固。掺杂剂在固体半导体中不良地扩散。在晶片开始凝固之后，掺杂剂不能进入熔体。之后，邻近晶片表面的熔体中的掺杂剂的浓度小于晶片开始形成的地方存在的掺杂剂的浓度。新的晶片区域从其掺杂剂浓度随时间的推移减少的熔体区域生长。这在晶片中建立了掺杂剂梯度，邻近模具具有较高浓度。能够修整梯度。梯度产生能够起漂移场或背表面场的作用的场。太阳能收集器能够在背表面上具有开放栅格导体和更好的光学反射器，固有的背表面场使所述更好的光学反射器变得可能。



CN 107408490 A

1.一种用于制作供用作太阳能收集器的半导体晶片的方法,所述方法包括以下步骤:

a. 提供具有表面的熔融半导体材料;

b. 提供包括成形表面的模具,所述模具还包括与所述半导体材料有关的主要掺杂剂;

c. 使所述成形表面与所述熔融材料接触,使得掺杂剂从所述模具迁移到所述熔融半导体材料中;以及

d. 维持条件,使得以晶片形式的半导体材料的本体在所述成形表面上凝固,其中第一表面接触所述成形表面,所述晶片具有掺杂剂浓度的分布图,在所述晶片的第一表面处存在较大的掺杂剂浓度,并且在所述晶片的第二表面处存在较小的掺杂剂浓度。

2.一种用于制作供用作太阳能收集器的半导体晶片的方法,所述方法包括以下步骤:

a. 提供具有表面的熔融半导体材料;

b. 提供包括成形表面的模具,所述模具还包括与所述半导体材料有关的掺杂剂;

c. 使所述成形表面与所述熔融材料接触达接触持续时间,使得对于所述接触持续时间的至少一部分,掺杂剂从所述模具迁移到所述熔融半导体材料中;以及

d. 维持条件,使得以晶片形式的半导体材料的本体在所述成形表面上凝固,所述晶片具有电阻率的分布图,在所述晶片的第一表面处存在相对较小的电阻率,并且在所述晶片的第二表面处存在相对较大的电阻率。

3.根据权利要求1和2中任一项所述的方法,还包括把凝固的晶片从所述成形表面卸下的步骤。

4.根据权利要求1和2中任一项所述的方法,所述模具包括在一个表面上的涂层,所述涂层包含所述主要掺杂剂。

5.根据权利要求1和2中任一项所述的方法,所述模具还包括本体,其中,所述主要掺杂剂分布在所述模具本体内。

6.根据权利要求1和2中任一项所述的方法,所述模具还包括本体,其中,所述主要掺杂剂以靠近一个表面的较高浓度处于所述模具本体内。

7.根据权利要求1和2中任一项所述的方法,所述维持条件的步骤包括:以半导体的凝固本体充当扩散阻挡物的形式在所述模具处提供所述主要掺杂剂,使得随着所述凝固本体生长,初始主要掺杂剂以第一速率迁移到所述熔融材料和所述凝固本体中,并且随后,主要掺杂剂以越来越小的速率迁移到所述熔融材料和所述凝固本体中,使得与稍后凝固的本体部分相比,较早凝固的本体部分每单位体积具有相对较多的主要掺杂剂。

8.根据权利要求3所述的方法,所述主要掺杂剂包括施主和受主类型中仅一种类型的电荷载流子,所述方法还包括:

进行(视情况而定,权利要求1或2的)步骤a,b,c和d至少两次;

在所述熔融材料中提供一些与所述主要掺杂剂相反的电荷载流子施主/受主类型的补偿掺杂剂。

9.根据权利要求8所述的方法,还包括:在所述熔融材料中提供一些与所述补偿掺杂剂相反的电荷载流子施主/受主类型的反补偿掺杂剂的步骤。

10.根据权利要求9所述的方法,所述补偿掺杂剂和所述反补偿掺杂剂均具有平衡偏析系数,所述反补偿掺杂剂的平衡偏析系数等于或小于所述补偿掺杂剂的平衡偏析系数。

11.根据权利要求8所述的方法,其中,提供一些补偿掺杂剂的步骤通过以根据以下关

系的浓度C_{cd}在所述熔体中提供所述补偿掺杂剂来实现：

C_{cd}近似等于$C_{md}*(k_{md}/k_{cd})$，其中：

C_{md}是所述主要掺杂剂的熔体浓度；

C_{cd}是所述补偿掺杂剂的熔体浓度；

k_{md}是所述主要掺杂剂的有效偏析系数；以及

k_{cd}是所述补偿掺杂剂的有效偏析系数。

12.根据权利要求1所述的方法，主要掺杂剂浓度在所述晶片的第一表面处小于或等于1×10^{20} N_x/cm^3，并且在所述晶片的第二表面处大于或等于约1×10^{15} N_x/cm^3，其中，对于电荷载流子受主掺杂剂，N_x意指电荷载流子受主的数量N_a，并且对于电荷载流子施主掺杂剂，N_x意指电荷载流子施主的数量N_d。

13.根据权利要求2所述的方法，所述主要掺杂剂是电荷载流子受主，所述电阻率在所述晶片的第一表面处大于或等于0.001欧姆-厘米，并且在所述晶片的第二表面处小于或等于约10欧姆-厘米。

14.根据权利要求1所述的方法，主要掺杂剂浓度在所述晶片的第一表面处小于或等于1×10^{19} N_x/cm^3，并且在所述晶片的第二表面处大于或等于约1×10^{17} N_x/cm^3，其中，对于电荷载流子受主掺杂剂，N_x意指电荷载流子受主的数量N_a，并且对于电荷载流子施主掺杂剂，N_x意指电荷载流子施主的数量N_d。

15.根据权利要求1所述的方法，所述主要掺杂剂是电荷载流子施主，所述电阻率在所述晶片的第一表面处大于或等于0.001欧姆-厘米，并且在所述晶片的第二表面处小于或等于约0.1欧姆-厘米。

16.根据权利要求1和2中任一项所述的方法，所述半导体包括p型半导体，所述主要掺杂剂选自由硼、铝、镓和铟组成的组。

17.根据权利要求1和2中任一项所述的方法，所述半导体包括n型半导体，所述主要掺杂剂选自由磷、砷、锑(Sb)和铋组成的组。

18.根据权利要求8所述的方法，所述半导体包括p型半导体，所述补偿掺杂剂选自由磷、砷、锑(Sb)和铋组成的组。

19.根据权利要求8所述的方法，所述半导体包括n型半导体，所述补偿掺杂剂选自由硼、铝、镓和铟组成的组。

20.根据权利要求18所述的方法，还包括在所述熔融材料中提供如下反补偿掺杂剂的步骤：该反补偿掺杂剂选自由铝、镓和铟组成的组。

21.根据权利要求19所述的方法，还包括在所述熔融材料中提供如下反补偿掺杂剂的步骤：该反补偿掺杂剂选自由砷、锑和铋组成的组。

22.根据权利要求4所述的方法，所述熔融材料包括硅，所述涂层包括选自由B_4C(碳化硼)和B_4Si(硼化硅)组成的组的掺杂剂。

23.根据权利要求1和2中任一项所述的方法，所述主要掺杂剂包括选自由碳化物、氧化物、氮化物和硅化物组成的组的化合物，或者选自由硼、铝、镓、铟、磷、砷、锑和铋组成的组的元素。

24.根据权利要求1和2中任一项所述的方法，进行维持步骤，以便在所述晶片的第一表面处提供足够高以便在用作太阳能收集器的晶片中建立背表面场的主要掺杂剂浓度。

25.根据权利要求24所述的方法，还包括提供如下部件的步骤：

a．以开放栅格形式的金属导体，所述金属导体耦合到所述晶片，接触所述晶片的所述第一表面；以及

b．光学反射器，所述光学反射器与所述第一表面隔开布置使得所述金属导体位于所述第一表面和所述光学反射器之间。

26.根据权利要求1所述的方法，所述掺杂剂浓度的分布图具有如下形状：该形状将在所述晶片本体内产生漂移电场，所述漂移电场目的在于在优选方向上驱策电荷载流子。

27.根据权利要求2所述的方法，所述电阻率的分布图具有如下形状：该形状将在所述晶片本体内产生漂移电场，所述漂移电场目的在于在优选方向上驱策电荷载流子。

28.一种供用作太阳能收集器的半导体晶片，所述晶片包括具有第一表面和第二表面的本体，所述本体具有掺杂剂浓度分布图，存在位于所述晶片的第一表面处的较大的掺杂剂浓度，以及到所述晶片的第二表面处的较小的掺杂剂浓度的连续过渡，较大浓度是较小浓度的至少三倍，进一步地，其中，存在于所述本体中的任何金属杂质以小于存在于所述第二表面的金属杂质的程度的十倍的程度存在于所述第一表面。

29.一种供用作太阳能收集器的半导体晶片，所述晶片包括具有第一表面和第二表面的本体，所述本体具有电阻率分布图，存在位于所述晶片的第一表面处的较小电阻率，以及到所述晶片的第二表面处的较大电阻率的连续过渡，较大电阻率是较小电阻率的至少三倍，进一步地，其中，存在于所述本体中的任何金属杂质以小于存在于所述第二表面的金属杂质的程度的十倍的程度存在于所述第一表面。

30.根据权利要求28和29中任一项所述的半导体晶片，所述半导体包括硅，并且所述掺杂剂包括硼。

31.根据权利要求28和29中任一项所述的半导体晶片，所述半导体包括硅，并且所述掺杂剂选自由硼、铝、镓和铟组成的组。

32.根据权利要求28和29中任一项所述的半导体晶片，所述半导体包括p型半导体，并且所述掺杂剂选自由硼、铝、镓和铟组成的组。

33.根据权利要求28和29中任一项所述的半导体晶片，所述半导体包括n型半导体，并且所述掺杂剂选自由磷、砷、锑(Sb)和铋组成的组。

34.根据权利要求28所述的半导体晶片，掺杂剂浓度在所述晶片的第一表面处小于或等于1×10^{20} N_x/cm^3，并且在所述晶片的第二表面处大于或等于约1×10^{15} N_x/cm^3，其中，对于电荷载流子受主掺杂剂，N_x意指电荷载流子受主的数量N_a，并且对于电荷载流子施主掺杂剂，N_x意指电荷载流子施主的数量N_d。

35.根据权利要求29所述的半导体晶片，所述电阻率在所述晶片的第一表面处大于或等于0.001欧姆-厘米，并且在所述晶片的第二表面处小于或等于约10欧姆-厘米。

36.根据权利要求28所述的半导体晶片，所述晶片的第一表面处的主要掺杂剂的浓度足够高，以便在用作太阳能收集器的晶片中建立背表面场。

37.根据权利要求29所述的半导体晶片，所述晶片的第一表面处的电阻率足够低，以便在用作太阳能收集器的晶片中建立背表面场。

38.根据权利要求36和37中任一项所述的半导体晶片，还包括：

a．以开放栅格形式的金属导体，所述金属导体耦合到所述晶片，接触所述晶片的所述

第一表面;以及

b. 光学反射器,所述光学反射器与所述第一表面隔开布置使得所述金属导体位于所述第一表面和所述光学反射器之间。

39.根据权利要求28所述的半导体晶片,掺杂剂浓度的分布图具有如下形状:该形状将在所述晶片本体内产生漂移电场,所述漂移电场目的在于在优选方向上驱策电荷载流子。

40.根据权利要求29所述的半导体晶片,所述电阻率的分布图具有如下形状:该形状将在所述晶片本体内产生漂移电场,所述漂移电场目的在于在优选方向上驱策电荷载流子。

41.一种太阳能收集器,包括多个半导体晶片,每个晶片包括具有第一表面和第二表面的本体,所述本体具有掺杂剂浓度分布图,存在位于所述晶片的第一表面处的较大的掺杂剂浓度,以及到所述晶片的第二表面处的较小的掺杂剂浓度的连续过渡,较大浓度是较小浓度的至少三倍,进一步地,其中,存在于所述本体中的任何金属杂质以小于存在于所述第二表面的金属杂质的程度的十倍的程度存在于所述第一表面。

42.一种太阳能收集器,包括多个半导体晶片,每个晶片包括具有第一表面和第二表面的本体,所述本体具有电阻率分布图,存在位于所述晶片的第一表面处的相对较小的电阻率,以及到所述晶片的第二表面处的相对较大的电阻率的连续过渡,进一步地,其中,存在于所述本体中的任何金属杂质以小于存在于所述第二表面的金属杂质的程度的十倍的程度存在于所述第一表面。

43.根据权利要求41和42中任一项所述的太阳能收集器,所述半导体包括硅,并且所述掺杂剂包括硼。

44.根据权利要求41和42中任一项所述的太阳能收集器,所述半导体包括硅,并且所述掺杂剂选自由硼、铝、镓和铟组成的组。

45.根据权利要求41和42中任一项所述的太阳能收集器,所述半导体包括p型半导体,并且所述掺杂剂选自由硼、铝、镓和铟组成的组。

46.根据权利要求41和42中任一项所述的太阳能收集器,所述半导体包括n型半导体,并且所述掺杂剂选自由磷、砷、锑(Sb)和铋组成的组。

47.根据权利要求41所述的太阳能收集器,掺杂剂浓度在所述晶片的第一表面处小于或等于1×10^{20} N_x/cm^3,并且在所述晶片的第二表面处大于或等于约1×10^{15} N_x/cm^3,其中,对于电荷载流子受主掺杂剂,N_x意指电荷载流子受主的数量N_a,并且对于电荷载流子施主掺杂剂,N_x意指电荷载流子施主的数量N_d。

48.根据权利要求42所述的太阳能收集器,所述电阻率在所述晶片的第一表面处大于或等于0.001欧姆-厘米,并且在所述晶片的第二表面处小于或等于约10欧姆-厘米。

49.根据权利要求41所述的太阳能收集器,所述晶片的第一表面处的主要掺杂剂的浓度足够高,以便在用作太阳能收集器的晶片中建立背表面场。

50.根据权利要求42所述的太阳能收集器,所述晶片的第一表面处的电阻率足够低,以便在用作太阳能收集器的晶片中建立背表面场。

51.根据权利要求49和50中任一项所述的太阳能收集器,还包括:

a. 以开放栅格形式的金属导体,所述金属导体耦合到所述晶片,接触所述晶片的所述第一表面;以及

b. 光学反射器,所述光学反射器与所述第一表面隔开布置使得所述金属导体位于所

述第一表面和所述光学反射器之间。

52.根据权利要求41所述的太阳能收集器，掺杂剂浓度的分布图具有如下形状：该形状将在所述晶片本体内产生漂移电场，所述漂移电场目的在于在优选方向上驱策电荷载流子。

53.根据权利要求42所述的太阳能收集器，所述电阻率的分布图具有如下形状：该形状将在所述晶片本体内产生漂移电场，所述漂移电场目的在于在优选方向上驱策电荷载流子。

用于创建具有分布掺杂的半导体晶片的方法以及具有分布场诸如漂移场和背表面场的晶片和太阳能电池组件

[0001] 相关文献

据此要求保护于2015年1月26日提交的、题为“METHODS OF CREATING A SEMICONDUCTOR WAFER HAVING A DRIFT FIELD WITH PROFILED DOPING AND WAFERS HAVING A PROFILED DRIFT FIELD”、发明人为Ralf Jonczyk等、申请人为马萨诸塞州贝德福德的1366 Technologies有限公司的美国临时申请号62/107,711的优先权，据此通过引用并入其完整的公开。据此还要求保护于2015年10月8日提交的、题为“METHODS FOR CREATING A SEMICONDUCTOR WAFER HAVING PROFILED DOPING AND WAFERS AND SOLAR CELL COMPONENTS HAVING A PROFILED FIELD, SUCH AS DRIFT AND BACK SURFACE”、发明人为Ralf Jonczyk等、申请人为马萨诸塞州贝德福德的1366 Technologies有限公司的美国临时申请号62/239,115的优先权，据此也通过引用并入其完整的公开。

背景技术

[0002] 通常能够使用Sachs等人的、题为“METHODS FOR EFFICIENTLY MAKING THIN SEMICONDUCTOR BODIES FROM MOLTEN MATERIAL FOR SOLAR CELLS AND THE LIKE”的于2012年10月23日授权的美国专利号8,293,009中公开的技术，从半导体熔体直接形成半导体晶片，该美国专利号8,293,009通过引用全部并入本文中)。

[0003] 常规的太阳能收集器由如下半导体晶片组成:该半导体晶片具有其中存在例如晶格空穴的多数载流子的相对较厚的部分和其中相反类型的载流子(在该情况下，为电子)为多数载流子的薄得多的部分。这两部分在称为p/n结的地方相接。在180微米厚的工业标准晶片中，p型部分将是180微米厚，并且n型部分将是约0.5微米厚。在这样的常规晶片中，遍及晶片的较厚部分，诸如p型晶片(诸如掺杂有硼的硅晶片)中的掺杂有受主(空穴)的p型部分，掺杂是均匀的。在这样的收集器中，少数电荷载流子以基本上随机的形式自由移动，(在每个部分中，但是这里主要关注的是较厚的部分)从其生成点随机扩散。一些少数载流子可能去向p/n结收集区域，一些可能去其他方向。这样的情形缺乏效率。已知的是，建立将朝向p/n结收集区域驱策少数电荷载流子的电场能够在其他事物相同的情况下提高效率。这样的电场被说成指向p/n结，并且将使生成的少数电荷载流子优先朝向收集p/n结移动。这样的方向偏好将增加太阳能电池的收集效率。据信这种效果不能通过用于从厚的铸块或砖块(brick)切下晶片的任何常规熔体凝固方法来实现。这样的场有时被称为漂移场。

[0004] 用以在晶片中创建这样的电漂移场的已知尝试建立了掺杂梯度，其建立了指向收集p/n结的电场。在公开为“WO2005122287A1”、题为“Method for the production of crystalline silicon foils”的PCT专利申请号PCT/NL2005/000422中描述了该已知工作。该专利申请被转让给Stichting Energie，并且下面该工作称为Stichting工作。Stichting工作具有显著的负面影响。主要的半导体材料是硅，并且掺杂剂是镓。通过对熔融本体进行快速冷却来创建掺杂水平的分布图，其中初始的快速冷却导致在初始凝固的表面处的受损偏析，并且随着冷却减缓，镓将优先偏析离开随后稍晚凝固的表面，这归因于镓的显著的平

衡偏析系数(约0.008)。受损的偏析暗示冷却足够快地发生,使得镓杂质的实际偏析系数是平衡偏析系数的10倍以上。偏析系数1表示液相和固相之间不存在偏析偏好,代表偏析系数的最大值。对于弱偏析掺杂剂,诸如平衡系数为0.8的硼,根据该损伤机制,最大增加将仅为1.25倍。

[0005] Stichting专利申请中没有提及这种快速冷却的必然结果,但是对于技术从业人员来说其是显然的。熔融材料内的金属杂质将也必然在大的且不可接受的程度上并入到初始快速冷却和凝固的半导体晶体的固体中。Stichting工作方法利用镓的相对显著的(数值上非常小的)偏析系数来实现浓度中的梯度。但是金属杂质也具有相对显著的(数值上非常小的)偏析系数,并且对于稼要在足以提供可用的掺杂分布图的程度上存在,还将必然的是,任何金属杂质也将在高的且因此不可接受的程度上存在于凝固晶体中。因此,尽管通过Stichting方法会创建掺杂分布图,但是具有在如下程度上的杂质的任何形成本体对于太阳能收集将不是实际有用的:相对于平衡偏析的至少一个数量级那么高的金属含量。

[0006] 稍微不同地说,为了从晶片的一部分到另一部分实现10倍的掺杂差异(一个数量级),Stichting方法将固有地具有该相同因子,即,在较高掺杂的区域中的金属是将存在于较低掺杂的区域中的金属的10倍。本领域的从业者理解,这样高的金属含量(以及还有这样的变化的金属含量(或其他杂质))具有严重的有害影响。例如,少数载流子寿命将低于另外没有这些杂质的情况下的少数载流子寿命。这样的较低的寿命导致运行不如具有较高寿命的电池的电池。

[0007] 一个假设但合理的情况说明了这些问题。考虑熔体中存在1ppm的金属的情况,其中,平衡偏析系数$k = 10^{-6}$,例如铁(Fe)。利用Stichting方法,这将导致晶片中的5×10^{11}原子/cm^3的金属。这将导致约7微秒的少数载流子寿命,这引起16.4%的效率。

[0008] 在已知的太阳能收集器中使用的、施加在晶片上的另一种场被称为背表面场(BSF)。常规电池通常具有背表面场。该场降低有效的背表面复合速率,并且提高了少数载流子的收集概率。实现这一点的典型方式是在处理期间,在背表面上提供铝或铝合金的薄层。铝的施加具有缺点。首先,其是处理中的单独步骤,由此添加复杂化,其在不要求这样的铝层的情况下将是不存在的。其次,铝是长波长光的相当差的反射器。因此,当存在铝背表面层时,相对高的量的这样的长波长的光不被反射并且被损失。能够反射并因此捕获这样的长波长的光中的一些或全部将是有益的。(作为澄清的一点,应该注意,BSF讨论需要两个完全不同的实体的排斥或反射—BSF驱策少数载流子离开背表面。某些光子不被充分地从背表面反射,因为它们被产生BSF的铝层吸收或至少没有被其反射)。

[0009] 因此,存在对如下半导体晶片的需要:该半导体晶片具有机构,其用于在某一方向上建立电场以将(主要是晶片的较厚部分中的)少数电荷载流子驱策到收集p/n结。还存在对具有优异电气性质和可接受的低杂质水平的这样的晶片的需要。还存在对由不具有显著偏析系数的掺杂剂掺杂的这样的晶片的需要。还存在对p型半导体的以及还有n型半导体的这样的掺杂剂分布的晶片的需要。还存在对制作这样的晶片的方法的需要。还存在对并入这样的晶片的太阳能收集器和太阳能板的需要。

[0010] 还存在对用于太阳能电池中的晶片的需要,其中能够建立BSF,而不需要专门用于该目的的处理步骤,并且在背表面处还不需要在光学上弱反射的铝层。还存在对如下晶片的需要:这样的晶片能够被构造成使得能够实现相对高的量的长波长光的反射,以及因此

其在晶片和电池内的捕获。

[0011] 因此，本发明的目的包括半导体晶片，其具有机构，所述机构用于在某一方向上建立电场以将少数电荷载流子驱策到收集p/n结。另外的目的包括具有优异的电气性质和相对低的杂质水平的这样的晶片。另外的目的是由不具有显著偏析系数的掺杂剂掺杂的这样的晶片。又另一目的包括p型半导体的以及还有n型半导体的这样的掺杂剂分布的晶片。还有另一目的是具有BSF的晶片，其不具有铝背表面。还有其他的目的是制备任何和所有这样的晶片的方法。还有另一目的是并入具有这样的漂移场或BSF或者两者的晶片的太阳能电池。又另一目的是比具有铝BSF平面的电池具有更高的用于收集长波长光的效率的太阳能电池。

附图说明

[0012] 这些目的和其他目的通过本发明来实现，其更全面地示出在附图的若干图中，若干图是：

图1A，其在横截面中示意性地示出用接近半导体材料的熔体的掺杂剂处理的模具；

图1B，其在横截面中示意性地示出与熔体接触的、经处理的图1A的模具，其中，熔体的上部分具有一些进入熔体的处理材料；

图1C，其在横截面中示意性地示出仍与熔体接触的、经处理的图1B的模具，其中，晶片在模具上凝固，并且其中，熔体的比图1B所示出的部分更大的部分具有一些进入熔体的更大部分的处理材料；

图1D，其在横截面中示意性地示出仍与熔体接触的、经处理的图1C的模具，其中较厚的量的晶片在模具上凝固，并且其中，熔体的甚至比图1C所示出的部分更大的部分具有一些进入熔体的更大部分的处理材料；

图2A，其在横截面中示意性地示出形成在如图1D所示出的模具上的晶片，其具有掺杂的梯度分布图；

图2B，其在横截面中示意性地示出在如下处理之后的图2A的晶片：已经向一侧添加n型材料的掺杂，由此形成p/n结，并且已经在与n型材料相反侧上形成更高掺杂的区域，其将使得产生BSF；

图3，其在横截面中示意性地示出本发明的模具，遍及其体积，所述模具被用掺杂材料处理；

图4，其在横截面中示意性地示出本发明的模具，其在一个表面上和附近的一对层或涂层中被用掺杂材料处理；

图5，其以图形形式示出根据本发明制备的代表性晶片的受主数量(Na / cm ^{3})和离模具侧的位置之间的关系；

图6A，其在横截面中示意性地示出用于具有铝合金背表面电极的太阳能收集器中的现有技术的晶片；

图6B，其在横截面中示意性地示出本发明的晶片，其用于太阳能收集器中，具有由于掺杂分布图的高掺杂的后表面，其没有铝合金背表面电极，而是具有开放栅格电极和高效率光学反射器；

图7，其以图形形式示出对于包括图6A和图6B中示出的那些的两个不同配置的、量子效

率相比于入射光波长之间的关系；

图8A是本发明的晶片的示意性表示，示出在晶粒边界处的施主补偿掺杂剂原子的偏析；以及

图8B是图8A所示出的本发明的晶片的示意性表示，还示出在晶粒边界处的受主反补偿掺杂剂原子的偏析。

[0013] 发明内容

在模具上形成晶片，该模具以某种方式设有掺杂剂。例如，模具能够具有包含掺杂剂的涂层。为了使用硅创建p型晶片，掺杂剂能够是硼，其提供额外的电子受主。当模具加热时，掺杂剂进入熔体(通过若干可能的方式)，由此对直接邻近模具的熔体区域进行掺杂，使得在该邻近区域中，掺杂剂(例如硼)的浓度与熔体块体中的掺杂剂的浓度相比相对较高。在非常短的时间内，半导体晶片开始在模具的表面上凝固。诸如硼的掺杂剂在固体硅中不显著扩散。因此，在形成固体晶片之后，掺杂剂不再能够从模具进入熔体，因为模具表面上的固体硅充当硼掺杂剂扩散阻挡物。此时和此后，邻近晶片的生长表面的熔体区域中的硼掺杂剂的浓度将小于存在于其中晶片首先开始形成的熔体区域中的浓度。随着晶片继续生长，晶片的新的附加区域从熔体的新的生长区域形成，其具有随着时间的推移连续变得越来越少的硼掺杂剂浓度。在每个相继的新生长区域中的这种持续的掺杂剂减少建立硼掺杂剂的浓度梯度或分布图，其中，在首先已凝固的、邻近模具的晶片处存在较高浓度，并且在最后凝固的、凝固的晶片的熔体侧处存在较低浓度的硼。梯度能够通过各种手段来修整。掺杂的梯度将产生指向特定方向的电场，并且该电场在任何位置的强度与该位置和邻近位置处的梯度的程度有关。这样的电场能够对用于太阳能收集器的晶片中的少数电荷载流子具有影响。

[0014] 一个梯度浓度分布图能够对于在晶片内创建漂移场有用。另一个分布图能够对于在晶片内创建背表面场有用。本发明的晶片能够用于太阳能电池中。由于漂移场，促进了更高的效率，这促进了电池内的载流子收集。由于在背表面上提供更好的反射器，也出现更高效率，由于掺杂分布图引起的固有的背表面场使所述更好的反射器变得可能，其能够消除铝合金背表面元件的行业标准的差反射器。

[0015] 以确定性方式与局部掺杂浓度有关的特性是局部电阻率。还存在电阻率的梯度，并且通过测量不同位置处的电阻率，能够确定浓度。因此，思考并分析掺杂剂浓度的梯度以及因此生成的电场梯度的等同方式是考虑从晶片的一个表面到另一个表面的电阻率分布图。

[0016] 方法发明包括从熔体制备一个这样的晶片的方法。方法发明还包括从同一熔体制备多个这样的晶片，包括用以在熔体内补偿熔体内的主要掺杂剂的积聚的步骤，否则其将太高以致不能用于如下晶片：该晶片要在目标净掺杂剂浓度下制造以实现用于太阳能电池中的目标体电阻率。通过随着形成越来越多的晶片周期性地向熔体提供相反的受主/施主类型的补偿掺杂剂(例如，为了补偿受主掺杂剂硼，能够使用施主掺杂剂磷)来实现补偿。在一些情况下，补偿掺杂剂可能不成比例地偏析到晶粒边界，这可能是不利的。在这样的情况下，本方法发明是添加反补偿掺杂剂(在硼(受主)和磷(施主)系统的情况下，反补偿掺杂剂将是具有适当大的偏析常数的受主诸如镓，以使在晶粒边界处的补偿掺杂剂的浓度的电气效应最小化。

具体实施方式

[0017] 如上面讨论的，供太阳能收集器使用的典型半导体晶片具有相对较厚的部分，其中多数载流子具有一种施主/受主类型，例如通常为p型。这样的晶片被形成，并且随后被处理，使得在主要为p型晶片的情况下，一面被掺杂以具有相反的施主/受主类型，因此n型的多数载流子。对于典型的晶片，第一部分将基本上是180微米的全部厚度，而另一类型部分将仅为约0.5微米厚。两部分之间的结称为p/n结。下面的讨论主要涉及一种用于制备通常为p型部分的相对较厚的部分的新方法。下面讨论的方法将典型地用于创建这样的晶片。在进行本文中所讨论的方法步骤之后，将在一个表面上创建p/n结和相反的载流子类型部分。这些方法也可用于创建厚的、主要为n型的晶片。在本发明的这样的晶片中，将存在从生长的晶片的一个面到另一个面的掺杂的梯度分布图。该掺杂梯度分布图将在成品生长晶片中产生电场，该场能够充当漂移场，并且还能够或者替代地充当背表面场(BSF)。

[0018] 图1A、1B、1C和1D示出以某种方式设有掺杂剂的模具110(有时也称为衬底)，将在其上形成晶片100(图2A)。例如，模具110能够具有包含掺杂剂114的涂层112。为了使用熔融硅创建p型晶片，掺杂剂能够是硼(其是电荷载流子受主)。图3中示意性地示出的替代实施例具有模具310，其具有遍及其本体均匀或者以某一其他模式分布的掺杂剂314。下面讨论模具掺杂剂处理的若干不同的实施例。针对本发明的主要典型使用将是与p型半导体晶片并且因此与受主掺杂剂一起。因此，讨论将主要集中在这样的组合。然而，本发明也可以与n型半导体和电荷载流子施主掺杂剂一起使用。(这样的系统的示例将是具有硼熔体补偿的磷掺杂的衬底。)又另一更相关的组合也是可能的，并且在下面被讨论。

[0019] 诸如硼的主要掺杂剂能够在这样的模具110的表面上的任何地方，或者在这样的模具310的本体内的任何地方。然而，据信如果其存在于最接近熔体的模具区域诸如涂层112或者本体310内的紧邻表面的区域中，则这提供了最大的优点，如下面讨论的那样。许多不同的半导体能够用作主要熔体成分。硅是非常常用的，并将在下面的讨论中用作代表性示例。同样，其他掺杂剂是可能的。在下面的讨论中，硼将被用作代表性的掺杂剂示例。然而，本公开的普遍性不意图被限于硅作为半导体或硼作为掺杂剂。所有合理的替代方案被认为是本发明的方面。例如，对于硅作为半导体，掺杂剂的示例包括但不限于：硼(B)、铝(Al)、镓(Ga)和铟(In)。对于n型晶片，掺杂剂包括但不限于：磷(P)、砷(As)、铅(Sb)和铋(Bi)。

[0020] 当模具110加热时，诸如当其与例如熔融硅的热半导体熔体116接触时，掺杂剂，诸如模具内的硼314(图3)或模具涂层112的硼114进入熔体116，由此对熔体116的直接邻近模具110的区域118b进行掺杂，使得与熔体116的体块(剩余区域)120中的硼的浓度相比，邻近模具的硼114b的浓度相对较高。将首先讨论如1A、1B、1C和1D所示出的使用涂层112的实施例。如图1C中示出的，在非常短的时间(例如，几毫秒到若干秒)内，半导体(例如硅)晶片100开始在模具110的表面122上凝固。

[0021] 可以用其他方式对模具加热(例如，能够在接触熔体之前对其预加热)。通常有利的是，当模具与液体硅接触时，其比熔体更冷，以使得最佳地允许热提取以及因此熔融硅的凝固。该凝固过程将使模具从其起始温度升温。

[0022] 硼在固体硅中不显著扩散。因此，如图1C中示出的，在形成固体晶片100之后，硼

114不能再从模具/衬底110进入熔体116，因为已经在模具表面122上形成固体硅100，并且固体硅充当硼扩散阻挡物。(关于本文讨论的其他掺杂剂和半导体晶片系统，情况通常也是这样)。通常几微米的固体材料的厚度足以防止进一步扩散。该厚度最初可以出现在模具表面上的间隔开的位置处，但是相对快地，模具上任何地方的凝固厚度足以防止进一步扩散。那时，熔体116的邻近晶片100的生长表面111的区域118c中的硼的浓度114c将小于紧随模具表面122与熔体116接触之后晶片100首先开始形成所在的区域118b中存在的浓度114b，如图1B示出的那样，因为硼114c原子通过对流扩散和移动远离模具110和生长晶片100并且远离邻近模具110和晶片100的生长表面100的区域118c到熔体116中。

[0023] 随着晶片100在接下来的几秒的时间尺度期间继续生长(即，变厚)，在表面111处，从熔体的邻近生长表面111的新生长区域118c、18d，形成晶片100的新的附加区域被形成，该新的生长区域118d具有随着时间的推移连续变得越来越少的硼浓度114d。对于生长晶片的每个相继量，新增长区域118总是这样轻微地逐渐进一步远离模具、掺杂剂的初始来源。掺杂剂已迅速扩散到熔体116的远离模具110的体块120中。

[0024] 图2A示出生长的硅晶片100。在每个相继的新生长区域118中的掺杂剂的持续减少在生长的晶片100中建立掺杂剂硼的梯度，如图2A中示出的那样，在晶片完成其形成时，其中晶片的邻近模具110及其表面122的部分132处存在较高浓度的硼，在熔体116的区域118具有相对较高浓度的硼时，所述表面132首先从熔体116的区域118凝固。在凝固晶片100的表面136处存在较低浓度的硼，在熔体具有相对较低浓度的硼的时间和位置处，所述表面136最后从熔体116的区域118(相对远离模具表面122，具有在那个位置处的硼含量)凝固。

[0025] 前述讨论是根据生长的晶片100的相继区域和熔体的相继的新生长区域118安排的，好像这些生长区域是分立的、逐层的诸如多片纸。实际上，晶片的生长是连续的、原子接原子的，并且掺杂剂到熔体中的扩散也是连续的、原子接原子的。并入到生长晶片中的掺杂剂的量取决于掺杂剂到熔体中、远离和离开熔体的连续相继的新生长区域的相对扩散速率，以及半导体晶片的生长速率。这两个速率受熔体中掺杂剂的扩散倾向、温度、晶体生长速度等的影响。因此，晶片中硼的浓度从最靠近模具形成的表面132到更远离模具、在熔体内的更深处形成的表面136平滑地变化。(图2A示出形成的晶片的三个不同区域，具有三个不同的离散的掺杂剂浓度，浓度由水平阴影线的紧密度指示，较紧密的影线指示较大的掺杂剂浓度。这不意味着实际地表示形成的晶片，而其仅仅是附图的限制，其必须以黑色和白色示出从邻近模具形成的表面132到更远离模具形成的表面136的物理情形，所述物理情形以灰度级的继续可能更好示出)。

[0026] 图5示出对于两个不同晶片(指定晶片1和晶片2)的p型掺杂浓度，每个示出：在紧邻模具的首先形成的晶片部分处约1×10^{19} N_a/cm^3的浓度以具有粗略指数衰减形状的平滑曲线下降，其中在距紧邻模具的首先形成的晶片部分约25到约150微米的位置范围中，N_a/cm^3浓度在约1×10^{17}和1.5×10^{17}之间。高达1×10^{20} N_a/cm^3的N_a被认为是可能的，并且还在距模具最远的最后形成的晶片的位置处，据信低至1×10^{15} N_a/cm^3的浓度是可能的。单位N_a代表受主的数量，如在电子受主中。对于n型掺杂剂，对应的单位将是N_d，其代表施主的数量，如在电子施主中。(在下面的一些情况下以及在权利要求中，视情况而定，取决于预期电子施主还是受主，表达N_x用于表示N_a或N_d)。如能够看到的，从相对较高浓度到相对较低浓度的过渡是平滑且连续的。

[0027] 不知道具有这样的掺杂梯度的半导体晶片之前已被制造,除了以在上面提及的使用Stichting方法的非常有限的类型之外。如上面所讨论的,该方法创建具有非常差的电气性质的半导体。

[0028] 回顾上面概述的关于杂质和Sticting方法的假设示例,在晶片中具有为10的掺杂差异因子,以及因此相同的杂质差异,以及5×10^{11}原子/cm^3的金属,导致约7微秒的少数载流子寿命,引起16.4%的效率,根据本发明制备的晶片将具有显著更好的性质。这样的晶片在该晶片中将具有5×10^{10} 原子/cm^3的金属,导致约70微秒的少数载流子寿命,引起18.4%的效率。这个示例是假设的,任何其他因素将进入任何实际物理情况中,但比较是恰当的。

[0029] 在本发明的掺杂剂分布晶片中,如果由掺杂有p型材料的熔体形成,则首先形成晶片,然后将在一个表面上创建相反类型(在该情况下,n型)的材料,由此创建p/n结。图2B示意性地示出本发明的p/n结与掺杂分布图之间的关系。对于如上面所讨论的那样具有掺杂分布图的由熔体形成的p型晶片,晶片100的p侧(更正性掺杂的侧)将是具有较高的p型掺杂剂硼浓度的侧242,其更靠近模具表面122形成。晶片的n侧(少正性掺杂的侧,或更负性的侧)将形成在具有初始较低的p型掺杂剂硼浓度的侧246上,其更远离模具表面122形成。形成n型(或相反掺杂的)部分250能够通过任何常规的或尚待开发的方法来完成。通常这样的部分的深度仅为约0.5微米厚。在典型应用中,硼p型掺杂提供约1×10^{16}/cm^3的N_a。n型掺杂提供约1×10^{19}/cm^3的N_d。因此,在侧246处,n型掺杂占优势。p/n结252位于n型部分250和具有初始较低的p型掺杂剂浓度的侧246之间。该晶片的面向太阳的侧将具有面向太阳的n型部分250。在与太阳将处于的地方相反的侧上还示出背表面场部分254(下面更详细地讨论),其邻近具有初始较高p型掺杂剂浓度的侧242。

[0030] 如上面所讨论的,这样的掺杂剂梯度是有益的,因为它建立了指向关于少数载流子的收集p/n结的电场。电场导致生成的少数电荷载流子优先朝向p/n结移动。这种方向偏好增加了太阳能电池的收集效率。据信这种效果不能通过任何常规的熔体掺杂方法来实现。(在p型半导体中,少数载流子是电子)。

[0031] 应当注意,考虑晶片本体内不同位置处的掺杂剂浓度仅是用以描述其结构和性质的一种方式。另一种方式是考虑遍及其本体的相同的不同位置处的材料电阻率。以下也是真的:由于不同的净掺杂浓度,在遍及本体的不同位置处的晶片的电阻率中将存在相应的和相关的差异。因此,还存在本体的电阻率中的梯度,该梯度通常与净掺杂梯度相反。由此,这意味着较低掺杂剂浓度的区域中的电阻率较高,而较高掺杂剂浓度的区域中的电阻率较低。还要注意的是,尽管这些浓度和电阻率的梯度是由上面描述的熔体凝固和偏析的现象生成的,但是相对难以测量在晶片内的不同位置处的材料浓度。然而,更容易测量在通过本体的这样的位置处的电阻率。(这能够通过以下来完成:测量本体的电阻率、去除材料的层,以及测量剩余本体的电阻率,由此可能根据差异确定已被去除的部分的电阻率)。根据该确定的电阻率,还可能确定已被去除的层的材料浓度,即掺杂浓度。一层接一层,能够测量并因此确定通过整个本体的电阻率分布图,以及因此还有掺杂浓度分布图。

[0032] 电阻率和掺杂剂或载流子浓度之间的关系是确定性的和非线性的。下面的表1示出使电阻率(欧姆-厘米)一方面与受主载流子浓度(原子/ c^3)相关并且还与施主载流子浓度相关的一组代表性的值:

电阻率（欧姆-厘米）	受主浓度（原子/cc^3）P 型掺杂剂	施主浓度（原子/cc^3）N 型掺杂剂
0.001	1.15×10^{20}	7.36×10^{19}
0.01	7.98×10^{18}	4.38×10^{18}
0.1	2.40×10^{17}	7.77×10^{16}
0.3	5.83×10^{16}	1.87×10^{16}
0.5	3.19×10^{16}	1.04×10^{16}
1	1.47×10^{16}	4.83×10^{15}
2	6.97×10^{15}	2.31×10^{15}
4	3.38×10^{15}	1.13×10^{15}
6	2.23×10^{15}	7.43×10^{14}
10	1.32×10^{15}	4.41×10^{14}

表1-电阻率与载流子浓度之间的关系。

[0033] 该关系也能够用图解法，诸如以双对数线图来表征。这样的曲线图在www.solecon.com/pdf/converting_resitivity_to_carrier_concentration_graph_sige.pdf上示出。这是Solecon Laboratories of Trademark Dr., Reno, NV的网站示出的工作。据此通过引用将那里示出的曲线图全部并入在本文中。垂直刻度表示载流子浓度/cm^3，其中水平刻度表示电阻率(欧姆-厘米)。载流子浓度和电阻率之间的关系通常示出较高的浓度与较低的电阻率相关，并且反之亦然。在双对数刻度上，斜率通常是负的。用于例如锗的同一半导体的n型和p型掺杂的曲线图通常是一致的并且间隔开，其中p型的曲线图朝右移置，通常使得对于n型半导体中的相同载流子浓度，在p型半导体中，将存在更高的电阻率。硅半导体的载流子浓度和电阻率之间的关系通常与针对锗半导体所描述的相同。使用扩展电阻分析(SRA)确定各值。作者解释，为了计算硅的载流子浓度值，他们使用从Thurber、Mattis、Liu和Filliben的National Bureau of Standards Special Publication 400-64、The Relationship Between Resistivity and Dopant Density for Phosphorus- and Boron-Doped Silicon(1981年5月)，表10、页码34和表14、页码40得到的迁移率值。为了计算锗载流子浓度值，他们使用从D.B Cuttriss的Bell System Technical Journal(1961年3月)，页码509得到的载流子迁移率值。

[0034] 对于在不调整熔体组分的情况下从单个熔体创建一个或小数量的晶片，上述过程在不修改的情况下工作得非常好。

[0035] 该过程呈现的一个挑战是，在不修改的情况下，随着制备越来越多的晶片，随着时间的推移，其将导致熔体中的掺杂剂(诸如硼)的浓度中的增加。那是因为，比在生产单个晶片的时间期间从模具移动的全部硼更少的硼将被并入到在该时间间隔期间正被形成的晶片中。在熔体变得对于基线掺杂水平而言过度富含掺杂剂(例如硼)之前，熔体中的这种浓度积累限制了能够生长的晶片的数量。准确而言，掺杂剂所提供的无论什么，电子施主或受主，熔体都已变得过度富含。最终，达到平衡，此时，在每个晶片的形成时从熔体中去除的硼的量等于在每个晶片生长周期时从模具添加到熔体的硼的量。达到该平衡时的硼浓度通常太高，以致不能从富含掺杂剂的熔体制备优质的常规太阳能电池晶片。

[0036] 为了补偿熔体中的硼的这种积累，一定量(下面规定)的不同材料(本文中称为补偿掺杂剂)，例如在硼主要掺杂剂的情况下补偿掺杂剂磷，能够被直接添加到熔体。(如下面所解释的，在一些情况下，存在需要又另一补偿掺杂剂的原因(出于不同原因)，并且因此在

一些情况下,可以将要描述的该补偿掺杂剂称为第一补偿掺杂剂)。

[0037] 硼是元素周期表的第III族的成员,并且具有接受或接收一个电子的倾向。因此,硼是电子受主。磷是元素周期表的第V族的成员,并且因此,其具有能够被捐赠给熔体的过量电子。因此,磷是电子施主。因此,磷补偿过量电子受主硼,因为磷提供过量的硼倾向于接受的电子,因此补偿过量的硼受主。单个磷原子捐赠单个电子,而单个硼原子接受单个电子。

[0038] 以适当量添加的磷将补偿过量的硼,并无限期地将晶片形成过程维持在期望的硼掺杂剂水平。要补偿的磷(补偿,施主掺杂剂)的量(如通过原子数量来测量)近似等于熔体中的硼(过量的,主要的,接受掺杂剂)的量(如通过原子数量来测量)乘以硼的偏析系数k并除以磷的偏析系数(具体地,对于硼,k = 0.8,并且对于磷,k = 0.3)。

[0039] 换句话说,熔体掺杂(受主或施主的浓度,视情况而定,取决于p型或n型半导体)应该理想地保持在如下条件下或接近如下条件:在该条件下,在不具有包含在模具的任何部分或模具涂层中的掺杂材料的模具上生长的晶片将具有高电阻率,诸如典型地,对于n型,大于1欧姆-厘米,并且对于p型,大于2欧姆-厘米。为了实现这一点,存在于模具或涂层中的、与主要类型相反类型的补偿掺杂材料的量应该优选地以由以下关系描述的浓度存在于熔体中:

C_{cd}近似等于C_{md} *(k_{md} / k_{cd})

其中:

C_{md}是模具主要掺杂剂(例如硼)的熔体浓度;

C_{cd}是补偿掺杂剂的熔体浓度(对于上面的硼主要掺杂剂的示例,为磷);

k_{md}是模具主要掺杂剂的有效偏析系数;以及

k_{cd}是补偿掺杂剂的有效偏析系数。

[0040] 所得到的晶片将具有可测量的硼浓度梯度(参见图5),例如从约 1×10^{19} N_a / cm^3至约1×10^{17} N_a / cm^3。在本文中公开的发明的一个方面是一件制品,该制品是具有如从一个表面到相反表面测量的、可测量的主要掺杂剂(诸如硼)浓度梯度的晶片。事实上,在熔体侧的掺杂和在衬底侧的掺杂之间的合理的最小差是三倍的因子。相比于包含相同数量受主的平坦掺杂分布图,这产生0.1%的效率增加。增益的大小取决于许多因素,诸如电池架构,晶片的少数载流子寿命,表面钝化等。用PERC架构实现上面的示例(0.1%增益,1/3的前后掺杂差异。在铝BSF架构的情况下,增益可能不同。如上面所提及的,难以直接测量晶片本体内的掺杂剂(诸如硼)浓度。因此,通过可测量的掺杂剂浓度,其是指能够通过如下操作来确定的掺杂剂浓度:通过现有的或尚待开发的手段直接测量掺杂剂浓度,或者通过如上面所讨论的那样一层接着一层测量电阻率,然后以某种其他方式诸如通过参考表诸如表1或曲线图,根据电阻率计算或确定与该电阻率相关的掺杂剂浓度,并且因此编制电阻率梯度分布图以及还有掺杂剂梯度分布图。

[0041] 应该周期性地或连续地添加补偿掺杂剂,以匹配来自模具的掺杂剂的添加速率。

[0042] 因此,本文中公开的发明的另一方面是一种制作晶片的方法,并且本文中公开的方法发明的更具体的方面是一种制作如上所述的具有可测量的掺杂剂(诸如硼)浓度或电阻率梯度的晶片的方法,并且本特定方法发明是如下方法:随着时间的推移,从熔体制造多个这样的晶片,同时保持相对类似的掺杂和电阻率分布图,即使在制备越来越多的晶片并

且更多的主要掺杂剂进入熔体时。

[0043] 现在转向讨论将被并入到晶片中的掺杂剂来源的位置，图1A中示出典型的位置，如模具110的成形表面122上的涂层，或如图3和图4中示出的，在模具110的本体内的某个地方，在其中当加热模具时掺杂剂能够移动通过模具的本体以离开模具并对熔体116进行掺杂的位置中。因此，如图1A中的114处示出的，掺杂剂114可以在模具110上的涂层(诸如释放层)的最外层112中。或者，如图3中示出的，其可以位于模具310的本体314内，均匀分布或在更集中的区域中，诸如越靠近成形表面322越集中。或者，如图4中示出的，其可以位于模具上的涂层的埋层414中，其中另一层424诸如释放层在表面处。

[0044] 更具体地，模具310其本身能够包含挥发性含硼化合物314，诸如：氧化硼、氮化硼、硼、硼酸以及硼硅酸盐玻璃。替代地或附加地，与熔体紧密接触的模具涂层112能够包含挥发性硼化合物和可溶于硅(在形成硅晶片的情况下，否则可溶于正被形成的半导体)的硼化合物，包括：氧化硼、氮化硼、硼、硼酸、硼硅酸盐玻璃、碳化硼、硼化硅。又另外替代地或附加地，不与熔体紧密接触的模具涂覆区域414能够包含挥发性硼化合物，包括：氧化硼、氮化硼、硼、硼酸、硼硅酸盐玻璃。

[0045] 要考虑的与掺杂剂的位置有关的另一问题是方式，所述掺杂剂通过所述方式从模具传递或迁移到熔融材料。据信存在三种不同的主要可能方式。一种将是将掺杂剂溶解到熔融硅中，然后进一步扩散到熔体中。这种溶解和扩散形式被认为给与许多益处。第二种将是从模具扩散到熔体的液体中。第三种且目前最不优选的是从模具蒸发到熔体中。

[0046] 依次转向这些中的每个，最优选的将是来自模具的诸如以B_4C(碳化硼)或B_4Si(硼化硅)的形式的掺杂剂将从模具(诸如从涂层)溶解到熔体中的场合。在熔体内，掺杂剂将分解成其成分，并且诸如硼的掺杂剂将进一步扩散到熔融材料的本体中。在其尚未使熔体中的它们达到饱和的程度上，诸如很可能情况是这样，诸如C或Si的其他成分也将扩散。由这种方式产生的优点在于，与其他方式不同，在同一模具上制备的每个晶片均接收相同量的掺杂剂，其中所述其他方式诸如下面提及的第三种，其中针对更早制备的晶片释放更多掺杂剂。

[0047] 其中掺杂剂从模具直接扩散到液体中、将从涂层或从模具其本身扩散到熔体中的第二种方式被认为是最不可能的，因为大多数(如果不是全部)材料将通过除仅仅扩散以外的某一模式(诸如通过溶解或蒸发)进入熔体。在任何情况下，对于其中掺杂剂与熔体实际接触的所有模式，扩散都将在某一程度上发生。

[0048] 第三种方式，直接蒸发，不是优选的。例如，可以将B_2O_3(氧化硼)或BN(氮化硼)加热到如下程度：其从其在模具上的位置(例如在涂层中)或其在模具中的位置直接蒸发，以作为气体直接传递到熔融半导体材料中。这不是优选地，因为预期将难以控制掺杂剂被释放到熔体中所达到的程度。掺杂剂的整个来源一次都变热，并且将通过蒸发释放硼，而不仅仅是与熔体接触的掺杂剂来源部分。因此，第一次加热模具时，更多的掺杂剂将被释放，例如，在仅仅一个热循环之后，小颗粒可能消失。或者该过程受掺杂剂颗粒到模具的表面的扩散限制。

[0049] 关于掺杂剂的位置和方式两者，一些示例是有说明性的。对于从与熔体直接接触的(诸如图4中在层424处或者图1B中在层112处示出的)模具涂层(诸如释放涂层)进行掺杂，在期望最小的蒸汽传输时，合适的掺杂剂来源将是Si_3N_4或SiO_2的涂层材料，以及B_4C或

SiB_4的掺杂剂。对于从不与熔体直接接触(诸如图4中在层414处示出的)的模具涂层的任何层进行掺杂,合适的掺杂剂来源将是Si_3N_4或SiC的涂层材料,以及BsO_3或BN的掺杂剂。对于从模具而不是涂层(诸如图3中的314处所示出的)进行掺杂,合适的模具材料将是SiC,以及B_2O_3或BN的掺杂剂。

[0050] 上面描述的基本方法也将对以下行得通:任何其他p型主要掺杂剂而不是硼(诸如铝(Al)、镓(Ga)、铟(In)),并且分别使用任何合适的n型掺杂剂来补偿熔体(磷(P))、砷(As)、锑(Sb)、铋(Bi))。然而,B和P对被认为极其有利于供生长硅晶片使用,因为在所有有效掺杂剂中,它们在硅中具有数值最高的偏析系数。(在凝固期间,具有相对较高的偏析系数的元素比其他元素偏析相对更少,并且照此,在凝固期间,具有最高偏析系数的那些的偏析最少。)因此,在凝固时,与在使用具有数值较小的偏析系数(具有较大的偏析倾向)的元素的状况下将引起的情况相比,掺杂剂B和补偿掺杂剂P将相对均匀地分布在晶体内。也可以使用类似但相关的过程来制备主要n型掺杂的晶片。在那种情况下,由模具或其上的涂层提供的主要掺杂剂将是n型掺杂剂(诸如P、As、Sb、Bi),并且熔体补偿掺杂剂将是p型掺杂剂(诸如B、Al、Ga、In)。

[0051] 下面的表A示出对于p型和n型半导体的代表性主要掺杂剂和补偿掺杂剂及其各自的偏析系数:

P 型		N 型	
主要掺杂剂	补偿掺杂剂	主要掺杂剂	补偿掺杂剂
B (0.8)	P (0.3)	P	B
Al (.002)	As (0.3)	As	Al
Ga (0.008)	Sb (0.023) (锑)	Sb (锑)	Ga
In (0.004)	Bi (0.0007)	Bi	In

表A-掺杂剂和平衡偏析常数。

[0052] 这种对半导体材料进行掺杂的方法可以应用于能够从熔体生长的任何半导体,包括硅(Si)、锗(Ge)、砷化镓(GaAs)等。从除了硅之外的半导体材料生长半导体晶片/本体将需要使用不同的掺杂剂(例如,作为对于GaAs晶片的主要掺杂剂的硅)和不同的补偿掺杂剂材料。

[0053] 下面的表B示出可用作来源的掺杂元素的化合物。x标记意味着化合物存在,例如,碳化硼,氧化硼等。(相反,对于P、As、Sb、Bi,不存在硅化物)。也可以使用纯的元素,并且Si、C、O、N的任何化合物可以掺杂有所述元素中的任一种,然后用作针对掺杂剂的来源。列出的化合物中的一些存在但是由于低稳定性、与水分的反应性、毒性等而不实用:

元素	B	Al	Ga	In	P	As	Sb	Bi
碳化物	x	x	x	x	x	x	x	x
氧化物	x	x	x	x	x	x	x	x
氮化物	x	x	x	x	x	x	x	
硅化物	x	x	x	x				

表B-掺杂元素的化合物。

[0054] 本文中公开的发明给与许多益处。一个益处是有益的电场,其改进少数载流子收

集，并且因此改进太阳能电池的效率。另一益处是在较低的电阻率下的较高效率，这意味着较高的填充因子是可能的。还可能与类PERC过程协同作用(对于类PERC的电池架构，较低的电阻率是有益的)。(PERC代表钝化的发射器后接触)。

[0055] 又另一益处与掺杂剂(或其相关，电阻率)的梯度能够自动产生钝化场的事实有关。(如图5中示出的曲线的左手侧上示出的那样，晶片的最靠近模具形成的部分中的非常高掺杂浓度证明了这一点)。钝化场将减少后表面处的复合。益处是，按常规将在电池处理期间应用的常规铝BSF(背表面场)不是必需的并且可以被消除。然后这将减少形成典型电池的步骤数量。

[0056] 另一优点由此形成。如果不需要Al BSF存在，则能够在晶片的背面使用开放的栅格接触，允许长波长光传递通过电池并且在模块背面的反射板处高效反射，然后返回再次传递通过电池。这在下面更详细地讨论。

[0057] 通过晶片厚度的掺杂(及其相关，电阻率)的梯度也能够提供所谓的背表面场(BSF)。图6A在横截面中示意性地示出并入BSF的已知太阳能电池600。BSF由太阳能电池背面(背对太阳的表面)处的特别高浓度的掺杂剂的区域662创建，这在电池背面处的半导体材料内创建强电场。该电场排斥接近电池背面的少数载流子，并防止其中的绝大多数到达半导体材料的特有背表面664。这是重要的，因为如果它们要到达该背表面664，则很可能它们将在该表面处复合，并且因此不再可用于在外部电路中创建电流。

[0058] 漂移场和背表面场两者均依赖于掺杂密度通过晶片厚度的空间变化，其中较高的掺杂密度朝向电池背面，并且较低的掺杂密度朝向电池正面。然而，它们在若干重要方面有所不同。首先，当漂移场延伸通过晶片厚度时，其是最有效的，因为照此，其将保持温和地将少数载流子推向收集结(而不是让其仅经受扩散)。相反，BSF被限制到电池晶片的背面部分。例如，在180-200微米厚度的电池晶片中，电池晶片的BSF区域可能是1-10微米厚，其中典型的厚度为约5微米。进一步地，BSF中的掺杂水平非常高以创建高电场，其然后有效地向正面排斥少数载流子。事实上，该掺杂水平如此之高，使得其能够在负面上影响该电池的后部分中的少数载流子扩散长度(或寿命)。对器件性能的净影响仍然是非常积极的，因为扩散长度的减小仅局部化于电池的特有背面，并且因为 BSF其本身使进入该区域的载流子的数量最小化。相反，漂移场中的较低掺杂水平对少数载流子扩散长度具有相对小的负面影响。这样的BSF电池示出在图6A中。

[0059] 用以创建BSF的最常见的方式是将铝浆丝网印刷到晶片的背面上，并在带式炉中烧它。这导致具有非常高掺杂密度的铝(p型掺杂剂)的硅的区域662。此外，在这后面，存在铝-硅合金(其许多为共晶成分)的层668。该铝合金区域668充当电池的后接触/导体。不幸的是，对于这样的常规BSF电池的操作，铝-硅合金不是特别好的光学反射器，其具有约60%的反射系数。因此，在其首次传递通过电池本体652时未被吸收的红外光的40％被该后接触吸收，并且不再可用于在第二次传递中返回行进通过电池本体652。这显著地限制由电池生成的电流，并且将电压限制为小的量。电池的面向太阳的表面可以设有带纹理的表面650与电气接触指状物670。

[0060] 如图6B中示出的，本发明的原生掺杂可以提供具有掺杂分布图的区域682，其起BSF的作用，而没有上面提及的缺点。在某些实施例中，特别高掺杂的该区域682(用于背表面)能够与通过电池晶片的厚度掺杂的分布漂移场的更广阔区域692一起被创建。(如图6B

中示出的，为了简化该图，区域692没有掺杂分布图的任何图形表示。然而，应当理解的是，可以有与如上面讨论的图2A和图2B中示出的掺杂分布图类似的平缓或较不平缓的掺杂分布图。)在其他实施例中，来自模具或模具涂层的掺杂剂的通量(flux)能够被设计成更窄地限制于电池晶片的背面。然后，这能够用于创建显著掺杂的BSF区域682，并且还创建仅仅非常轻微地掺杂的漂移场区域692，使得尽管会存在漂移场，但它的梯度将是非常平缓的或较不陡峭的。或者，两种效应都能够用相同的掺杂或用不同的掺杂式样来实现。

[0061] 存在若干种用于创建起BSF的作用的原生掺杂的方法。典型的BSF将具有约$1\times10^{18}/cm^3$受主。为了实现这一点，将在模具内提供大量的受主掺杂剂，诸如硼。为了与正侧掺杂相比增强背侧掺杂，半导体晶体可以在初始成核之后相对缓慢地生长，这将为已经在熔体中的受主提供更多的时间来扩散到熔体更深处，远离凝固晶体，从而允许与紧邻模具生长的初始层相比，晶体中的大部分中的低得多的受主(硼)浓度。BSF的强度与背面处的掺杂与晶片的块体中的掺杂的比例成比例。附加地或者替代地，在凝固的较早部分期间，通过提供更高的真空(或压差)能够增强成核，如下面讨论的那样。这将导致晶体凝固和生长更早地开始，同时将在模具附近、在本体将从其凝固的熔体部分中形成掺杂剂浓度。在上面参考的Sachs等人的专利号8,293,009中描述了随时间的推移或在不同位置中改变真空(或压差状态)的技术。已经制备了如下晶片：该晶片在邻近模具面形成的晶片表面处具有$1\times10^{18}/cm^3$受主的载流子浓度。

[0062] 上文提到在凝固期间调节真空压力或压差状态。这参考8,293,009专利中公开的方法。其中描述的模具为多孔的是有益的(如下面讨论的)。在与熔融材料的表面接触的模具表面与模具的背表面之间提供压差，使得在接触时，朝向模具面汲取熔融材料。模具的多孔性使得熔融材料不被汲取到孔隙中。这通过如下实现：孔隙足够小使得表面张力和其他现象防止熔融材料在材料凝固之前进入孔隙。它们也足够多使得能够建立压差，尽管其各个尺寸小。压差能够通过如下来建立：提供真空，或者通过将熔融材料的表面提供在大气压以上的压力下，其中模具的相反表面处于较小的压力下，使得压差提供迫使熔融材料然后迫使凝固本体朝向模具面的力。通过提供这种压差，与没有压差的情况相比，熔融材料和模具面之间的接触力增强，这提供了更快速的凝固。还可以通过各种手段，诸如在模具面中的具体位置处的热插入物或空隙，跨模具面在各个位置处提供增强的压差，如与其他未增强的位置相反的。通过多孔，这意指充满非常小的孔和通道的本体，使得存在用于气体从模具的一个表面流动到另一个表面的连续路径。孔隙非常小。其通常为微米级，诸如直径为10微米，可能高达30或40微米直径。其有许多，覆盖模具的表面并传递通过其本体的大体积。路径是弯曲的，诸如在天然海绵中。如本文中所定义的，多孔不包括从一个表面传递到另一个表面的宏观简单的空穴，诸如钻通模具本体的孔。

[0063] 图6B示出具有BSF区域682并具有后电极698的电池晶片601，所述后电极698为与正面面向太阳的电极699的指状物673类似的指状物671的形式，其也示出指状物。光学(通常为白光)反射器695(其可能是镜面的或漫射的)在后电极698后面(相对于太阳)。该反射器可以是在模块的封装期间使用的背板。在电池晶片的背面和反射器之间可以存在物理空间687，或者可以不存在空间。以这种方式，在其第一次传递通过硅的主要本体693时未被吸收的光子将离开电池晶片，被光学反射器695反射并且从背表面重新进入电池晶片，用于第二次传递通过硅本体693以及另外的被吸收的机会。背面接触的大部分的光学反射率处于

由放置在电池晶片后面的材料695的反射率支配的那种状况下，其可以大于90％，并且在许多情况下大于95％。电池晶片的面向太阳的表面可以设有与图6A中示出的现有技术实施例类似的有纹理的表面651。

[0064] 图7用图解法示出针对两种类型的电池的量子效率(QE)测量结果。针对图6A中示出的结构的光响应以虚线示出，并且通常在另一曲线的内侧。针对图6B中示出的、本发明的具有原生BSF和反射性背板的结构的光响应以实线示出，并且通常在另一曲线的外侧。因此，如能够看到的，对于图6B中示出的发明的结构，电池的光响应较高。如预期的那样，增加的QE在曲线图900nm-1200nm上的光谱波长的红外区域中，因为正是这些较长波长其能够穿透到电池背面。结果是效率更高的电池。

[0065] 本领域中已知晶片的基本电池结构和某一形式的BSF，例如通过在接触烧步骤期间熔合铝提供的，由开放区域、栅格状电极和反射器镶衬(back)的。一个示例是PASHA电池结构。还已知通过单独的掺杂步骤提供BSF，以在电池的背表面附近提供更重的掺杂。创建这样的结构需要单该独的掺杂步骤。认为本发明在没有用于创建这样的掺杂BSF的单独步骤的情况下创建这样的掺杂BSF，即通过在晶片的生长阶段期间与漂移场一起创建BSF，如上面所解释的那样。因此，本文的另一发明涉及制造这样的结构的新颖且非显而易见的方法，其中根据上面讨论的方法，在晶片生长过程期间创建对于创建BSF所需的掺杂。

[0066] 已经确定，在任何特定系统中，诸如使用硅作为半导体、硼作为主要掺杂剂、并且磷作为补偿掺杂剂，可能出现不期望的情况。回想：在从同一容器和熔体制备许多串晶片时，随着时间的推移，将补偿掺杂剂添加到熔体的块体以保持在从该同一熔体制备的一系列晶片中的每个新制备的晶片的电阻率是相同的。必须进行这，尽管随着时间的推移熔体中存在主要掺杂剂(例如硼)的增加的积聚的事实。

[0067] 不期望的现象是具有比主要掺杂剂更低的偏析系数的补偿掺杂剂更强烈地偏析到晶粒边界。参见例如图8A，其示意性地示出Si晶体800以及在晶粒边界860处积累的低偏析系数补偿掺杂剂D。这通常是不期望的，因为在晶粒边界860附近的较高浓度的补偿掺杂剂D导致在晶粒边界附近存在较高浓度的、补偿掺杂剂需要的载流子类型D(在P的情况下，这些是施主，并且因此使用字母D来表示它们)。照此，将在晶粒内建立指向晶粒边界的电场，并且因此，少数载流子将被汲取到边界。这样的情况是不期望的，因为那不是期望引导这些载流子的地方。它们要被远离具有较高浓度的受主掺杂剂A的晶片的表面242，朝向将邻近表面246形成的p/n结(尚未形成，并且因此未在图8A中示出)引导，所述表面246具有较低浓度的受主掺杂剂A。

[0068] 已经确定，这种不期望的效果能够通过提供第二补偿掺杂剂的反直觉步骤来克服，所述第二补偿掺杂剂在本文中称为反补偿掺杂剂，例如在Si/B/Ph系统的情况下，铝(Al)反补偿掺杂剂。铝是与主要掺杂剂相同类型的载流子施主/受主。因此，铝是受主，如同硼一样。最有益的是，反补偿掺杂剂的偏析系数在数值上小于第一补偿掺杂剂的偏析系数，并且在数值上尽可能接近第一补偿掺杂剂的系数值。具有在数值上较小的偏析系数，反补偿掺杂剂甚至比补偿掺杂剂更强烈地迁移到晶粒边界。因此，在这些边界处，正是受主/施主角色抵消补偿由于相对较高浓度的补偿掺杂剂而存在的过度的施主/受主。

[0069] 在其中主要掺杂剂的偏析系数在数值上低于第一补偿掺杂剂的偏析系数的情况下，没有必要使用第二、反补偿掺杂剂(并且因此，补偿掺杂剂简单地是补偿掺杂剂，而不是

第一补偿掺杂剂)。针对硅半导体的非常有用的组合使用硼作为主要掺杂剂,磷作为补偿掺杂剂,并且Ga(镓)作为第二反补偿掺杂剂。B具有最大的偏析系数(最小的偏析),为0.8,后面是为0.3的P以及为0.008的Ga。

[0070] 表C示出如表A所示出的用于诸如硅的P型半导体晶体和N型半导体两者的主要(衬底)掺杂剂、补偿掺杂剂和第二反补偿掺杂剂的不同组合,但是具有与反补偿掺杂剂有关的另外的信息。针对每个元素的偏析系数也在第一次提及该元素时被提供:

P型			N型		
主要掺杂剂	补偿掺杂剂	反补偿掺杂剂	主要掺杂剂	补偿掺杂剂	反补偿掺杂剂
B (0.8)	P (0.3)	Al	P	B	As
Al (.002)	As (0.3)	Ga	As	Al	Sb
Ga (0.008)	Sb (0.023)	In	Sb	Ga	Bi
In (0.004)	Bi (0.0007)		Bi	In	
B (0.8)	P (0.3)	Ga			

表C-用于P型和N型半导体的主要掺杂剂、补偿掺杂剂和反补偿掺杂剂的组合。

[0071] 上面的表C中列出的化合物能够用于提供反补偿掺杂剂以及主要掺杂剂和补偿掺杂剂。在其中将n型掺杂剂和p型掺杂剂两者添加到熔体的情况下,能够使用化合物半导体来添加第二、反补偿掺杂剂。例如,在硼主要掺杂剂的情况下,能够使用InP(磷化铟)。磷将提供补偿掺杂,而铟将以与上面的表中的Ga相同的方式提供反补偿。但P和In将作为复合剂而不是作为单独的添加剂被提供。

[0072] 示例

已经生长了晶片,并且已经制备了太阳能电池。太阳能电池示出在非常低的电阻率下的高效率。例如,在使用该方法的晶片上制备的太阳能电池仅具有0.3欧姆-厘米的平均体电阻率,效率比具有2.2欧姆-厘米的电阻率的控制晶片高2%。图5中示意性地示出的掺杂分布图是通过如下测量的:选择性地一层接着一层去除硅并测量剩余晶片的电阻率。一般地,在具有较高掺杂剂浓度的区域中存在较低的电阻率,并且反之亦然。(通过测量电阻率推断掺杂,因为测量形成的晶片中的材料的浓度是困难的,然而,一层一层地测量电阻率不是特别困难。因此当考虑对本文中的权利要求的侵犯时,从一个表面到另一个的电阻率分布图的存在可以被认为是相应的掺杂剂浓度分布图的证据。此外,展现电阻率分布图的晶片——在一个表面(通常为不面向太阳的背表面,其中在p型晶片中存在较高的掺杂剂浓度)处具有较低的电阻率,而在另一表面(在那种情况下,其将是面向阳光的表面)处具有较高电阻率,被认为是本发明,如同包括这样的晶片的太阳能电池和制备这样的晶片的方法那样。

[0073] 平均净受主浓度为约5×10^{15} /cm^3,在背表面(在面向模具的侧上形成)处具有约10倍更多的掺杂。电池具有铝背表面场,而不是原生BSF,也如上面所讨论的那样。硼掺杂剂为约1×10^{18}原子/cm^3。杂质含量最小,并且在任何情况下,小于在平衡偏析时存在的量的10

倍。存在如下补偿掺杂剂的范围:从没有(在运行最开始时)到在运行结束时的约1×10^{18}原子/cm^3(其中制备了约2,000个晶片。

[0074] 本文中公开的发明解决了许多问题。本发明允许从形成的晶片的一个表面到另一个表面的掺杂剂梯度的低成本建立。迄今为止,已知在硅晶片中建立掺杂剂梯度的方法导致低质量的硅(诸如掺杂镓的RGS(衬底上的带状生长)或者使非常昂贵的(外延生长的硅)。

[0075] 应当注意,用以给晶片提供掺杂水平的分布图的前述技术中许多/任何能够与任何其他技术一起使用。例如,向模具提供掺杂剂(例如在涂层中、在模具的本体中或在模具表面附近)的任何方式,能够与随着时间的推移补偿熔体中的过量掺杂剂的任何方法一起使用,并且反补偿补偿掺杂剂到晶粒边界的过度偏析的任何方法也能够与提供掺杂分布图的任何其他方法一起使用。在一定程度上和位置中提供掺杂剂以创建BSF能够与用于掺杂剂补偿以及还有用于抵消补偿掺杂剂在晶粒边界处的积累的任何技术一起使用。用于形成任何曲线或形状的掺杂剂分布图的技术能够与补偿和反补偿技术以及还有与形成BSF的方法一起使用。

[0076] 本公开描述和公开了一个以上发明。所述发明在本文件和相关文件的权利要求书中阐述,所述相关文件不仅如提交的,而且还如在基于本公开的任何专利申请的审查期间提出的。发明人意图到现有技术所允许的最大限度,要求保护所有各种发明,如其随后被确定为的那样。本文中所描述的特征并不是本文中公开的每个发明所必需的。因此,发明人意图除了基于本公开的任何专利的任何特定权利要求中要求保护的特征以外,本文中描述的特征不应并入到任何这样的权利要求中。

[0077] 例如,漂移场的发明对于BSF的发明不是必需的,并且反之亦然。能够建立平缓的漂移场,并且其不具有极其高掺杂的BSF。BSF能够设有相对高掺杂的区域,并且晶片的其余部分能够是相对均匀的,基本上没有漂移场,或者仅有轻微程度的漂移场。对于单个晶片形成,或者甚至对于一串晶片,不必要在熔体中提供补偿掺杂剂,只要熔体中主要掺杂剂的浓度不变得太大以致不能形成优质的晶片。能够使用掺杂剂补偿的其他方法。类似地,不需要使用用以防止补偿掺杂剂在晶粒边界处的过度积累的反补偿方法,其在本文中被公开提供具有甚至更小的偏析系数的反掺杂剂。对于一些应用,可以容忍这样的累积,或者能够使用抵消所述累积的其他方法。

[0078] 一些硬件的组合或步骤的组在本文中被称为发明。然而,这不是承认任何这样的组合或组必须是具有可专利性的不同发明,特别是如关于将在一个专利申请中被审查的发明的数量或发明的单一性由法律和规章所设想的。其意图是说明发明的实施例的简短方式。

[0079] 同此提交了摘要。要强调的是,提供该摘要以符合需要将允许审查员和其他搜索者快速确定本技术公开的主题的摘要的规定。在理解如下的情况下提交摘要:其将不用于解释或限制权利要求的范围或意义,如专利局的规定所约定的那样。

[0080] 上述讨论应该被理解为说明性的,并且不应该在任何意义上被认为是限制性的。虽然已经参考其优选实施例特别示出和描述了本发明,但是本领域技术人员将理解的是,在不脱离如由权利要求限定的本发明的精神和范围的情况下,在其中可以做出形式和细节方面的各种改变。

[0081] 下面的权利要求书中的所有装置或步骤加上功能元件的相应结构、材料、动作和

等同物旨在包括用于与如具体要求保护的其他要求保护的元件组合地执行功能的任何结构、材料或动作。

[0082] 发明的方面

本发明的以下方面意图在本文中进行描述，并且本部分要确保它们被提及。它们被命名为方面，并且尽管它们看起来与权利要求类似，但它们并不是权利要求。然而，在未来的某一时候，申请人保留在该申请和任何相关申请中要求保护这些方面中的任何和所有的权利。

[0083] A1．一种用于制作供用作太阳能收集器的半导体晶片的方法，所述方法包括以下步骤：

a．提供具有表面的熔融半导体材料；

b．提供包括成形表面的模具，所述模具还包括与所述半导体材料有关的主要掺杂剂；

c．使所述成形表面与所述熔融材料接触，使得掺杂剂从所述模具迁移到所述熔融半导体材料中；以及

d．维持条件，使得以晶片形式的半导体材料的本体在所述成形表面上凝固，其中第一表面接触所述成形表面，所述晶片具有掺杂剂浓度的分布图，在所述晶片的第一表面处存在较大的掺杂剂浓度，并且在所述晶片的第二表面处存在较小的掺杂剂浓度。

[0084] A2．一种用于制作供用作太阳能收集器的半导体晶片的方法，所述方法包括以下步骤：

a．提供具有表面的熔融半导体材料；

b．提供包括成形表面的模具，所述模具还包括与所述半导体材料有关的掺杂剂；

c．使所述成形表面与所述熔融材料接触达接触持续时间，使得对于所述接触持续时间的至少一部分，掺杂剂从所述模具迁移到所述熔融半导体材料中；以及

d．维持条件，使得以晶片形式的半导体材料的本体在所述成形表面上凝固，所述晶片具有电阻率的分布图，在所述晶片的第一表面处存在相对较小的电阻率，并且在所述晶片的第二表面处存在相对较大的电阻率。

[0085] A3．根据方面1和2中任一方面所述的方法，还包括把凝固的晶片从所述成形表面卸下的步骤。

[0086] A4．根据方面1至3中任一方面所述的方法，所述模具包括在一个表面上的涂层，所述涂层包含所述主要掺杂剂。

[0087] A5．根据方面1至3中任一方面所述的方法，所述模具还包括本体，其中，所述主要掺杂剂分布在所述模具本体内。

[0088] A6．根据方面1至3中任一方面所述的方法，所述模具还包括本体，其中，所述主要掺杂剂以靠近一个表面的较高浓度处于所述模具本体内。

[0089] A7．根据方面1至6中任一方面所述的方法，所述维持条件的步骤包括：以半导体的凝固本体充当扩散阻挡物的形式在所述模具处提供所述主要掺杂剂，使得随着所述凝固本体生长，初始主要掺杂剂以第一速率迁移到所述熔融材料和所述凝固本体中，并且随后，主要掺杂剂以越来越小的速率迁移到所述熔融材料和所述凝固本体中，使得与稍后凝固的本体部分相比，较早凝固的本体部分每单位体积具有相对较多的主要掺杂剂。

[0090] A8．根据方面1至7中任一方面所述的方法，所述主要掺杂剂包括施主和受主类型

中仅一种类型的电荷载流子，所述方法还包括：

进行(视情况而定，方面1或2的)步骤a，b，c和d至少两次；

在所述熔融材料中提供一些与所述主要掺杂剂相反的电荷载流子施主/受主类型的补偿掺杂剂。

[0091] A9．根据方面8所述的方法，还包括：在所述熔融材料中提供一些与所述补偿掺杂剂相反的电荷载流子施主/受主类型的反补偿掺杂剂的步骤。

[0092] A10．根据方面9所述的方法，所述补偿掺杂剂和所述反补偿掺杂剂均具有平衡偏析系数，所述反补偿掺杂剂的平衡偏析系数等于或小于所述补偿掺杂剂的平衡偏析系数。

[0093] A11．根据方面8所述的方法，其中，提供一些补偿掺杂剂的步骤通过以根据以下关系的浓度C_{cd}在所述熔体中提供所述补偿掺杂剂来实现：

C_{cd}近似等于$C_{md}*(k_{md}/k_{cd})$

C_{md}是所述主要掺杂剂的熔体浓度；

C_{cd}是所述补偿掺杂剂的熔体浓度；

k_{md}是所述主要掺杂剂的有效偏析系数；以及

k_{cd}是所述补偿掺杂剂的有效偏析系数。

[0094] A12．根据方面1所述的方法，主要掺杂剂浓度在所述晶片的第一表面处小于或等于1×10^{20} N_x/cm^3，并且在所述晶片的第二表面处大于或等于约1×10^{15} N_x/cm^3，其中，对于电荷载流子受主掺杂剂，N_x意指电荷载流子受主的数量N_a，并且对于电荷载流子施主掺杂剂，N_x意指电荷载流子施主的数量N_d。

[0095] A13．根据方面2所述的方法，所述主要掺杂剂是电荷载流子受主，所述电阻率在所述晶片的第一表面处大于或等于0.001欧姆-厘米，并且在所述晶片的第二表面处小于或等于约10欧姆-厘米。

[0096] A14．根据方面1所述的方法，主要掺杂剂浓度在所述晶片的第一表面处小于或等于1×10^{19} N_x/cm^3，并且在所述晶片的第二表面处大于或等于约1×10^{17} N_x/cm^3，其中，对于电荷载流子受主掺杂剂，N_x意指电荷载流子受主的数量N_a，并且对于电荷载流子施主掺杂剂，N_x意指电荷载流子施主的数量N_d。

[0097] A15．根据方面2所述的方法，所述主要掺杂剂是电荷载流子施主，所述电阻率在所述晶片的第一表面处大于或等于0.001欧姆-厘米，并且在所述晶片的第二表面处小于或等于约0.1欧姆-厘米。

[0098] A16．根据方面1和2中任一方面所述的方法，所述半导体包括p型半导体，所述主要掺杂剂选自由硼、铝、镓和铟组成的组。

[0099] A17．根据方面1和2中任一方面所述的方法，所述半导体包括n型半导体，所述主要掺杂剂选自由磷、砷、锑(Sb)和铋组成的组。

[0100] A18．根据方面8所述的方法，所述半导体包括p型半导体，所述补偿掺杂剂选自由磷、砷、锑(Sb)和铋组成的组。

[0101] A19．根据方面8所述的方法，所述半导体包括n型半导体，所述补偿掺杂剂选自由硼、铝、镓和铟组成的组。

[0102] A20．根据方面18所述的方法，还包括在所述熔融材料中提供如下反补偿掺杂剂的步骤：该反补偿掺杂剂选自由铝、镓和铟组成的组。

[0103] A21．根据方面19所述的方法，还包括在所述熔融材料中提供如下反补偿掺杂剂的步骤：该反补偿掺杂剂选自由砷、锑和铋组成的组。

[0104] A22．根据方面4所述的方法，所述熔融材料包括硅，所述涂层包括选自由B_4C(碳化硼)和B_4Si(硼化硅)组成的组的掺杂剂。

[0105] A23．根据方面1和2中任一方面所述的方法，所述主要掺杂剂包括选自由碳化物、氧化物、氮化物和硅化物组成的组的化合物，或者选自由硼、铝、镓、铟、磷、砷、锑和铋组成的组的元素。

[0106] A24．根据方面1和2中任一方面所述的方法，进行维持步骤，以便在所述晶片的第一表面处提供足够高以便在用作太阳能收集器的晶片中建立背表面场的主要掺杂剂浓度。

[0107] A25．根据方面24所述的方法，还包括提供如下部件的步骤：

a．以开放栅格形式的金属导体，所述金属导体耦合到所述晶片，接触所述晶片的所述第一表面；以及

b．光学反射器，所述光学反射器与所述第一表面隔开布置使得所述金属导体位于所述第一表面和所述光学反射器之间。

[0108] A26．根据方面1所述的方法，所述掺杂剂浓度的分布图具有如下形状：该形状将在所述晶片本体内产生漂移电场，所述漂移电场目的在于在优选方向上驱策电荷载流子。

[0109] A27．根据方面2所述的方法，所述电阻率的分布图具有如下形状：该形状将在所述晶片本体内产生漂移电场，所述漂移电场目的在于在优选方向上驱策电荷载流子。

[0110] A28．一种供用作太阳能收集器的半导体晶片，所述晶片包括具有第一表面和第二表面的本体，所述本体具有掺杂剂浓度分布图，存在位于所述晶片的第一表面处的较大的掺杂剂浓度，以及到所述晶片的第二表面处的较小的掺杂剂浓度的连续过渡，较大浓度是较小浓度的至少三倍，进一步地，其中，存在于所述本体中的任何金属杂质以小于存在于所述第二表面的金属杂质的程度的十倍的程度存在于所述第一表面。

[0111] A29．一种供用作太阳能收集器的半导体晶片，所述晶片包括具有第一表面和第二表面的本体，所述本体具有电阻率分布图，存在位于所述晶片的第一表面处的较小电阻率，以及到所述晶片的第二表面处的较大电阻率的连续过渡，较大电阻率是较小电阻率的至少三倍，进一步地，其中，存在于所述本体中的任何金属杂质以小于存在于所述第二表面的金属杂质的程度的十倍的程度存在于所述第一表面。

[0112] A30．根据方面28和29中任一方面所述的半导体晶片，所述半导体包括硅，并且所述掺杂剂包括硼。

[0113] A31．根据方面28和29中任一方面所述的半导体晶片，所述半导体包括硅，并且所述掺杂剂选自由硼、铝、镓和铟组成的组。

[0114] A32．根据方面28和29中任一方面所述的半导体晶片，所述半导体包括p型半导体，并且所述掺杂剂选自由硼、铝、镓和铟组成的组。

[0115] A33．根据方面28和29中任一方面所述的半导体晶片，所述半导体包括n型半导体，并且所述掺杂剂选自由磷、砷、锑(Sb)和铋组成的组。

[0116] A34．根据方面28所述的半导体晶片，掺杂剂浓度在所述晶片的第一表面处小于或等于1×10^{20} N_x/cm^3，并且在所述晶片的第二表面处大于或等于约1×10^{15} N_x/cm^3，其中，对于电荷载流子受主掺杂剂，N_x意指电荷载流子受主的数量N_a，并且对于电荷载流子施主掺

杂剂，N_x意指电荷载流子施主的数量N_d。

[0117] A35．根据方面29所述的半导体晶片，所述电阻率在所述晶片的第一表面处大于或等于0.001欧姆-厘米，并且在所述晶片的第二表面处小于或等于约10欧姆-厘米。

[0118] A36．根据方面28所述的半导体晶片，所述晶片的第一表面处的主要掺杂剂的浓度足够高，以便在用作太阳能收集器的晶片中建立背表面场。

[0119] A37．根据方面29所述的半导体晶片，所述晶片的第一表面处的电阻率足够低，以便在用作太阳能收集器的晶片中建立背表面场。

[0120] A38．根据方面36和37中任一方面所述的半导体晶片，还包括：

a．以开放栅格形式的金属导体，所述金属导体耦合到所述晶片，接触所述晶片的所述第一表面；以及

b．光学反射器，所述光学反射器与所述第一表面隔开布置使得所述金属导体位于所述第一表面和所述光学反射器之间。

[0121] A39．根据方面28所述的半导体晶片，掺杂剂浓度的分布图具有如下形状：该形状将在所述晶片本体内产生漂移电场，所述漂移电场目的在于在优选方向上驱策电荷载流子。

[0122] A40．根据方面29所述的半导体晶片，所述电阻率的分布图具有如下形状：该形状将在所述晶片本体内产生漂移电场，所述漂移电场目的在于在优选方向上驱策电荷载流子。

[0123] A41．一种太阳能收集器，包括多个半导体晶片，每个晶片包括具有第一表面和第二表面的本体，所述本体具有掺杂剂浓度分布图，存在位于所述晶片的第一表面处的较大的掺杂剂浓度，以及到所述晶片的第二表面处的较小的掺杂剂浓度的连续过渡，较大浓度是较小浓度的至少三倍，进一步地，其中，存在于所述本体中的任何金属杂质以小于存在于所述第二表面的金属杂质的程度的十倍的程度存在于所述第一表面。

[0124] A42．一种太阳能收集器，包括多个半导体晶片，每个晶片包括具有第一表面和第二表面的本体，所述本体具有电阻率分布图，存在位于所述晶片的第一表面处的相对较小的电阻率，以及到所述晶片的第二表面处的相对较大的电阻率的连续过渡，进一步地，其中，存在于所述本体中的任何金属杂质以小于存在于所述第二表面的金属杂质的程度的十倍的程度存在于所述第一表面。

[0125] A43．根据方面41和42中任一方面所述的太阳能收集器，所述半导体包括硅，并且所述掺杂剂包括硼。

[0126] A44．根据方面41和42中任一方面所述的太阳能收集器，所述半导体包括硅，并且所述掺杂剂选自由硼、铝、镓和铟组成的组。

[0127] A45．根据方面41和42中任一方面所述的太阳能收集器，所述半导体包括p型半导体，并且所述掺杂剂选自由硼、铝、镓和铟组成的组。

[0128] A46．根据方面41和42中任一方面所述的太阳能收集器，所述半导体包括n型半导体，并且所述掺杂剂选自由磷、砷、锑(Sb)和铋组成的组。

[0129] A47．根据方面41所述的太阳能收集器，掺杂剂浓度在所述晶片的第一表面处小于或等于1×10^{20} N_x/cm^3，并且在所述晶片的第二表面处大于或等于约1×10^{15} N_x/cm^3，其中，对于电荷载流子受主掺杂剂，N_x意指电荷载流子受主的数量N_a，并且对于电荷载流子施

主掺杂剂，N_x意指电荷载流子施主的数量N_d。

[0130] A48．根据方面42所述的太阳能收集器，所述电阻率在所述晶片的第一表面处大于或等于0.001欧姆-厘米，并且在所述晶片的第二表面处小于或等于约10欧姆-厘米。

[0131] A49．根据方面41所述的太阳能收集器，所述晶片的第一表面处的主要掺杂剂的浓度足够高，以便在用作太阳能收集器的晶片中建立背表面场。

[0132] A50．根据方面42所述的太阳能收集器，所述晶片的第一表面处的电阻率足够低，以便在用作太阳能收集器的晶片中建立背表面场。

[0133] A51．根据方面49和50中任一方面所述的太阳能收集器，还包括：

a．以开放栅格形式的金属导体，所述金属导体耦合到所述晶片，接触所述晶片的所述第一表面；以及

b．光学反射器，所述光学反射器与所述第一表面隔开布置使得所述金属导体位于所述第一表面和所述光学反射器之间。

[0134] A52．根据方面41所述的太阳能收集器，掺杂剂浓度的分布图具有如下形状：该形状将在所述晶片本体内产生漂移电场，所述漂移电场目的在于在优选方向上驱策电荷载流子。

[0135] A53．根据方面42所述的太阳能收集器，所述电阻率的分布图具有如下形状：该形状将在所述晶片本体内产生漂移电场，所述漂移电场目的在于在优选方向上驱策电荷载流子。

[0136] 已经对本发明进行描述，要求保护的范围见权利要求书。

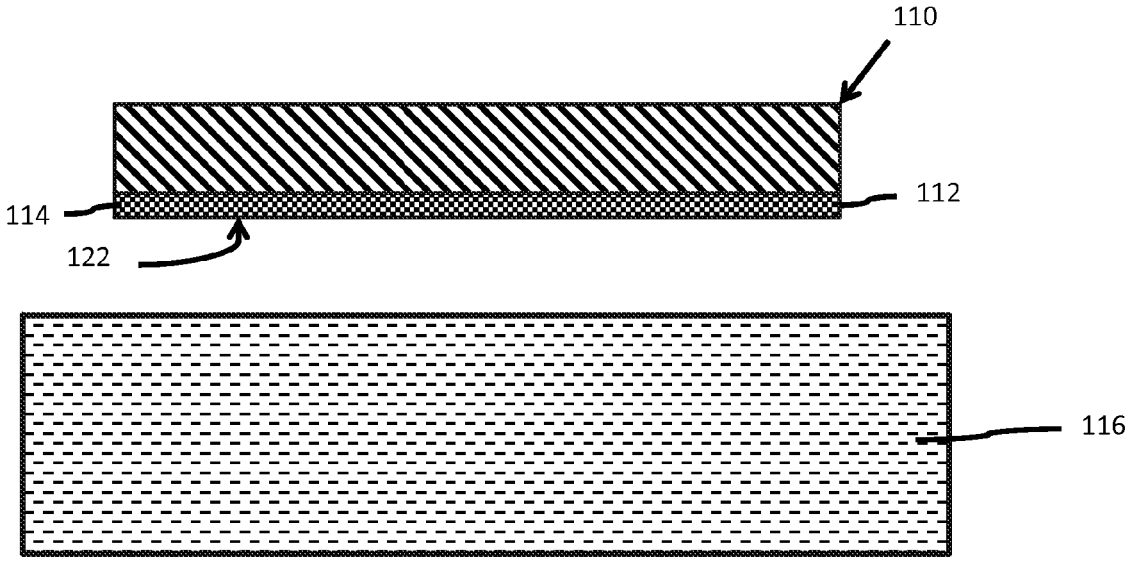


图 1A

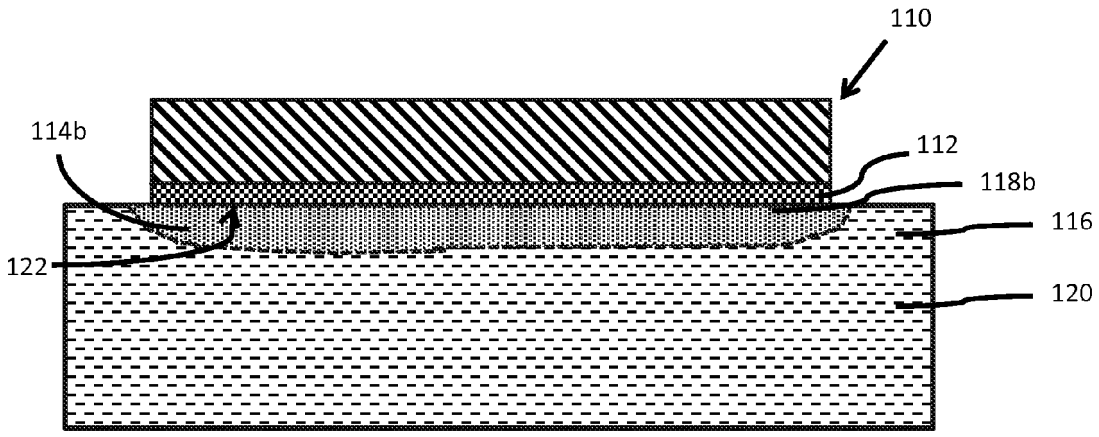


图 1B

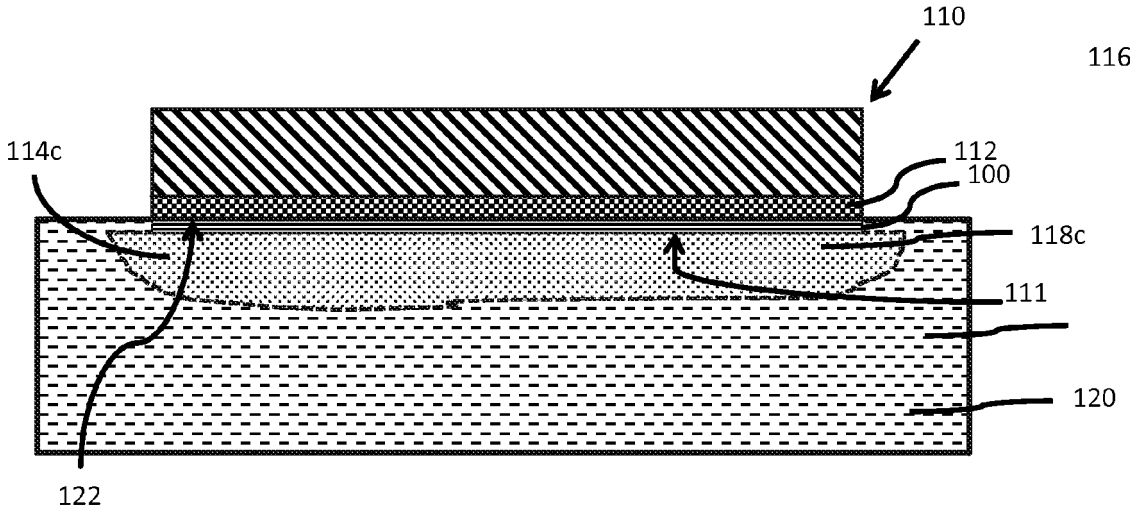

110
116
114c
112
100
118c
111
120
122

图 1C

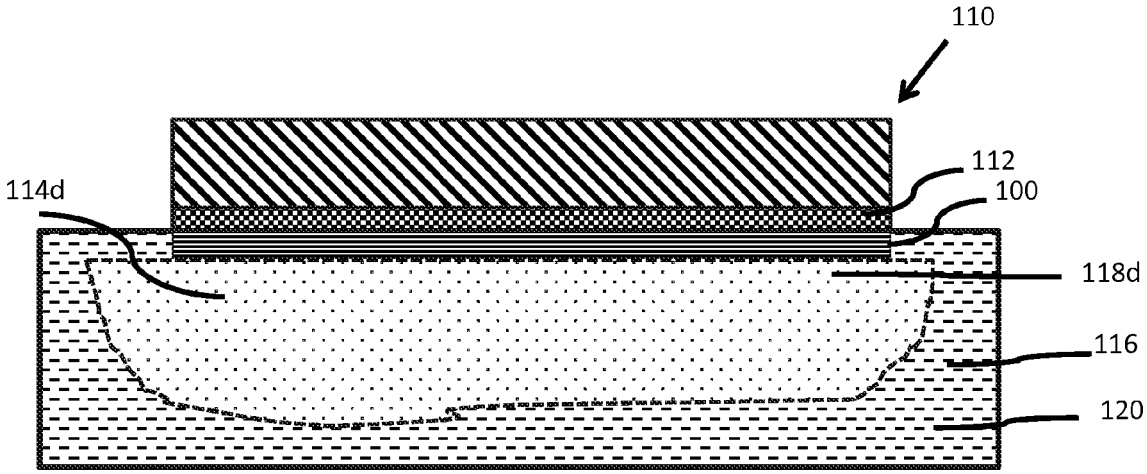

110
114d
112
100
118d
116
120

图 1D

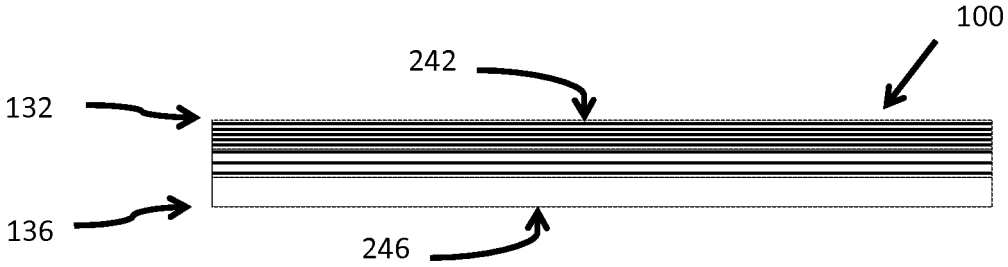

100
242
132
136
246

图 2A

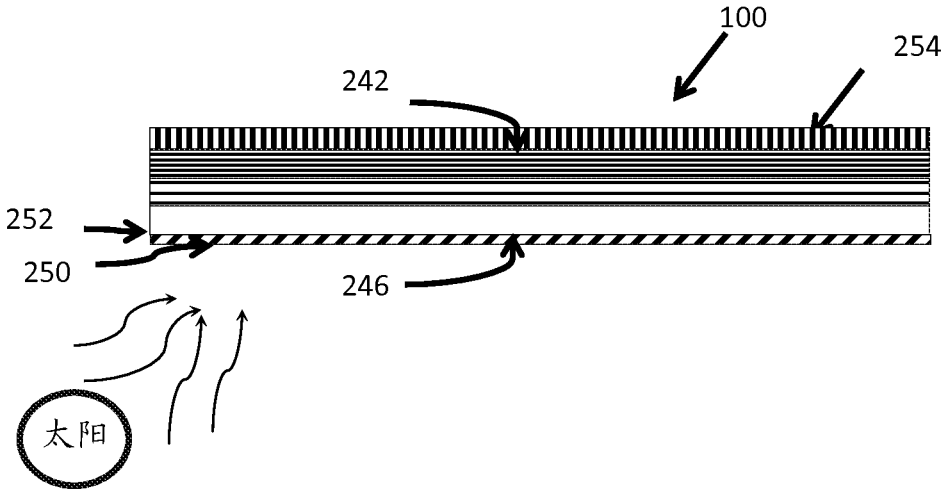


图 2B

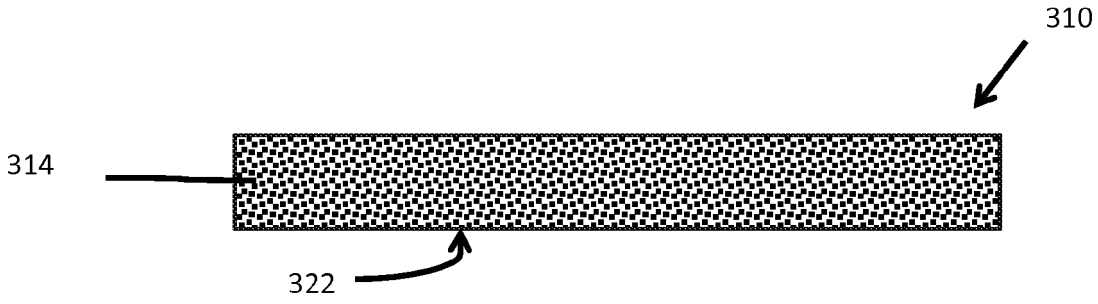


图 3

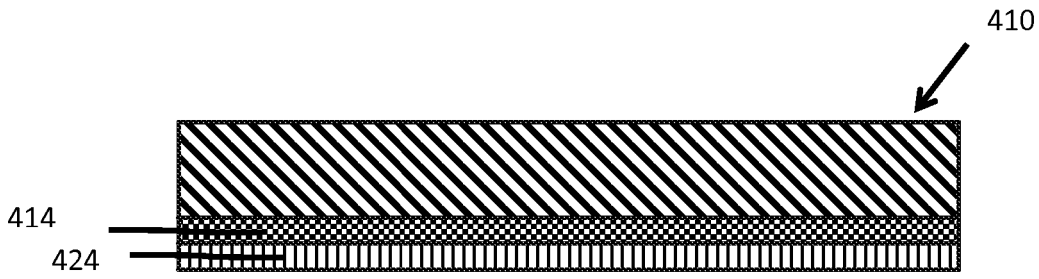


图 4

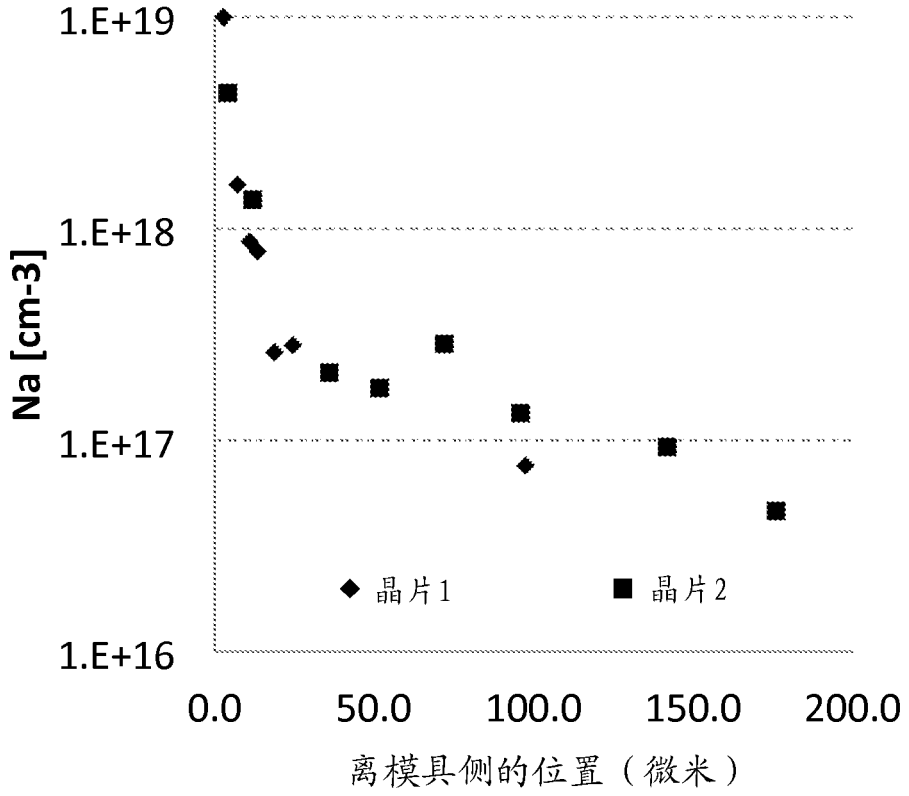
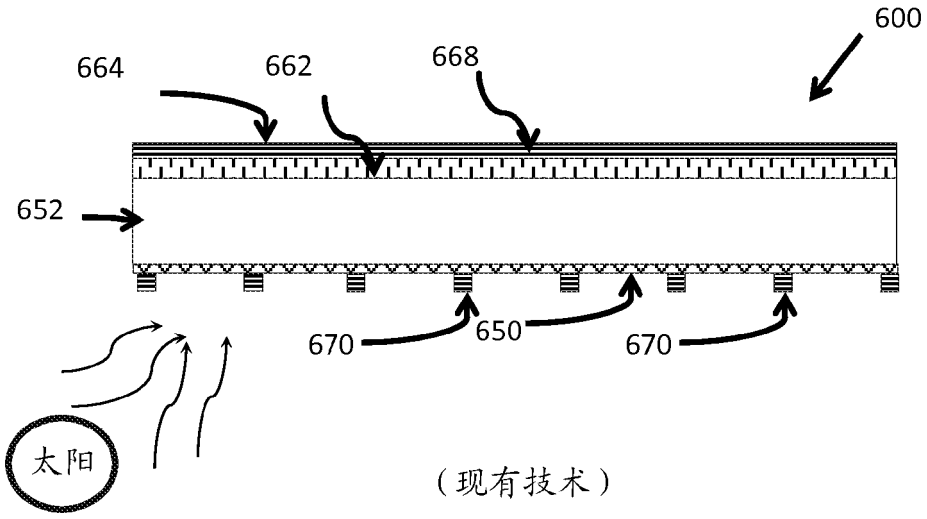

1.E+19
1.E+18
1.E+17
1.E+16
Na [cm-3]
晶片1
晶片2
0.0
50.0
100.0
150.0
200.0
离模具侧的位置（微米）

图 5


600
664
662
668
652
670
650
670
太阳

（现有技术）

图 6A

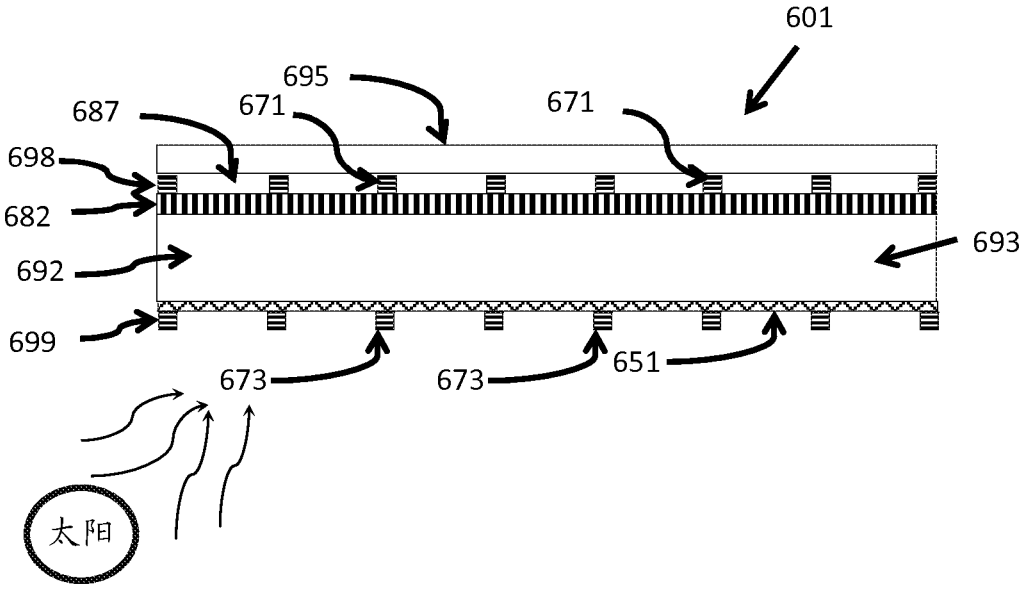

601
695
687
671
671
698
682
693
692
699
673
673
651
太阳

图 6B

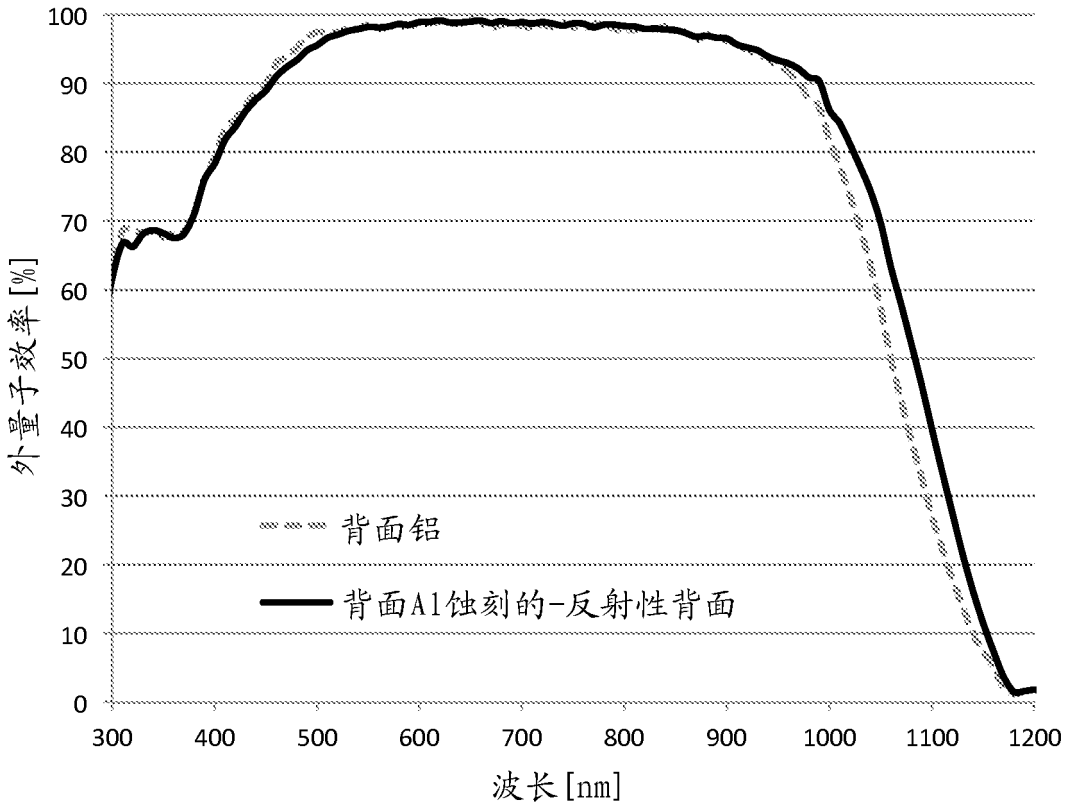

100
90
80
70
60
50
40
30
20
10
0
外量子效率[%]
300
400
500
600
700
800
900
1000
1100
1200
波长[nm]
背面铝
背面Al蚀刻的-反射性背面

图 7

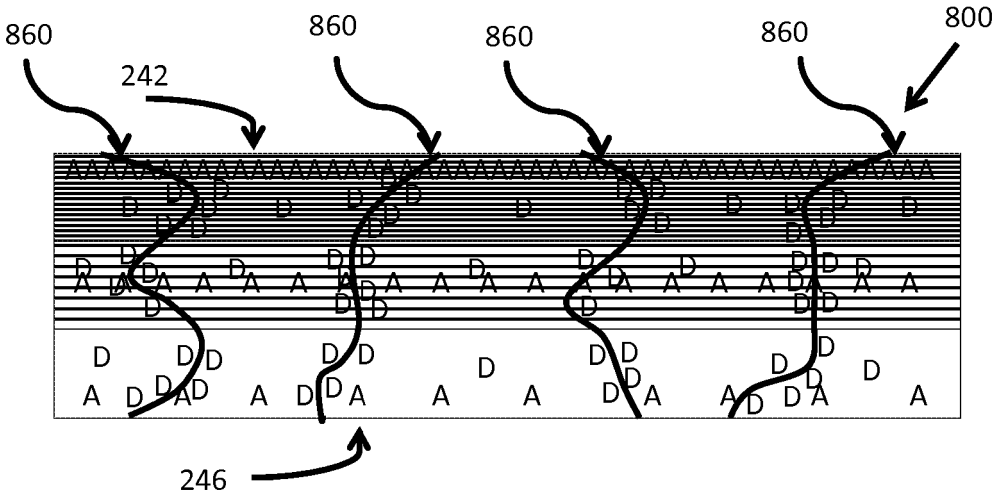


图 8A

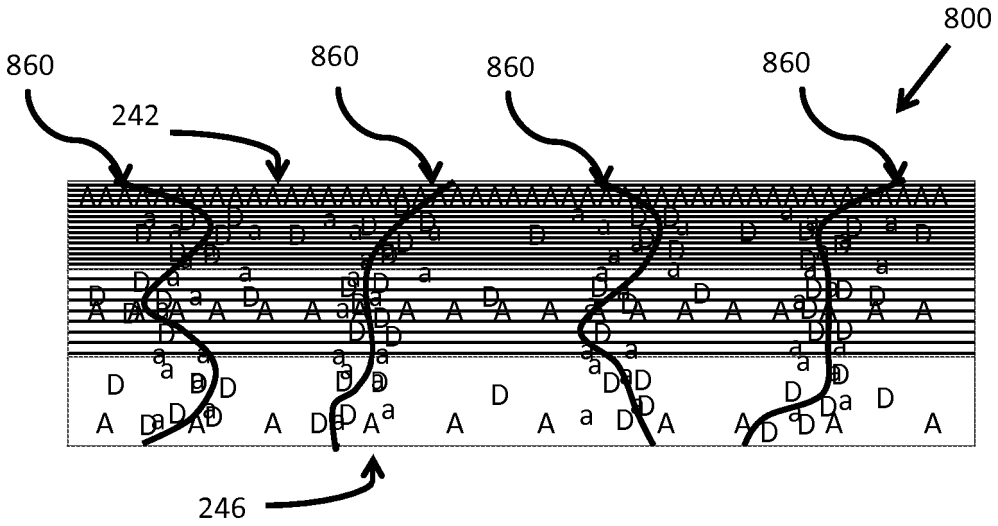


图 8B