United States
Zambuto

3,793,626
[45] Feb. 19, 1974

[54] **REFRESHED CRT DISPLAY WITH ECG**

[76] Inventor: **Raymond Peter Zambuto,** 354 Whipple Rd., Tewksbury, Mass. 01876

[22] Filed: **Sept. 30, 1971**

[21] Appl. No.: **185,322**

[52] **U.S. Cl.**..... **340/172.5,** 340/324 A, 128/2.06
[51] **Int. Cl.**..... **G06f 3/14,** G06f 15/42
[58] **Field of Search** ..... 340/172.5, 324 A; 235/197, 235/198, 181; 128/2.06

[56] **References Cited**

UNITED STATES PATENTS

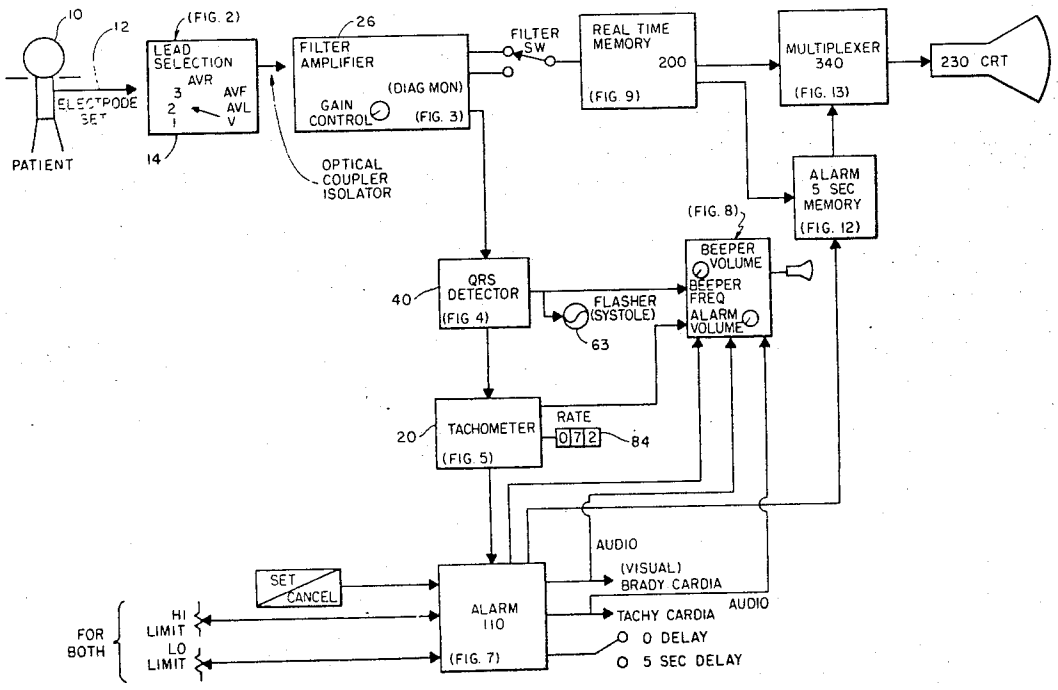
3,652,999	3/1972	Hjort	340/172.5
3,333,247	7/1967	Hadley et al	340/172.5
3,406,387	10/1968	Werme	340/172.5
3,442,264	5/1969	Levitt	235/181
3,566,365	2/1971	Rawson	340/172.5

Primary Examiner—Paul J. Henon
Assistant Examiner—John P. Vandenburg
Attorney, Agent, or Firm—Richard L. Stevens

[57] **ABSTRACT**

A monitor for the display of electrocardiogram (ECG) signals. The signals from the patient are digitized and enter a main memory. The data is recycled and continually updated. The data is displayed as real time on a cathode ray tube (CRT) in such a manner that the data originally entered moves from right to left across the scope in the same position. Thus, at approximately five seconds the data is at the left of the screen. All subsequent data follows the same pattern whereby the display on the CRT appears as a continuously moving waveform. An alarm memory receives data five seconds old and stores the data for five seconds. If the ECG signals from the patient violate certain limits, an alarm is actuated. The data in the alarm memory at the time of the alarm is sealed off and displayed as a stationary waveform on the CRT with the real time display.

33 Claims, 14 Drawing Figures



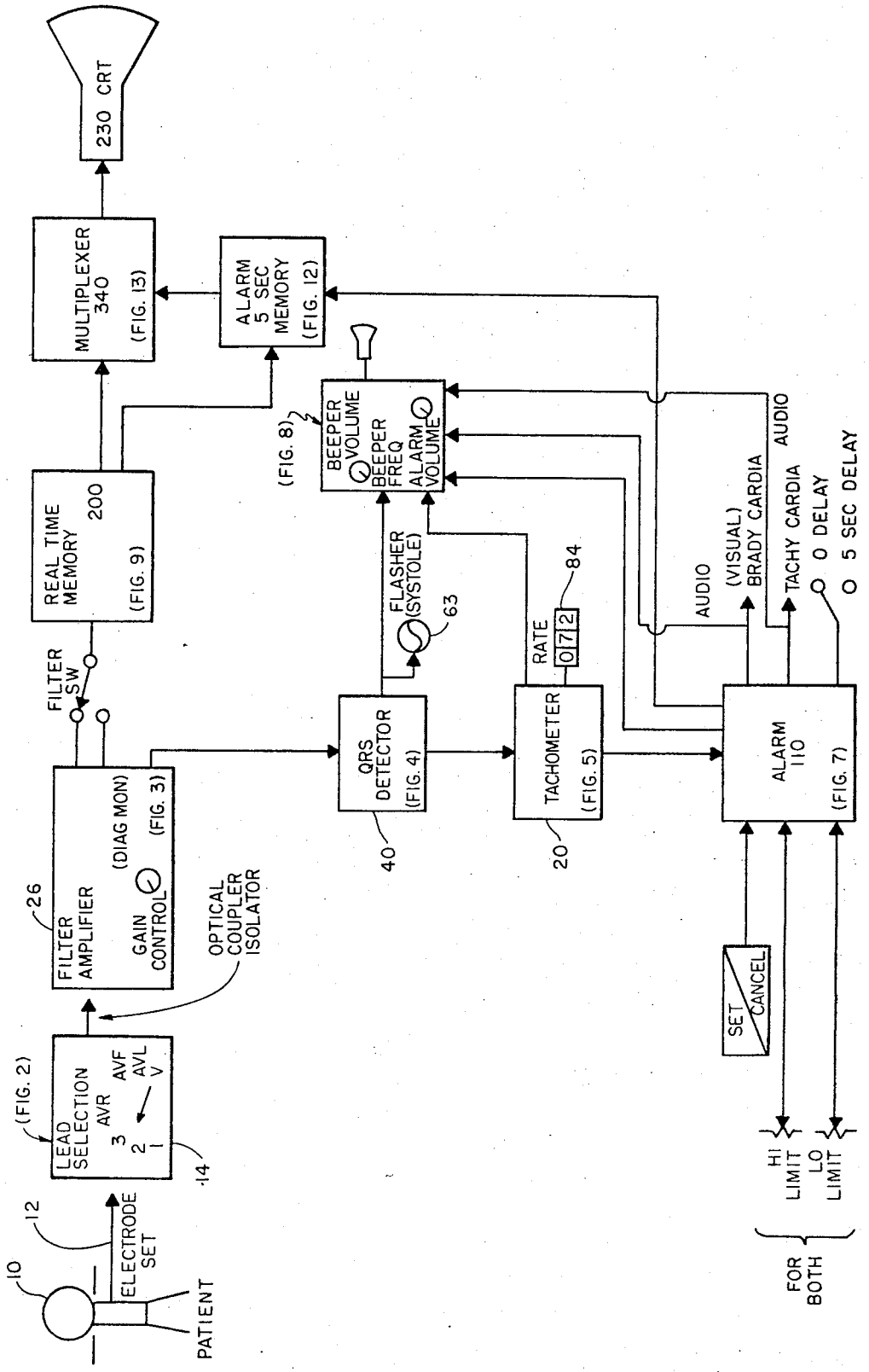

230 CRT
MULTIPLEXER 340 (FIG. 13)
ALARM 5 SEC MEMORY (FIG. 12)
(FIG. 8)
BEEPER VOLUME
BEEPER FREQ
ALARM VOLUME
REAL TIME MEMORY 200 (FIG. 9)
FILTER SW
FLASHER (SYSTOLE)
63
RATE
072
84
AUDIO
(VISUAL) BRADY CARDIA
TACHY CARDIA
AUDIO
0 DELAY
0 5 SEC DELAY
QRS DETECTOR (FIG. 4)
40
TACHOMETER (FIG. 5)
20
ALARM 110 (FIG. 7)
FILTER AMPLIFIER
26
(DIAG MON)
GAIN CONTROL
(FIG. 3)
OPTICAL COUPLER ISOLATOR
SET
CANCEL
(FIG. 2)
LEAD SELECTION
AVR
AVF
AVL
V
3
2
1
14
12
ELECTRODE SET
10
PATIENT
HI LIMIT
LO LIMIT
FOR BOTH

FIG. 1

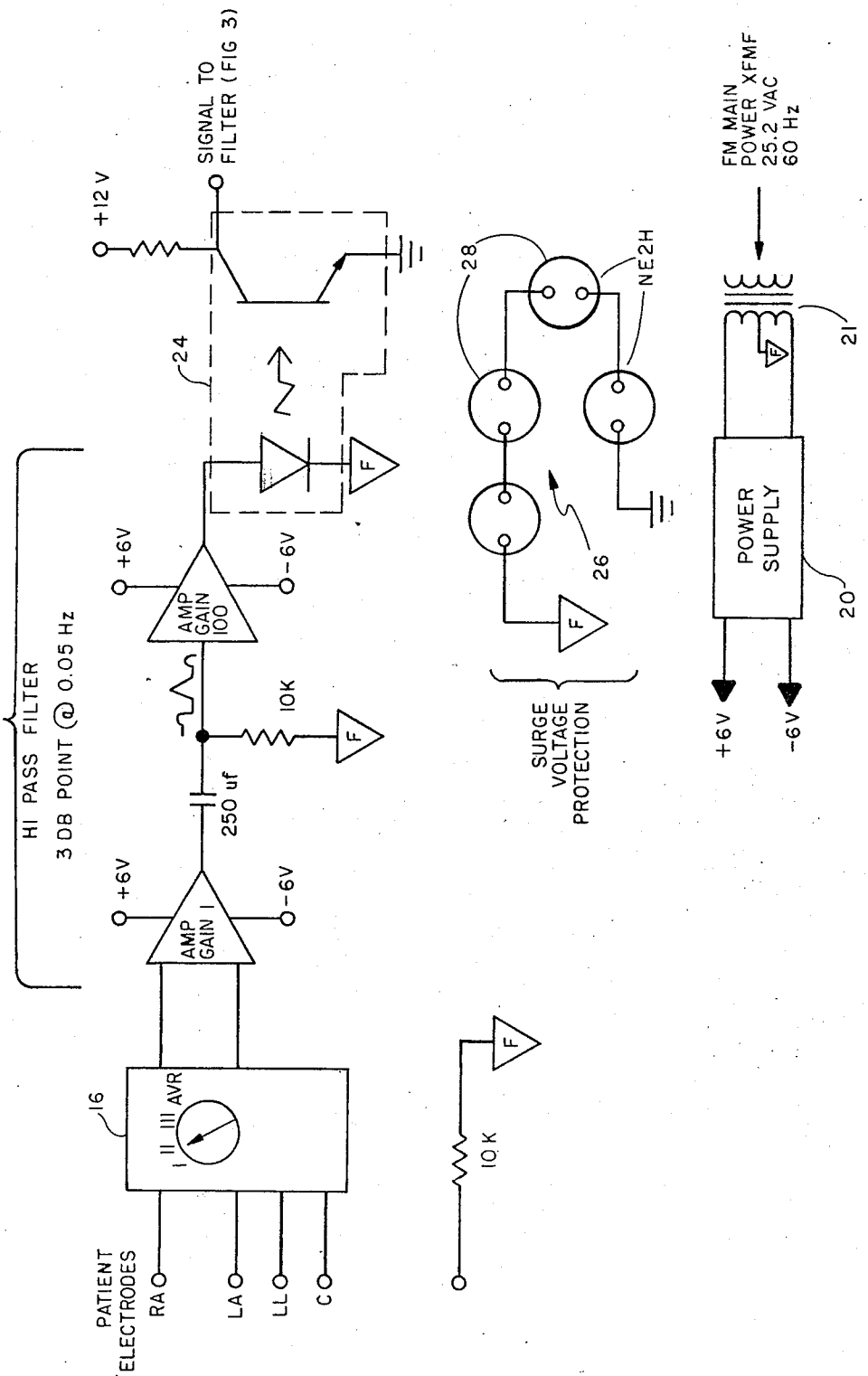

PATIENT ELECTRODES
RA
LA
LL
C
16
I II III AVR
AMP GAIN 1
AMP GAIN 100
HI PASS FILTER
3 DB POINT @ 0.05 Hz
+6V
-6V
250 uf
10K
F
+12 V
SIGNAL TO FILTER (FIG 3)
24
SURGE VOLTAGE PROTECTION
28
NE2H
26
FM MAIN POWER XFMF 25.2 VAC 60 Hz
21
POWER SUPPLY
20

FIG. 2

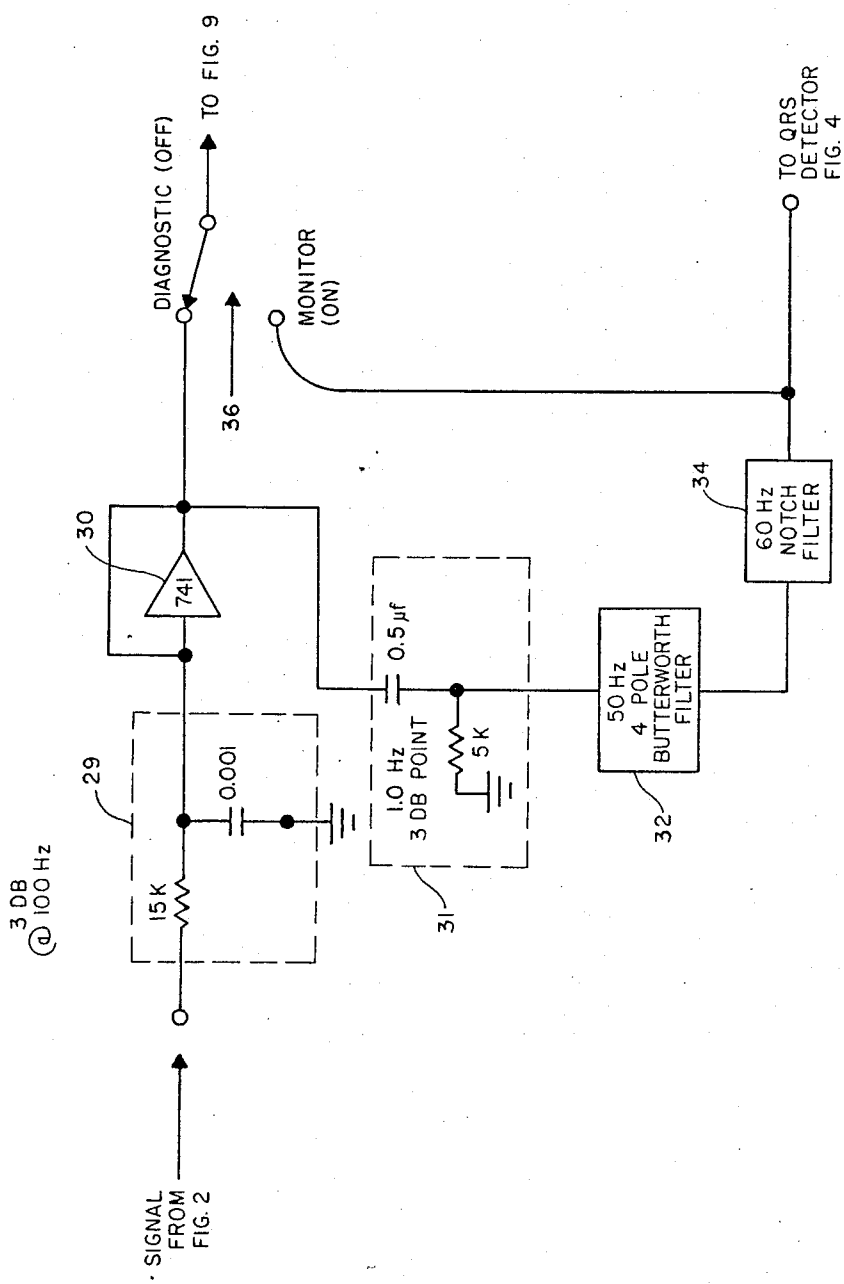

TO FIG. 9
DIAGNOSTIC (OFF)
MONITOR (ON)
36
TO QRS DETECTOR FIG. 4
30
741
34
60 Hz NOTCH FILTER
0.5 μf
1.0 Hz 3 DB POINT
5 K
50 Hz 4 POLE BUTTERWORTH FILTER
29
0.001
15 K
3 DB @ 100 Hz
31
32
SIGNAL FROM FIG. 2

FIG. 3

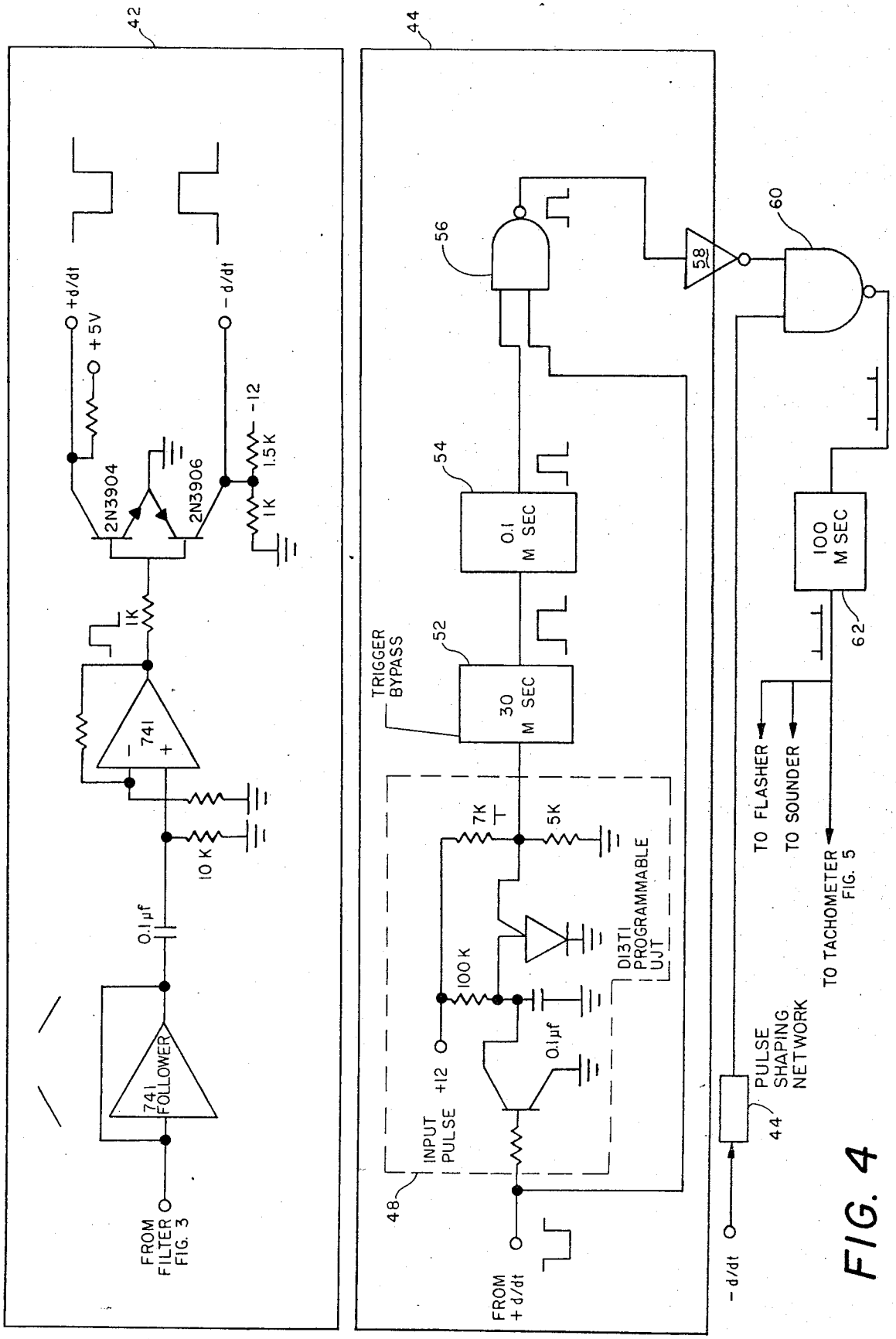

42
44
+d/dt
+5V
-d/dt
-12
2N3904
2N3906
1.5K
1K
1K
741
10K
0.1μf
741 FOLLOWER
FROM FILTER FIG. 3
56
58
60
54
0.1 M SEC
TRIGGER BYPASS
52
30 M SEC
100 M SEC
62
7K
5K
100K
0.1μf
DI3TI PROGRAMMABLE UJT
INPUT PULSE
+12
48
FROM +d/dt
-d/dt
PULSE SHAPING NETWORK
44
TO FLASHER
TO SOUNDER
TO TACHOMETER FIG. 5

FIG. 4

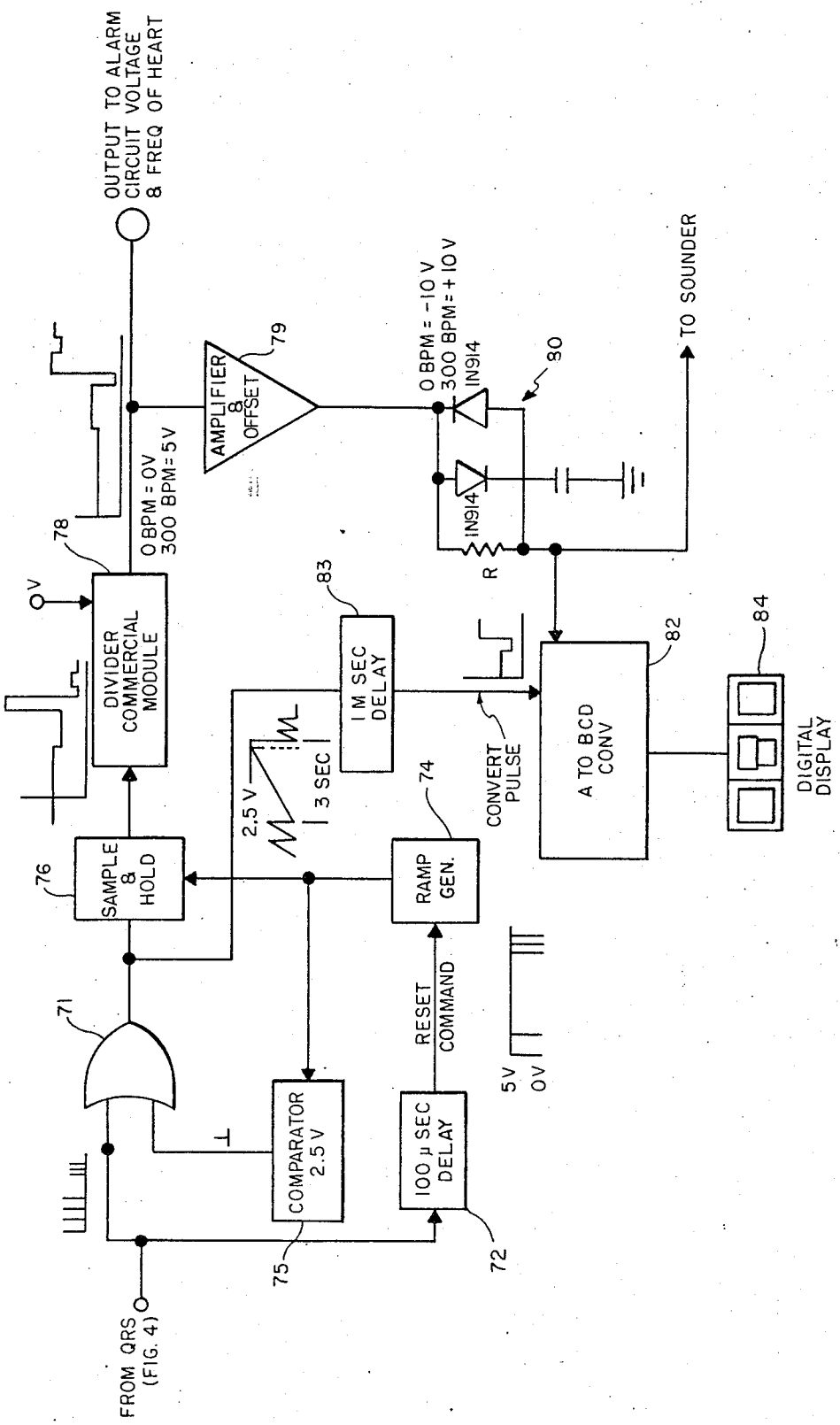

OUTPUT TO ALARM CIRCUIT VOLTAGE & FREQ OF HEART
AMPLIFIER & OFFSET
79
0 BPM = -10 V
300 BPM = +10 V
IN914
80
TO SOUNDER
IN914
R
0 BPM = 0V
300 BPM = 5V
78
0V
DIVIDER COMMERCIAL MODULE
83
1 M SEC DELAY
82
84
A TO BCD CONV
DIGITAL DISPLAY
CONVERT PULSE
2.5 V
3 SEC
74
RAMP GEN.
76
SAMPLE & HOLD
71
RESET COMMAND
5V
0V
COMPARATOR 2.5 V
100 μ SEC DELAY
75
72
FROM QRS (FIG. 4)

FIG. 5

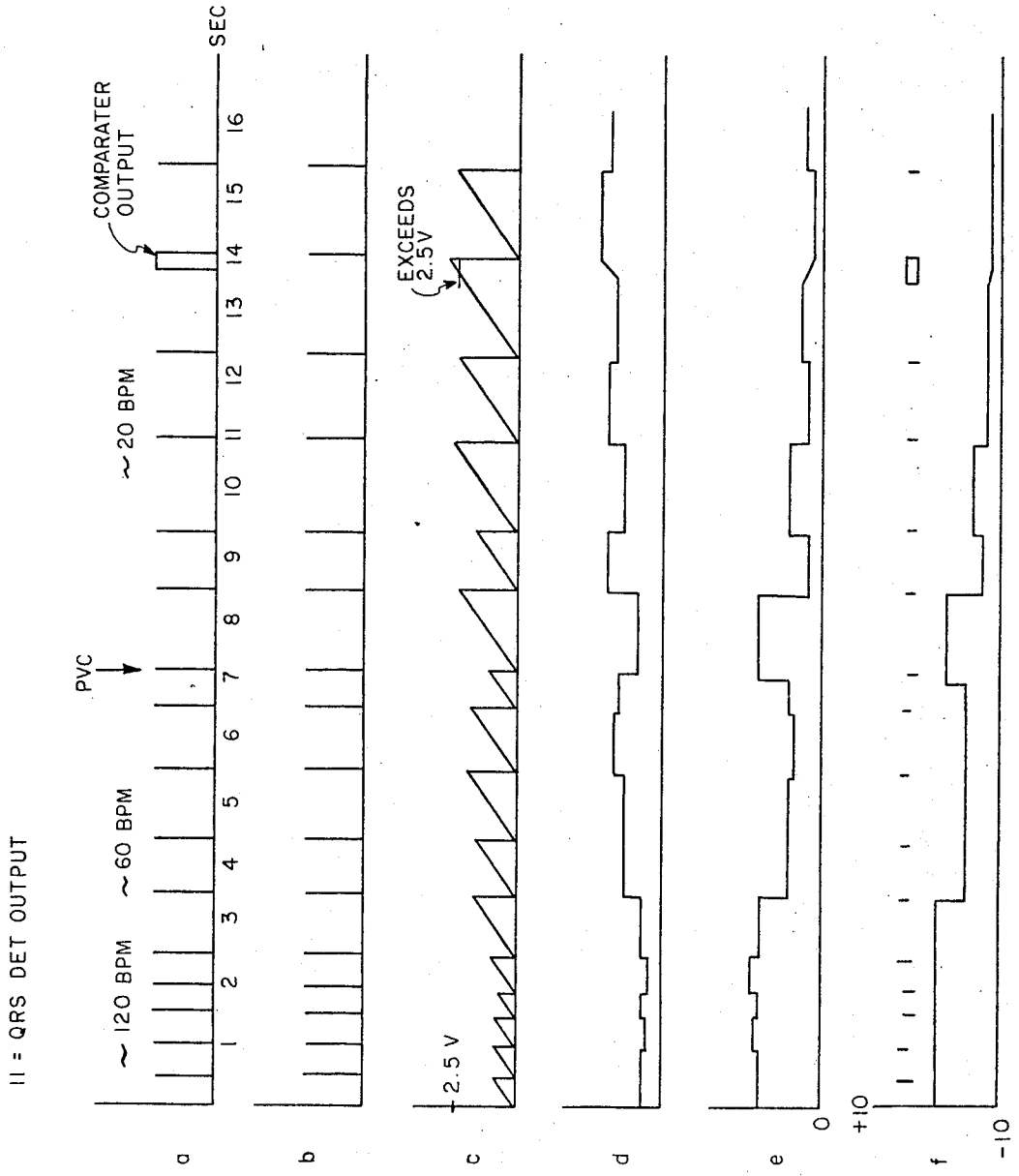

II = QRS DET OUTPUT
~120 BPM
~60 BPM
PVC
~20 BPM
COMPARATER OUTPUT
SEC
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
a
b
2.5 V
EXCEEDS 2.5V
c
d
0
e
+10
-10
f

FIG. 6

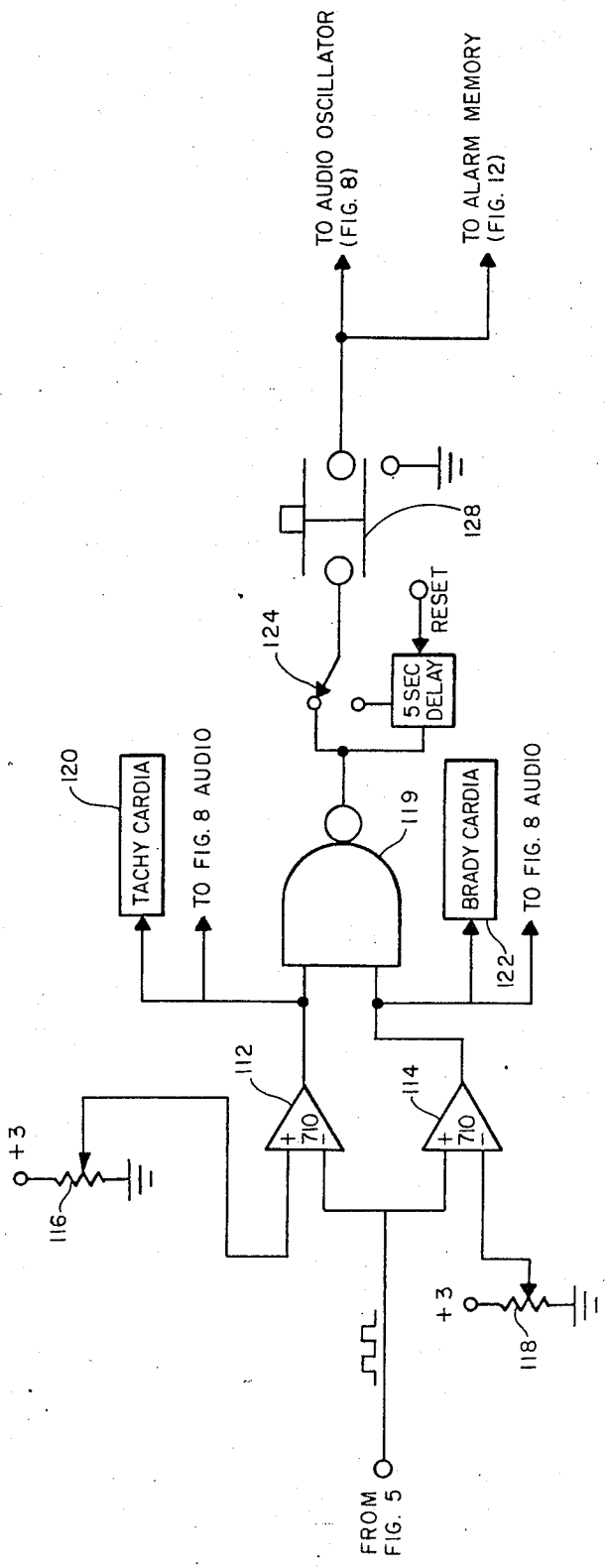

TO AUDIO OSCILLATOR (FIG. 8)
TO ALARM MEMORY (FIG. 12)
128
RESET
5 SEC DELAY
124
120
TACHY CARDIA
TO FIG. 8 AUDIO
119
BRADY CARDIA
TO FIG. 8 AUDIO
122
112
114
710
710
+3
116
+3
118
FROM FIG. 5

FIG. 7

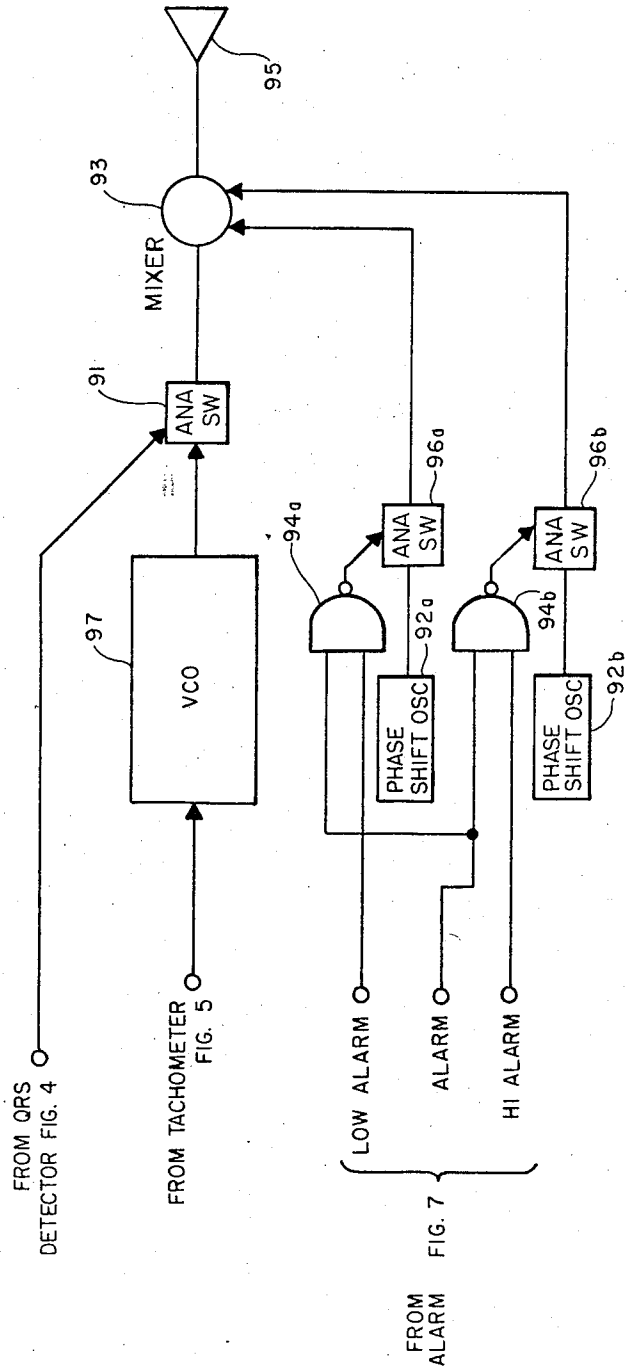

95
93
MIXER
91
ANA SW
97
VCO
94a
96a
ANA SW
92a
PHASE SHIFT OSC
94b
96b
ANA SW
92b
PHASE SHIFT OSC
FROM QRS DETECTOR FIG. 4
FROM TACHOMETER FIG. 5
LOW ALARM
ALARM
HI ALARM
FROM ALARM FIG. 7

FIG. 8

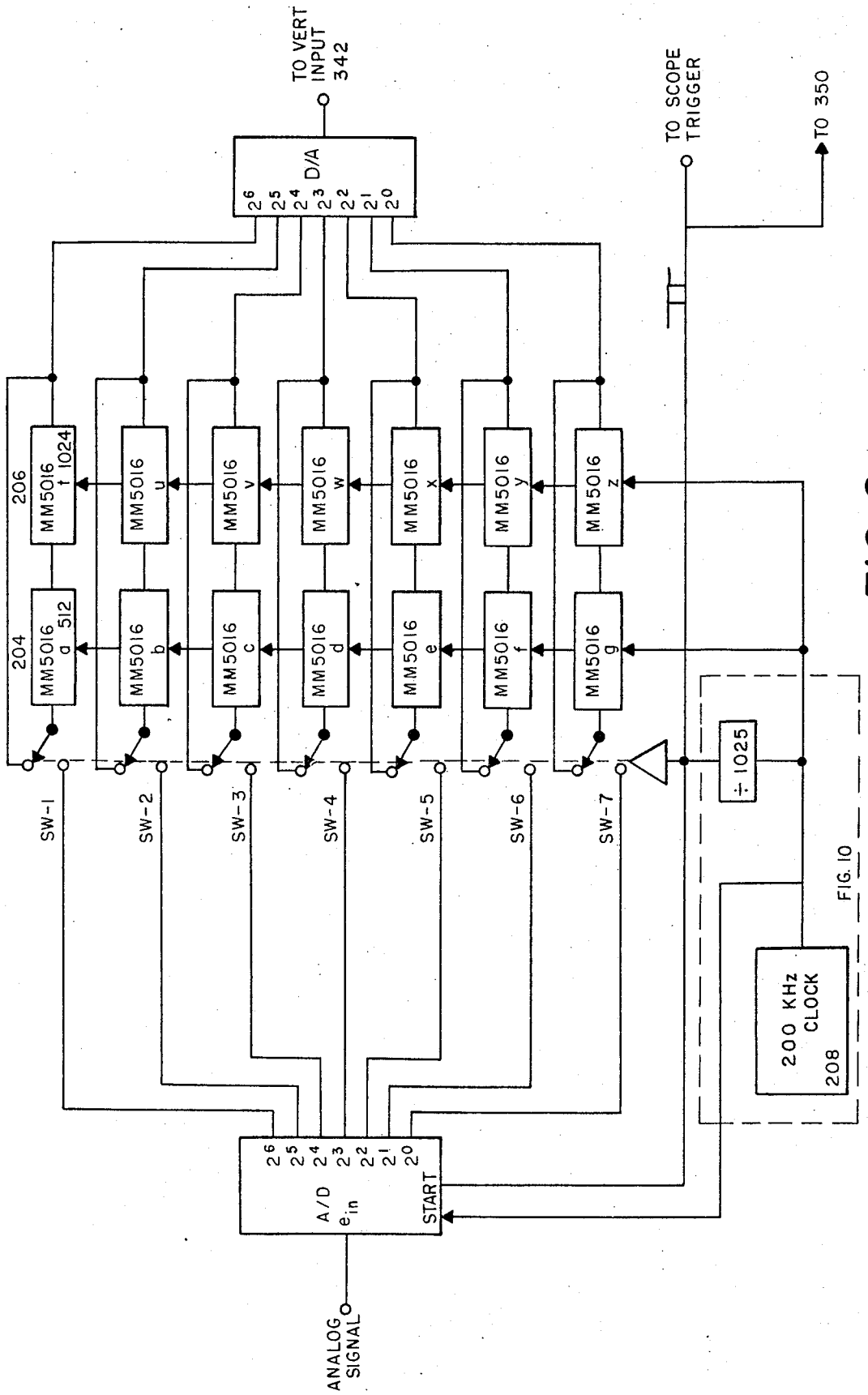

TO VERT INPUT 342
D/A
TO SCOPE TRIGGER
TO 350
206
204
MM5016 t 1024
MM5016 u
MM5016 v
MM5016 w
MM5016 x
MM5016 y
MM5016 z
MM5016 a 512
MM5016 b
MM5016 c
MM5016 d
MM5016 e
MM5016 f
MM5016 g
SW-1
SW-2
SW-3
SW-4
SW-5
SW-6
SW-7
÷ 1025
200 KHz CLOCK
208
FIG. 10
A/D
START
ANALOG SIGNAL

FIG. 9

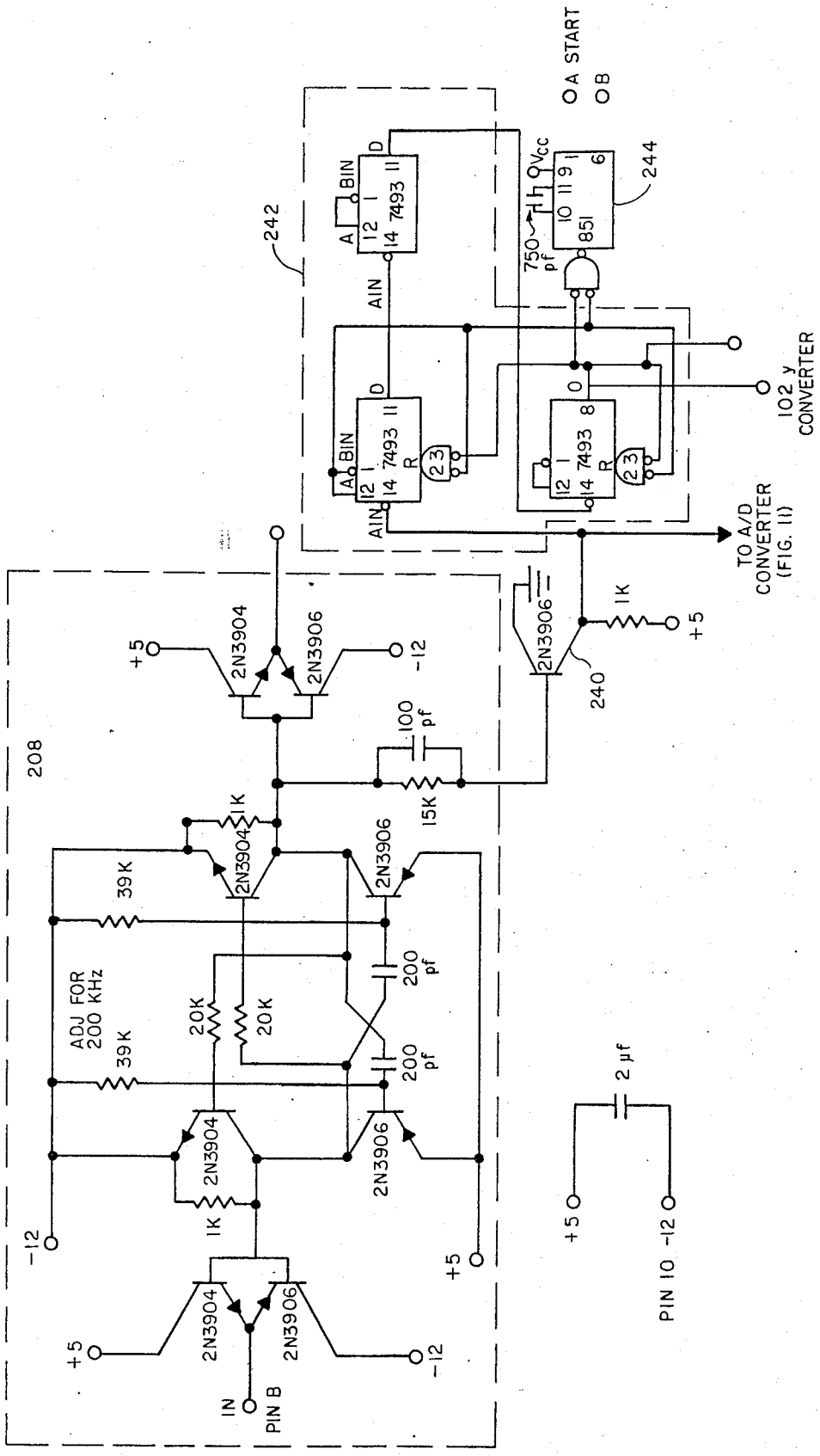

A START
B
242
BIN
AIN
7493
244
750 pf
Vcc
851
102 y CONVERTER
TO A/D CONVERTER (FIG. 11)
208
2N3904
2N3906
+5
-12
100 pf
15K
1K
240
39K
20K
200 pf
ADJ FOR 200 KHz
2 µf
PIN 10
IN
PIN B

FIG. 10

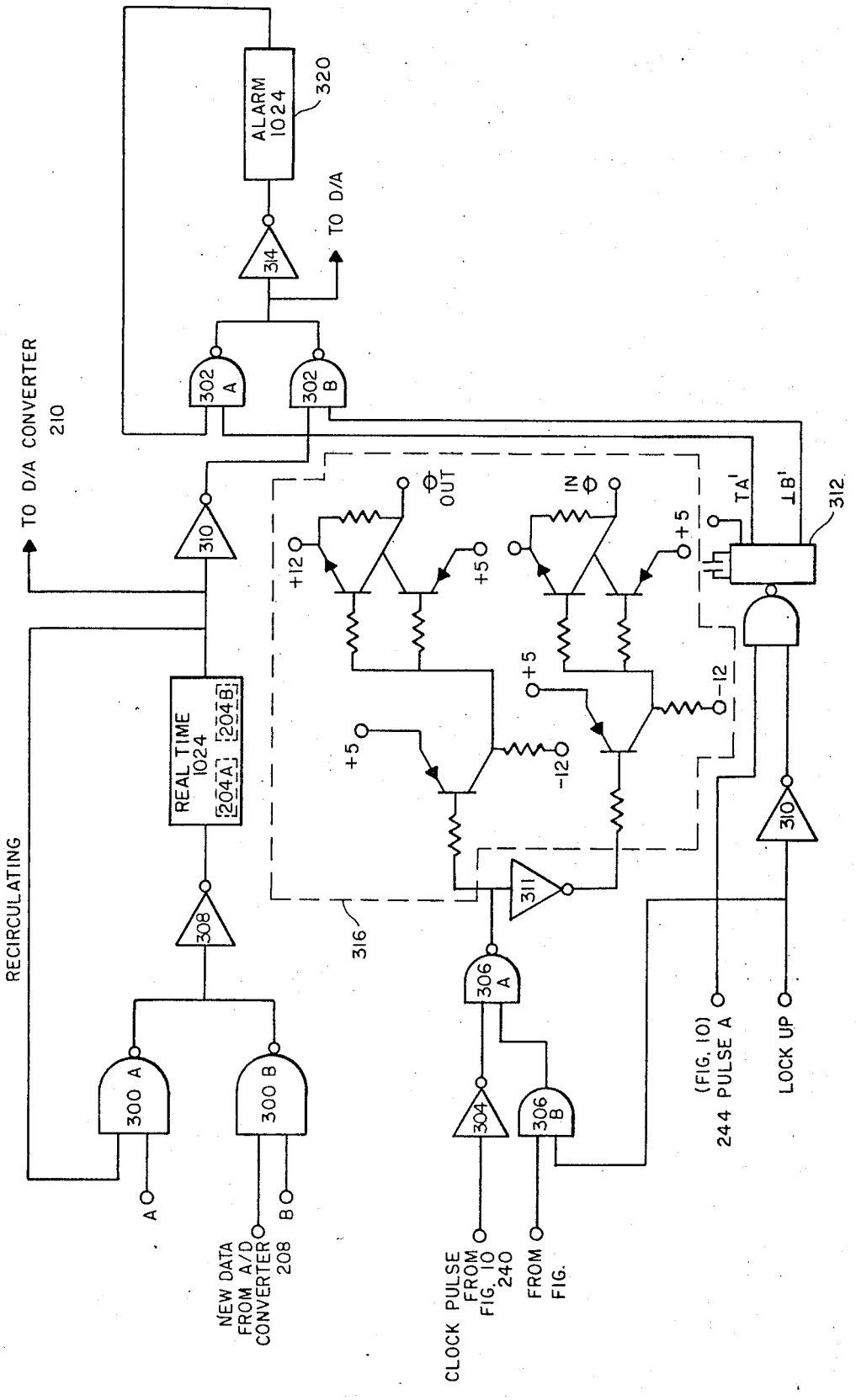

ALARM 1024
320
TO D/A
314
302 A
302 B
TO D/A CONVERTER 210
310
OUT
IN
+12
+5
+5
TA'
TB'
312
REAL TIME 1024
204A
204B
+5
-12
+5
-12
RECIRCULATING
308
311
316
306 A
310
300 A
300 B
304
306 B
(FIG. 10) 244 PULSE A
LOCK UP
A
B
NEW DATA FROM A/D CONVERTER 208
CLOCK PULSE FROM FIG. 10 240
FROM FIG.

FIG. 11

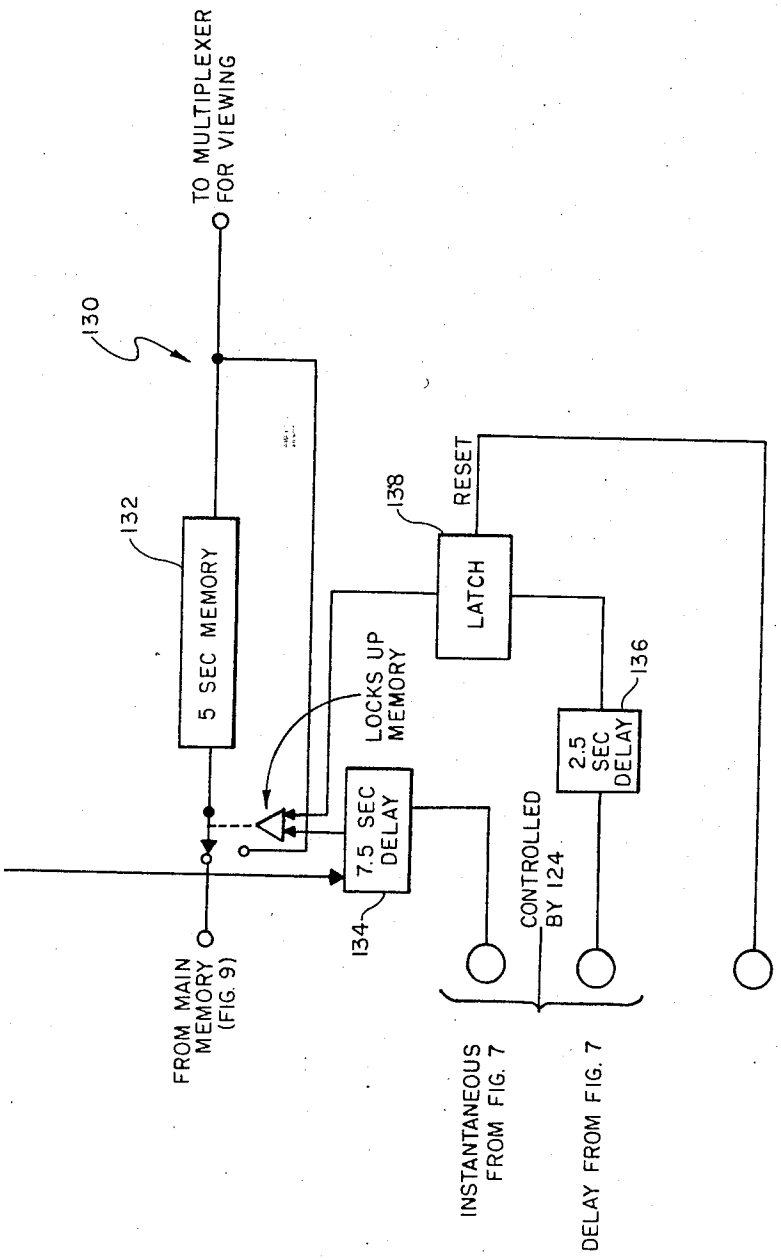

TO MULTIPLEXER FOR VIEWING
130
132
5 SEC MEMORY
LOCKS UP MEMORY
138
LATCH
RESET
136
2.5 SEC DELAY
7.5 SEC DELAY
134
CONTROLLED BY 124
FROM MAIN MEMORY (FIG. 9)
INSTANTANEOUS FROM FIG. 7
DELAY FROM FIG. 7

FIG. 12

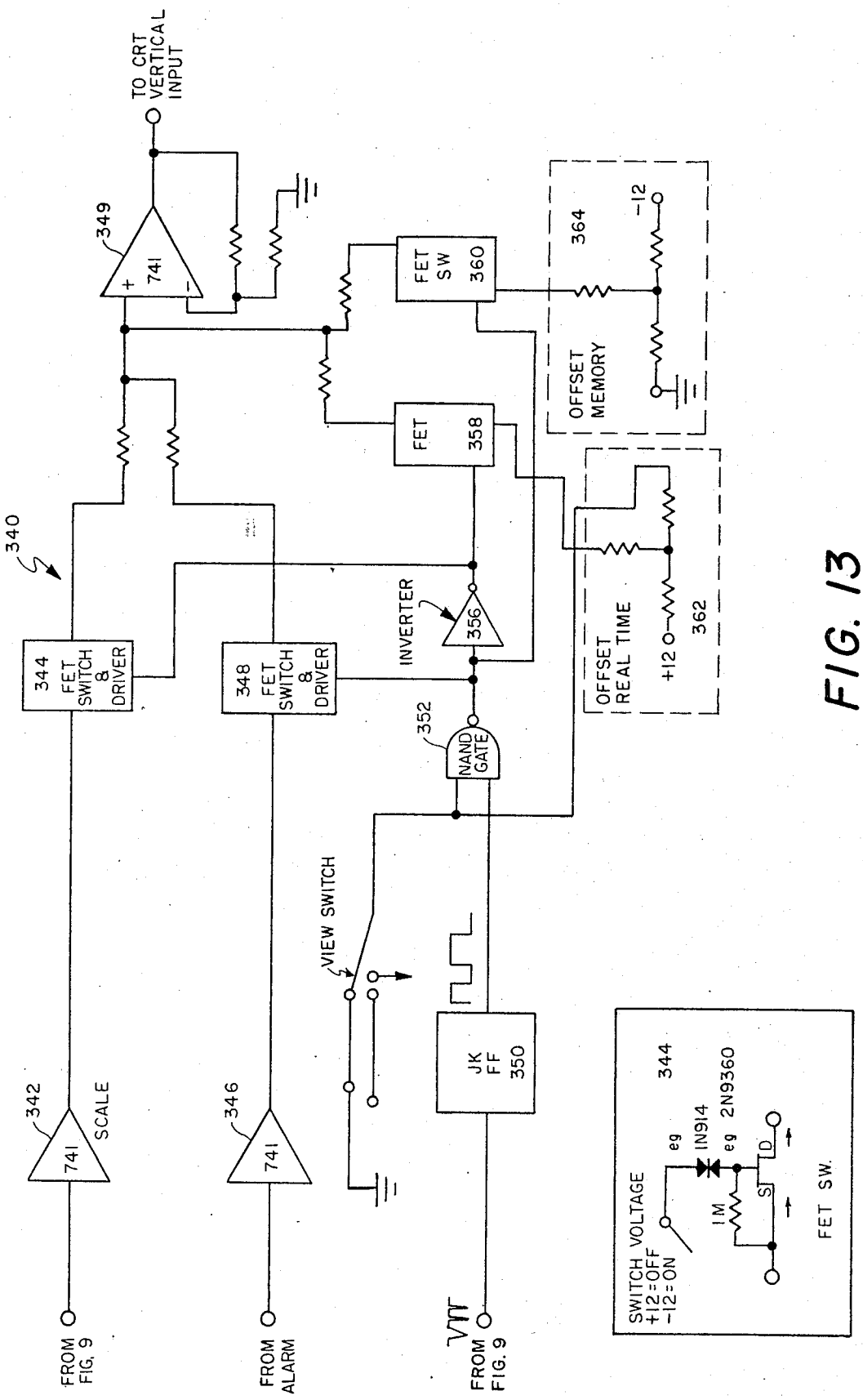

TO CRT VERTICAL INPUT
349
741
FET SW 360
FET 358
364
-12
OFFSET MEMORY
340
344 FET SWITCH & DRIVER
348 FET SWITCH & DRIVER
INVERTER
356
OFFSET REAL TIME
+12
362
352
NAND GATE
VIEW SWITCH
JK FF 350
342
741
SCALE
346
741
FROM FIG. 9
FROM ALARM
FROM FIG. 9
SWITCH VOLTAGE +12=OFF -12=ON
344
eg IN914
eg 2N9360
1M
S
D
FET SW.

FIG. 13

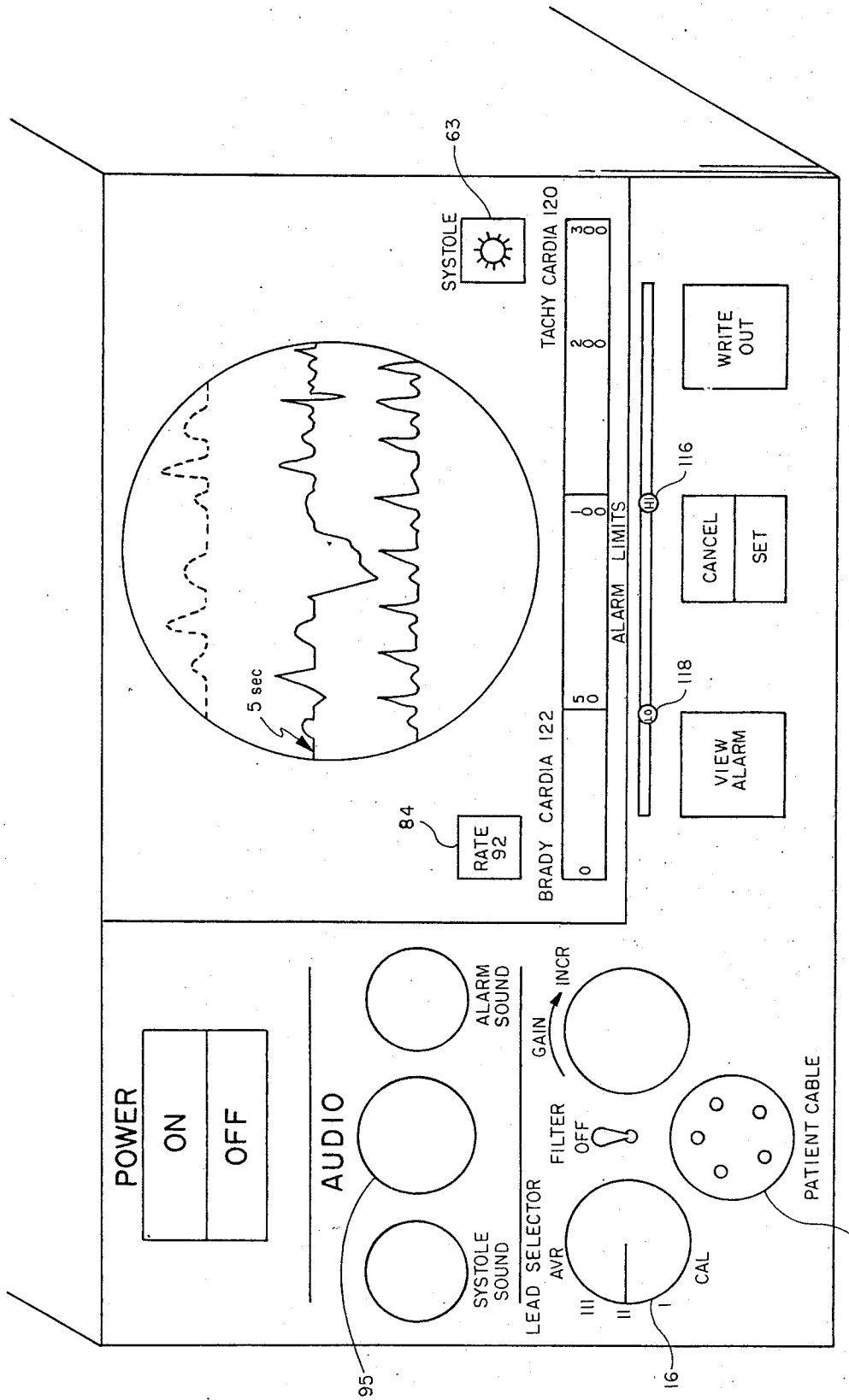

POWER
ON
OFF
AUDIO
ALARM SOUND
SYSTOLE SOUND
LEAD SELECTOR
AVR
III
II
I
CAL
FILTER
OFF
GAIN
INCR
PATIENT CABLE
15
16
95
84
RATE 92
5 sec
63
SYSTOLE
BRADY CARDIA 122
TACHY CARDIA 120
ALARM LIMITS
116
118
VIEW ALARM
CANCEL
SET
WRITE OUT

FIG. 14

REFRESHED CRT DISPLAY WITH ECG

BACKGROUND OF THE INVENTION

The cathode ray tube was commercially introduced into medical monitoring in the nineteen fiftys. The display produced consisted in writing the electrocardiogram across the screen of the tube. In this type of display a narrow beam of electrons is directed onto a phosphor coated screen. Electrons striking the screen at a particular location cause the phosphor at that location to glow. Diversion of the electron beam from that location will cause the glowing phosphor to fade out. Thus in the conventional display a bright spot is seen to move across the screen at 25 mm/sec. moving vertically in direct proportion to the electrical signals from the patient's heart. This type of display has remained essentially unchanged. It suffers from the fact that while the phosphor does continue to glow slightly after the electron beam passes over it, in the ambient light levels of today's hospitals, the display is far from optimal in terms of readability and recognition of arrythmias.

Recently, a new type of display has appeared. This is the "infinite persistence" type display. Within this type of display, the electrocardiogram signal information is preserved at full brilliance on the screen for some predetermined amount of time (usually 1 to 10 seconds), giving the operator a clear view of arrythmias. A number of approaches have been made in this area. Among these have been (a) direct display of the data on a commercial storage cathode ray tube, (b) temporary storage of the data on a delay line and display on a television raster system, and (c) digitization of the data, temporary storage in a central computer, and conventional sweep display. Each of the above systems suffers from very definite drawbacks. Display of the data on a storage CRT suffers from two shortcomings in that the life of the storage tube itself is limited as compared with conventional CRT's, and the data itself is "printed" across the screen. This means that information appearing on the right side of the screen is erased as soon as it appears, and only information presented on the left side of the screen remains in view long enough for verification of possible arrythmias. These defects are eliminated by the raster display system. In this method the signal is passed through an acoustic delay line and stored there temporarily. As new data is fed into the line, old data (4–8 seconds) is removed. Thus the most recent history of the patient's ECG is retained. This memory is continually scanned and presented on a vertical raster display. This type of display uses a standard long-life CRT. The data itself is "pulled" across the screen. New data appears on the right side of the screen and moves slowly leftward across the screen, disappearing at the left edge of the screen. Thus, a given ECG complex remains visible on the screen for several seconds after occurrence.

The raster display system currently available also has certain disadvantages. The display itself is composed of a series of dots and has a discontinuity which is particularly noticeable in the QRS complex. The only available system is in the form of a central Nurses' station display. This system accepts conventional signals from bedside monitors, creates the nonfading display, and presents it to the central Nurses' display. Optionally, the persistent display may appear also at the bedside.

This central processor concept allows for no failure margin. If the central delay line undergoes a major failure, the entire display system for up to four patients is affected.

The conventional swept display takes the data from the patient, converts it to a series of digital signals and stores it in a central computer. Like the raster display the data in memory is continually updated, and the data is "pulled" across the screen from right to left. Unlike the raster display, however, the data appears more continuous than segmented. The unit itself is once again central and a failure can affect up to eight patient displays both at the bedside and the Nurses' station, leaving the medical staff with no analog waveform display.

SUMMARY OF THE INVENTION

My invention embodies an apparatus and method for the storing of signals and eventual waveform display of the signals. The signals preferably are stored in at least two conditions, real time, and delay or alarm time. The real time signals are displayed in analog form on a recording medium. A waveform corresponding to the real time signal is analyzed to determine if it violates a preset condition or predetermined limits. If the limits are violated, then the stored alarm signals may then be displayed on the same or a different recording medium. Both the real time and alarm signals may be displayed on the same cathode ray tube, two different cathode ray tubes, on a cathode ray tube and an analog pen recorder, on two analog write-out devices, such as pen recorders, or in any other recording medium wherein the signals may be displayed in analog form, or may be sent in either analog or digital form to a computer for processing.

My invention is directed to an apparatus and method wherein the electrocardiogram signal (ECG) from the patient is stored in a memory and continually recycled and refreshed and displayed in analog form as a real time display. Preferably, new data appears on one side of a recording medium, such as a tube, and sweeps across the medium and is discharged a predetermined time later. All subsequent data follows the same pattern to provide a waveform which moves across the medium. The invention includes means to select an electrocardiogram signal, means to continuously display said signal, means to analyze the signal to determine if it falls within predetermined limits, means to store the signal as an alarm signal, and means to display the alarm signal.

More particularly, my invention is directed to a medical monitor for display of the electrocardiogram. Data from a patient is locally digitized, stored in a shift register, updated, and presented as a swept display. The patient is isolated from the monitor to eliminate fibrillation. A circuit analyzes a waveform corresponding to the ECG signal and determines if it violates certain limits. An alarm system is activated if the signal exceeds the established limits and the alarm condition is represented, visually and/or auditory. All of this is accomplished by a compact self-contained and independent monitor at the patient's bedside. In a group of eight (8) monitored patients, if a monitor fails only one patient's data is affected. The individual monitors can function without a central Nurses' station in the Emergency Ward, Operating Room, Cardiac Catheterization Laboratory, and as a mobile monitor in any part of the hospi-

tal. The invention includes the method of selecting an electrocardiogram signal, displaying continuously said signal for a predetermined time, analyzing said signal to determine if it falls within predetermined limits, storing the electrocardiogram signal as an alarm signal, and displaying said stored alarm signal as desired.

Briefly, certain features of the invention include a persistent or nonfading display, a totally floating input to assure patient isolation from the unit per se, a pattern recognition device for detection of the electrocardiogram signal to distinguish it from background noise, a digital display of the heartbeat updated on a beat-to-beat basis, and a time delay memory such as a five second auxiliary memory unit to freeze arrythmias or alarm conditions without disturbing the real time displays.

Signals from the patient are fed into an isolated front end wherein the selected electrocardiogram (ECG) signal is amplified and preferably filtered and optically coupled to the main frame of the instrument. The floating front end concept ensures that there is no electrical communication between the patient and the remainder of the system. This provides that in the event the patient is raised to some potential, such as by coming into contact with a source, there is no current path to ground through the patient and this prevents microshock. The front end is protected against defibrillation.

Once the signal has been transferred to the remainder of the system, it follows two paths.

To display the ECG signal, it is filtered to either a diagnostic or monitor band width depending upon the extent of analysis desired. After the signal has been filtered, it is amplified and then is fed into the display system. The signal passes to an analog-to-digital converter and is sampled a predetermined number of times, such as 200 times a second. Each time it is sampled a binary number, such as a seven digit binary number, is generated the value of which binary number corresponds to the amplitude of the sample. A plurality of these binary samples are stored in a real time shift register memory. Each time the ECG signal is sampled the binary number generated is entered into the memory displacing the number which represents the sample taken a predetermined sample time earlier. At the same time, the entire memory is being sampled at high speeds. The binary numbers are reconverted into the original signal and rapidly and repeatedly displayed on a cathode ray tube. In essence, the resultant display resembles an electronic analog pen recorder with the paper moving from right to left.

The second path which the signal follow is to a QRS waveform detector and then to a tachometer. The QRS detector itself is a pattern recognition device which detects the duration in time of the first excursion (be it plus or minus) taken in the QRS complex. The duration of this first excursion is approximately 10–40 milliseconds for both normal and infarcted hearts as nearly as has been determined. By allowing an appropriate window in time for the duration of this excursion, it can be extracted from background noise of similar amplitude. The tachometer includes a multiple beat rejection circuit which discards bogus beats caused by a patient motion. Such QRS appearing artifact is identified by the indication that it usually occurs in a salvo of rapidly successive peaks. This will not eliminate all artifactual beats but it is clearly an improvement over the present situation in commercially employed equipment. Once the beats are detected, the rate is obtained by inversion of the period between beats. This yields a continually updated rate. The rate is displayed digitally on the front panel of the instrument, and the rate voltage is sent to the alarm section of the unit.

In an alarm section of the unit, there are two comparators to compare the incoming rate voltage with high and low rate limits which are preset from the front panel. With the alarm enabled, violation of either limit will cause actuation of a signal, such as a buzzer, light, or both, each of which preferably correspond to the type of alarm detected; that is, exceedingly fast or slow heartbeat.

Another feature of the invention is an alarm memory in which data, preferably a predetermined time period old, such as five seconds, is continuously fed into the alarm memory. In the event of a violation of an alarm limit which is received on a delayed basis, this memory is sealed off. This captures the event causing the alarm, along with the data preceding and succeeding the alarm event. The information remains locked in this memory until the next alarm occurs unless cancelled or written out. The contents of the alarm memory may at any time be viewed by actuating a switch to display the alarm memory on the cathode ray tube which display preferably appears stationary and below the real time signal.

BREIF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of the total invention;

FIG. **2** is a partially schematic and partially circuit diagram of the flotaing front end;

FIG. **3** is a block diagram of the filter;

FIG. **4** is a circuit diagram of the QRS wave detector;

FIG. **5** is a partially block and partially circuit diagram of the tachometer;

FIG. **6** is an illustration of the waveforms occurring in the tachometer;

FIG. **7** is a circuit diagram of the alarm system;

FIG. **8** is a block diagram of the audio oscillator circuit;

FIG. **9** is a block diagram of the real time memory;

FIG. **10** is a partially circuit and partially block diagram of the timing board employed with the real time memory;

FIG. **11** is a circuit diagram of the interconnection between the real time memory and the alarm memory including the timing for the alarm memory;

FIG. **12** is a block diagram of the alarm memory;

FIG. **13** is a circuit diagram of the multiplexer; and

FIG. **14** is a schematic illustration of the front panel of the instrument.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The instrument is shown generally in FIG. **1** wherein a patient is shown at **10** and connected with the three-standard-limb leads or Eindhoven Triangle with additional sternal and/or auxiliary leads which communicate with a patient cable **12** which plugs into a patient cable jack **15** on the front panel of the instrument as shown in FIG. **14.** The floating front end **14** is optically coupled to a filter-amplifier **26** shown in greater detail in FIG. **3.** The signal is filtered and then is directed to a real time memory **200** shown in greater detail in FIG. **9,** then to the multiplexer **340** shown in greater detail in FIG. **13,** and then to the oscillograph of the cathod

ray tube **230.** The signal is also sent to the QRS detector **40** shown in FIG. **4,** the tachometer **70** shown in FIG. **5,** and the digital display **84.** The signal from the tachometer is in communication with the alarm system **110** shown in FIG. **7;** and if an alarm is actuated, it communicates with the alarm memory system **130** shown in FIG. **12.**

FLOATING FRONT END

Referring to FIG. **2,** the signal from the patient is selected by actuation of the multiple lead selection switch **16** which is also shown in FIG. **14** of the front panel of the instrument and may select any of various wet or dry electrode combinations from among the possible right arm (RA), left arm (LA), left leg (LL), and chest (C) combinations. The switch **16** as shown in FIG. **2** is in the **2** position to the RA-LL combination. The lead selection switch may also select a one millivolt calibration signal. Once the switch has selected the combinations of electrodes which will be chosen for display, the signal is amplified and filtered at **18** and optially communicated to the filter-amplifier of FIG. **3** by the optical coupler **24,** such as a Monsanto Optical Isolator MCT–**2.**

The power supply **20** for the floating front end is a standard configuration zener regulated power supply. The grounds to the floating front end are identified as ▽F.

The supply **20** is coupled to a main power transformer (not shown) of the instrument which is actuated by the OFF-ON switch on the front panel. This communication is by a low capacitance 60 HZ power transformer **21,** such as by a Stevens-Arnold isolation coupling No. IT–3408. To prevent a power surge a circuit **26** having neon tubes **28** (NE2H) is employed. When the voltage across them is less than 280 volts, the tubes form an open circuit. If voltage is 280 or greater, then the circuit **26** will act as a short circuit. With the tubes in the open circuit mode, there is no direct electrical communication between the patient and the main power ground of the instrument as shown.

Once the signal has been transferred to the remainder of the system, it will eventually go to the oscillograph of the cathode ray tube and also to the pattern recognition devices, the digital display, and the auxiliary alarm components as required.

FILTER-AMPLIFIER

The signal from the front end **14** of FIG. **2** is filtered as shown in FIG. **3.** As mentioned in the discussion of FIG. **2,** the signal through floating front end is initially filtered at the lower 3 DB point at 0.05 HZ. With the switch **36** on the diagnostic position, the signal is filtered at **29** with the upper 3 DB point at 100 HZ. The signal is amplified at gain adjust **30** and then goes to the real time memory of FIG. **9.** Accordingly, when the switch **36** is on diagnostic, the signal will be filtered at the 3DB point with the upper limit at 100 HZ and the lower point at 0.05 HZ. After passing through filter **29,** the signal then flows through gain adjust **30** wherein the signal may be amplified from 1 to 20 and then through switch **36.**

As shown in FIG. **3,** the signals to the QRS detector of FIG. **4** are always between the 1.0 and 40 HZ levels. It should be noted that the filter diagnostic settings correspond with the specifications of the American Heart Association for analog ECG data to be recorded.

QRS DETECTOR

Referring to FIG. **4,** the QRS detector **40,** a signal as shown enters the wave-shaping network shown at **42.** The wave-shaping network is capable of producing two pulses whose waveforms are shown as +d/dt and −d/dt. The +d/dt and −d/dt pulses are then transmitted to circuit **44** which circuit produces a pulse corresponding in duration to ramp signals with slew rates in excess of +50 V per second or −50 V per second. Thus, the signal from the wave-shaping network **42** goes directly to gate **56** and into matching network **48.**

The duration of the first linear rise or fall of the signal is approximately 10–40 milliseconds for both normal and infarcted hearts as nearly as has been determined. By allowing an appropriate window in time for the duration of this slope, such as from 10 to 40 milliseconds, it can be extracted from background noise of similar amplitude. Thus, a pattern recognition device for detection of the electrocardiographic signal is provided to distinguish it from background noise. When the pulse enters the compare network **48,** an input pulse is entered into the network to determine whether or not the pulse received from the wave-shape network has a duration of at least 10 milliseconds. If the pulse received meets the minimum threshold level, 10 milliseconds, then a new pulse is generated by the network **48** which triggers the monostable multivibrator **52** which generates a new pulse of 30 milliseconds. This pulse in turn triggers the next monostable multivibrator **54** to generate a pulse of 0.1 milliseconds which is input to gate **56.**

If the pulse from the wave-shaping network **42** which was transmitted directly to gate **56** ends prior to the pulse being received from the multivibrator **54,** then in this condition gate **56** will be triggered to send a pulse to gate **60** when the pulse is received from the multivibrator. If the pulse from the multivibrator **54** is received by gate **56** prior to the end of the pulse directly from the waveforming network. then gate **56** will not be triggered and no pulse will be sent to gate **60.** Therefore, if the pulse entering the compare network **48** is less than 10 milliseconds, no pulse will be received from the multivibrator **54** by gate **56** and thus gate **56** will not be actuated under any condition. If the pulse as compared is 10 milliseconds or more, then the multivibrator will transmit a pulse to gate **56.** In order for the gate **56** to trigger a pulse to gate **60,** the signal received by gate **56** directly from the pulse-shaping network must end prior to receiving the pulse from the multivibrator; that is, it must be 40 milliseconds or less. Thus, it is seen that if duration of the pulse initially received does not fall within the predetermined window or between 10 to 40 milliseconds, no further signal will be transmitted.

A similar pulse-shaping network, such as **44,** to analyze and compare the −d/dt waveform has not been shown but functions in the same manner as the circuit **44** and feeds its input to gate **60.** If the pulses from network **42** are between the limits set, then they will normally be received in quick succession by gate **60.** In any event, even if they vary be a few milliseconds, any pulse received by gate **60** on either input will generate a pulse to trigger the nonretriggerable 100 millisecond delay **62.**

Once the nonretriggerable delay has been actuated upon receipt of a pulse from gate **60,** a pulse is generated shown as the QRS output to tachometer in FIG. **5.**

No new pulses will be generated for 100 milliseconds. This prevents bogus signals from being generated caused by possible overlapping of the signals from the gates.

The pulse is also sent to flasher **63** shown on FIGS. **1** and **12**, and to the audio oscillator as will be descirbed in more detail in the description of FIG. **8**. The flasher systole **63** is simply a light emitting diode, such as a Monsanto MV50, actuated upon receipt of a signal from the multivibrator **62**. Any suitable visual indicator may be employed.

TACHOMETER

Referring to FIG. **5**, the pulses from the QRS detector of FIG. **4** enter the tachometer; specifically, the pulse enters the "OR" gate **71** then to the sample and hold circuit **76** and the delay circuit **72**, which triggers the ramp generator **74**.

The pulse shapes are shown in FIG. **6** divided into three sections, 120 beats per minute (BPM), 60 BPM, and 20 BPM. Also shown in the 20 BPM section is the comparator output. Sample command from the gate **71** is shown as line a, the 100 microsecond delay pulse is shown as line *b*, the signal from the ramp generator is shown as line *c*, the sample and hold circuit output as line *d*, the divider output as line *e*, and smoothing circuit output as line *f*. As indicated, the sample and hold circuit selects that value of the slope from ramp generator **74** and provides and holds the waveform or voltage proportional to the period between pulses as shown in line **6***d*. Each time a pulse is received from the QRS detector, the ramp generator **74** is reset to zero by the 100 microsecond delay circuit **72**. If no pulse is received from the QRS detector within the time period corresponding to the time it takes the ramp generator to reach a threshold value of 2.5 volts as determined by the comparator **74**, the ramp generator will provide a signal to gate **71** to trigger a pulse corresponding in time to the 2.5 volt value, the sample and hold circuit thus generating a new waveform. The preset 2.5 volt value of the comparator corresponds to a heart rate of 20 beats/min. or approximately 3 seconds between beats. This is also shown in FIG. **6**.

The pulse from the sample and hold circuit is received by the analog divider **78**, wherein a one volt input at *b* provides the numerator for the division and the sample and hold output provides the denominator. The signal from the analog divider **78** is a voltage proportional to the frequency of the pulses. The output of the analog divider ranges from 0 V for 0 BPM to 5 V for 300 BPM. This signal is received by an amplifier and offset circuit **79** wherein the 0 to 300 BPM voltage range is changed to ±10 volts. From amplifier **79** the signal enters smoothing circuit **80** which is designed to prevent the transmission of any further signals to the analog to BCD converter unless they exceed certain limits. As shown, a short term change in BPM of ±11 or less, (±0.7 V) will not be reflected on the digital display **84**. Thus, the smoothing circuit **80** prevents flicker. The one millisecond delay circuit **83** prevents entry of any signals into the converter **82** until the other components of this circuit have stabilized, particularly the sample and hold and ramp generator circuits. The converter **82** includes a gate which will transmit information to the display when signals are received from both the delay circuit **83** and the smoothing circuit **80**.

ALARM

Referring now to FIG. **7**, the alarm circuit is shown generally at **110** and receives a signal from the tachometer described in FIG. **5** which signal corresponds to the rate voltage sent to the digital display **84**. Comparators **112** and **114** are preset through variable resistors **116** and **118** to determine the high and low limits of the rate voltage which should not be violated, such as a high limit of approximately 2 volts corresponding to 120 BPM and a low limit of approximately 0.6 volts corresponding to 40 BPM. The incoming signal from the tachometer is analyzed in the comparators. If neither condition is violated, no alarm signal is generated by gate **119**. Violation of either limit will provide a signal and as shown will (a) actuate the front panel lamp, such as a MV–50, either tachycardia **120** or the bradycardia **122** depending upon whether the upper or lower limit has been violated; (b) provide an audio signal, high or low, transmitted to the audio oscillator of FIG. **8**; (c) transmit a further signal to the audio oscillator of FIG. **8**; and (d) transmit a signal to the alarm memory of FIG. **12**.

Two switches are shown, an alarm set-reset switch **128** and an alarm response switch **124**, which includes a five second delay latch circuit **126**. When in the normal position, switch **124** allows the signal to be transmitted instantaneously to the audio oscillator and the alarm memory. When actuated, the alarm response switch **124** will delay the alarm signal for five seconds by engaging the latch circuit **126**.

Since it is possible for the unit to receive abberrant beats, this capability of selecting a five second delay to the alarm system is provided. If the alarm condition persists for five seconds, then the instrument will generate an alarm, but not before. The five second delay circuit may then be reset after the alarm condition has been checked through the switch **128** which also cancels the signal to the audio oscillator of FIG. **8**. In instantaneous mode the alarm is reset automatically when the alarm condition ceases.

AUDIO OSCILLATOR

Referring to FIG. **8**, a block diagram of the audio oscillator is shown wherein a QRS detector input line is shown receiving the signals from FIG. **4** which flow directly to an analog switch **91**. From the switch they go to the mixer **92** where they are amplified through the speaker **95**. The signals from the QRS detector provide the actual impetus for the sound corresponding to the heartbeat. A voltage controlled oscillator (VCO) systole sound is shown at **97** and receives a signal from the smoothing circuit of the tachometer of FIG. **5**. This determines the frequency or the pitch at which the signal received from the QRS detector output will be heard. The alarm circuit pulses are received from low alarm, high alarm, and from the gate **119**. A signal from high alarm will be transmitted to gate **94***b*. If a signal if received from gate **119** of FIG. **7**, then the gate will actuate analog switch **96***b* which receives the characteristic sound from the phase shift oscillator **92***b*. The signal goes to the mixer **93** and then to the speaker **95** also shown on the front panel. The mixer is of the type which is adapted to receive and pass all signals simultaneously, as is well known in the art. It serves no other function than to allow the various signals to pass through a common point to the speaker **95**. The VCO

97 may be adjusted to vary the volume of the systole sound to give an indication of the heartbeat, and the phase shift oscillators may also be adjusted to change the level of sound of the high and low alarms. These are shown on the front panel.

REAL TIME MEMORY

Referring to FIG. **9**, the real time memory is shown generally at **200**. The analog signal from FIG. **3** is received by the analog-to-digital converter where the analog is sampled and digitized each time a start pulse occurs, as will be explained later. As shown, this is 200 times per second. the a/d converter is of a standard downcounter design. The output of the a/d conversion is a 7 bit binary signal. Shift registers **204***a–g*, **206***t–z*, are each 512 bits long, and each have a binary input and a two phase clock input together with memory cells as with all commercially available shift registers, such as National Semiconductor MM5016. The clock input of the shift registers receives a continuous series of pulses at the rate of 204.8 KHZ/sec. from the clock **208.** The digital signal appearing at the input of the registers will appear at the output of the registers after one-two-hundredth seconds or 1024 clock times. As shown, the output of the shift registers, for example shift registers **204***a* and **206***t* . . . **204***g* and **206***z*, are wired back to the inputs and data is continually passed back through the registers or recirculated. Switches SW–1 through SW–7 with continual clock pulses to the 1024 bit registers from the clock operate with the following cycles synchronized to the clock. For 1024 clock times, recirculation takes place, then for 1 clock time new data from the a/d converter **202** is entered into the register and the register and the cycle repeats. The result of this operation is that the registers are continually being updated with new information at the rate of 200 pieces of data per second. The output of the register is fed to a continuous d/a converter which produces an analog voltage from the 7 bit register **210.**

The two phase clock **208,** shown in greater detail in FIG. **10,** provides two modes of operation during a clock time. The modes are respectively to read data and then shift data. On the read mode of the first clock pulse the data from the a/d converter is read or examined, and on the shift mode of the first clock pulse the data is entered into the first position of the register **204***a*. On the second clock time, the read pulse, new data is entered into the first position of the shift register while the old data shifts to the second position of the shift register. This continues on until completion of the 1024 clock time. On the 1025 clock time the original data is reentered into position **1.** At the end of the 1025 time, the switch SW–1 is actuated to allow entry of new data. At the end of 1026 pulses or the first pulse of the second cycle, the original data is in position **2** and the new data is now in position **1.**

Stated another way, referring specifically to registers **204***a* and **206***t*, which in series make up a 1024 bit register, a piece of data entering register **204***a* in the first position at time 0 will at time 1023 be in the 1024 position of shift register **206***t*. During clock time 1025 this bit of information will have been recirculated and entered shift register **204***a* in the second position of the 1024 positions available. At clock time 1025, switch SW–1 is actuated and new data is introduced into the first position of shift register **204***a* with the old data now in the second position of shift register **204***a*. With the 1025 clock times later the data in positions **1** and **2** will have recirculated through shift registers **204***a* and **206***t* and will have entered the second and third positions of shift register **204***a*. At clock time 2050 switch SW–1 is actuated and new data is entered into the first position of shift register **204***a*. From the above values it is seen that in approximately five seconds the first bit of information entered into the first position of register **204***a* will have recirculated approximately 1,024 times and be in the 1024th position of shift register **206***t*. The same sequence is followed for shift registers **204***b–g* and **206***u–z*.

Referring to FIG. **10,** the two phase clock is shown generally at **208.** The circuit generates complementary pulses, ϕ in and ϕ out. These voltages are alternately emitted at +5 (and when not at a voltage of +5, they are at a voltage of −12). As described above, these pulses are transmitted to the shift registers and correspond to the read pulse and shift pulse for each clock time. When the shift pulse goes to the shift registers, it also enters the level shifter shown at **240.** This level shifter allows the 5 volt output to alternate between +5 and 0 volts. The output from the level shifter **240** goes to the a/d converter shown in FIG. **9,** to the divide by 1025 circuit or register **242,** and to gate **306***b* of FIG. **11.** This circuit **242** is comprised of three divide by **16** counters **480***a, b,* and *c*. During clock time 1, the register reads zero. During clock time 2, the register reads one. During clock time 3, the register reads two, etc., until during clock time 1025, the register reads 1024. At the end of clock time 1025, the register reverts to the zero state. When the register reverts to zero, a signal is gated to pulse generator **244** which which actuates switches SW–1 to SW–7 to allow for the entry of new data into the shift registers. As shown the pulse generator has two outputs A and B. During clock times 1–1025 the output from A allows recirculation of data and the output from B inhibits entry of new data. When the signal is gated to the pulse generator **244,** the outputs of A and B are reversed.

Referring to FIG. **11,** the switching and command mechanism for the real time memory is shown in FIG. **11** for shift registers **204***a* and **206***t*, it being understood that similar command and switching mechanisms are duplicated for the remaining shift registers. The switching and command and the timing for the alarm memory are also shown. Gates **300***a* and **300***b* are synchronized with the clock times and upon completion the 1025 clock time, new data is entered into the first position of the **204***a* register and at the same time this new data is transmitted to the digital-to-analog converter **210** of FIG. **9.** This condition occurs when the input to the **300***a* gate is 0 and the input to the **300***b* gate is 1. These inputs are 0 from A and 1 from B of the pulse generator **244.** On the 1024 clock times, the input to the gate **300***a* is **1** and the input to the gate **300***b* is 0. This prevents the transmission of new data to the registers and allows recirculation of the present data to the shift registers. When the new data is accepted at the end of the 1025 clock times, the old data leaving the 1024 position of register 206*t*, goes to inverter **310,** then to gate **302***b* and to D/A **210.**

The alarm memory **320** comprises the same number of shift registers and of the same characteristics as of the real time memory **200.** Thus, the data which is five seconds old is entered into the alarm memory **320.** This five second old data is recycled in the same manner as

the new data which enters the real time memory **200.** New five second old data discharged from the real time memory **200** is entered into the alarm memory every 1025 clock times.

Shown in dotted lines is a two-phase clock **316** similar to clock **208** in that it provides θ in and θ out pulses for the alarm memory. The input to inverter **304** is from the level shifter **240** of FIG. **10.** The two inputs to pulse generator **312** are from the alarm circuit and from the divide circuit **242** of FIG. **10.** The input to pulse generator is from inverter **310** and from the pulse generator **244** of FIG. **10.** The pulse generator provides two outputs A' and B' to gates **302***a* and **302***b*. For 1024 clock times recirculation in the alarm memory takes place and for 1025 clock times new data from the real time memory is entered.

When an alarm signal is entered into the gate **306***b* and inverter **310,** the clock **316** provides the two-phase read and shift modes for the register of the alarm memory and **1024** clock pulses per cycle. Pulse generator **312** is inhibited and the values of A' and B' are held at +5 volts and 0 volts respectively whereby gate **302***b* is inhibited from allowing new data to enter the alarm memory and in essence isolates the alarm memory.

This condition remains until a view button is actuated at which time the information in the alarm memory will be displayed. The introduction of information from the alarm system does not affect the real time memory and that information is continuously displayed on the cathode ray tube.

Thus, it is seen that the data in the registers is read and displayed at each time (t) new data is entered. The data is displayed each time (t) while it moves up in position in the registers, the position in the registers corresponding to the position on the screen. The data will be displayed for a time $t.n$ where n is the total times (t) it takes for the data to move from position **1** to 1024. This time n may vary depending upon the shift register used, i.e. the number of positions desired. That is, a time greater than or less than five seconds may be employed, say for example four seconds or six seconds.

In the preferred embodiment the five second old data from the real time memory is transferred to the alarm memory with an age of $t.n$ recirculated n^a times (where n^a equals the total time (t) it takes for the data to move from position 1 to 1024 in the alarm memory) which in the example equals n and is discarded at time $t.n^1$. Of course, the duration of recirculation in the alarm memory may vary and the transfer from the real time memory to the alarm memory may occur prior to the time $t.n$ of the real time recirculation, at time $t.n$ as in the example or subsequent to time $t{\cdot}n$. Further, the total time to enter and be discarded from the register n^a may also vary.

ALARM MEMORY

Referring to FIG. **12,** the alarm memory is shown generally at **130** and includes a five second memory **132** into which memory data, which is five seconds old, is continuously loaded therein from the real time memory of FIG. **9**; and when the data becomes ten seconds old, it is lost. The information is stored in the memory which is the same as shown for the real time memory **200.** The timing pulses for the registers are derived from circuits as shown in FIG. **11**; and the number and positions of registers, switches, etc., are the same, except, of course, there is no a/d converter since the five second old data is received in digitized form. Two discreet time delay circuits **134,** a 7.5 second delay circuit, and **136,** a 2.5 second delay circuit, are provided.

When the alarm response switch **124** of FIG. **7** is in instantaneous mode, the 7.5 second time delay circuit **134** is actuated. When in the instantanoous mode in the event of an alarm, the alarm signal to the delay circuit **134** does not enter memory **132** until 7.5 seconds subsequent to the receipt of the alarm signal. At the termination of the 7.5 seconds the memory **132** is sealed off as previously explained. This captures the event causing the alarm along with data 2.5 seconds earlier and later. It will remain locked in the memory **132** until the next alarm occurs or unless cancelled or written out, such as on the oscillograph of the cathode ray tube. When in the five second delay mode through switch **124** the 2.5 delay circuit is actuated to allow for the total 7.5 second delay in sealing the memory. Reset switch **124** resets the latch circuit **138.**

MULTIPLEXER

Referring to FIG. **13,** the multiplexer is shown generally at **340** and vertical input (FIG. **9**) from the d/a converter main memory flows to amplifier **342** to field effect transistor switch **344** shown in greater detail in the dotted lines, then to the mixing, scaling and offset circuit **349** which simply comprises an operational amplifier configured as a weighted summing amplifier with dc inputs to bias the output from **358** or **360** and signal inputs for display from **344** or **348** as shown, and then to the vertical input to the CRT. Input from the alarm memory passes through amplifier **346** to field effect transistor switch **348** similar to FET switch **344** and then to the mixing, scaling, and offset circuit **349.** Input from the clock **208** (see FIG. **9**), specifically the level shifter **240,** provides a blanking pulse to the JK flip-flop **350** whereby each time a blanking pulse is received this flip-flop changes state. NAND gate **352** receives inputs from the flip-flop **350** and view switch **354.**

With the view switch **354** in the position shown, or OFF, it is grounded and the signal from the NAND gate **352** inhibits FET **348** and FET **360.** The inverter provides a signal which turns on FET **344** and **358.** When the view switch is OFF, the output from gate **352** is always a predetermined value, specifically in this instance **5** volts, which allows the input from the main memory to be displayed on the CRT in a conventional manner as shown in FIG. **14.**

When the view switch **354** is actuated ON, the blanking input to JK flip-flop **350** goes to NAND gate **352.** Thus, on each return sweep of the CRT which corresponds to the input of the blanking pulse FET's **344** and **358** and FET's **348** and **360** are alternately turned on and inhibited. With the view switch actuated ON and engaged with the +5 volt source when FET's **344** and **358** are on, circuit **362** is engaged whereby the signal to the scaling circuit is between +5 and +12 volts. When FET's **348** and **360** are on (**344** and **358** being inhibited), circuit **364** is engaged whereby the signal transmitted to the mixing and scaling circuit varies between ground and −12. Therefore, when the view switch is actuated, the offset circuits **362** and **364** offset the displays of the real time and memory on the scope. Circuit **362** in combination with FET **358** offsets the real time display upwardly which is continuously displayed. Circuit **364** offsets the memory display downwardly. Since the information received from the alarm

memory is the continuously recirculated data as previously described, no new data is introduced into the alarm memory until specifically cleared by actuating the set-reset button **124**; and therefore, the memory data will appear as a permanent trace on the lower portion of the scope. This is also shown in FIG. **14** in the schematic illustration of the front panel.

The signals are displayed on the scope of a cathode ray tube, such as a Tektronix 560 Series, wherein the vertical input is from the mixing, scaling and offset circuit **349** (FIG. **13**) and the horizontal sweep trigger input from the a/d converter **202** (FIG. **9**). As shown in FIG. **14**, the real time display during normal operation is across the center of the tube. When an alarm condition is displayed, it is frozen on the lower portion of the screen and the real time is displaced upwardly as shown in the dotted lines.

OPERATION

In the operation of our invention the power switch is actuated and the limit switches on the front panel of the device as shown on FIG. **14** are set to establish the upper and lower limits for the alarm circuit shown in FIG. **7**. For example, the upper limit may be set at +2 volts corresponding to 120 BPM and the lower limit set at 0.6 volts corresponding to 40 BPM. The alarm system is set in the five second delay mode through actuation of the switch **124** which engages latch circuit **138** of FIG. **12**, the band width filter for the electrocardiogram signal is set at diagnostic, the patient cable switch is set to lead **2** wherein the lead is attached to the right arm, left leg, and a reference lead to the right leg. The signal from the patient passes through the floating front end and is filtered at the diagnostic level and then passes to the real time memory of FIG. **9**. As previously described, the signals from the patient are continually sampled, digitized, recirculated, passed to the multiplexer **340** of FIG. **13**, and displayed on the scope of the cathode ray tube **230**. As shown in FIG. **14**, when the information in the alarm memory is not displayed, the real time signals appear as a moving trace from the right to left of the scope in the center of the scope as shown. A signal from the analog to digital converter **202** of FIG. **9** goes directly into the cathode ray tube as the horizontal sweep trigger input. The vertical input for the cathode ray tube is from the mixing, scaling, and offset circuit **349** of FIG. **13**.

At the same time that the signal is transferred to the real time memory **200** and displayed on the scope of the cathode ray tube, it is filtered and passed to the QRS detector of FIG. **4**. If the patient has a heartbeat of 80 BPM, the QRS detector will analyze the duration of the linear rise and fall of the signal and distinguish it from background noise. Assuming the heartbeat at this time is normal, the signal will be sent by the QRS detector to the flasher and sound system of FIG. **8** as previously described. The flashing light and audio signals are shown in FIG. **14** at **63** and **95**. The signal entering the tachometer is converted to a digital representation of its value corresponding to beats per minute and is shown at **84** reflected as **80**. The signal generated by the divider **78** then goes to the alarm circuit of FIG. **7**. With 80 BPM the voltage would be approximately 1.3 volts. This signal is transferred to the comparators of the alarm circuit, which comparators were set at a high level of 2 volts corresponding to approximately 120 BPM and 0.6 volts corresponding to approximately 40 BPM. Since neither condition is violated, there is no signal generated by gate **119**. Thus, while the heart rate in beats per minute is within the limits set by the comparators **112** and **114**, no further signal is sent to the alarm memory and therefore, there is no change in the operation of the multiplexer and the signal is continuously displayed as described above.

Assuming that the patient now has a spell of sinus tachycardia, the signal to the filter and the real time memory **200** will continue as before and enter the multiplexer (FIG. **13**) at **343**. The horizontal sweep trigger pulse from the real time memory directly to the horizontal input of the cathode ray tube will also continue as before. With the heartbeat now 160 BPM the QRS detector circuit will examine the pulses to determine their slope. If they fall within the 10 to 40 millisecond window, then, of course, they are transmitted to the flasher and audio signal and to the tachometer. With a rate of 160 BPM entering the sample and hold circuit **76** (FIG. **5**), a voltage output from divider **78** goes to amplifier and offset circuit **79**, then to the converter **82** where a digital display reflecting the 160 BPM would be displayed. The voltage from the digital divider with a value of about 2.6 volts corresponding to the 160 BPM goes to the comparators **112** and **144** of the alarm circuit which have been set at 2 to 0.6 volts for the upper and lower limits. Thus, the 2.6 volt value would violate the upper limit of comparator **112** causing gate **119** to generate a signal. Also, the front panel lamp, in this instance the tachycardia **120**, is actuated, a high alarm signal is transmitted to the oscillator of FIG. **8**, and a further signal of the audio oscillator of FIG. **8** is transmitted, and the signal from gate **119** is transmitted to the alarm memory of FIG. **12**. Since the switch **124** is in the five second delay mode, no signal will be received by the alarm memory from gate **119** until the condition has existed for five seconds. Therefore, as soon as the condition exists for five seconds, then, of course, the signal is transmitted to the alarm memory.

If no signal were received from the QRS circuit, then referring to FIG. **5**, the sample and hold circuit would generate a 2.5 volt level which is approximately 3 seconds between heartbeats or a rate of 20 BPM or less. The ramp generator **74** of FIG. **5** when it reaches a threshold value of 2.5 volts as determined by the comparator **75** will provide a signal to gate **71** to trigger a pulse corresponding in time to the 2.5 volt value. This value, of course, of 0.4 volts to the alarm system would also exceed the preset limits and actuate the alarm system. Returning to the specific example, when in the five second delay mode the latch circuit **136** which provides a 2.5 second delay is actuated at the termination of the five seconds from when the alarm signal was first received as previously described. The data in the alarm memory is sealed off and remains in a recirculation mode or state. To view the display of the condition which caused the alarm the view switch of FIG. **13** is actuated and the real time display is displaced upwardly on the screen as shown in dotted lines in FIG. **14** and the display of the alarm condition appears on the lower half of the screen as a permanent display. After the data has been examined, then the information may be cleared by actuation of the set-reset button **124** of FIG. **7**.

Having described my invention, what I now claim is:

1. A device for analysis and display of electrocardiogram (ECG) signals which comprises:
a. means to provide an ECG signal;
b. a real time memory which includes:
1. means to receive the ECG signal and convert the signal to digitized form;
2. means to store the digitized signal for a first predetermined time which corresponds to the time required for the digitized signal to enter, be recycled, and discarded;
c. means in communication with the real time memory to display continuously the digitized signal in the real time memory in analog form on a medium;
d. means to analyze the ECG signal to determine if the signal falls within at least one predetermined limit, which limit corresponds to a rate value which describes an alarm condition and means to provide an alarm signal of the limit is violated;
e. an alarm memory which includes:
1. means to receive the ECG signal in digitized form;
2. means to store the digitized signal for a second predetermined time, which corresponds to the time required for the digitized signal to enter, be recycled, and discarded from the alarm memory; and
3. means responsive to the presence of the alarm signal to lock in place and prevent the discard of the digitized signal stored in the alarm memory; and
f. means in communication with the alarm memory to display in analog form the digitized signal locked in the alarm memory on a medium.

2. The device of claim 1, which includes means to distinuguish the ECG signal from background noise, whereby only those ECG signals falling within a defined range are selected for analysis.

3. The device of claim 2, wherein the means to distinguish the ECG signal from background noise includes a wave-shaping network to convert the signal to a pulsed signal and a matching network to determine if the duration of the pulsed signal is within the defined range.

4. The device of claim 3, which includes means to establish the defined range between 10–40 milliseconds.

5. The device of claim 1, which includes means to convert the ECG signal to a wave form which has a rate voltage inversely proportional to the duration between successively generated ECG signals.

6. The device of claim 5, which includes means to display the value inversely proportional to the duration between pulses in digital form.

7. The device of claim 1, which includes means to determine if the ECG signal falls within upper and lower limits, which limits correspond to rate values which describe alarm conditions whereby an alarm signal is generated when either limit is violated.

8. The device of claim 7, which includes means to establish the upper and lower limits as voltage limits.

9. The device of claim 7, which includes means to delay the transmission of the alarm signal to the alarm memory.

10. The device of claim 1, which includes means to transfer the digitized signals from the real time memory to the alarm memory.

11. The device of claim 1, which includes means to transfer the digitized signals discarded from the real time memory to the alarm memory.

12. The device of claim 1, which includes means to delay the locking of the digitized signal in the alarm memory subsequent to the receipt of the alarm signal whereby the digitized signal corresponding to the ECG signal which ECG signal violated the limit and generated the alarm signal is locked in the alarm memory in a position intermediate its entry and discard from the alarm memory.

13. The device of claim 1, which includes the means to display the information locked in the alarm memory on the same medium that the digitized signal in the real time memory is displayed.

14. The device of claim 13, wherein the medium is a cathode ray tube.

15. A device for the analysis and display of electrocardiogram (ECG) signals, which comprises:
a. means to provide an ECG signal;
b. a real time memory which includes;
1. means to receive the ECG signal and convert the signal to digitized form;
2. means to store the digitized signal for a first predetermined time, which corresponds to the time required for the digitized signal to enter, be recycled, and discarded;
c. means to analyze the ECG signal to determine if the signal falls within predetermined upper and lower limits, which means includes:
1. means to distinguish the ECG signal from background noise;
2. means to convert the distinguished ECG signal to a wave form which has a rate voltage inversely proportional to the duration between successively generated ECG signals; and
3. means to provide an alarm signal when either the upper or lower limit is violated;
d. means to transfer the digitized ECG signals from the real time memory to an alarm memory, which alarm memory includes;
1. means to receive the digitized signals from the real time memory;
2. means to store the digitized signals therein for a second predetermined time which corresponds to the time required for the digitized signal to enter, be recycled, and discarded; and
3. means responsive to the presence of the alarm signal to lock in position and prevent the discard of the digitized signal in the alarm memory; and
e. means in communication with the real time memory and the alarm memory to display continuously the digitized signal in the real time memory in analog form and to display the digitized signal in the alarm memory in analog form.

16. The device of claim 15, wherein the means to distinguish the ECG signal from background noise includes a wave-shaping network to convert the signal to a pulsed signal and a matching network to determine if the pulsed signal is within a defined range.

17. The device of claim 15, which includes means to delay the transmission of the alarm signal to the alarm memory.

18. The device of claim 15, which includes means to transfer the digitized signals from the real time memory

to the alarm memory when the digitized signals are discarded from the real time memory.

19. The device of claim **15,** wherein the alarm memory includes means to delay the locking of the signals in the alarm memory subsequent to the receipt of the alarm signal whereby the digitized signal corresponding to the ECG signal which ECG signal violated the limit and generated the alarm signal is locked in the alarm memory in a position intermediate its entry and discard from the alarm memory.

20. The device of claim **19,** wherein the means to delay the locking of the information in the alarm memory includes at least one latch circuit.

21. The device of claim **15,** which includes means to display the digitized signal in the alarm memory at any time subsequent to the locking of the signals in the memory.

22. The device of claim **15,** which includes means to display on the same medium the digitized signal in the real time memory and the digitized signal in the alarm memory, the signals spaced apart from one another along a vertical axis.

23. The device of claim **15,** which includes means to display digitally the rate voltage.

24. The device of claim **15,** which includes means to display audibly the analyzed ECG signals.

25. A method for the analysis and display of electrocardiogram (ECG) signals, which includes:

a. providing an ECG signal;

b. converting said ECG signal to digitized form and storing the same in a real time memory for a first predetermined time which corresponds to the time required for the digitized signal to enter, be recycled, and discarded;

c. displaying continuously in analog form the digitized signal in the real time memory on a medium;

d. analyzing the ECG signal to determine if the signal falls within predetermined limits, which limits correspond to rate values which describe alarm conditions;

e. providing an alarm signal when either of the limits is violated;

f. receiving and storing the ECG signals in digitized form in an alarm memory for a predetermined second time which corresponds to the time required for the signal to enter, be recycled, and discarded;

g. locking and preventing the discard of the digitized signal in the alarm memory in response to the alarm signal of step (e); and

h. displaying in analog form the digitized signal locked in the alarm memory.

26. The method of claim **25,** which includes distinguishing the ECG signal from background noise.

27. The method of claim **26,** which includes converting the distinguished ECG signal to a wave form, which has a rate voltage inversely proportional to the duration between successively generated ECG signals.

28. The method of claim **25,** which includes displaying the rate voltage in digital form.

29. The method of claim **25,** which includes transferring the digitized signal in the real time memory to the alarm memory.

30. The method of claim **29,** which includes transferring the digitized signal to the alarm memory upon discharge of the signal from the real time memory.

31. The method of claim **25,** which includes delaying the locking of the digitized signal in the alarm memory subsequent to the receipt of the alarm signal whereby the digitized signal corresponding to the ECG signal which ECG signal violated the limit and generated the alarm signal is locked in the alarm memory in a position intermediate its entry and discard from the alarm memory.

32. The method of claim **25,** which includes displaying the digitized signal in the real time memory and the digitized signal in the alarm memory, in analog form on the same medium, said signals spaced apart from one another along a vertical axis.

33. The method of claim **32,** which includes displaying the digitized signals in the alarm memory at a time subsequent to the locking of the signals in the alarm memory.

* * * * *