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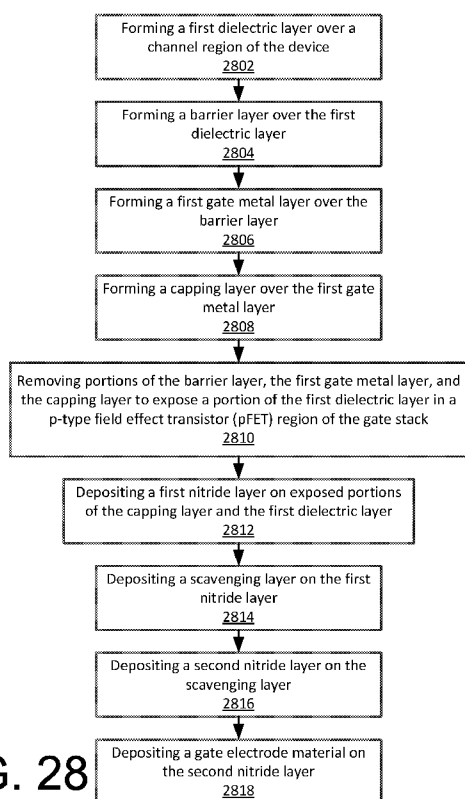


FIG. 28

(57) Abstract: A method for fabricating a gate stack of a semiconductor device comprising forming a first dielectric layer over a channel region of the device, forming a barrier layer over the first dielectric layer, forming a first gate metal layer over the barrier layer, forming a capping layer over the first gate metal layer, removing portions of the barrier layer, the first gate metal layer, and the capping layer to expose a portion of the first dielectric layer in a p-type field effect transistor (pFET) region of the gate stack, depositing a first nitride layer on exposed portions of the capping layer and the first dielectric layer, depositing a scavenging layer on the first nitride layer, depositing a second nitride layer on the scavenging layer, and depositing a gate electrode material on the second nitride layer.





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SEMICONDUCTOR DEVICE GATE STACK

BACKGROUND

[0001] The present invention generally relates to semiconductor devices, and more specifically, to metal-oxide-semiconductor field effect transistor (MOSFET) gates.

[0002] The MOSFET is a transistor used for amplifying or switching electronic signals. The MOSFET has a source, a drain, and a metal oxide gate electrode. The metal gate is electrically insulated from the main semiconductor n-channel or p-channel by a thin layer of insulating material, for example, silicon dioxide or glass, which makes the input resistance of the MOSFET relatively high. The gate voltage controls whether the path from drain to source is an open circuit (“off”) or a resistive path (“on”).

[0003] N-type field effect transistors (nFET) and p-type field effect transistors (pFET) are two types of complementary MOSFETs. The nFET uses electrons as the current carriers and with n-doped source and drain junctions. The pFET uses holes as the current carriers and with p-doped source and drain junctions.

SUMMARY

[0004] According to an aspect of the present invention, a method for fabricating a gate stack of a semiconductor device comprising forming a first dielectric layer over a channel region of the device, forming a barrier layer over the first dielectric layer, forming a first gate metal layer over the barrier layer, forming a capping layer over the first gate metal layer, removing portions of the barrier layer, the first gate metal layer, and the capping layer to expose a portion of the first dielectric layer in a p-type field effect transistor (pFET) region of the gate stack, depositing a first nitride layer on exposed portions of the capping layer and the first dielectric layer, depositing a scavenging layer on the first nitride layer, depositing a second nitride layer on the scavenging layer, and depositing a gate electrode material on the second nitride layer.

[0005] According to another aspect of the present invention, a semiconductor device includes a gate stack arranged over a channel region of the device, the gate stack comprising an n-type field effect transistor (nFET) portion comprising a dielectric layer arranged on a substrate, a barrier layer arranged on the dielectric layer, a first gate metal layer arranged on the barrier layer, a capping layer arranged on the first gate metal layer, a first nitride layer arranged on the capping layer, a scavenging layer arranged on the first nitride layer, a second nitride layer arranged on the scavenging layer, and a gate electrode arranged on the second nitride layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

FIGS. 1-11 illustrate an exemplary method for forming a gate stack of an exemplary FET device:

FIG. 1 illustrates a top view of a substrate with semiconductor fins and arranged on the substrate.

FIG. 2 illustrates a cutaway view along the line A-A of FIG. 1 of the fins and the substrate.

FIG. 3 illustrates a cut-away view along the width of the gate stack (longitudinal direction).

FIG. 4 illustrates a barrier layer is deposited over the oxide layer.

FIG. 5 illustrates the resultant structure following the deposition of a layer of nFET gate metal.

FIG. 6 illustrates the resultant structure following the formation of a cap layer that may include, for example, a nitride material such as TiN.

FIG. 7 illustrates the resultant structure following a patterning and etching process that removes portions of the barrier layer, the gate metal and the cap layer.

FIG. 8 illustrates the formation of a nitride layer.

FIG. 9 illustrates the deposition of a scavenging layer.

FIG. 10 illustrates the resultant structure following the deposition of a PWF layer.

FIG. 11 illustrates the resultant structure following the deposition of gate electrode over exposed portions of the PWF layer.

FIGS. 12-15 illustrate another exemplary method for forming an alternate embodiment of a gate stack:

FIG. 12 shows the formation gate stack having an nFET portion and a pFET portion.

FIG. 13 illustrates the resultant structure following a lithographic patterning and etching process.

FIG. 14 illustrates the deposition of a scavenging layer.

FIG. 15 illustrates the resultant structure following the deposition of a PWF layer.

FIGS. 16-20 illustrate another exemplary method for forming another alternate embodiment of a gate stack:

FIG. 16 shows the formation of a gate stack having an nFET portion and a pFET portion.

FIG. 17 illustrates the resultant structure following a lithographic patterning and etching process.

FIG. 18 illustrates the deposition of a barrier layer that is deposited over the oxide layer.

FIG. 19 shows the deposition of a gate metal over the barrier layer in the nFET portion and the pFET portion.

FIG. 20 illustrates the resultant structure following the deposition of a PWF layer over the gate metal layer.

FIGS. 21-24 illustrate another exemplary method for forming another alternate embodiment of a gate stack:

FIG. 21 shows the formation of a gate stack having an nFET portion and a pFET portion.

FIG. 22 illustrates the resultant structure following a lithographic patterning and etching process that removes exposed portions of the capping layer and the scavenging layer.

FIG. 23 illustrates the resultant structure following the deposition of a gate metal layer

FIG. 24 illustrates the resultant structure following the deposition of a PWF layer over the gate metal layer.

FIG. 25 illustrates a top view of an exemplary embodiment of a finFET device.

FIG. 26 illustrates a cutaway view along the line B-B of FIG. 25 of the gate stack on the fin.

FIG. 27 illustrates a cutaway view along the line C-C of FIG. 25 of the gate stack on the fin.

FIG. 28 illustrates a block diagram of an exemplary method for forming a semiconductor device as described above in FIGS. 1-11.

DETAILED DESCRIPTION

[0007] The methods and embodiments described herein provide a robust tunable nFET gate stack in a MOSFET device. In FET devices, metal nitrides such as, for example, TiN and TaN provide a good work function material in the gate stacks to achieve a desired threshold voltage (V_t) in pFET devices. As the scaling of FET devices continues to decrease, multi-gate devices such as finFETs are used to achieve performance goals. Atomic layer deposition (ALD) is used to deposit a uniform layer of the work function metal to reduce V_t variation and control the V_t of the FET devices. Changing the characteristics of work function metals in a replacement metal gate fabrication process using ALD has become more challenging.

[0008] Through experimentation, it has been found that the pV_t has become less stable and the V_t has become difficult to control when untreated TiN or TaN is used as the work function metal of pFET devices because the response of oxygen vacancy in high-k dielectric materials with respect to the thermal budget in the replacement metal gate fabrication process.

[0009] The performance and reliability of nFET devices may be improved using a D_2 or high pressure annealing process. However, the process may lead to unstable pV_t when the pFET includes a conventional work function metal such as, for example, TiN.

[0010] The methods and embodiments described herein provide for a gate stack with a relatively weak oxygen-scavenge stack to define and adjust the pV_t as opposed to a single metal nitride layer such as, for example, TiN and TaN. The weak oxygen-scavenge stack may be formed by deposition or integration, and may include, for example, a barrier layer such as, TiN or TaN and a strong oxygen-scavenge material such as TiAlC, TiAl, Al, Ti, NbAl, and TaAlC.

[0011] The following definitions and abbreviations are to be used for the interpretation of the claims and the specification. As used herein, the terms "comprises," "comprising," "includes," "including," "has," "having," "contains" or "containing," or any other variation thereof, are intended to cover a non-exclusive inclusion. For example, a composition, a mixture, process, method, article, or apparatus that comprises a list of elements is not necessarily limited to only

those elements but can include other elements not expressly listed or inherent to such composition, mixture, process, method, article, or apparatus.

[0012] As used herein, the articles "a" and "an" preceding an element or component are intended to be nonrestrictive regarding the number of instances (i.e. occurrences) of the element or component. Therefore, "a" or "an" should be read to include one or at least one, and the singular word form of the element or component also includes the plural unless the number is obviously meant to be singular.

[0013] As used herein, the terms "invention" or "present invention" are non-limiting terms and not intended to refer to any single aspect of the particular invention but encompass all possible aspects as described in the specification and the claims.

[0014] As used herein, the term "about" modifying the quantity of an ingredient, component, or reactant of the invention employed refers to variation in the numerical quantity that can occur, for example, through typical measuring and liquid handling procedures used for making concentrates or solutions. Furthermore, variation can occur from inadvertent error in measuring procedures, differences in the manufacture, source, or purity of the ingredients employed to make the compositions or carry out the methods, and the like. In one aspect, the term "about" means within 10% of the reported numerical value. In another aspect, the term "about" means within 5% of the reported numerical value. Yet, in another aspect, the term "about" means within 10, 9, 8, 7, 6, 5, 4, 3, 2, or 1% of the reported numerical value.

[0015] It will also be understood that when an element, such as a layer, region, or substrate is referred to as being "on" or "over" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or "directly over" another element, there are no intervening elements present, and the element is in contact with another element.

[0016] It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being

“directly connected” or “directly coupled” to another element, there are no intervening elements present.

[0017] FIGS. 1-11 illustrate an exemplary method for forming a gate stack of an exemplary FET device.

[0018] FIG. 1 illustrates a top view of a substrate 102 with semiconductor fins 112 and 114 arranged on the substrate 102. In the illustrated embodiment, channel regions of the fins 112 and 114 have been exposed following the removal of a sacrificial gate stack (not shown), which was previously patterned on the substrate 102 and the fins 112 and 114. A spacer material 104 is formed around the sacrificial gate stack. An insulator material such as, for example, an oxide or other dielectric material is formed around the spacer material 104. In the illustrated embodiment, the fins 112 will partially define the channel region and source/drain regions of the completed device. The fins 112 will partially define an nFET device, while the fin 114 will partially define a pFET device. The gate stack (described below) is divided into two portions an nFET portion 108 and a pFET portion 110. Non-limiting examples of suitable fin materials include Si (silicon), strained Si, SiC (silicon carbide), Ge (geranium), SiGe (silicon germanium), SiGeC (silicon-germanium-carbon), Si alloys, Ge alloys, GaAs (gallium arsenide), InAs (indium arsenide), InP (indium phosphide), or any combination thereof.

[0019] In the illustrated embodiment, the fins 112 and 114 are arranged on the substrate 102 that includes an insulator layer such that a semiconductor on insulator (SOI) substrate may be used. Alternate exemplary embodiments may form fins on a bulk semiconductor substrate.

[0020] FIG. 2 illustrates a cutaway view along the line A-A of FIG. 1 of the fins 112 and 114 and the substrate 102.

[0021] FIG. 3 illustrates a cut-away view along the width of the gate stack (longitudinal direction) through and parallel to the gate. For simplicity, the fins 112 and 114 have been removed from the figures to better illustrate the formation of the exemplary gate stacks. In finFET device fabrication, the layers of the gate stack are arranged conformably over the channel regions of the fins 112 and 114. The embodiments described herein are not limited to

finFET devices or other multi-gate devices, and may be used to fabricate, for example, planar FET devices, nanowire devices, tunneling devices, and so on. In such a fabrication scheme for planar FET devices, the substrate 102 would include a semiconductor material, and the gate stacks would be formed in a similar manner on the substrate 102.

[0022] In FIG. 3 an oxide (dielectric) layer 302 that may include, for example SiO_2 or HfO_2 is deposited over the channel region of the device and on portions of the substrate and annealed to begin forming the replacement metal gate. The oxide layer 302 has a thickness of from 10 to 100 angstroms. The oxide layer 302 may be deposited by, for example, a high aspect ratio plasma (HARP), a high temperature oxide (HTO), a high density plasma (HDP), or an atomic layer deposition (ALD) process, or any combination thereof. The dielectric layer 302 and subsequent layers described herein is formed over the channel region conform not only over the fins 112 (described above) but also conform over the sidewalls of the 104 (of FIG. 1). Likewise, layers formed subsequently conform to the profile of the previous layers.

[0023] In the exemplary method, the nFET stack is formed prior to forming the pFET stack. The nFET stack includes a strong oxygen-scavenge stack, while the subsequently formed pFET stack includes a weak oxygen-scavenge stack.

[0024] One difference between nFET strong oxygen-scavenge stack and the pFET if a single metal layer is used is that the enthalpy change to form metal oxide is much higher for nFET than that for pFET. For example, Al is used for nFET and Ni is used for pFET. In another hand, the oxygen-scavenge stack can be formed by same materials and the same structure but with different film thickness or different film composition. For example, TiN/TiAl/TiN stack is used as oxygen-scavenge stack. If the layers are similar except for the TiAl thickness, thicker TiAl will form stronger oxygen-scavenge stack, but thinner TiAl will form the weak oxygen-scavenge stack. Another hand, if the TiAl thickness and top TiN thickness are same, the bottom TiN difference can also form stronger oxygen-scavenge stack by using thinner bottom TiN and weaker oxygen-scavenge stack by using thicker bottom TiN.

[0025] Referring to FIG. 4 a barrier layer 402 is deposited over the oxide layer 302. The barrier layer 402 may include metal nitrides and metal carbides, for example, TiN, TaN, TiC, TaC, and be formed by, for example, an atomic layer deposition process.

[0026] FIG. 5 illustrates the resultant structure following the deposition of a layer of nFET gate metal 502 such as, for example, TiAlC or TiAl, Ti, Al, NbAlC, over the barrier layer 402, using for example, an ALD process.

[0027] FIG. 6 illustrates the resultant structure following the formation of a cap layer 602 that may include, for example, a nitride material such as TiN.

[0028] FIG. 7 illustrates the resultant structure following a patterning and etching process that removes portions of the barrier layer 402, the gate metal 502 and the cap layer 602 from the pFET portion 110 of the gate stack. The etching process may include any suitable etching process or combination of processes such as, for example, reactive ion etching, which exposes a portion of the oxide layer 302.

[0029] FIG. 8 illustrates the formation of a nitride layer 802 using for example an ALD process that deposits the nitride layer 802 on the exposed portions of the oxide layer 302 and on the cap layer 602. The nitride layer 802 may include, for example, TiN or TaN.

[0030] FIG. 9 illustrates the deposition of a scavenging layer 902 that may include, for example, TiAlC or TiAl, Ti, Al, TiAlC, NbAlC over the nitride layer 802. The scavenging layer 902 and the nitride layer 802 define a weak oxygen-scavenge stack.

[0031] FIG. 10 illustrates the resultant structure following the deposition of a pFET work function (PWF) metal layer 1002 over the scavenging layer 902. The PWF layer 1002 includes, for example, a TiN or TaN material that may be formed by, for example, an atomic layer deposition process.

[0032] FIG. 11 illustrates the resultant structure following the deposition of gate electrode 1102 over exposed portions of the PWF layer 1002. The gate electrode 1102 may include, for

example, tungsten that is formed using a relatively cool filling deposition process followed by a planarizing process such as, chemical mechanical polishing (CMP).

[0033] FIG. 11 illustrates an exemplary embodiment of a gate stack 1100 that includes an nFET portion 108 and a pFET portion 110.

[0034] FIGS. 12-15 illustrate another exemplary method for forming an alternate embodiment of a gate stack.

[0035] FIG. 12 shows the formation gate stack having an nFET portion 108 and a pFET portion 110. The fabrication of the gate stack begins with the deposition of an oxide (dielectric) layer 302 on the substrate or fin, a nitride layer 802 is disposed on the oxide layer 302. A layer of nFET gate metal 502 such as, for example, TiAlC or TiAl, Ti, Al, TiAlC, NbAlC is deposited over the nitride layer 802, and a capping layer 602 that may include, for example, TiN is deposited over the gate metal 502.

[0036] FIG. 13 illustrates the resultant structure following a lithographic patterning and etching process such as, for example, reactive ion etching that removes exposed portions of the capping layer 602 and the gate metal 502 from the pFET portion 110 to expose the nitride layer 802 in the pFET portion 110.

[0037] FIG. 14 illustrates the deposition of a scavenging layer 902 that may include, for example, TiAlC or TiAl, Ti, Al, TiAlC, NbAlC over the nitride layer 802 in the pFET portion and over the capping layer 602 in the nFET portion 108.

[0038] FIG. 15 illustrates the resultant structure following the deposition of a PWF layer 1002 over the scavenging layer 902. After the PWF layer 1002 is deposited, the gate electrode 1102 is formed over the PWF layer 1002 in a similar manner as described above and planarized using a suitable planarization process, such as, for example, chemical mechanical polishing.

[0039] FIG. 15 illustrates an exemplary embodiment of a gate stack 1500 that includes an nFET portion 108 and a pFET portion 110.

[0040] FIGS. 16-20 illustrate another exemplary method for forming another alternate embodiment of a gate stack.

[0041] FIG. 16 shows the formation of a gate stack having an nFET portion 108 and a pFET portion 110. The fabrication of the exemplary gate stack begins with the deposition of an oxide (dielectric) layer 302 on the substrate or fin, a nitride layer 802 is disposed on the oxide layer 302. A scavenging layer 902 that may include, for example, TiAlC or TiAl, Ti, Al, TiAlC, NbAlC is disposed over the nitride layer 802. A capping layer 602 that may include, for example, TiN is deposited over the scavenging layer 902.

[0042] FIG. 17 illustrates the resultant structure following a lithographic patterning and etching process that removes exposed portions of the capping layer 602, the scavenging layer 902, and the nitride layer 802 from the nFET portion 108 of the gate stack, which exposes a portion of the oxide layer 302 in the nFET portion 108.

[0043] FIG. 18 illustrates the deposition of a barrier layer 402 that is deposited over the oxide layer 302 in the nFET portion 108 and the capping layer 602 in the pFET region 110.

[0044] FIG. 19 shows the deposition of a gate metal 502 over the barrier layer 402 in the nFET portion 108 and the pFET portion 110.

[0045] FIG. 20 illustrates the resultant structure following the deposition of a PWF layer 1002 over the gate metal layer 502. Following the formation of the PWF layer 1002, the gate electrode 1102 is formed over the PWF layer 1002 in a similar manner as described above and planarized using a suitable planarization process, such as, for example, chemical mechanical polishing.

[0046] FIG. 20 illustrates another alternate exemplary embodiment of a gate stack 2000 that includes an nFET portion 108 and a pFET portion 110.

[0047] FIGS. 21-24 illustrate another exemplary method for forming another alternate embodiment of a gate stack.

[0048] FIG. 21 is similar to FIG. 16 described above, and shows the formation of a gate stack having an nFET portion 108 and a pFET portion 110. The fabrication of the exemplary gate stack begins with the deposition of an oxide (dielectric) layer 302 on the substrate or fin, a nitride layer 802 is disposed on the oxide layer 302. A scavenging layer 902 that may include, for example, TiAlC or TiAl, Ti, Al, TiAlC, NbAlC is disposed over the nitride layer 802. A capping layer 602 that may include, for example, TiN is deposited over the scavenging layer 902.

[0049] FIG. 22 illustrates the resultant structure following a lithographic patterning and etching process that removes exposed portions of the capping layer 602 and the scavenging layer 902 from the nFET portion 108 of the gate stack. The etching process exposes the nitride layer 802 in the nFET portion 108 of the gate stack.

[0050] FIG. 23 illustrates the resultant structure following the deposition of a gate metal layer 502 over the nitride layer 802 in the nFET portion 108 and over the capping layer 602 in the pFET portion 110 of the gate stack.

[0051] FIG. 24 illustrates the resultant structure following the deposition of a PWF layer 1002 over the gate metal layer 502. Following the deposition of the PWF layer 1002, the gate electrode 1102 is formed over the PWF layer 1002 in a similar manner as described above and planarized using a suitable planarization process, such as, for example, chemical mechanical polishing.

[0052] FIG. 24 illustrates another alternate exemplary embodiment of a gate stack 2400 that includes an nFET portion 108 and a pFET portion 110.

[0053] FIG. 25 illustrates a top view of an exemplary embodiment of a finFET device. In this regard, the fins 112 and 114 are arranged on the substrate 102. The gate stack 2400 is arranged over channel regions of the fins 112 and 114. The fins 112 and 114 include source/drain regions 2502 that may be formed by, for example, an ion implantation process or an epitaxial growth process. Though the illustrated exemplary embodiment in FIG. 25 includes the gate stack 2400, any of the gate stacks 1100, 1500, or 2000 may be formed as described

above over the fins 112 and 114. Alternatively, the gate stacks 1100, 1500, 2000, or 2400 may be formed on a semiconductor substrate to form a planar FET that has source and drain regions that may be partially defined by the semiconductor substrate.

[0054] FIG. 26 illustrates a cutaway view along the line B-B of FIG. 25 of the gate stack 2400 on the fin 112. FIG. 27 illustrates a cutaway view along the line C-C of FIG. 25 of the gate stack 2400 on the fin 114.

[0055] FIG. 28 illustrates a block diagram of an exemplary method for forming a semiconductor device as described above in FIGS. 1-11. Referring to FIG. 28, in block 2802, a first dielectric layer is formed over a channel region of the device. In block 2804, a barrier layer is formed over the first dielectric layer. A first gate metal layer is formed over the barrier layer in block 2806. In block 2808, a capping layer is formed over the first gate metal layer. In block 2810, portions of the barrier layer, the first gate metal layer, and the capping layer are removed to expose a portion of the first dielectric layer in a p-type field effect transistor (pFET) region of the gate stack. A first nitride layer is deposited on exposed portions of the capping layer and the first dielectric layer in block 2812. In block 2814, a scavenging layer is deposited on the first nitride layer. A second nitride layer is deposited on the scavenging layer in block 2816. In block 2818, a gate electrode material is deposited on the second nitride layer.

[0056] The methods and embodiments described herein provide for a gate stack with a relatively weak oxygen-scavenge stack to define and adjust the pVt as opposed to a single metal nitride layer such as, for example, TiN and TaN. The weak oxygen-scavenge stack may be formed by deposition or integration, and may include, for example, a barrier layer such as, TiN or TaN and a strong oxygen-scavenge material such as TiAlC or TiAl, Ti, Al, TiAlC, NbAlC.

[0057] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the

marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

CLAIMS

1. A method for fabricating a gate stack of a semiconductor device, the method comprising:
 - forming a first dielectric layer over a channel region of the device;
 - forming a barrier layer over the first dielectric layer;
 - forming a first gate metal layer over the barrier layer;
 - forming a capping layer over the first gate metal layer;
 - removing portions of the barrier layer, the first gate metal layer, and the capping layer to expose a portion of the first dielectric layer in a p-type field effect transistor (pFET) region of the gate stack;
 - depositing a first nitride layer on exposed portions of the capping layer and the first dielectric layer;
 - depositing a scavenging layer on the first nitride layer;
 - depositing a second nitride layer on the scavenging layer; and
 - depositing a gate electrode material on the second nitride layer.
2. The method of claim 1, wherein the first dielectric layer includes an oxide material.
3. The method of claim 1, wherein the barrier layer includes a metal nitride material.
4. The method of claim 1, wherein the first gate metal layer includes TiAlC or TiAl, Ti, Al, TiAlC, NbAlC.
5. The method of claim 1, wherein the first nitride layer includes TiN or TaN.
6. The method of claim 1, wherein the first nitride layer includes TaN.
7. The method of claim 1, wherein the second nitride layer includes TiN.
8. The method of claim 1, wherein the gate electrode material includes W.

9. The method of claim 1, further comprising forming a source/drain region adjacent to the gate stack prior to forming the gate stack.
10. The method of claim 1, further comprising prior to forming the gate stack:
forming a sacrificial gate stack over the channel region of the device;
forming a spacer along sidewalls of the sacrificial gate stack;
forming a source/drain region of the device adjacent to the sacrificial gate stack;
forming a layer of insulator material around the spacer; and
removing the sacrificial gate stack to expose the channel region of the device.
11. A semiconductor device comprising:
a gate stack arranged over a channel region of the device, the gate stack comprising an n-type field effect transistor (nFET) portion comprising:
a dielectric layer arranged on a substrate;
a barrier layer arranged on the dielectric layer;
a first gate metal layer arranged on the barrier layer;
a capping layer arranged on the first gate metal layer;
a first nitride layer arranged on the capping layer;
a scavenging layer arranged on the first nitride layer;
a second nitride layer arranged on the scavenging layer; and
a gate electrode arranged on the second nitride layer.
12. The device of claim 11, further comprising a p-type field effect transistor (pFET) portion comprising:
the dielectric layer arranged on the substrate;
the first nitride layer arranged on the dielectric layer;
the scavenging layer arranged on the first nitride layer;
the second nitride layer arranged on the scavenging layer; and
the gate electrode arranged on the second nitride layer.
13. The device of claim 11 or claim 12, wherein the first dielectric layer includes an oxide material.

14. The device of claim 11 or claim 12, wherein the barrier layer includes a metal nitride material.
15. The device of claim 11 or claim 12, wherein the gate electrode material includes W.

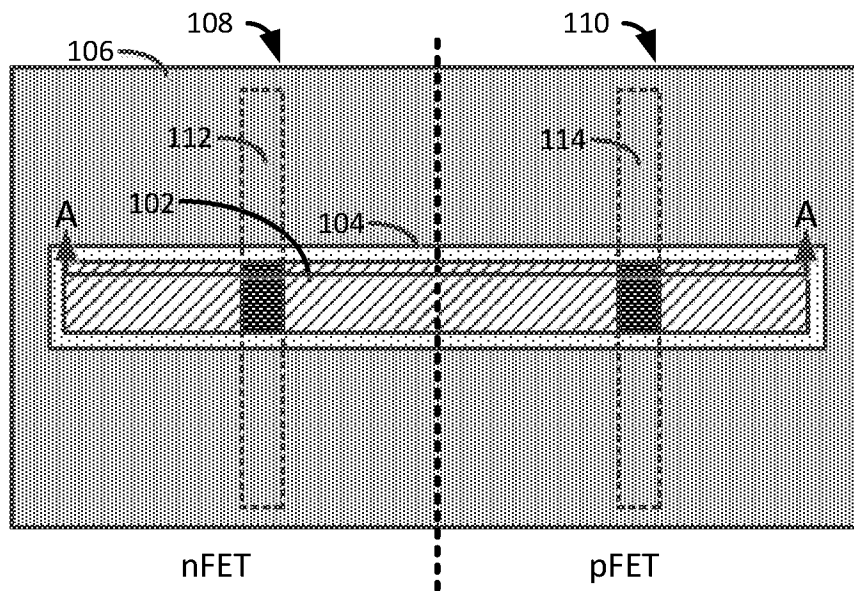


FIG. 1

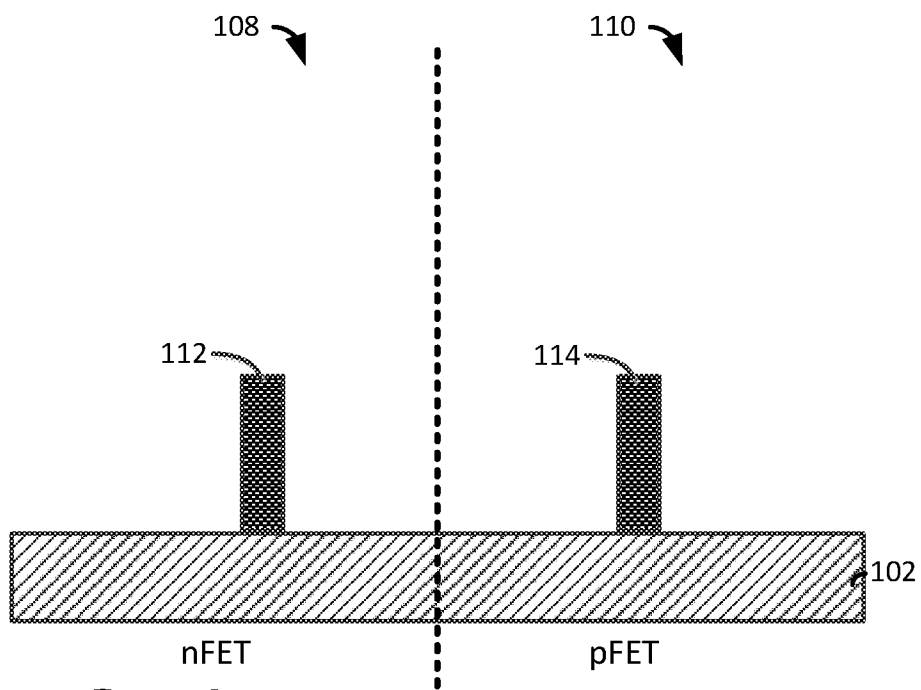


FIG. 2

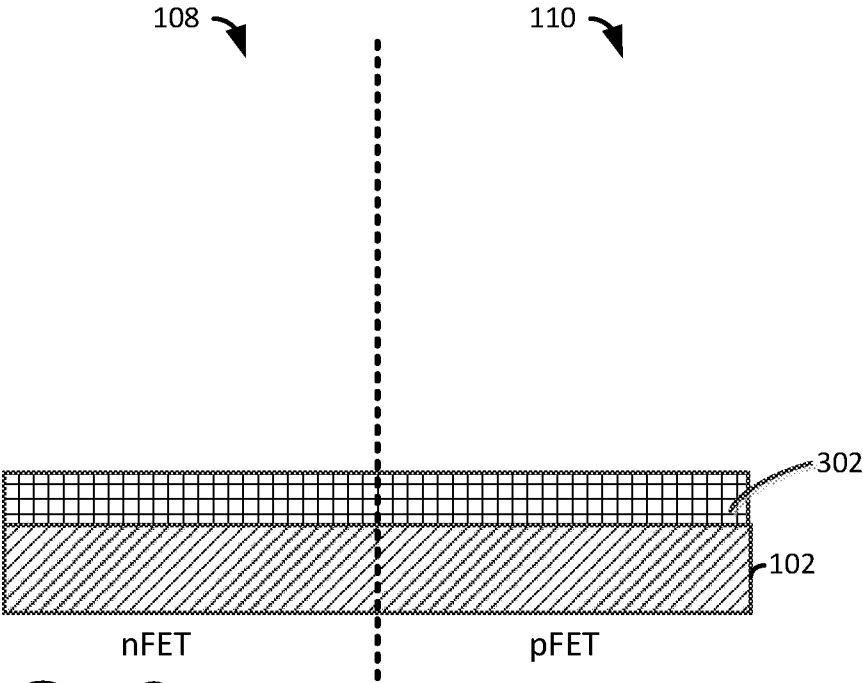


FIG. 3

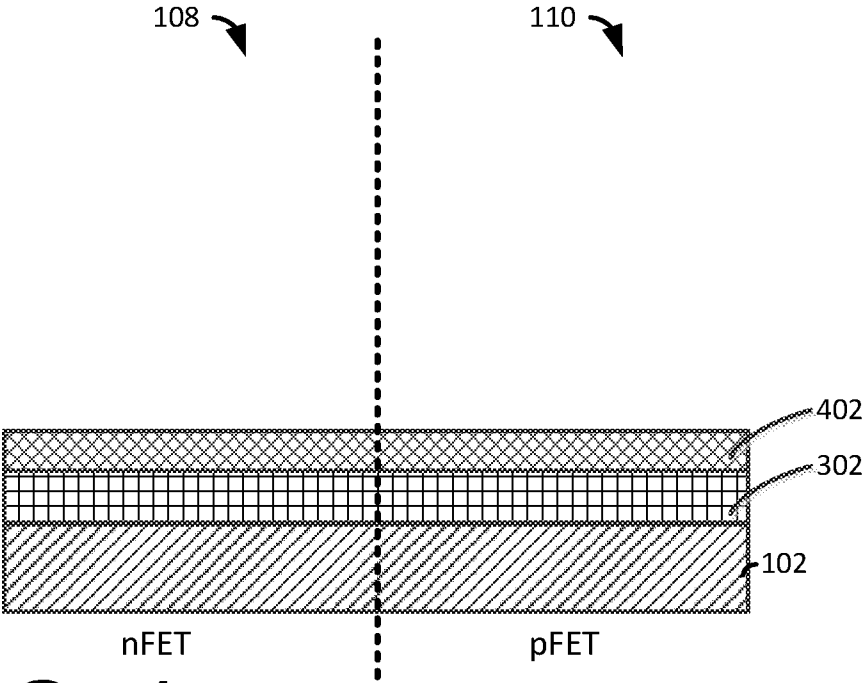
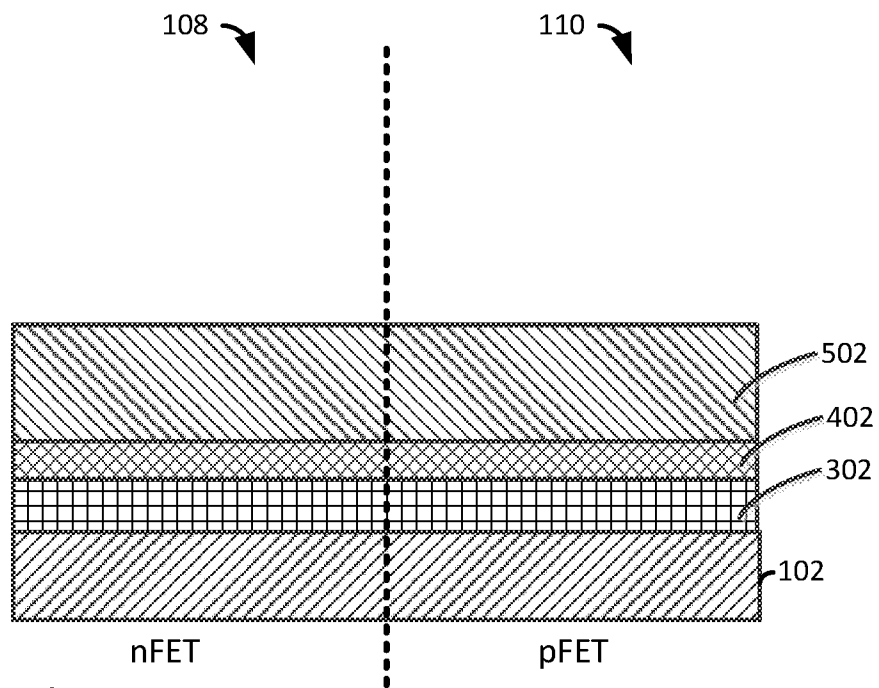
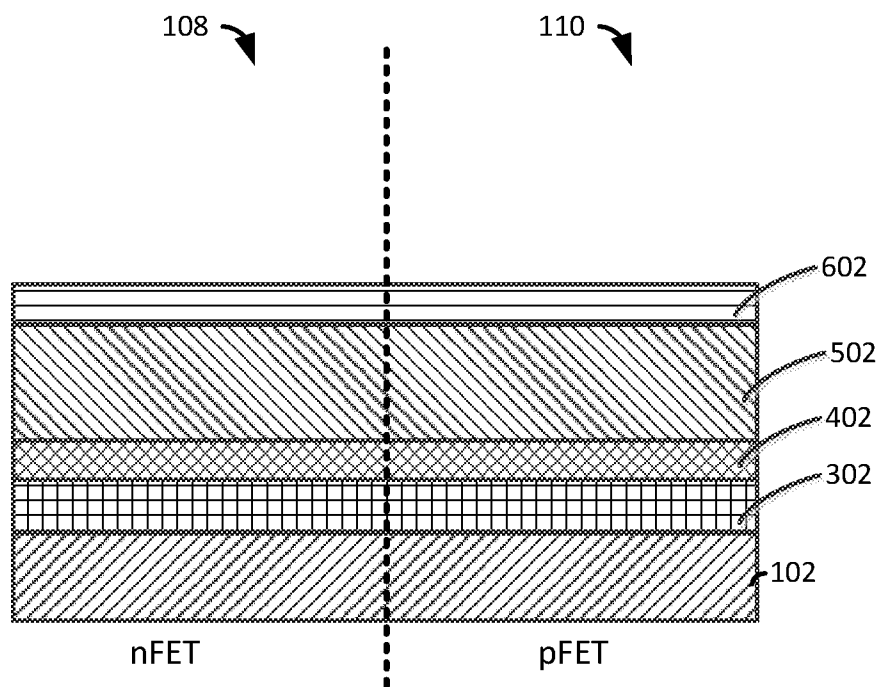


FIG. 4

**FIG. 5****FIG. 6**

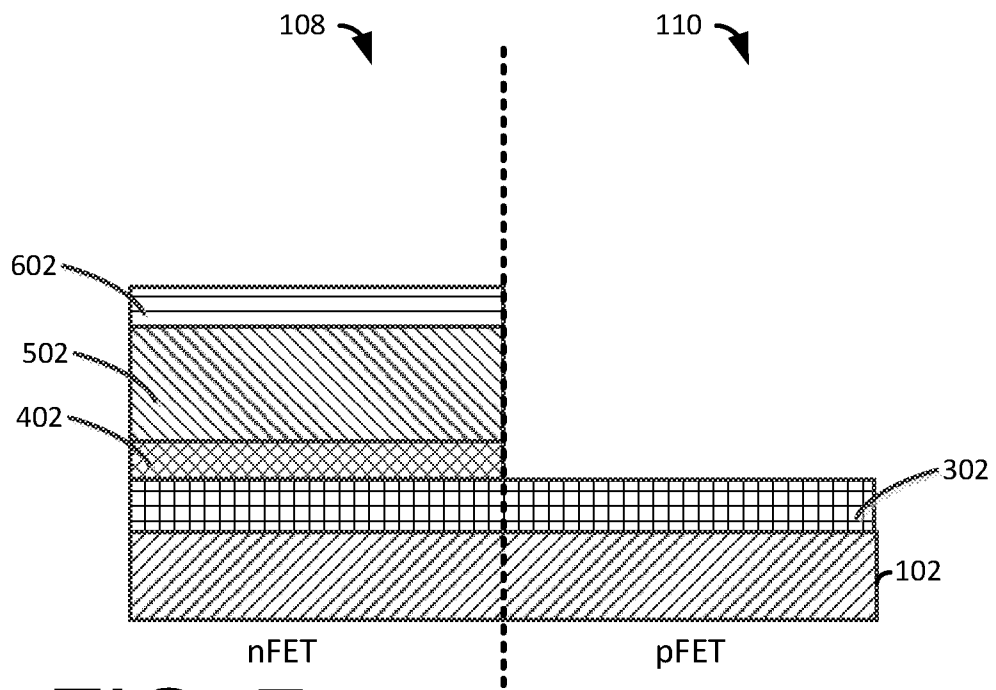


FIG. 7

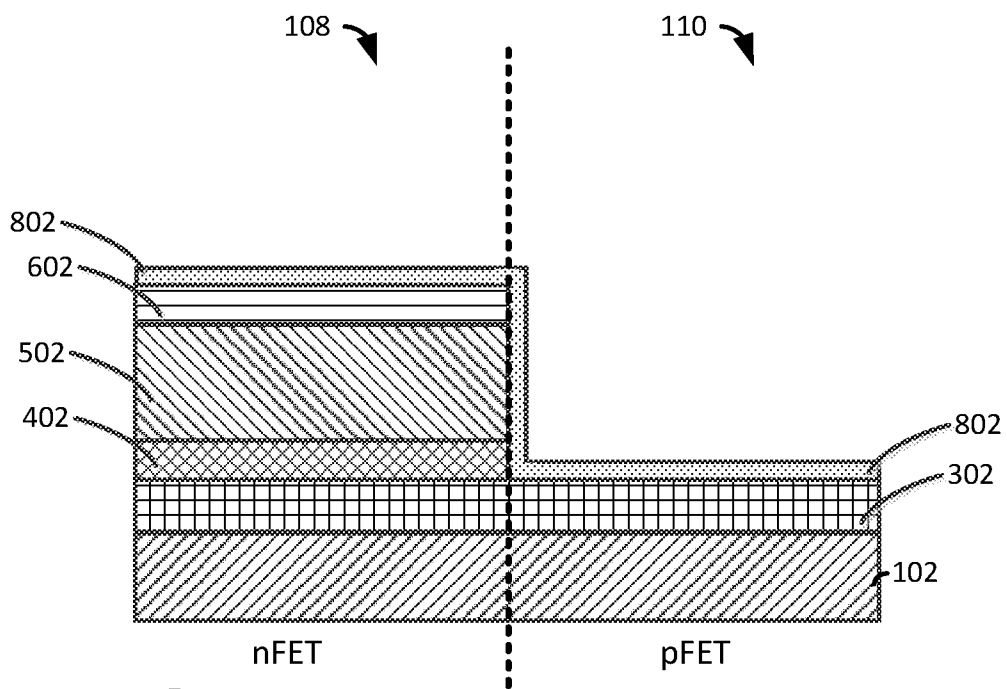


FIG. 8

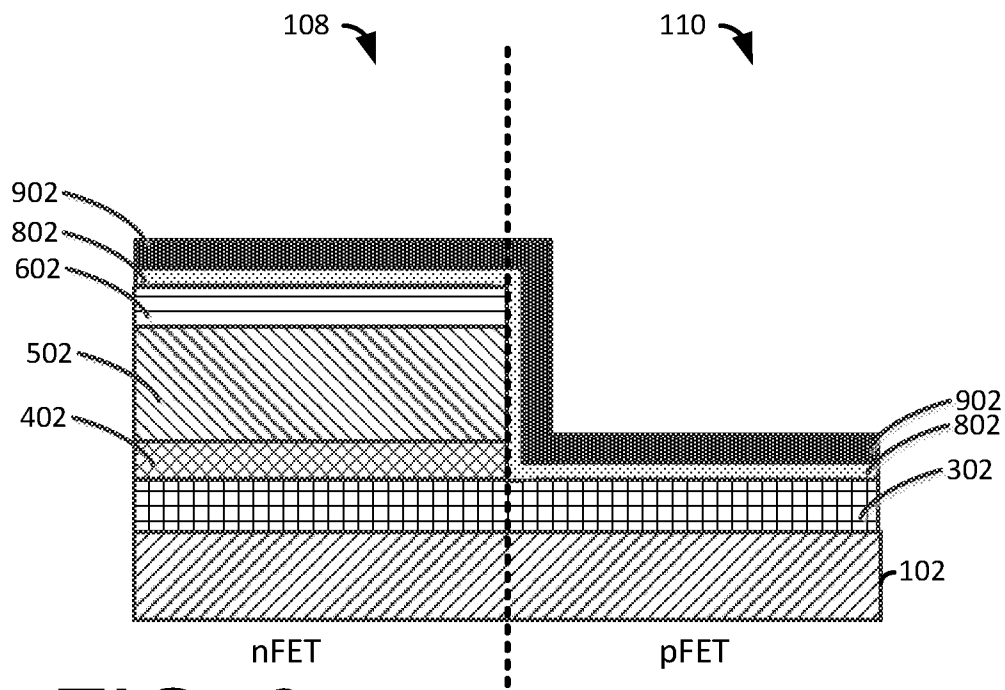


FIG. 9

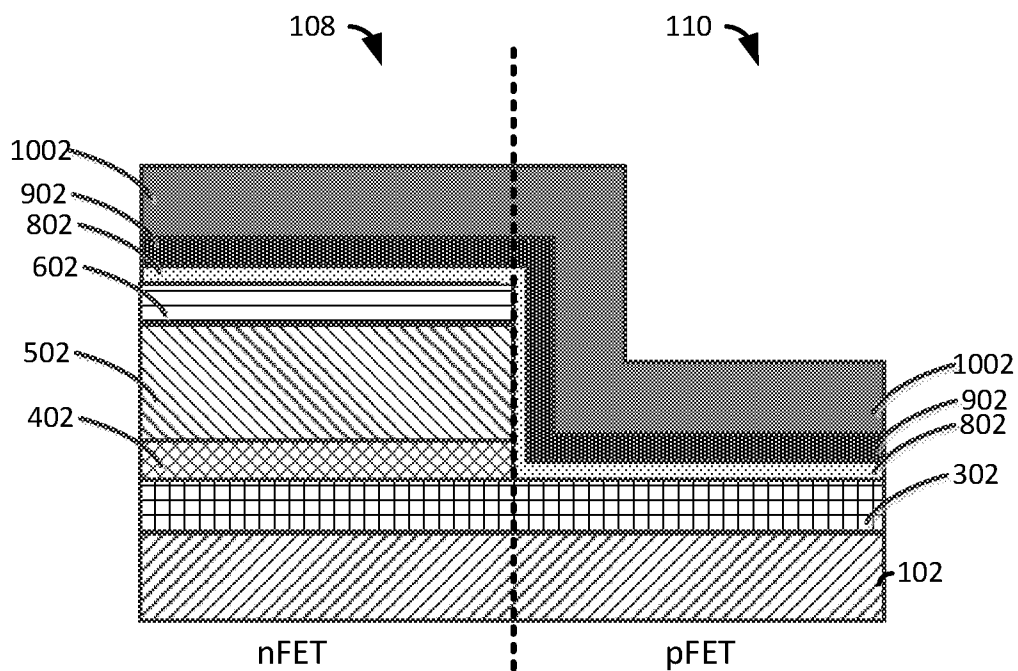


FIG. 10

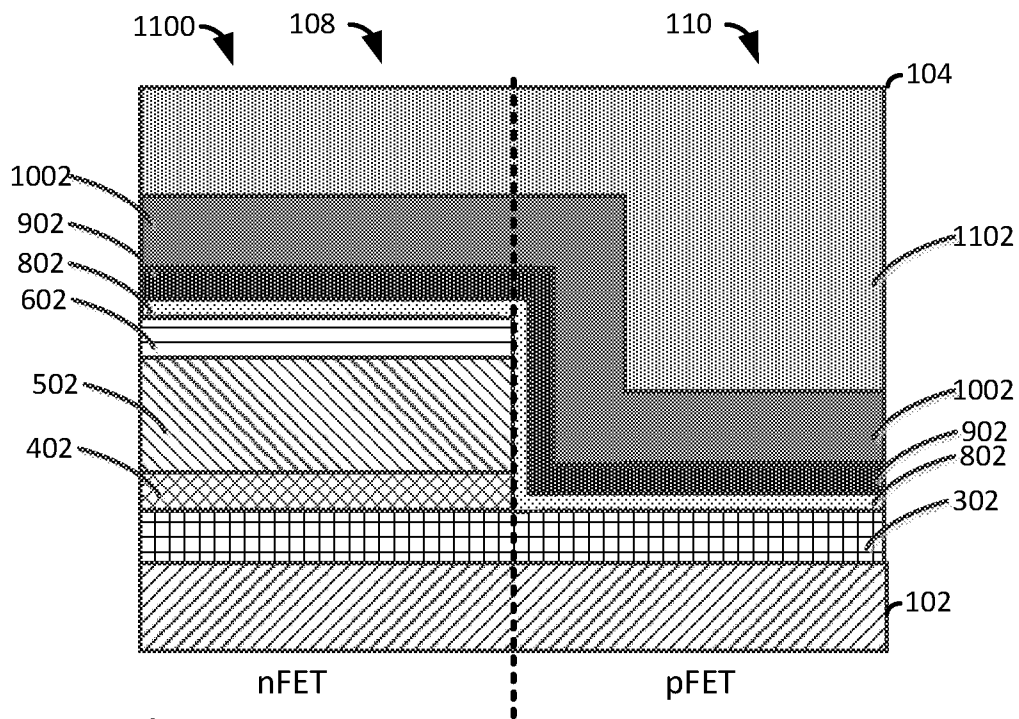


FIG. 11

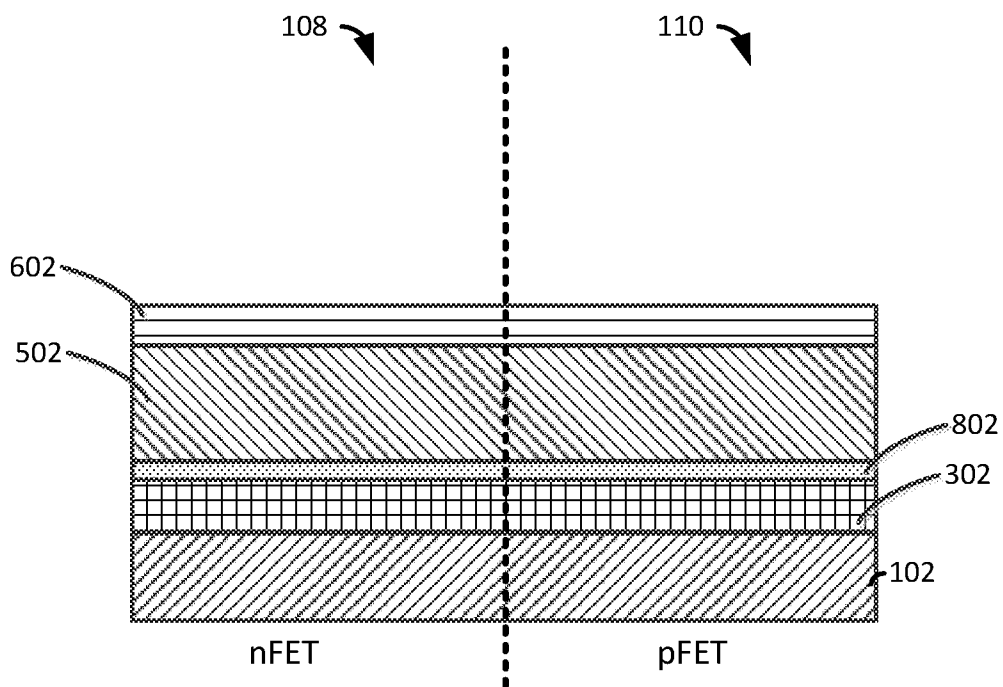


FIG. 12

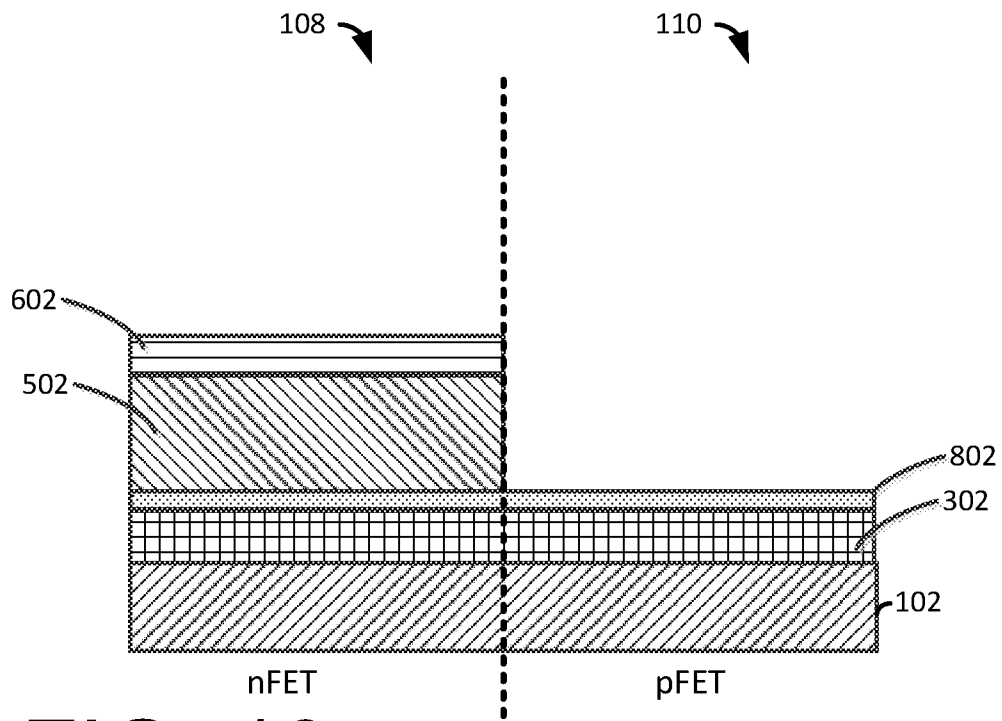


FIG. 13

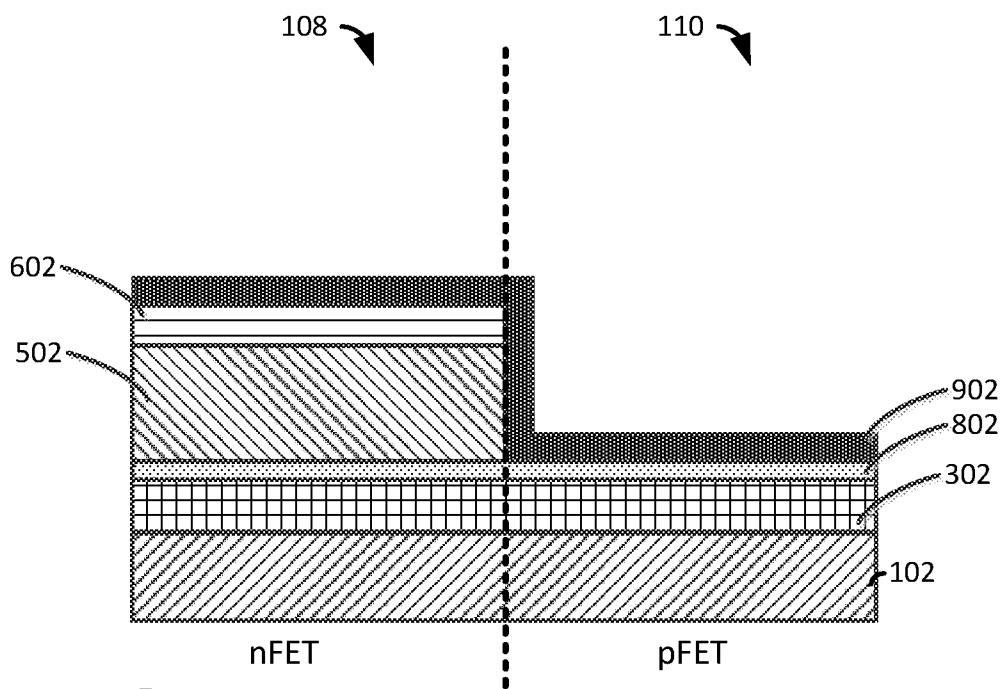


FIG. 14

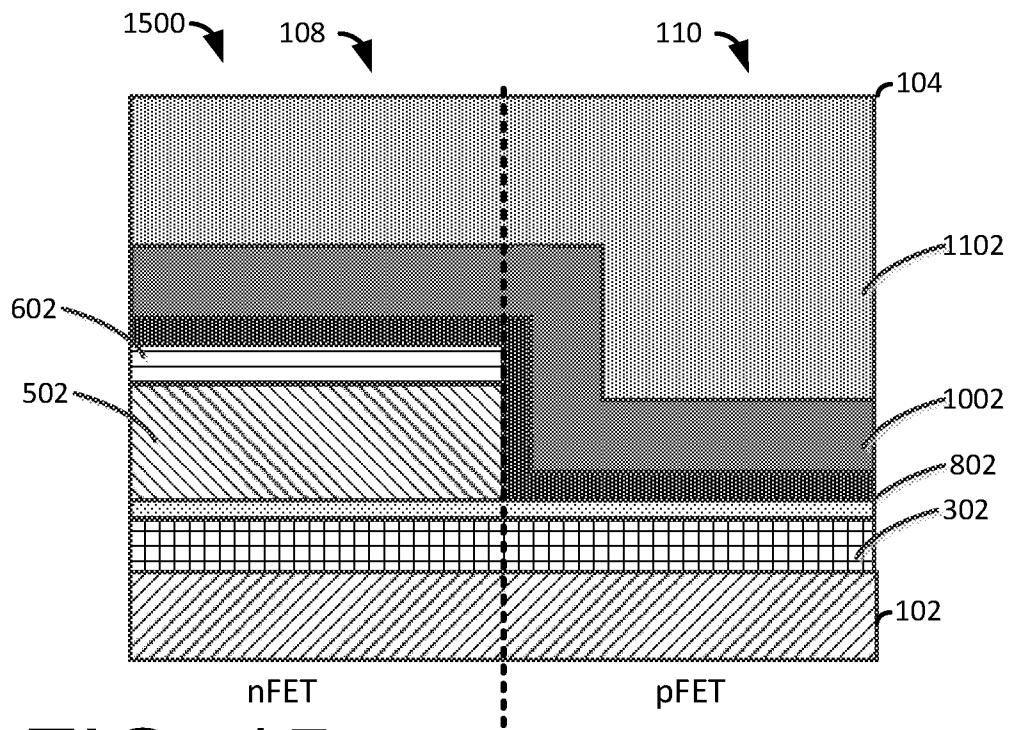


FIG. 15

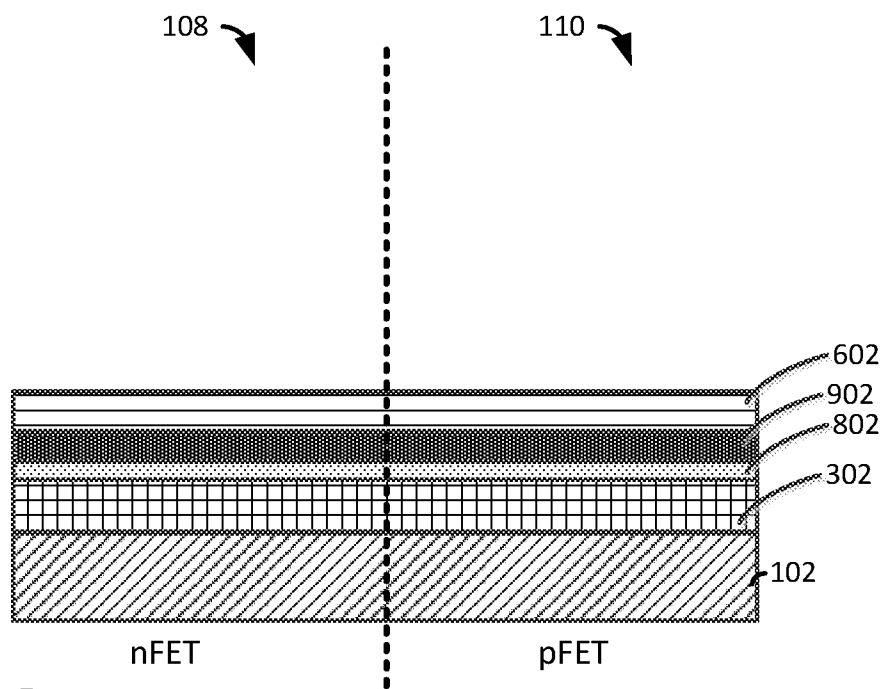


FIG. 16

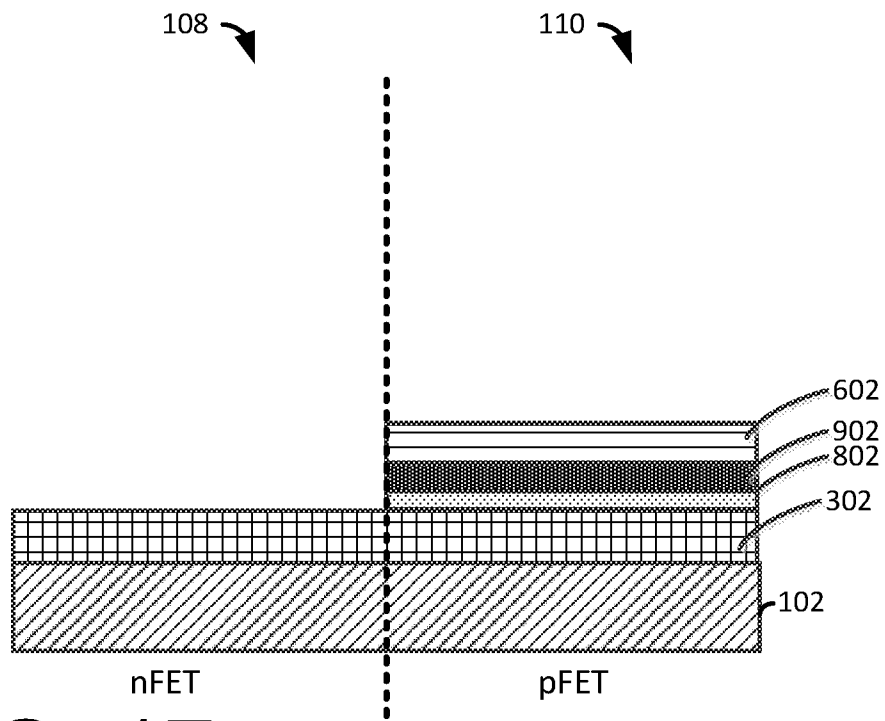


FIG. 17

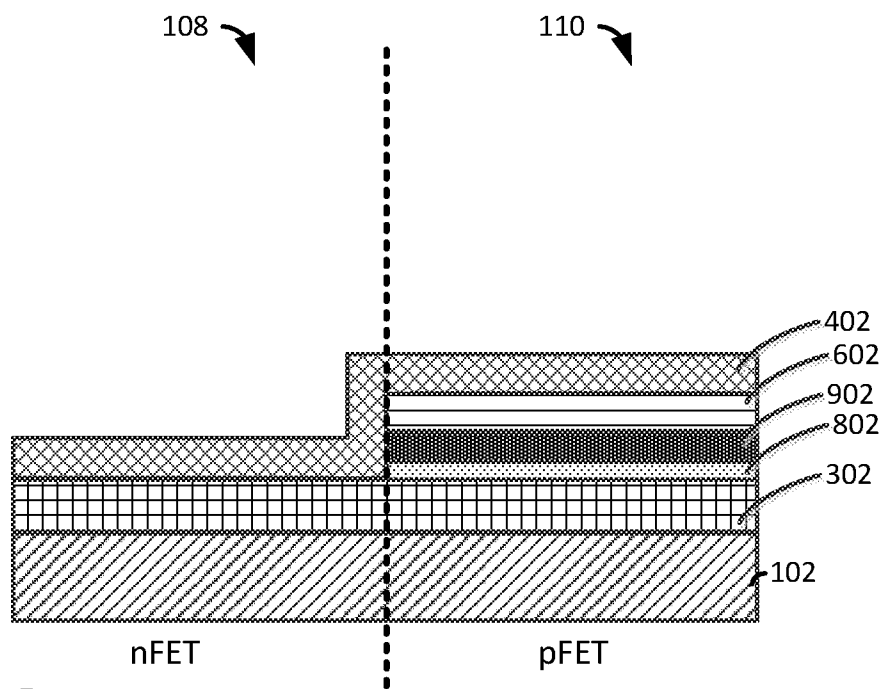


FIG. 18

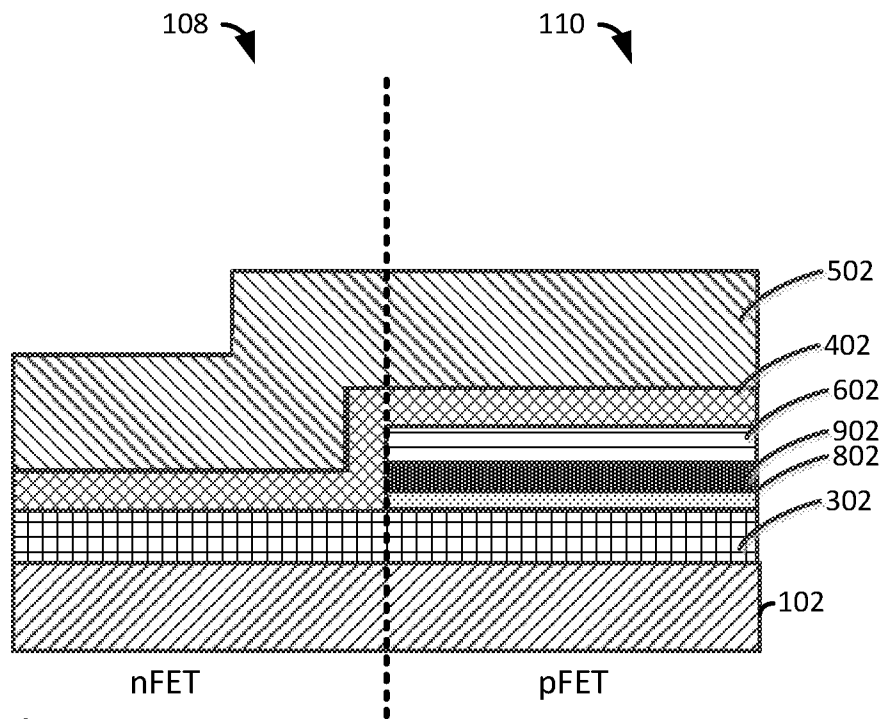


FIG. 19

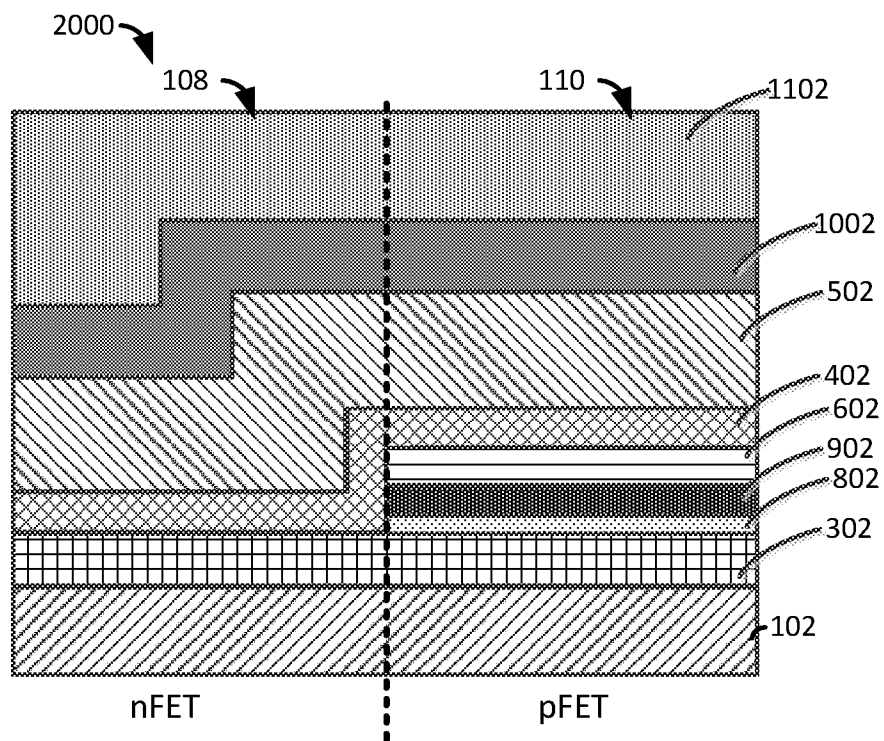


FIG. 20

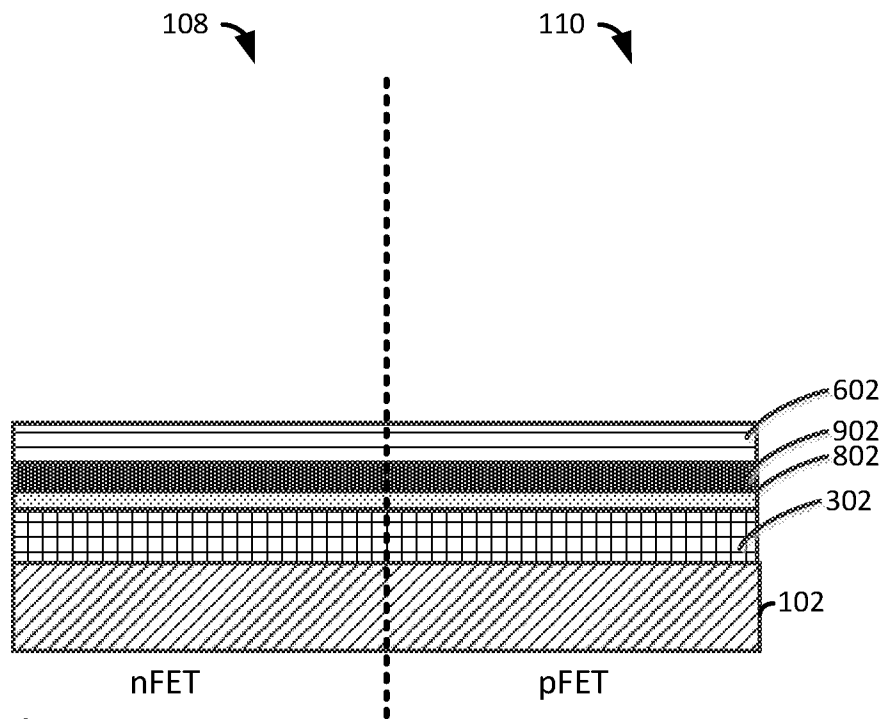


FIG. 21

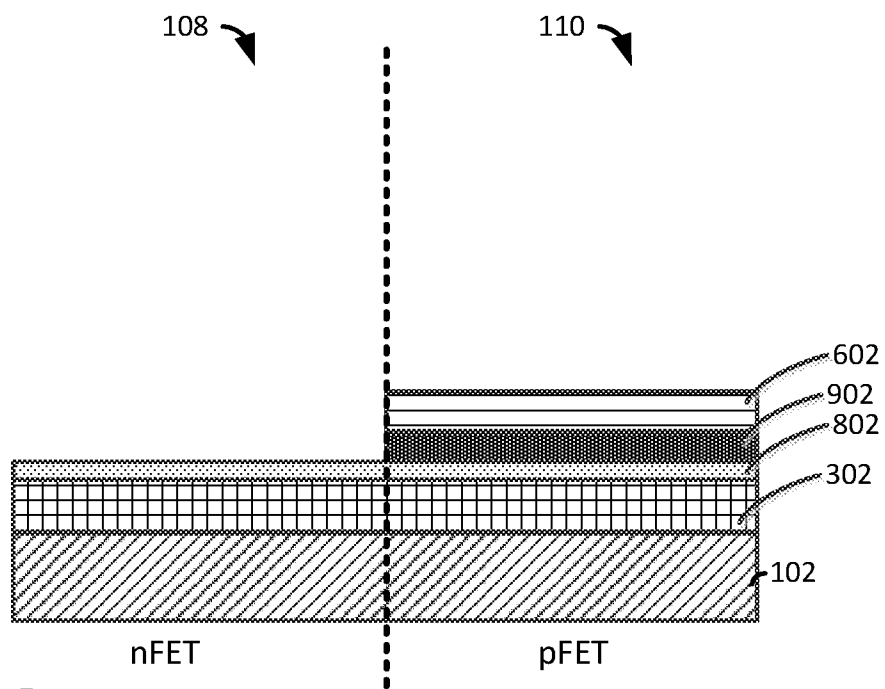


FIG. 22

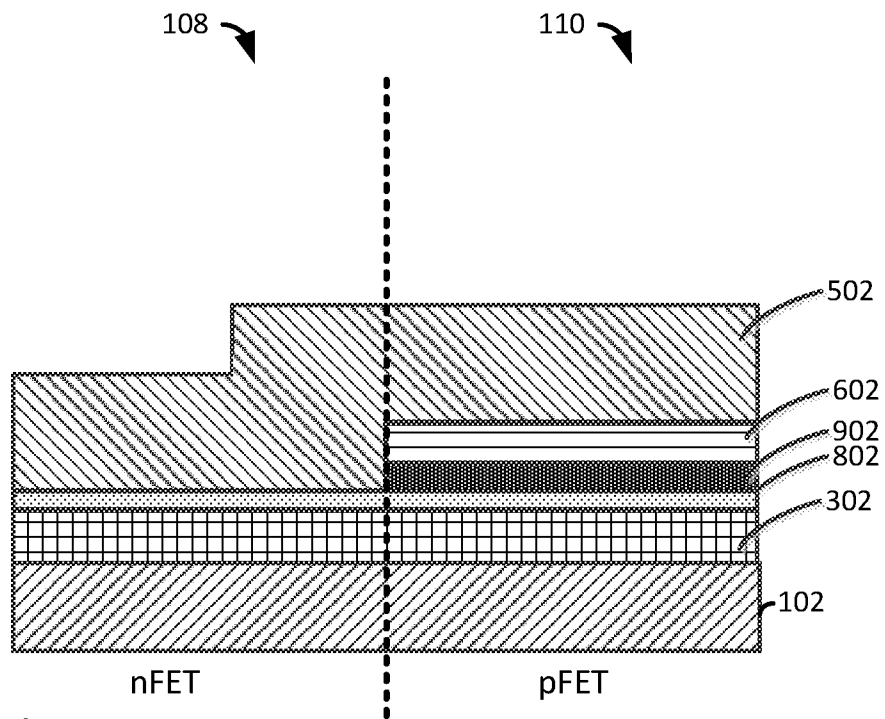


FIG. 23

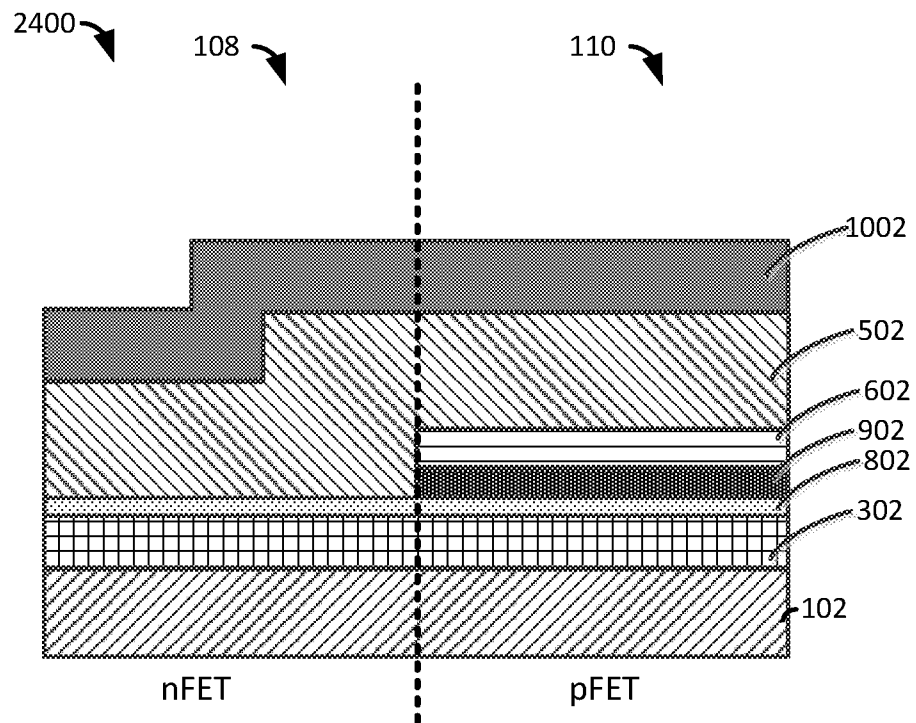


FIG. 24

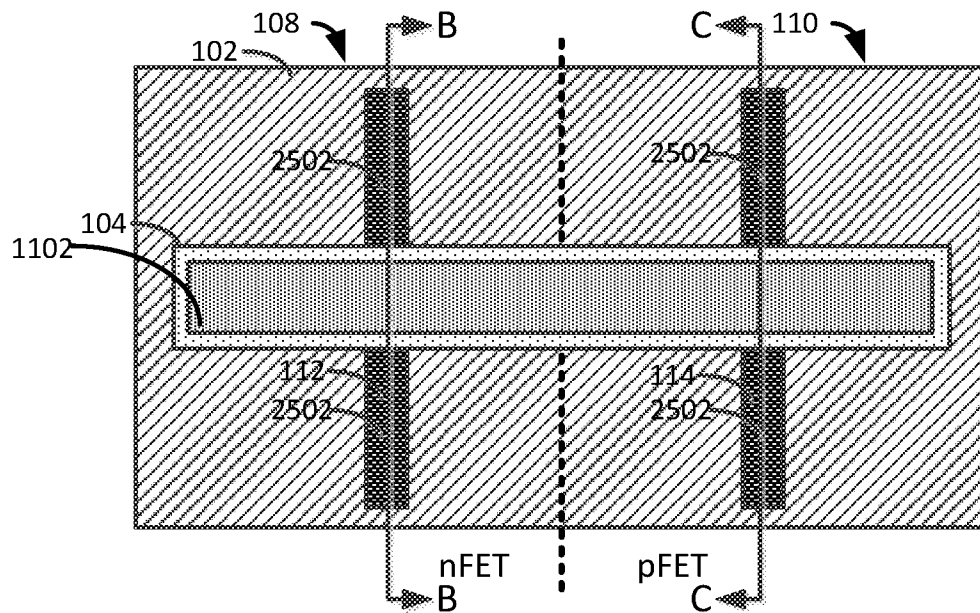


FIG. 25

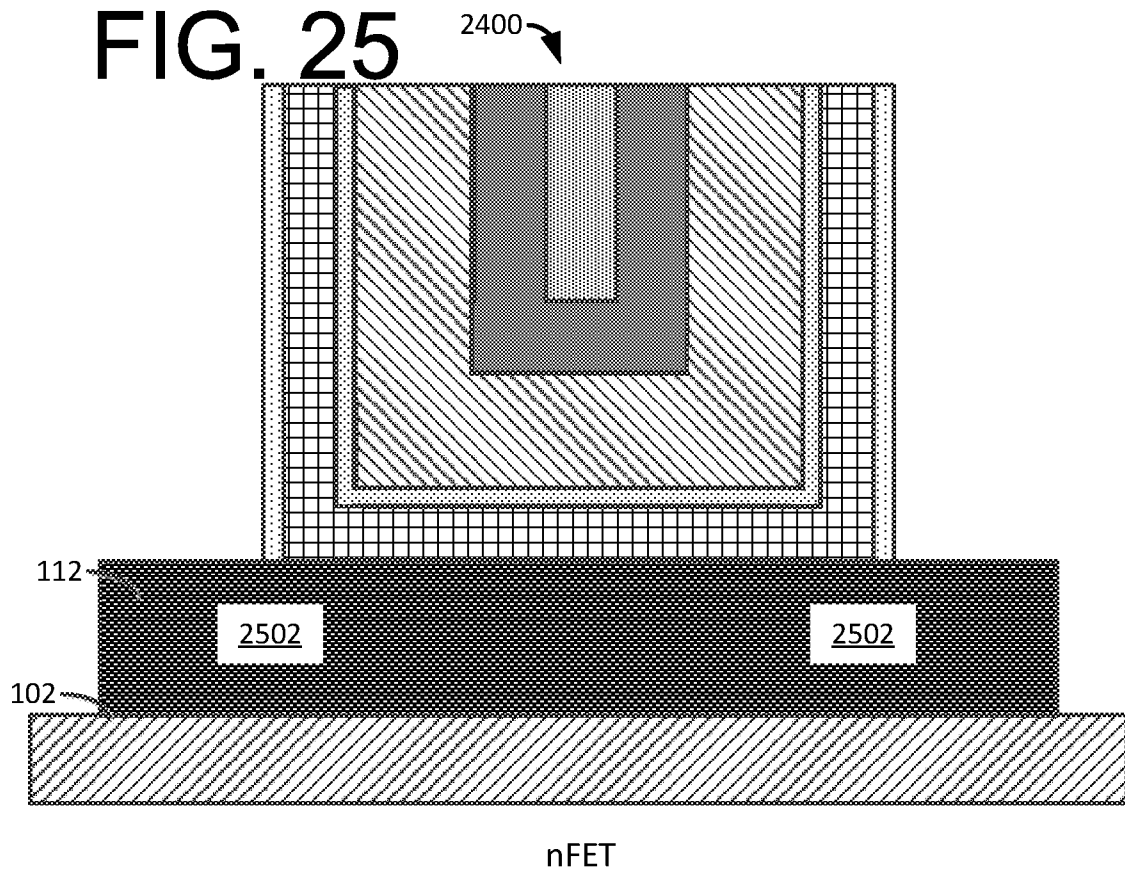


FIG. 26

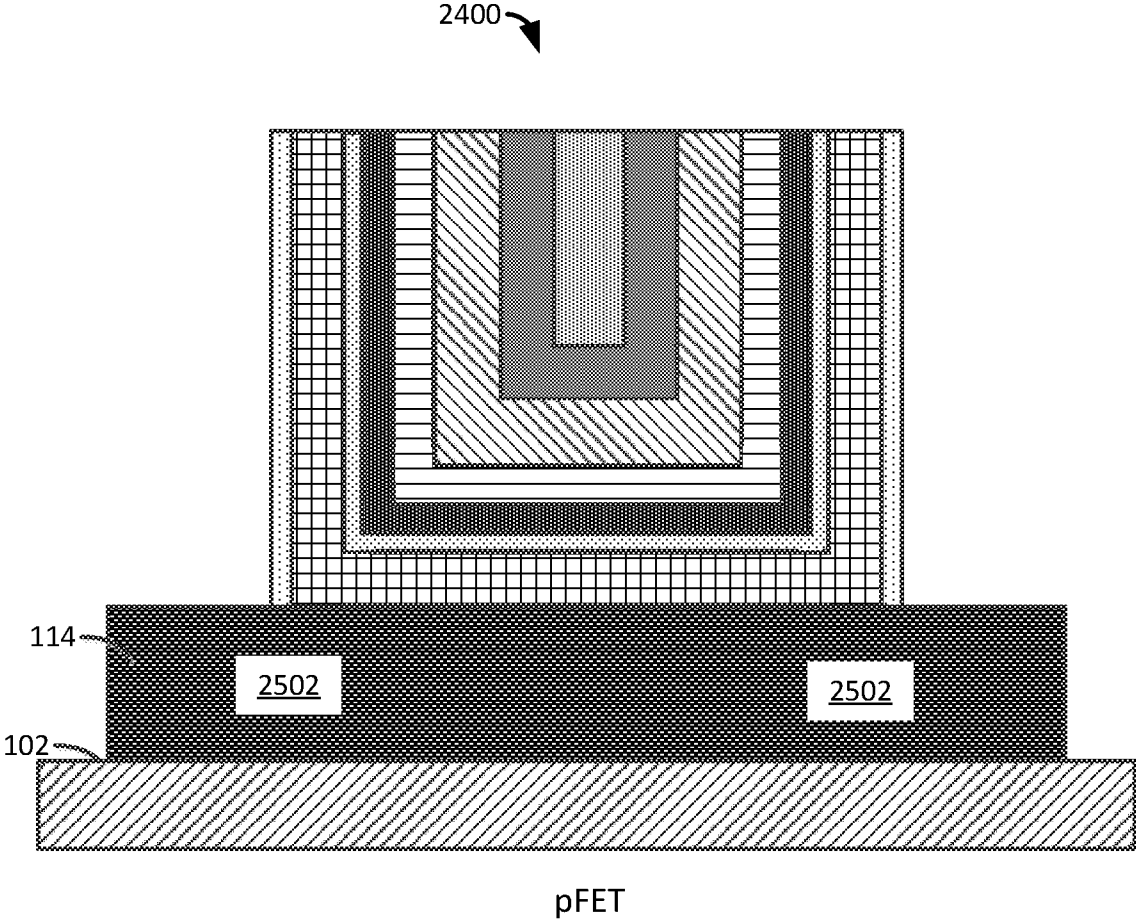
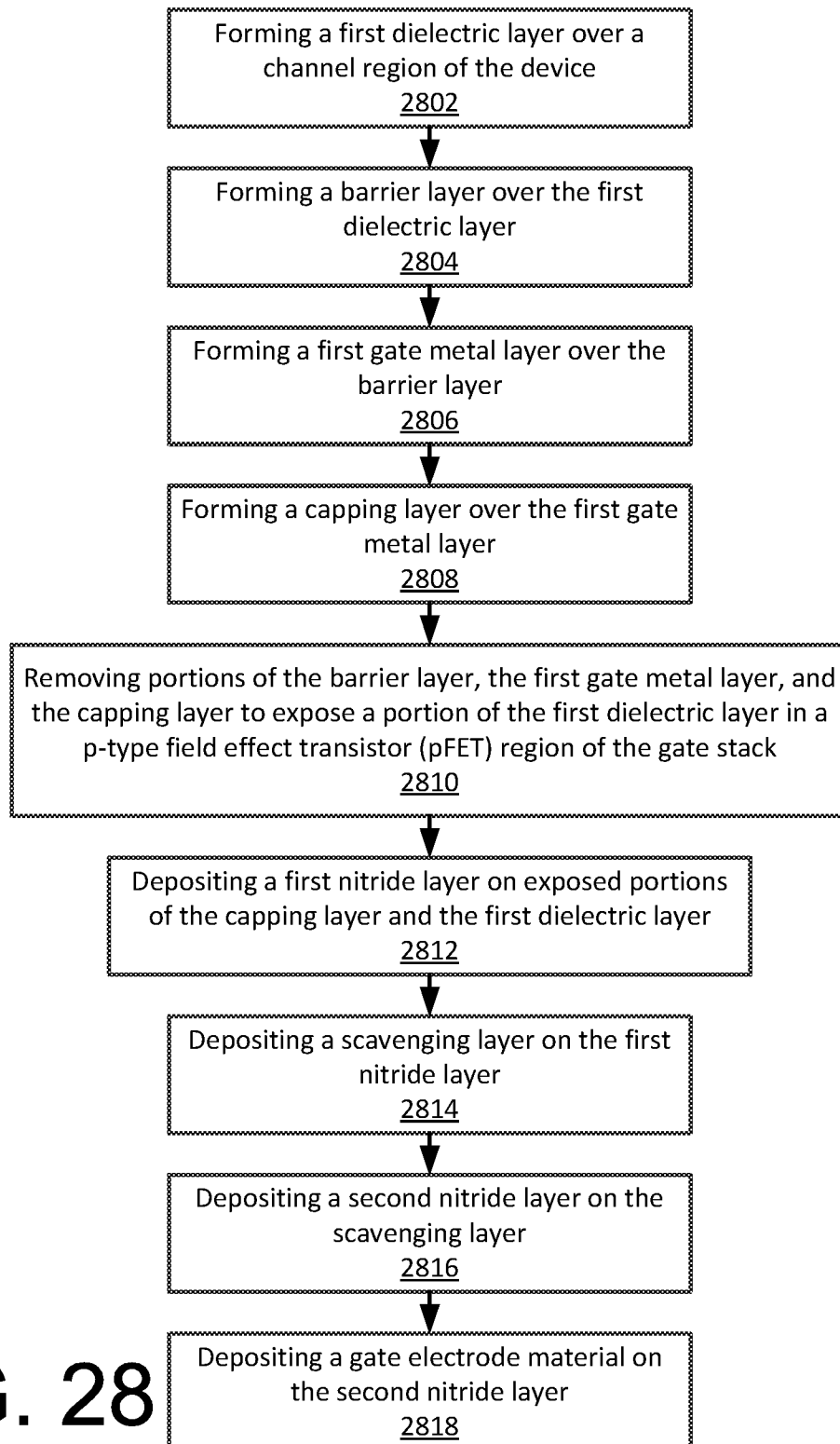


FIG. 27

**FIG. 28**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2017/050049

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/49(2006.01)i; H01L 21/8238(2006.01)i; H01L 27/092(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS;DWPI:gate, stack, dielectric, barrier, capping, scavenging, oxygen, strong, weak, nitride, second, another

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014004695 A1 (ANDO ET AL.) 02 January 2014 (2014-01-02) the whole document	1-15
A	CN 101930996 A (INT BUSINESS MACHINES CORP) 29 December 2010 (2010-12-29) the whole document	1-15
A	CN 103021862 A (TAIWAN SEMICONDUCTOR MFG CO LTD) 03 April 2013 (2013-04-03) the whole document	1-15

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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“E” earlier application or patent but published on or after the international filing date

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“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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“&” document member of the same patent family

Date of the actual completion of the international search

07 April 2017

Date of mailing of the international search report

24 April 2017

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Telephone No. (86-10)62411794

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/IB2017/050049

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				TW	201314790	A	01 April 2013
				US	2013078779	A1	28 March 2013
				TW	I456666	B	11 October 2014
				US	8597995	B2	03 December 2013
				KR	20130033266	A	03 April 2013