# United States Patent [19]

**Silverberg**

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[45] **Dec. 11, 1973**


[54] **OUTPUT KEYBOARD APPARATUS AND SIGNAL TRANSLATING METHODS THEREFOR**


[75] Inventor: **Morton Silverberg,** Rochester, N.Y.

[73] Assignee: **Xerox Corporation,** Stamford, Conn.



[22] Filed: **Aug. 2, 1972**

[21] Appl. No.: **277,264**

[52] **U.S. Cl.** ..... **340/365 C,** 178/17 C, 197/98, 340/365 S

[51] **Int. Cl.** ..... **G06f 3/02**

[58] **Field of Search** ..... 340/365 C, 365 L; 179/90 K; 178/17 C; 197/98



[56] **References Cited**

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3,691,555 9/1972 Looschen ..... 340/365 C



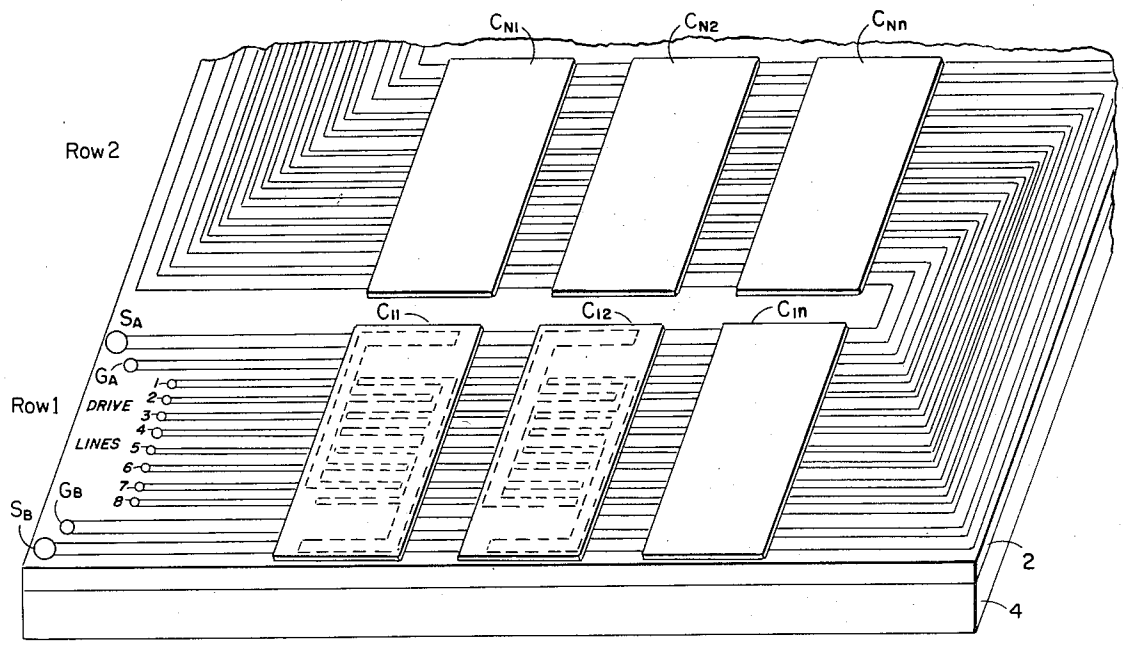
*Primary Examiner*—Thomas B. Habecker
*Assistant Examiner*—Robert J. Mooney
*Attorney*—James J. Ralabate



[57] **ABSTRACT**

Output keyboard apparatus and signal translating methods therefor are provided in accordance with the teachings of the present invention wherein, in at least one exemplary embodiment, sense conductors and a plurality of drive lines are associated with a selected number of keys within an output keyboard arrangement. A conductor arrangement which acts as a coding and coupling device is provided in association with each of the selected number of keys to selectively couple, upon the actuation of the key associated therewith, signals from the plurality of drive lines to the sense conductors in a predetermined coding sequence representative of the key depressed.


**44 Claims, 11 Drawing Figures**



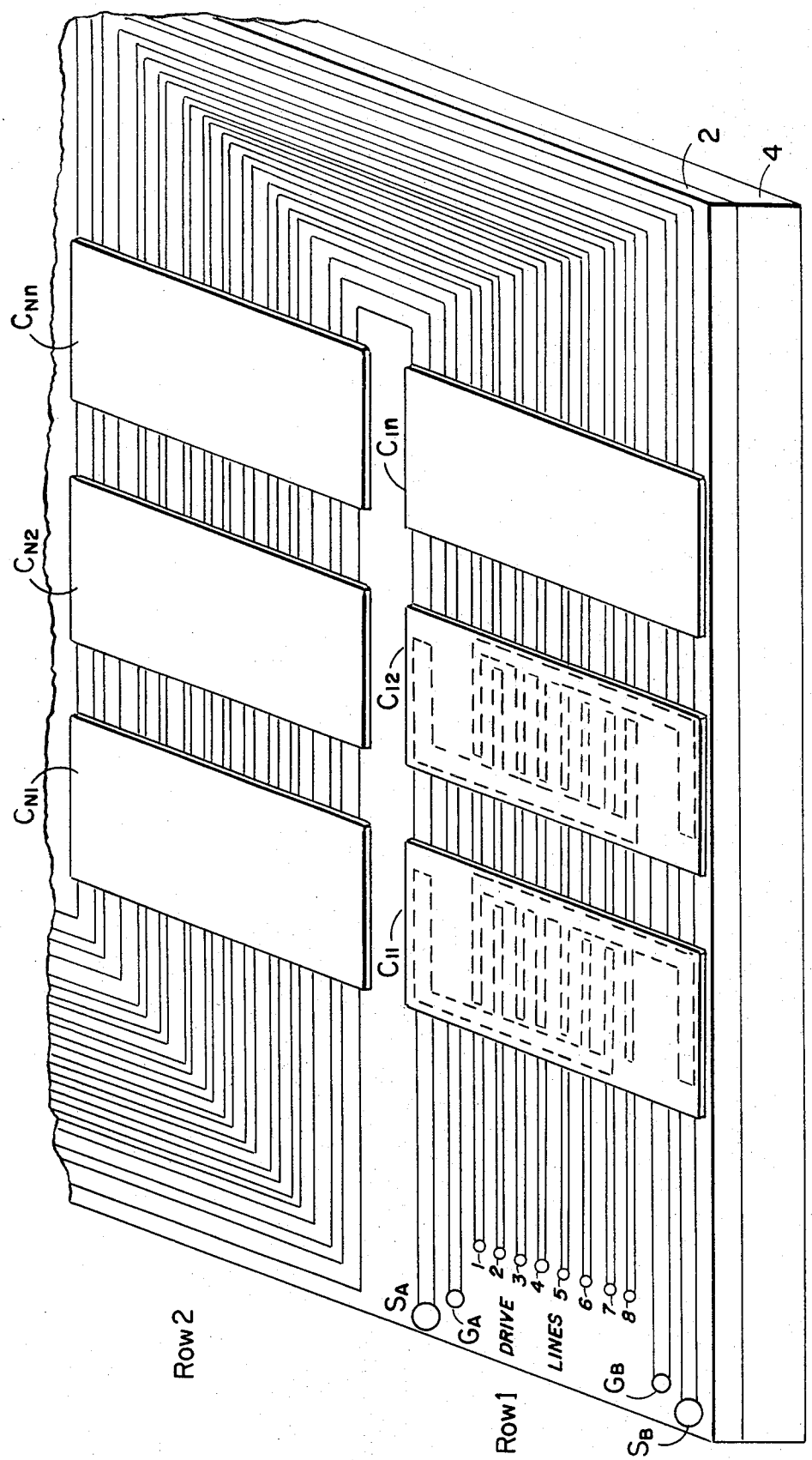

2
4
$C_{Nn}$
$C_{In}$
$C_{N2}$
$C_{I2}$
$C_{NI}$
$C_{II}$
$S_A$
$G_A$
1
2
3
4
5
6
7
8
DRIVE LINES
$G_B$
$S_B$
ROW 2
ROW 1

FIG. 1

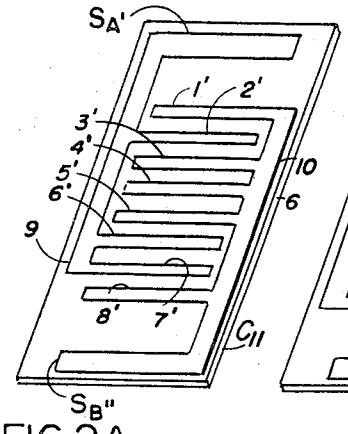



FIG.2A

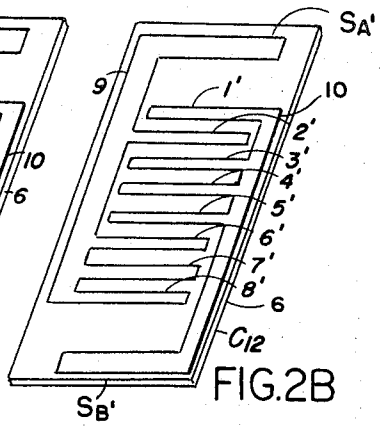



FIG.2B

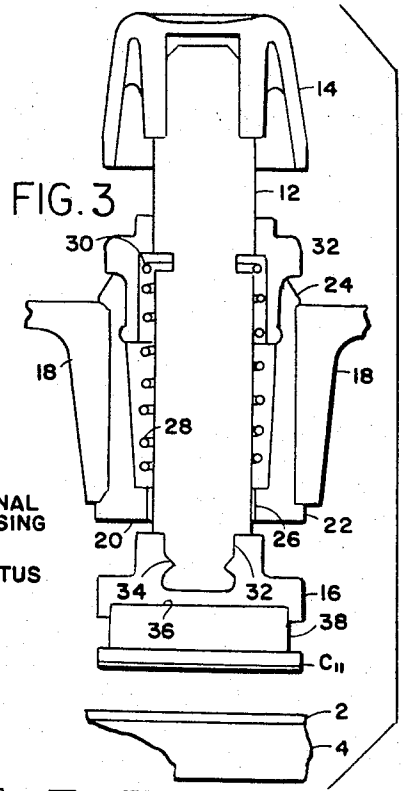



FIG.3

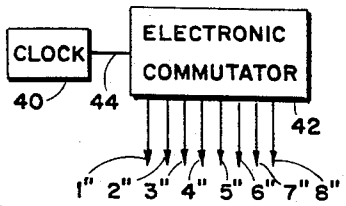



FIG.4A

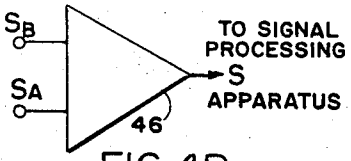



FIG.4B

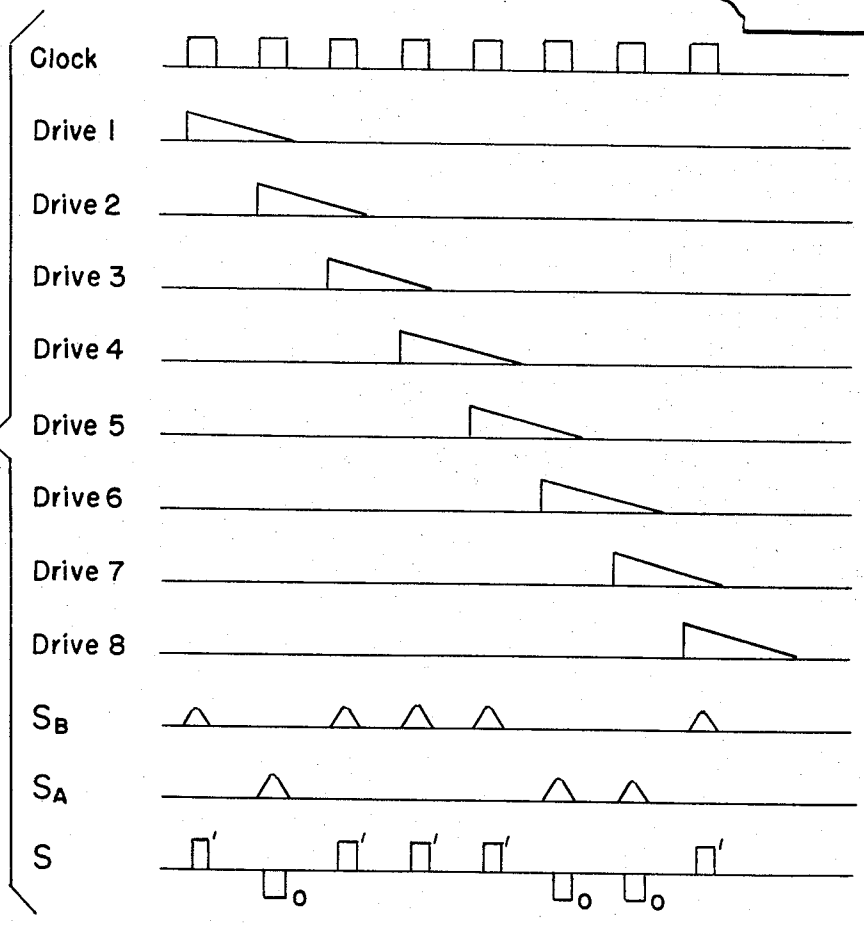



FIG.5

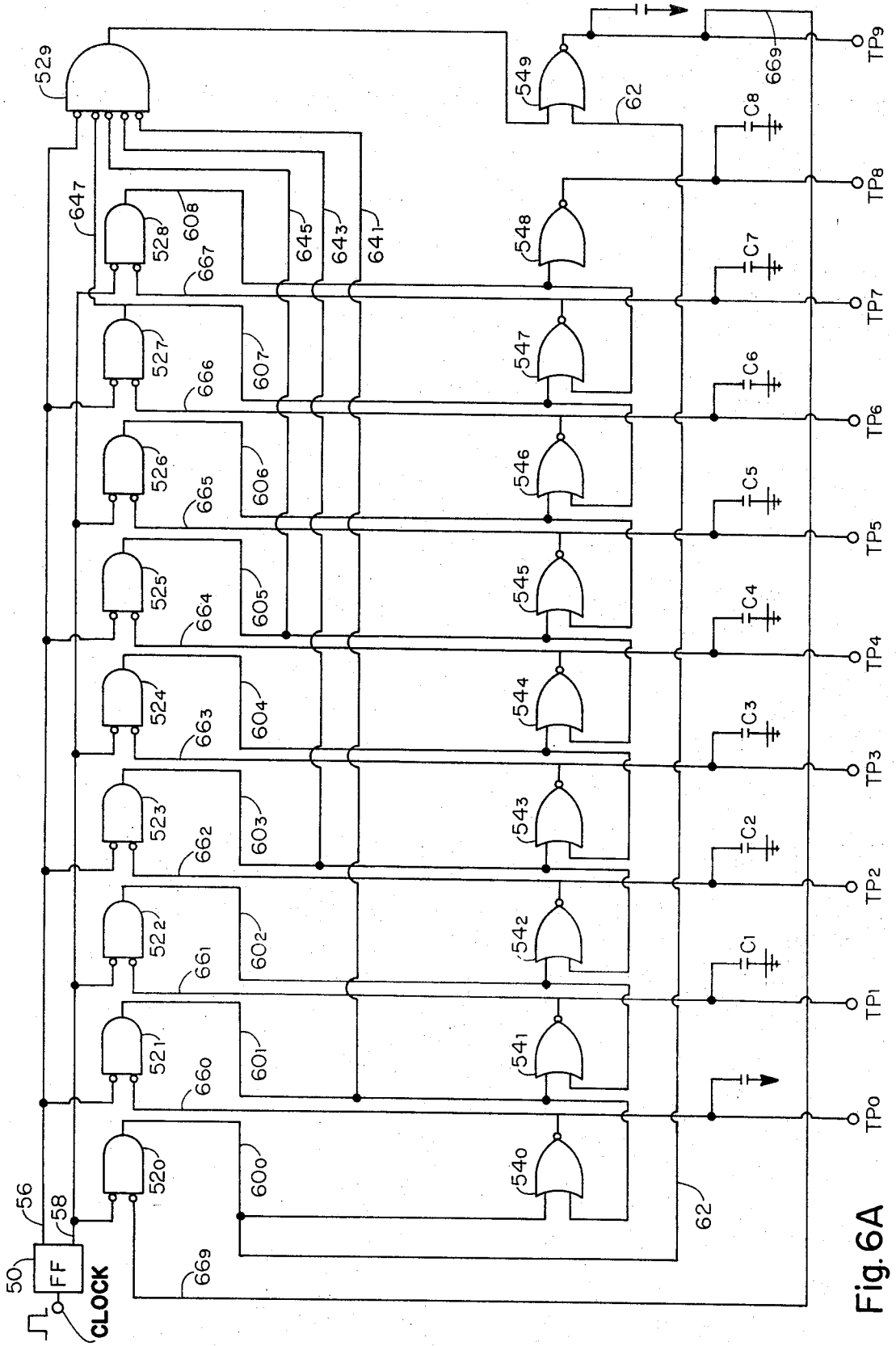

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601
660
520
600
669
56
58
50
FF
CLOCK
549
548
547
546
545
544
543
542
541
540
62
669
C8
C7
C6
C5
C4
C3
C2
C1
TP9
TP8
TP7
TP6
TP5
TP4
TP3
TP2
TP1
TP0

Fig. 6A

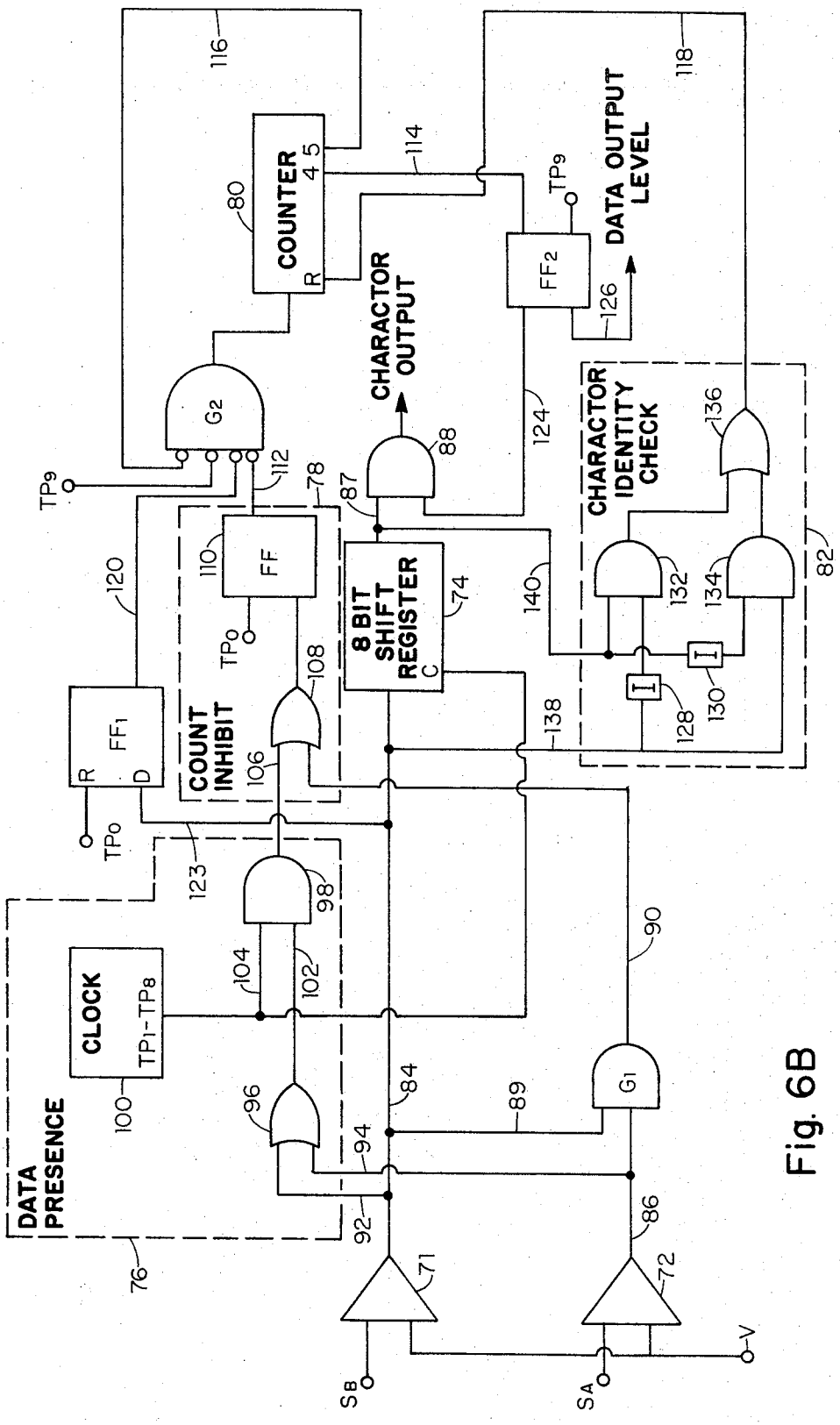

DATA PRESENCE
CLOCK
TP1-TP8
COUNT INHIBIT
FF
FF1
8 BIT SHIFT REGISTER
COUNTER
4 5
R
CHARACTOR OUTPUT
DATA OUTPUT LEVEL
FF2
CHARACTOR IDENTITY CHECK
G1
G2
TP0
TP9
SA
SB
V
76
78
80
82
84
86
87
88
89
90
92
94
96
98
100
102
104
106
108
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Fig. 6B

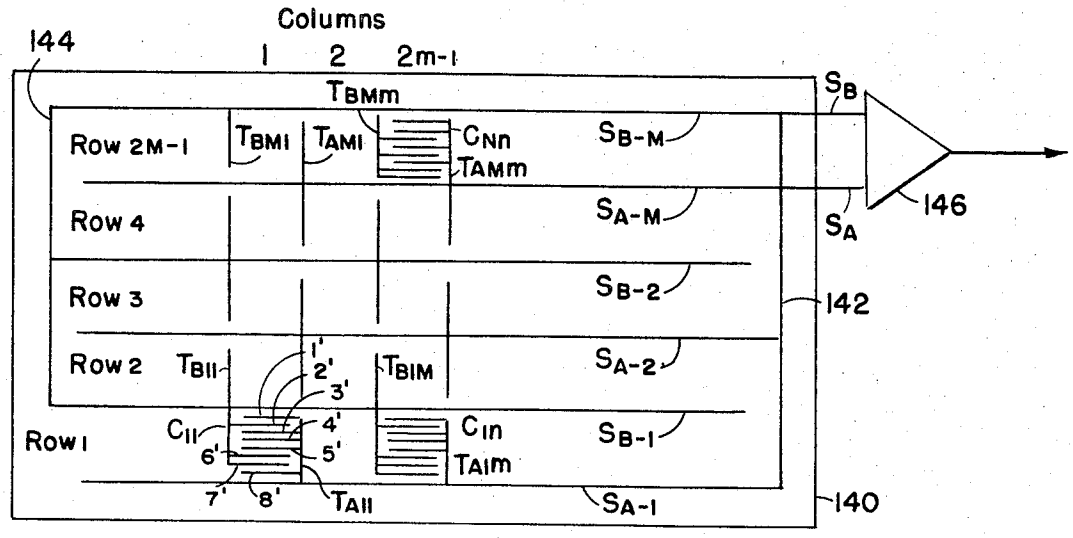

Columns
144
1
2
2m-1
TBMm
SB
Row 2M-1
TBM1
TAM1
CNn
TAMm
SB-M
Row 4
SA-M
SA
146
Row 3
SB-2
142
Row 2
TB11
1'
2'
3'
TB1M
SA-2
Row 1
C11
4'
6'
5'
C1n
TA1m
SB-1
7'
8'
TA11
SA-1
140

FIG. 7A

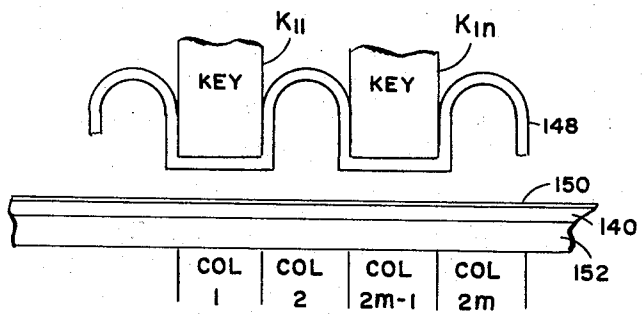

K11
K1n
KEY
KEY
148
150
140
152
COL 1
COL 2
COL 2m-1
COL 2m

FIG. 7B

# OUTPUT KEYBOARD APPARATUS AND SIGNAL TRANSLATING METHODS THEREFOR

This invention relates to selective signal translation techniques and more particularly to keyboard signal translating methods and apparatus therefor wherein input information is directly encoded and placed in a desired bit format so that it may be directly employed without further transformation.

The development of the vast majority of current state of the art keyboard arrangements may be directly tied to the development of the typewriter, calculator and printing arts wherein the primary function of each key in the keyboard was to enable the printing of the alphanumeric character or symbol associated with that key. Therefore, when it becomes necessary for such keyboard arrangements to do more than drive a print hammer or printing sphere, for instance to drive a CRT or to provide an output suitable for recording or transmission, output keyboard arrangements where developed by deriving an individual signal or group of signals as a function of the key actuated in previously developed keyboard structure and thereafter suitably altering the signals obtained to place them in appropriate form for further utilization. For instance, in the case of output keyboard arrangements present in multi-hammer typewriters, calculators and printers, the required output signals were generally obtained by providing an individual switch for each key. Each switch was adapted to be closed upon the depression of the key associated therewith and the output of each switch was applied to a coding arrangement in the form of a diode matrix, encoding tree or the like so that generally an eight bit code, capable of representing both character and function information, was obtained in parallel format. Thereafter, a parallel to series conversion was frequently employed to place the eight bit code in a form which could be directly utilized.

In output keyboard arrangements employed with equipment utilizing a printing sphere or similar other forms of single element printing devices, the depression of a key in the keyboard mechanically encodes the position of a plurality of bails or the like which control the mechanical positioning of the single element printing device. Therefore, individual switch means may here be associated with each of the bails to directly provide a plurality of encoded signals in a parallel bit form representative of the key depressed. However, even though mechanical encoding here replaces the electrical encoding necessary in the case of equipment employing a plurality of separate print hammers, the multi-bit parallel output of this form of output keyboard arrangement must frequently be serialized prior to its subsequent utilization.

Although the design of keyboard arrangements of the foregoing kind have been greatly improved by the substitution of microswitches and subsequently reed switches for the independent switch means originally employed to thereby reduce chatter and render them highly reliable, the basic design techniques for the majority of conventional keyboard arrangements have remained the same. Thus, if mechanical encoding is not associated with each key, a sense line must be provided for each key in the keyboard arrangement so that each independent key signal may be amplified, encoded and thereafter placed in a suitable bit format; while when mechanical encoding is employed a plurality of switch



means must be maintained in a manner to sense the condition of the mechanical encoding expedients and thereafter the coded signals obtained therefrom must be amplified, stored and placed in an appropriate serial or parallel format. Therefore, not only are such conventional keyboard arrangements highly expensive to produce when viewed from the standpoint of their mechanical complexity and sophistication but in addition thereto, a large number of switch means and individual sense lines must be provided to obtain the requisite number of independent signals to identify each key in the keyboard arrangement and, once such independent signals are obtained, appropriate electrical structure must be provided to amplify and serialize such independent signals in order to place them in a format in which they may be utilized. This has resulted in keyboard arrangements whose structure from both a mechanical and electrical standpoint is highly complex and costly to manufacture.

As the driving of a print hammer or single element printing device is often not the primary function of present day output keyboard arrangements and, in any event, since the printing function, using either impact or non-impact printing techniques, can be readily achieved as a function of the electrical signals provided by output keyboard arrangements, various improvements in output keyboard arrangements have been made with a view to reducing the mechanical complexity thereof. For instance, inductively coupled keyboard arrangements such as disclosed in U.S. Pat. No. 3,363,737, as issued to Tasahu Wada et al. on April 5, 1967, have been proposed. These inductively coupled keyboard arrangements are highly simplified from a mechanical standpoint because magnet means associated with each key are employed in such manner that the flux linked by sense conductors which are also associated with each key is changed each time a key is depressed to thereby provide the output from each key depressed on an independent conductor. The outputs in each conductor are then encoded in a diode matrix and subsequently serialized so that while the resulting keyboard arrangement provides minimal mechanical complexity, the requisite electrical apparatus therefor is similar to that described above. Similarly, in U.S. Pat. No. 3,419,697, as issued to D.C. Gove on Dec. 31, 1968, there is disclosed capacitively coded push button apparatus suitable for use in keyboard arrangements. In this apparatus, electrostatic shielding have coding apertures therein is displaced as each key is depressed so that such apertures allow selective capacitive coupling between a transmission bar and receiving strips which are also associated with each key. This apparatus it not highly simplified from a mechanical or fabrication viewpoint because close manufacturing tolerances are required; however, it is highly advantageous because direct electrical coding is established at each key and hence the common bit positions associated with each key may be applied in parallel to a suitable parallel to serial converter to provide the advantages of the mechanical coding keyboard arrangements mentioned above without the mechanical complexity and switch means required thereby. However, even with this advantageous form of output keyboard arrangement, independent amplifier means are required for each of the relatively weak signal parallel outputs obtained, parallel to series converter means are needed to serialize the coded output obtained, the need for close manufactur-

ing tolerances for the individual key structures is present and since at least each apertured electrostatic shield associated with each key structure is different, the manufacturing steps associated therewith are not as simplified and uniform as would otherwise be desirable. Furthermore, the physical disposition required for the coding apertures and the receiving strips in the capacitively coded keyboard apparatus disclosed in U.S. Pat. No. 3,419,697, supra, would appear to limit the number of bits which are practically available and hence limit the application of this apparatus to calculator embodiments or the like which do not require a large number of key identifying signals.

Therefore, it is an object of the present invention to provide keyboard signal translating methods and apparatus therefor for enabling input information to be directly encoded and placed in a desired bit format.

It is a further object of the present invention to provide improved keyboard signal translating methods and apparatus therefor wherein printed circuit techniques are employed to achieve highly simplified keyboard structure.

It is an additional object of the present invention to provide improved keyboard signal translating methods and apparatus therefore wherein a large number of code bits are readily available to enable the direct coding of input information from any practical number of input keys.

It is another object of the present invention to provide keyboard signal translating methods and apparatus therefor having a repetitive output occurring at a sufficiently rapid rate to allow testing prior to utilization.

It is a further object of the present invention to provide keyboard signal translating methods and apparatus therefor which enables the formation of keyboards wherein desired numbers of keys may readily be added or subtracted.

Other objects and advantages of the present invention will become clear from the following detailed description of several exemplary embodiments thereof, and the novel features will be particularly pointed out in conjunction with the appended claims.

In accordance with this invention, improved output keyboard signal translating methods and apparatus therefor are provided wherein sensing means and a plurality of drive conductors are associated with a selected number of keys within an output keyboard arrangement and coding means associated with each of said selected number of keys are provided to selectively couple, upon the depression of the key associated therewith, signals from said plurality of drive conductors to said sensing means in a predetermined coding sequence representative of the key depressed.

The invention will be more clearly understood by reference to the following detailed description of several exemplary embodiments thereof in conjunction with the accompanying drawings in which:

FIG. 1 is a pictorial view of an examplary embodiment of the present invention;

FIGS. 2A and 2B are detailed views of coding and coupling means employed in the exemplary embodiment of the present invention illustrated in FIG. 1;

FIG. 3 illustrates exemplary depressible key structure for the exemplary embodiment of the invention depicted in FIG. 1;

FIGS. 4A and 4B illustrate exemplary input and output circuitry for the exemplary embodiment of this invention depicted in FIG. 1 wherein FIG. 4A schematically shows input circuitry for the drive conductors illustrated in FIG. 1 and FIG. 4B schematically shows differential amplifier means for the sensing means illustrated in FIG. 1;

FIG. 5 is a timing diagram illustrating an exemplary cycle of operation for the exemplary embodiment of the invention depicted in FIG. 1;

FIGS. 6A and 6B illustrate another form of input and output circuitry for the exemplary embodiment of the invention depicted in FIG. 1; and

FIGS. 7A and 7B illustrate another exemplary embodiment of the present invention.

Referring now to the drawings and more particularly to FIG. 1 thereof, there is shown an exemplary embodiment of output keyboard apparatus in accordance with the teachings of the present invention. The exemplary embodiment of the instant invention depicted in FIG. 1 comprises a printed circuit board 2, a ground plane 4 therefor and a plurality of coding and coupling elements $C_{11}$–$C_{Nn}$. The printed circuit board 2 may comprise a conventional printed circuit board having a plurality of printed conductors $S_A$, $G_A$, 1–8, $G_B$ and $S_B$ formed thereon. The printed conductors $S_A$, $G_A$, 1–8, $G_B$ and $S_B$ may be formed by conventional etching or plating techniques or the like or alternatively, the printed conductors may be formd with conductive inks because, as shall be seen below, the capacitive coupling employed in this embodiment of the instant invention does not require that substantial currents be utilized. In fact, as essentially zero current is required to be carried by the plurality of printed conductors $S_A$, $G_A$, 1–8, $G_B$ and $S_B$, high quality printed conductors are not required and this reduces the fabrication costs of the printed circuit board 2 to a substantial degree. The printed conductors $S_A$, $G_A$, 1–8, $G_B$ and $S_B$ are disposed in serpentine fashion on the printed circuit board 2 in the manner indicated in FIG. 1 so that a plurality of rows 1 and 2 are formed thereby with the printed conductors $S_A$, $G_A$, 1–8, $G_B$ and $S_B$ in adjacent rows being oppositely directed in order to achieve noise reduction. Although only two rows 1 and 2 of printed conductors have been illustrated in FIG. 1, it will be appreciated that as many rows of printed conductors $S_A$, $G_A$, 1–8, $G_B$ and $S_B$ may be employed as desired and that each row will underlie a row or column, as desired, of keys in the keyboard arrangement formed. Furthermore, although a single printed circuit board 2 will normally be employed for all of the character and function keys present on the keyboard due to the large and readily variable number of coded bits available with the instant invention, a plurality of separate printed circuit boards may be employed to separate function and character information or for other arbitrary separations should such separations be desired. It should be noted, however, that usually a single printed circuit board 2 will be preferred as one highly advantgeous attribute of this configuration is that all bits read therefrom are presented in serial format.

The printed conductors $S_A$ and $S_B$ are sense conductors which, as shall be seen below, receive discretely coded bit information for each key depressed directly in serial format. For the purpose of the instant disclosure, printed conductor $S_A$ should be considered to be the Zero (0) bit sense conductor while printed conductor $S_B$ is the One (1) bit sense conductor; however, as will be appreciated by those of ordinary skill in the art,

this assignment is strictly arbitrary and may be varied at will.

The printed conductors **1–8**, as indicated in FIG. **1**, are drive lines which have pulses applied in sequence thereto in such manner that only one drive line receives the leading edge of a drive pulse at a given instant aNd the pulsing sequence for all of such drive lines is completed at least once for each readout of the coded bit information sequence associated with each key. Each of the drive lines **1–8** here represents one bit in the code sequence associated with each key and, as shall be seen below, the manner in which information applied to each of the drive lines **1–8** is selectively coupled to sense conductors $S_A$ or $S_B$ is determined by the coding arrangement associated with each key. Although any number of drive lines may be employed to provide as large or as small a number of distinct bits for coding as is desired, eight (**8**) printed conductors **1–8** have here been shown at eight (**8**) bits are normally sufficient for the appropriate coding of character and function information in most keyboard arrangements and are readily converted to an ASCII code format which is highly desirable when viewed from the standpoint of the data format required by many types of utilization equipment presently available.

The printed conductors $G_A$ and $G_B$ are conductors which are grounded in order to aid in isolating sense conductors $S_A$ and $S_B$ to thereby reduce noise and cross-talk between drive lines **1–8** and the sense conductors $S_A$ and $S_B$. Grounded conductors $G_A$ and $G_B$ are optional, as are many of the noise reduction techniques employed herein; however, it is preferred that some noise reduction techniques be employed so that clearly defined code sequences are produced on the sense conductors $S_A$ and $S_B$ and spurious outputs do not result. Although in the embodiment of this invention illustrated in FIG. **1**, the printed conductors $S_A$, $G_A$, **1–8**, $G_B$ and $S_B$ have been illustrated as being of different widths, this mode of illustration has been employed primarily to aid the reader in identifying the various types of conductors present on the printed circuit board **2** and hence it should be appreciated that any widths may be employed for the printed conductors and that all of the printed conductors may be the same width or alternatively differing widths therefor could be employed. Alternatively, although printed conductors on a printed circuit board have been here employed, it should be appreciated that printed circuit cable or the like could be employed with equal facility.

The ground plane **4** may take the form of a conductive plate or layer upon which the printed circuit board **2** is disposed. The ground plane **4** is preferably referenced to ground and serves to reduce noise induced in all of the printed conductors $S_A$, $G_A$, **1–8**, $G_B$ and $S_B$ on the printed circuit board **2** and particularly in the sense conductors $S_A$ and $S_B$ which are of primary concern. The ground plane **4** is generally required because any printed conductor or loop acts as an antenna whose sensitivity is determined to a substantial degree by the area occupied thereby. A ground plane, however, as well known to those of ordinary skill in the art limits the sensitivity of such printed conductors or loops by making them sensitive only to low impedance inputs. Therefore, as most types of noise pickup are generally classifiable as a high impedance input, a high quality ground plane will accomplish a marked reduction in the noise coupled to the sense conductors $S_A$ and $S_B$ and will substantially improve the signal-to-noise characteristics manifested thereby. Thus, although any conductive layer could be employed in an underlying relationship with the printed circuit board **2**, a high quality ground plane, such as a conductive plate, closely associated therewith is preferred. Furthermore, although the use of the ground plane **4**, the grounded conductors $G_A$ and $G_B$ and the serpentine winding configuration of the printed conductors $S_A$, $G_A$, **1–8**, $G_B$ and $S_B$ have been here illustrated as exemplary noise reduction techniques, any of the conventional noise reduction techniques employed in the computer arts may be used in conjunction with the present invention as additions or substitutions for any or more of those indicated above.

The plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ are arranged in rows and columns, as indicated in FIG. **1**, above the surface of the printed circuit board **2** with each coding and coupling element $C_{11}$–$C_{Nn}$ disposed in overlying relationship with respect to all of the printed conductors $S_A$, $G_A$, **1–8**, $G_B$ and $S_B$ in the row **1** or **2** or printed circuit board **2** over which that coding and coupling element is disposed. As shall be seen below, each one of the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ is associated with one key in the keyboard arrangement and hence there would ordinarily be one coding and coupling element for each key in the keyboard arrangement formed. Each of the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ is normally disposed in a horizontal plane which is sufficiently above the surface of the printed circuit board **2** so that no coupling between the printed conductors $S_A$, **1–8** and $S_B$ and individual ones of the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ results but may be displaced downward, in response to the depression of the key associated therewith, so as to be selectively brought into a capacitive coupling relationship with the printed conductors $S_A$, **1–8** and $S_B$. Each of the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ may take the form of a small printed circuit board having a printed conductor portion present on the lower surface thereof, as indicated by the dashed lines in elements $C_{11}$ and $C_{12}$, which corresponds to and is in registration with each of the printed conductors $S_A$, **1–8** and $S_B$ in the row of the printed circuit board **2** which that element overlies.

The nature of each of the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ may best be appreciated by an inspection of FIGS. **2A** and **2B** which are detailed views of coding and coupling means employed in the exemplary embodiment of the present invention shown in FIG. **1** and more particularly show coding and coupling elements $C_{11}$ and $C_{12}$ as viewed from the bottom. As shown in FIGS. **2A** and **2B** each of the exemplary coding and coupling elements $C_{11}$ and $C_{12}$ comprises a small printed circuit board **6** or spot having sense conductor coupling portions $S_A'$ and $S_B'$ and drive line sensing portions **1'–8'** formed thereon. The drive line sensing portions **1'–8'** are selectively connected to the sense conductor coupling portions $S_A'$ or $S_B'$ through conductor segments **9** and **10** in accordance with a predetermined coding technique so that an interdigitated coding configuration is formed which is unique to each of the coding and coupling elements $C_{11}$–$C_{Nn}$ and hence unique to the key in the keyboard arrangement associated therewith. For instance, if it is recalled that sense conductor $S_A$ represents the Zero (**0**) sense conductor

while sense conductor $S_B$ represents the One (1) sense conductor, it will be seen that for coding and coupling element $C_{11}$ as shown in FIG. 2A, the manner in which drive line sensing portions 2', 6' and 7' are connected through conductor segment 9' to sense conductor coupling portion $S_A'$ and drive line sensing portions 1', 3' – 5' and 8' are connected through conductor segment 10' to sense conductor coupling portion $S_B'$ forms an interdigitated coupling arrangement coded **10111001.** Similarly, the coding and coupling element $C_{12}$, as shown in FIG. 2B, has drive line sensing portions 2' and 6'–8' connected to sense conductor coupling portions $S_A'$ and drive line sensing portions 1' and 3'–5' connected to sense conductor coupling portion $S_B'$ so that the exemplary interdigitated coupling arrangement is coded **10111000.** In this manner, all of the coding and coupling elements $C_{11}$–$C_{Nn}$ present in the output keyboard arrangement depicted in FIG. 1 will be uniquely coded according to an eight bit binary code. Therefore, as an eight bit binary code is normally adequate to provide a unique code designation for all character and function information associated with the keys of conventional keyboard arrangements, the selective coding arrangementt depicted in FIGS. 2A and 2B would normally fulfill the requirements of most output keyboard designs; however, as will be apparent to those of ordinary skill in the art, more or less coding capacity may be readily provided by merely adding or subtracting drive lines on the printed circuit board 2 and adding or subtracting corresponding drive line sensing portions on each of the coding and coupling elements $C_{11}$–$C_{Nn}$. The sense conductor coupling portions $S_A'$ and $S_B'$ and drive line sensing portions 1'–8' may be formed on each of the small printed circuit boards or spots 6 forming the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ by any of the conventional techniques for forming printed conductors mentioned above.

As previously mentioned, each of the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ is associated with an individual key in the output keyboard arrangement formed and is normally disposed in a horizontal plane which is sufficiently above the surface of the printed circuit board 2 so that no coupling between the printed conductors $S_A$, 1–8 and $S_B$ and individual ones of the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ results. However, as was also brought out above, each of the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ may be displaced downwardly, in response to the depression of the key associated therewith, so as to be selectively brought into a capacitive coupling relationship with printed conductors $S_A$, 1–8 and $S_B$. In the exemplary embodiment of the invention illustrated in FIGS. 1 and 2A and 2B, capacitive coupling is not established between the printed conductors $S_A$, 1–8 and $S_B$ on the printed circuit board 2 and printed conductors $S_A'$, 1'–8' and $S_B'$, respectively, on the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ until an individual one of such plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ is displaced to within a few millimeters of the printed circuit board 2 by the depression of the key associated therewith. When this capacitive coupling relationship is established, however, each pulse applied in sequence to the drive conductors 1–8, as shall be considered in detail below, is sensed by the drive line sensing portion 1'–8' associated therewith, applied to the sense conductor coupling portion $S_A'$ or $S_B'$ connected thereto and thereafter capacitively coupled from the appropriate sense conductor coupling portion $S_A'$ or $S_B'$ back to its underlying sense conductor $S_A$ or $S_B$. In the embodiment of the invention illustrated in FIG. 1, there is a capacitance of approximately one picofarad (1 pf) associated with the capacative coupling in each direction and, although not illustrated, a thin insulating layer is provided over printed conductors $S_A$, $G_A$, 1–8, $G_B$ and $S_B$ and/or $S_A'$, 1'–8' and $S_B'$ so that shorting between the printed conductors being brought into close proximity will not result. Thus it will be appreciated that when one of the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ is brought into a coupling relationship with the row of printed conductors $S_A$, $G_A$, 1–8, $G_B$ and $S_B$ on the printed circuit board 2 which it overlies, as each of the drive lines 1–8 on the printed circuit board 2 is pulsed in sequence, each pulse will be capacitively coupled to the drive line sensing portion 1'–8' overlying the drive lines 1–8 and applied to the sense conductor coupling portion $S_A'$ or $S_B'$ connected thereto as determined by the coding arrangement for that coding and coupling element. Conversely, each drive line pulse which is thereby sensed and coded by its selective application to the sense conductor coupling portion $S_A'$ or $S_B'$ is capacitively coupled back to the underlying sense conductors $S_A$ or $S_B$ on the printed circuit board whereby for each key depressed in the keyboard arrangement, a series of eight coded pulses representing the key depressed is applied to the sense conductors $S_A$ and $S_B$ on the printed circuit board 2 where they may be subsequently employed in a manner to be further described below.

FIG. 3 illustrates exemplary depressible key structure for the exemplary embodiment of the invention depicted in FIG. 1 and more particularly depressible key structure which may be employed to selectively displace a coding and coupling element $C_{11}$–$C_{Nn}$ associated with that key into a capacitive coupling relationship with the printed conductors $S_A$, 1–8 and $S_B$ in an underlying row on the printed circuit board 2. At the outset, it should be appreciated that it is considered desirable that output keyboard arrangements according to the present invention convey an external physical appearance and touch characteristics which are similar to those exemplified by conventional keyboard arrangements within corresponding types of utilization equipment. Thus, if output keyboard arrangements according to the present invention are to be employed in typewriters, calculators, teleprinters or the like, the depressible keys therefor would generally be arranged in a similar manner to the arrangements generally employed in equipments of this type and the touch characteristics of the depressible key structure should be similar to that which operators of such equipments have grown accustomed to due to past experience with conventional equipment. Therefore, although any depressible keyboard structure capable of selectively displacing an associated coding and coupling element into a capacitive coupling relationship with an underlying row of printed conductors on the printed circuit board 2 could be employed; the depressible key structure depicted in FIG. 3 is considered to be highly desirable for utilization with typewriter, teleprinter or similar other types of equipment as it is inexpensive to manufacture while providing touch characteristics which are similar to those presently found in high quality typewriters or the like.

The exemplary depressible key structure shown in FIG. 3 comprises a central shaft **12** having a molded cylindrical button **14** mounted on a first end portion thereof and a housing **16** for supporting a coding and coupling element $C_{11}$ thereon mounted to a second end portion thereof. The central shaft **12** is mounted within the external housing **18** of the keyboard structure by a cylindrically shaped sleeve member **20** which is provided with a pair of annular shoulders **22** and **24** which enable the sleeve member **20** to be snapped into place from the underside of external housing **20.** The second end portion of the central shaft **12** protrudes through an apertured portion **26** of the sleeve member **20** and a bias return and touch spring **28** is disposed about the central shaft **12** to maintain the instant depressible key structure in a normally upwardly displaced condition and provide appropriate pressure or feel when the key is depressed. A stop ring **30** is mounted concentrically about the central shaft **12** to provide a bearing surface for the bias return and touch spring **28** and a cylindrical retaining member **32** is provided to complete and enclose the mounting assembly for the central shaft **12.** The cylindrical retaining member **32** is adapted, as shown, for pressure engagement, or alternatively, may threadably engage the sleeve member **20** so that when the cylindrical retaining member **32** is in place, the mounting assembly for the central shaft **12** is rapidly mounted in place within the external keyboard housing **18.** The molded cylindrical button **14** may take any conventional form of key indicia commonly employed in typewriters, calculators, teleprinters or the like and bears a designation of the character or function associated with that key on the surface thereof. The molded cylindrical button **14** is adapted to be force fit over the first end portion of the central shaft **12** in the manner indicated in FIG. **3.**

The housing **16** for supporting the coding and coupling element $C_{11}$ may take the form of a molded plastic member having a vertically disposed cup-like chamber **32** therein adapted to fit over a restricted section of the second end portion of the central shaft **12** as shown. The cup-like chamber may have an annular shoulder **34** formed on an interior wall thereof to engage a grooved portion of the central shaft **12** as shown or, alternatively, spring retaining clips may be employed. The underside of housing **16** may have a rectangular chamber **36** formed therein which is adapted to receive a cushioning pad **38** or the like. The cushioning pad **38** may comprise a suitable sponge material such as molded sponge rubber or the like and preferably has harder rubberlike material coated on the upper and lower surfaces thereof to provide a more appropriate bonding surface for adhesive or the like. The cushioning pad **38** is fixedly mounted within the rectangular chamber **36** by adhesive material or the like while the coding and coupling element $C_{11}$ associated with that key is fixedly mounted to the lower surface of cushioning pad **38** with adhesive or similar material.

When the depressible key structure is mounted in the keyboard housing **18,** the coding and coupling element $C_{11}$ is disposed, in the manner illustrated in FIG. **1,** over an appropriate row of the printed circuit board **2** in such manner that the printed circuit conductors $S_A'$, **1'–8'** and $S_B'$ are in registration with the printed circuit conductors $S_A$, **1–8** and $S_B$, as aforesaid, on the printed circuit board **2.** In the condition illustrated in FIG. **3,** the coding and coupling element $C_{11}$ may be considered to be maintained about an eighth (⅛) of an inch above the surface of the printed circuit board **2** so that no capacitive coupling between the coding and coupling element $C_{11}$ and the printed conductors $S_A$, **1–8** and $S_B$ on the printed circuit board **2** results. When, however, the cylindrical molded button **14** is depressed, the coding and coupling element $C_{11}$ will be displaced in a downward direction until the insulating layers (not shown) on the printed circuit board **2** and/or the coding and coupling element $C_{11}$ touch to thereby effect capacitive coupling between the coding and coupling element $C_{11}$ associated with the indicia or the cylindrical molded button **14** and printed conductors $S_A$, **1–8** and $S_B$ on the printed circuit board. The compressibility of the cushioning pad **38** prevents damage to the surface being selectively brought into contact in this manner while the conjoint action of the bias return and touch spring **28** and cushioning pad **38** provide the key structure depicted with a touch characteristic similar to that of a typewriter or teletype key. Alternatively the downward displacement of the central shaft **12** may be limited so that physical contact between the adjacent surfaces of the coding or coupling element $C_{11}$ and the printed circuit board is avoided.

FIGS. **4A** and **4B** illustrate exemplary input and output circuitry for the exemplary embodiment of this invention depicted in FIG. **1** wherein FIG. **4A** schematically shows input circuitry for the drive lines **1–8** depicted in FIG. **1** and FIG. **4B** schematically shows differential amplifier means for sense conductors $S_A$ and $S_B$ as shown in FIG. **1.** The exemplary input circuitry for the drive lines **1–8** as schematically illustrated in FIG. **4A** comprises clock pulse generator means **40** and electronic commutator means **42.** The clock pulse generator means **40** may take any conventional form of this well-known class of devices which is capable of producing clock pulses at a selected frequency whenever the output keyboard arrangement contemplated by the instant invention is energized. For the purposes of the instant disclosure it may be assumed that the clock pulse generator means **40** operates at a frequency of ten kilocycles (10 kc), although, as shall become apparent below, the frequency of the clock pulse generator means **40** does not substantially effect the operation of the instant invention so long as reasonably high frequencies are employed. The output of the clock pulse generator means **50** is connected through conductor **44** to the input of the electronic commutator means **42.** The electronic commutator means **42** may take the form of a conventional ring counter, a shift register which includes a recognition gate to detect the eighth pulse produced and cause resetting, or similar other forms of conventional circuitry capable of receiving a plurality of clock pulses and sequentially producing an output on one of eight output conductors for each eight clock pulses received and thereafter being capable of being energized to repeat the sequence. The electronic commutator **42** includes eight output conductors indicated as **1''–8''** in FIG. **4A** and thus functions to pulse each of said eight output conductors in sequence each time a sequence of eight clock pulses is received from the clock pulse generator means **44.** The output conductors **1''–8''** of the electronic commutator means **42** are connected to the input terminals of drive lines **1–8** on the printed circuit board **2,** as shown in FIG. **1,** so that each of the drive lines **1–8** is pulsed in sequence each time the electronic commutator means **42** re-

ceives eight clock pulses from the clock pulse generator means **40**, and as stated above, each of the drive lines **1–8** on the printed circuit board **2** must be pulsed at least once in a given sequence to provide a single cycle of operation wherein the complete code associated with a depressed key is read out. The output pulses produced by the electronic commutator means **42** may have a typical amplitude of ten volts (10 v); however, any consistent amplitude within a range of one to one hundred volts (1–100 v) is acceptable. As the instant invention employs leading edge capacitive coupling, the rise or fall time, depending on whether positive or negatively directed pulses are employed, for the leading edge of pulses produced by each stage of the electronic commutator means **42** must be rapid to ensure good capacitive coupling from the drive lines **1–8.** For the exemplary clocking rate of ten kilocycles (10 kc) described above, a rise or fall time of one microsecond (1 $\mu$s) for the leading edge of the pulses produced by the electronic commutator is acceptable. Conversely, as leading edge coupling is employed, the trailing edge of each pulse produced by each stage of the electronic commutator means **42** is preferably relatively slow to decay or return to the reference potential and hence for this reason large pull up resistors and capacitors may be added to each output stage of the electronic commutator means **42.** Of course, as the capacitive coupling relationship is governed by the relationship $i = c(dv/dt)$, either the leading or trailing edge of th pulses applied to the drive lines **1–8** may be relied upon for coupling by making the transistion time of that edge rapid. Alternatively, as will be apparent to those of ordinary skill in the art, bipolar signals could be capacitively coupled by relying on both rapidly rising and decaying pulses.

The differential amplifier means **46** shown in FIG. **4B** serves an an output device for the sense conductors $S_A$ and $S_B$ on the printed circuit board **2** and more particularly acts to algebraically subtract simultaneously applied input signals as present on sense conductors $S_A$ and $S_B$ to provide bipolar signals representing the code pulses coupled to sense conductors $S_A$ and $S_B$ while removing spurious noise and cross-talk components coupled to both of said sense conductors. The differential amplifier means **46** may comprise any of the conventional forms of this well-known class of devices and acts in the well-known manner to algebraically subtract first and second input signals applied thereto and produces a resulting output signal representing the different therebetween. A first input to the differential amplifier means **46,** as indicated in FIG. **4B,** is connected to printed sense conductor $S_B$ while the second input thereto is connected to the printed sense conductor $S_A$ on the printed circuit board **2.** The opposite ends of the sense conductors $S_A$ and $S_B$, as will be apparent to those of ordinary skill in the art, are allowed to float. Therefore, as positively directed pulses representing one (**1**) bits are present on sense conductor $S_B$ while positively directed pulses representing Zero (**0**) bits are present on sense conductor $S_A$, the output of the differential amplifier means **42** will contain both positively directed pulses representing the One (**1**) bits present on sense conductor $S_B$ and negatively directed pulses representing inverted Zero (**0**) bits present on sense conductor $S_A$. Furthermore, spurious noise and cross-talk components which are equally induced in each of sense conductors $S_A$ and $S_B$ will be cancelled and for this reason, as will be apparent to those of ordinary skill in the art, the direct capacitive coupling between the respective drive lines **1–8** and each of sense conductors $S_A$ and $S_B$, which is responsible for cross-talk, should not only be minimized between the nearest drive lines **1** and **8** and sense conductors $S_A$ and $S_B$, respectively, but should also be equalized for the more remotely located drive conductors so the cross-talk induced in each of the sense conductors $S_A$ and $S_B$ from each of the drive conductors **1–8** will be eaual. This can be done, for instance, by adding external capacitance to the driver output stages associated with particular ones of the drive conductors **1–8.** In addition, further noise reduction may be obtained by setting threshold recognition levels for the inputs of the differential amplifier means **46** so that spurious signals below the threshold set will not be applied to the differential amplifier means **46.**

The operation of the instant embodiment of the present invention will be explained in conjunction with FIG. **5** which is a timing diagram graphically illustrating an exemplary cycle of operation for the exemplary embodiment of the invention shown in FIG. **1.** The timing diagram depicted in FIG. **5** assumes that the exemplary input circuit for the drive conductors shown in FIG. **4A** is connected to drive lines **1–8** on the printed circuit board **2,** i.e. that outputs **1''–8''** of the electronic commutator means are connected to drive lines **1–8** on the printed circuit board **2;** that the differential amplifier means **46,** as shown in FIG. **4B,** is connected in the manner described above to sense conductors $S_A$ and $S_B$; and that coding and coupling element $C_{11}$, as shown in FIG. **2A,** has been placed in a coupling relationship with the printed circuit board **2** by the depression of the key associated therewith as aforesaid. Under the foregoing conditions, the clock pulse generator means **40** will apply clock pulses, as indicated in the line annotated "clock" in FIG. **5,** to conductor **44** and hence the electronic commutator **42** will pulse one of the outputs **1''–8''** thereof and thus the drive lines **1-8** connected thereto each time a clock pulse is received. Thus, as indicated in the line annotated "Drive **1**" in FIG. **5,** when the first clock pulse in a given cycle is received by the electronic commutator means **42,** a rapidly rising, more slowly decaying drive pulse is applied to the printed drive conductor **1** while similar pulses, as shown in FIG. **5,** are applied to drive lines **2–8** as the second through eighth clock pulses are applied to the electronic commutator **42.** Accordingly, for a clock frequency of ten kilocycles (10 kc) as aforesaid, one drive line **1–8** is pulsed every one hundred microseconds (100 $\mu$s) with the entire drive cycle being completed in eight-tenths of a millisecond (0.80 ms); however, faster rates may be readily achieved by increasing the frequency of the clock generator means **40.**

As the coding and coupling element $C_{11}$, shown in FIG. **2A,** is in a coupling relationship with row **1** of the serpentine printed conductors $S_A$, **1–8** and $S_B$, each drive pulse applied to the drive lines **1–8** will be capacitively coupled to the drive line sensing portion **1'–8'** on the coding and coupling element $C_{11}$ in an overlying and coupling relationship therewith. Thereafter, each pulse so coupled to the drive line sensing portions **1'–8'** on the coding and coupling element $C_{11}$ is applied to sense conductor coupling portion $S_A'$ or $S_B'$ on the coding and coupling element $C_{11}$ connected to that drive line sensing portion **1'–8'** through conductor segments **9** and **10** and then capacitively coupled back to the

sense conductor $S_A$ or $S_B$ underlying that sense conductor coupling portion $S_A'$ or $S_B'$. Thus, the leading edge of the pulse applied to drive line **1**, as shown in FIG. **5**, is capacitively coupled to drive line sensing portion **1'** on the coding and coupling element $C_{11}$, applied through conductor segment **10** to sense conductor coupling portion $S_B'$ and capacitively coupled to sense conductor $S_B$ on printed circuit board **2**, as shown in FIG. **5** on the line annotated $S_B$, to thereby represent a One (**1**) bit. One hundred microseconds (100 $\mu$s) later, a drive pulse is applied to drive line **2**, also shown in FIG. **5**, and the leading edge of this pulse is capacitively coupled to drive line sensing portion **2'** on the coding and coupling element $C_{11}$, applied through conductor segment **9** to sense conductor coupling portion $S_A'$ and capacitively coupled to sense conductor $S_A$ on printed circuit board **2**, as shown in FIG. **5** on the line annotated $S_A$, to thereby represent a Zero (**0**) bit. Similarly, in each of the remaining six (**6**) one hundred microsecond (100 $\mu$s) intervals in the exemplary eight-tenths millisecond (0.8 ms) cycle, the leading edge of the drive pulses applied to drive lines **3–8** will be capacitively coupled to drive line sensing portions **3'–8'** on the overlying coding and coupling element $C_{11}$, coded by the selective connection thereof to sense conductor coupling portions $S_A'$ and $S_B'$ and capacitively coupled to their underlying sense conductors on the printed circuit board **2** so that pulses illustrated in the lines annotated $S_B$ and $S_A$ in FIG. **5** are obtained in the selectively timed relationship shown. As the sense conductors $S_A$ and $S_B$ are connected, as aforesaid, to the differential amplifier means **46** shown in FIG. **4B**, the positively directed pulses selectively coupled to the sense conductors $S_A$ and $S_B$ by the coding and coupling element $C_{11}$ are subtracted to produce the bipolar waveform illustrated in the line annotated "S" in FIG. **5** whereby an eight (**8**) bit binary code sequence uniquely representing the key depressed is read out of the exemplary keyboard arrangement according to the instant invention directly in serial format so that it may be directly employed in utilization apparatus without subsequent modification. Although the exemplary cycle of operation described in conjunction with FIG. **5** was set forth in terms of reading out the eight (**8**) bit code associated with the coding and coupling element $C_{11}$, it will be appreciated that each key employed in a designated output keyboard will have a different eight (**8**) bit code associated therewith due to the selective coding of its coding and coupling element $C_{11}$–$C_{Nn}$ and hence for each key depressed, a different, unique eight (**8**) bit code will be read out.

As the complete readout operation of an eight (**8**) bit serial code associated with the depression of a single key in the exemplary keyboard arrangement takes place within an interval of eight-tenths of a millisecond (0.8 ms), it will be appreciated that such code will generally be read out a plurality of times in the time interval required for the key to be fully depressed and then returned to its normal non-coupled condition. This form of repetitive readout may be assured by increasing the clocking rate by a factor of ten (10) or one hundred (100) and the repetitive readout thereby obtained may be utilized to perform a plurality of checks with respect to the accuracy and propriety of the codes being produced. Thus, by monitoring and checking certain aspects of an output code which is repetitively produced, such desirable attributes as an anti-rollover function, parity checks, duration checks and the like may be readily provided in the output keyboard arrangements according to the instant invention. FIGS. **6A** and **6B** illustrate another form of input and output circuitry for the exemplary embodiment of the invention depicted in FIG. **1** and more particularly, FIG. **6A** shows circuitry which insures that the output codes produced by the instant invention are produced in an appropriately marked, repetitive manner and FIG. **6B** depicts output circuitry, which employs the repetitive readout to perform exemplary checks with respect to the accuracy and propriety of the data read out.

The exemplary input circuit depicted in FIG. **6A** takes the form of an electronic commutator circuit which provides a sequence of ten (10) outputs on separate lines for each series of five (5) clock pulses received thereby wherein the first and last outputs produced provide a logical marking function while the intermediate eight (**8**) outputs produced are employed to provide drive pulses to drive lines **1–8** on the printed circuit board **2** as shown in FIG. **1**. As shall be seen below, the output pulses applied to drive lines **1–8** by the electronic commutator circuit depicted in FIG. **6A** are negatively directed pulses rather than the positively directed drive pulses discussed in conjunction with FIGS. **4A** and **5**; however, as will be appreciated by those of ordinary skill in the art, this does little more than change the polarity of the resulting output codes obtained and hence the polarity of the drive signals which are merely a matter of choice. The electronic commutator circuit illustrated in FIG. **6A** comprises a flip-flop **50**, AND gates $\mathbf{50_0}$–$\mathbf{52_9}$, NOR gates $\mathbf{54_0}$–$\mathbf{54_9}$ and output terminals $TP_0$ –$TP_9$, wherein the numerical subscripts associated with the numbers designating the AND gates, NOR gates and output terminal indicates the stage in which these elements are present within the electronic commutator so that common elements within each stage may be readily identified. The flip-flop **50**, the AND gates $\mathbf{52_0}$–$\mathbf{52_9}$ and the NOR gates $\mathbf{54_0}$–$\mathbf{54_9}$ may each comprise conventional logic components such as TTL components, MSI components or conventional logic structure formed with individual circuit elements which are readily available in the marketplace and perform the usual logical functions generally ascribed to such components. Thus, flip-flop **50** may take the form of a conventional bistable multivibrator having a first output connected to conductor **56** wich follows the input applied thereto and having a second output connected to conductor **58** which is inverting and produces the complement of the signal present at the first output thereof. Similarly, the AND gates $\mathbf{52_0}$–$\mathbf{52_9}$ have inverting inputs as indicated and function in the conventional manner to provide a high level at the outputs thereof whenever all of the inputs thereto are low while providing a low level output whenever any one or more of the inputs thereto are high. Conversely, NOR gates $\mathbf{54_0}$–$\mathbf{54_9}$ function as inverting OR gates in the conventional manner, to provide a low level output whenever any one of the inputs thereto are high while producing a high level output only when all of the inputs thereto are low. A first input to each of the AND gates in the odd numbered stages of the electronic commutator, i.e. AND gates $\mathbf{52_1}$, $\mathbf{52_3}$, $\mathbf{52_5}$, $\mathbf{52_7}$ and $\mathbf{52_9}$, is connected to conductor **56** and hence to the output of the flip-flop **50** which follows the input thereto while first inputs to each of the even stage AND gates $\mathbf{52_0}$, $\mathbf{52_2}$, $\mathbf{52_4}$, $\mathbf{52_6}$ and $\mathbf{52_8}$ are connected to the

complementary output of flip-flop **50** through conductor **58.** The input to the flip-flop **50** is connected as indicated to a conventional clock pulse generator which here may be assumed to provide clock pulses at a frequency of five kilocycles (5 kc). The outputs of each of the AND gates $52_0$–$52_9$ are connected through conductors $60_0$–$60_9$, respectively, to a first input of the NOR gate $54_0$–$54_9$ present in its own stage of the electronic commutator and AND gates $52_0$–$52_8$ are also connected to a second input of the NOR gate in the preceding stage of the electronic commutator, it being noted that the output of AND gate $52_0$ is connected to a second input of NOR gate $54_9$ through conductor **62** to form a ring configuration. Additionally, the outputs of the AND gates $52_1$, $52_3$, $52_5$ and $52_7$ are connected through conductors $64_1$, $64_3$, $64_5$ and $64_7$, respectively, to individual inputs of AND gate $52_9$ so that, as shall be seen below, no output can be produced by the last stage of the electronic commutator while the leading edges of drive pulses are being applied to drive lines **1–8.** The output of each of the NOR gates $54_0$–$54_9$ is connected to the output terminals $TP_0$–$TP_9$ of the stage of the electronic commutator in which it resides and the outputs of NOR gates $54_0$–$54_7$ and $54_9$ are connected to a second input of the AND gate in the following stage through conductors $66_0$–$66_7$ and $66_9$, it being noted that the output of NOR gate $54_9$ is connected to the second input of AND gate $52_0$ to again form a ring configuration. The output terminals $TP_1$–$TP_8$ of stages **1–8** of the electronic commutator are connected to drive lines **1–8** of the embodiment of the invention shown in FIG. **1** and act to supply drive pulses thereto while output terminals $TP_0$ and $TP_9$ are connected, as shall be seen below, to the output circuitry illustrated in FIG. **6B.** Capacitors $C_1$–$C_8$ are loading capacitors employed, as aforesaid, to provide the requisite external capacitance for the drive lines **1–8** to insure that the rise time of the trailing edges of the drive pulses applied thereto is much larger than the fall time of the leading edges of such pulses.

In the operation of the electronic commutator illustrated in FIG. **6A,** it will be assumed that clock pulses are being applied to the input of flip-flop **50** at a rate of five kilocycles (5 kc) and that a low level is present on conductor $66_9$ due to a previous cycle of operation; however, for reasons which will become apparent below, the output of NOR gate $54_9$ will also be low just prior to any cycle of operation of the electronic commutator. When the first clock pulse applied to flip-flop **50** is received, the flip-flop **50** will apply a high level output to conductor **56** and a low level output to conductor **58** which is connected to the inverting output thereof. As a low level is already present at the second input of AND gate $52_0$ which is connected through conductor $66_9$ to the output of NOR gate $54_9$, as aforesaid, when conductor **58** goes low in response to the receipt of the first clock pulse applied to flip-flop **50,** the coincident logic conditions, i.e., low levels at all inputs, for AND gate $52_0$ will be met and the output of AND gate $52_0$ will go high. The remaining AND gates $52_1$–$52_8$ will, however, be maintained in their low output logic state as their second inputs, connected to conductors $66_0$–$66_7$, respectively, are in a high logic condition while And gate $52_9$ is also in a low output condition due to the input on conductor **56.** The high logic level thereby produced at the output of AND gate $52_0$ is applied through conductor $60_0$ to the first input of NOR gate $54_0$ and through conductor **62** to the second input of NOR gate $54_9$. As any high level applied to NOR gates $54_0$–$54_9$ will satisfy the input logic conditions therefor, NOR gate $54_9$ is maintained in its previously established low output condition while NOR gate $54_0$ goes low. The low level now present at the output of NOR gate $54_0$ is applied to output terminal $TP_0$ to produce a negatively directed output pulse thereat and through conductor $66_0$ to the second input of AND gate **52,** where it acts to prime this gate. When the first clock pulse applied to flip-flop **50** terminates, a low logic level is applied to conductor **56** while a high logic level is applied to conductor **58.** The high logic level applied to conductor **58** places the AND gate $52_0$ in its low condition and hence the maintaining levels applied to NOR gate $54_9$ through conductors $60_0$ and **62** is removed so that NOR gate $54_9$ goes high. However, as the second input to AND gate **52,** which is connected to the output of NOR gate $54_0$ through conductor $66_0$ is already low, the low logic level now applied to conductor **56** places AND gate $52_1$ in its high output state. The high output state of AND gate $52_1$ is applied through conductor $60_1$ to the second input of NOR gate $54_0$ to maintain this gate in a low condition and to a first input of NOR gate $54_1$ to place it in its low state. Additionally, the high level output of AND gate $52_1$ is applied through conductor $64_1$ to an input of AND gate $52_9$ where it acts to further inhibit this gate. The low level output of NOR gate $54_1$ is applied directly to output terminal $TP_1$ as a negatively directed drive pulse and through conductor $66_1$ to prime the second input of AND gate $52_2$.

When the second clock pulse is applied to the flip-flop **50** conductor **58** goes low while conductor **56** goes high. As the second input to AND gate $52_2$ has already been primed, this AND gate is switched to its high output state; however, as the low level on conductor $66_9$ has been removed and none of the other even stage AND gates $52_4$, $52_6$ or $52_8$ has been primed, none of these other AND gates are placed in their high states. In addition, the high logic level on conductor **56** places the previously enabled AND gate $52_1$ in its low state which terminates the maintaining logic level applied to NOR gate $54_0$ and hence terminates the output pulse at terminal $TP_0$ and the priming level applied to the second input of AND gate $52_1$ through conductor $66_0$. The high logic level now present at the output of AND gate $52_2$ is applied through conductor $60_2$ to the second input NOR gate $54_1$ where it acts as a maintaining level to continue the output produced at terminal $TP_1$ and the priming level to its own second input, and is additionally applied to the first input or NOR gate $54_2$ to switch this gate to its low logic state. The low logic output level of NOR gate $54_2$ is directly applied to output terminal $TP_2$ where it acts as a negatively directed drive pulse and to the second input of AND gate $52_3$ where it acts to prime this gate. When the second clock pulse applied to the flip-flop **50** terminates, conductor **56** goes low and conductor **58** goes high. The high level on conductor **58** places AND gate $52_2$ in a low output state whereby the maintaining level on NOR gate $54_1$ is removed to terminate the output pulse at terminal $TP_1$. The low level on conductor **58** switches AND gates $52_3$ high to maintain NOR gate $54_2$ in the on condition and hence continue the output pulse applied to terminal $TP_2$ and to place NOR gate $54_3$ in its output level whereby a negatively directed drive pulse is applied to

output terminal $TP_3$, AND gate $52_4$ is primed and AND gate $52_9$ is inhibited through conductor $64_3$. This continues, as shall be apparent to those of ordinary skill in the art, in the foregoing manner as each clock pulse is received and then terminates so that a pulse having a duration equal to the reciprocal of the frequency of the clock pulses is produced at each of the output terminals $TP_0$–$TP_9$; and as a pulse is produced at one of the outputs of the electronic commutator for both the leading and trailing edges of the clock pulses, the output frequency of the electronic commutator is twice the frequency of the clock pulses received thereby.

When the fifth clock pulse applied to the flip-flop **50** terminates, a low level will be applied to conductor **56** and the outputs of AND gates $52_1$, $52_3$, $52_5$ and $52_7$ will all be low so that the AND conditions on the five (**5**) input AND gate $52_9$ are finally met. AND gate $52_9$ thereby goes high to place NOR gate $54_9$ in a low output condition to thereby place a low level or negatively directed output pulse on output terminal $TP_9$ indicating that one cycle of operation for the electronic commutator has been completed and priming the second input of AND gate $52_0$ through conductor $66_9$ for the next cycle of operation. The purpose of AND gate $52_9$ is to inhibit a pulse at output terminal $TP_9$ until the entire cycle of operation of the electronic commutator depicted in FIG. **6A** has been completed. This enables the pulse produced at $TP_9$, as shall be seen below, to clearly define the end of a read cycle to the utilization equipment. Thus, as signals at $TP_0$ and $TP_9$ may be employed to define the beginning and end of each read cycle in output keyboard arrangements according to the present invention while drive pulses present at output terminals $TP_1$–$TP_8$ are coupled to drive lines **1–8** as shown in FIG. **1**, appropriate start, stop and timing information is directly available for use in output circuitry for receiving the directly coded serial information produced by output keyboard arrangements according to the instant invention. Furthermore, as will be appreciated from the foregoing explanation of the operation of the electronic commutator shown in FIG. **6A**, the output of AND gate $52_9$ will be high to force the output of NOR gate $54_9$ low each time a cycle of operation is initiated.

The exemplary electronic commutator depicted in FIG. **6A** employs a clock having a frequency of five kilocycles (5 kc) and completes an entire character read cycle for the exemplary embodiment of the invention depicted in FIG. **1** upon the receipt of five (**5**) clock pulses. This means that the complete readout operation of an eight (**8**) bit serial code associated with the depression of a single key in the exemplary keyboard arrangement will take place within an interval of one millisecond (1 ms) and ensures that each character will be read out a plurality of times in the time interval required for the key to be fully depressed and then returned to its normal non-coupled condition. FIG. **6B** illustrates output circuitry, which employs this repetitive readout to perform a plurality of checks with respect to the accuracy and propriety of the data read out prior to supplying character information associated with the particular key depressed to utilization apparatus therefor. The output circuit described in conjunction with FIG. **6B** employs a plurality of flip-flops, logical gates of various types, a register and a counter and it should be appreciated at the outset that each of these devices may comprise conventional TTL or MSI components or may be formed with individual circuit elements at the option of the designer. Furthermore, in FIG. **6B**, certain types of logic arrangements have been relied upon to facilitate the utilization of the logic components employed; however, as will be apparent to those of ordinary skill in the art, so long as the function of such logic arrangements are achieved, differing forms of logical arrangements may be employed.

The exemplary output circuit illustrated in FIG. **6B** comprises first and second differential amplifier means **71** and **72**, shift register means **74**, AND gates $G_1$ and $G_2$, a data presence detector circuit indicated by the dashed block **76**, a count inhibit circuit indicatd by the dashed block **78**, flip-flops $FF_1$ and $FF_2$, counter means **80** and a character identity check circuit indicated by the dashed block **82**. The differential amplifier means **71** and **72** may take the form of operational amplifiers or any of the other conventional types of differential amplifier means described above in connection with FIG. **2B**. An inverting input to differential amplifier **71** is connected, as indicated, to sense conductor $S_B$ while an inverting input to differential amplifier means **72** is connected to sense conductor $S_A$ on the printed circuit board **2**. The non-inverting inputs of each of the differential amplifier means **71** and **72** are commoned to a negative potential level indicated as −V which acts, in the well-known manner, to set a negative threshold level for each of the differential amplifier means **71** and **72** so that negative pulses on sense conductors $S_A$ and $S_B$ which are smaller in magnitude than such threshold level are not recognized. The negative threshold thereby serves to eliminate weak input signals on sense conductors $S_A$ and $S_B$ such as noise and cross-talk while actual bit information is raised to standard logic levels and presented at the outputs of the differential amplifier means **71** and **72**. As the sense conductors $S_B$ and $S_A$ are connected to the inverting inputs of the differential amplifier means **71** and **72** and the drive lines **1–8** of the printed circuit board **2** are in this case driven by the negatively directed pulses provided by the input circuit depicted in FIG. **6A**, One (**1**) bit information will here be represented by positive levels which appear at the output of differential amplifier means **71** while Zero (**0**) bit information is represented by positive levels which appear at the output of differential amplifier means **72**. The output of the differential amplifier means **71** is connected through conductor **84** to an input of the shift register means **74** while the output of differential amplifier means **72** is connected to an input of AND gate $G_1$.

The shift register means **74** comprises a conventional eight (**8**) bit serial in, serial out shifting configuration which acts in the well-known manner to shift bits applied thereto from the output of the first differential amplifier means **71** at a rate determined by the clocking pulses applied to the input annotated C. The clock pulses applied to input C of the shift register means **8**, as shall be seen below, correspond to the application of drive pulses to drive lines **1–8** from the output of terminals $TP_1$–$TP_9$. Output pulses from the second differential amplifier means **72**, which represent Zeros (**0**'s), as aforesaid, are not applied to the input of shift register means **74**, as the absence of a pulse on conductor **84** when a clock pulse is applied to input C is clocked through the shift register **74** as a Zero (**0**) so that the propriety of the serial bit configuration is maintained. The output of the shift register means **74** is connected

through conductor **87** and AND gate **88** to the character output terminal indicated. Thus, whenever AND gate **88** is enabled, character information in the form of an eight (**8**) bit code representing the key depressed is applied in serial format to the character output terminal and thereafter to utilization circuitry therefor.

AND gate $G_1$ is a conventional AND gate which functions in the well-known manner to produce a high level output whenever both inputs thereto are high while providing a low level output whenever any other input conditions obtain. The purpose of AND gate $G_1$ is to perform a check to insure that a data bit is not simultaneously present on both the One (**1**) sense conductor $S_B$ and the Zero (**0**) sense conductor $S_A$ and to eliminate any character sequence of eight (**8**) code bits in which this condition occurred. This check is directed primarily against operating conditions where two or more keys in the output keybaord arrangement are depressed at the same time and hence provides an anti-rollover function for the instant invention. The AND gate $G_1$ is connected through conductor **86** to the output of differential amplifier means **72** and through conductor **88** to the output of differntial amplifier means **71.** Therefore, the only time that AND gate $G_1$ will produce a high logic level output is when a pulse representing a One (**1**) bit is present at the output of differential amplifier means **71** and simultaneously therewith a pulse representing a Zero (**0**) bit is present at the output of differential amplifier means **72** which is the condition which this gate is relied upon to detect. The output of AND gate $G_1$ is connected through conductor **90** to an input of the count inhibit circuit indicated by the dashed block **78** and, as shall be seen below, whenever a high logic level is produced by AND gate $G_1$, the eight (**8**) bit character in which said high logic level output is produced is disregarded.

The output of the first and second differential amplifier means **71** and **72** are also connected through conductors **92** and **94,** respectively, to inputs of the data presence detector circuit indicated by the dashed block **76.** The purpose of the data presence detector is to insure that at least one code bit, either a One (**1**) or a Zero (**0**), is received each time a drive line **1–8** is pulsed at output terminals $TP_1$–$TP_8$ of the input circuit shown in FIG. **6**A. The data presence detector circuit indicated by the dashed block **76** comprises NOR gate **96,** AND gate **98** and clock pulse generator means **100.** The NOR gate **96** functions as an inverting OR gate in the same manner described for NOR gates $54_0$–$54_9$ described in conjunction with FIG. **6**A in that it will produce a low logic level output whenever at least one high logic level input is applied thereto while producing a high logic level output only when all of the inputs thereto are low. As the inputs to NOR gate **96** are connected through conductors **92** and **94** to the outputs of differential amplifiers **71** and **72,** respectively, it will be appreciated that the output of NOR gate **96** will be low whenever a One (**1**) or a Zero (**0**) code bit is present at the output of either of the differential amplifier means **71** or **72** and will go high only when no pulse is present at either output. The output of NOR gate **96** is connected through conductor **102** to one input of AND gate **98.** The AND gate **98** may take the same form as AND gate $G_1$ and accordingly produces a high logic output only when both of the inputs thereto are high while producing a low logic output for all other input conditions. The other input of AND gate **98** is connected through conductor **104** to the output of clock pulse generator means **100.** The clock pulse generator means **100** functions to produce a clock pulse having a predetermined duration each tine a drive pulse is applied to output terminals $TP_1$–$TP_8$ of the input circuit depicted in FIG. **6**A. Accordingly, the clock pulse generator means **100** may take the form of a monostable multivibrator or other conventional forms of slave oscillators adapted to be triggered by eadh of the pulses applied to output terminals $TP_1$–$TP_8$. Alternatively a schmitt trigger circuit could be employed to produce a positive level for the entire duration that overlapping pulses are applied to output terminals $TP_1$–$TP_8$; however, under these conditions a separate clock would be required for the shift register means **74.** Thus, the clock pulse generator means **100** applies a pulse or logically high input through conductor **104** to the C input of the shift register means **74** and to one input of the AND gate **98** whenever a drive pulse is applied to drive lines **1–8** while NOR gate **96** applies a high input to the other input of AND gate **98** only under a condition when a pulse representing a data bit is not present at either of the outputs of differential amplifiers **71** or **72.** This means that a high logic level output will be produced by the AND gate **98** only under a condition where at least one code bit is not received, in the readout of a given character, each time a drive line is pulsed which is the condition which the data presence detector circuit indicated by the dashed block **76** seeks to detect. The output of AND gate **98** like the output of AND gate $G_1$ is connected through conductor **106** to an input of the count inhibit circuit indicated by the dashed block **78** and, as shall be seen below, whenever a high logic level is produced by AND gate **98,** the eight (**8**) bit character in which said high logic level output is produced is disregarded.

The count inhibit circuit indicated by the dashed block **78** functions to receive an inhibit signal, as represented by a high level or failed test output at either of the AND gates $G_1$ or **98,** at any time during a given eight (**8**) bit character read sequence and to produce an inhibit or high level signal from the time the failed test signal is received until the next eight (**8**) bit character read sequence is initiated. Thus, once a high level output is received from AND gates $G_1$ or **98** indicating that one bit position in an eight (**8**) bit character being read has failed the tests performed thereby, the count inhibit circuit indicated by the dashed block **78** generates an inhibit signal for the remaining bit positions of the eight (**8**) bit character sequence being shifted through the shift register means **74** regardless of whether or not the remaining bit positions present in that sequence pass the tests imposed by AND gate $G_1$ and the data presence circuit **76.** The count inhibit circuit indicated by the dashed block **78** comrpises OR gate **108** and flip-flop **110.** The OR gate **108** acts in the well-known manner to produce a high logic level output whenever any one of the inputs thereto is high while providing a low level output only when both of the inputs thereto are low. OR gate **108** thereby produces a low level output only when the bit position being tested pass both of the tests imposed by the AND gate $G_1$ and the data presence circuit indicated by the dashed block **76** while producing a high logic level output any time a given bit position fails the tests imposed. The output of the OR gate **108** is connected to the set input of flip-flop **110** while the reset input of the flip-

flop **110** is connected to terminal $TP_0$ of the input circuit illustrated in FIG. **6A** in the manner indicated in FIG. **6B**. The flip-flop **110** is thus reset to its low output state each time a character read sequence is initiated by the reset signal applied from terminal $TP_0$ and is maintained in this condition unless a high level setting pulse is received from OR gate **108**. Once set by OR gate **108**, the flip-flop **110** will be maintained in its high level output state until it is again reset at the beginning of a new character read sequence by a pulse applied from terminal $TP_0$. Thus, it will be seen that flip-flop **110** is employed as a memory element to produce a high level output for a sufficient interval of time to complete a given eight (**8**) bit character readout sequence any time any bit position in that sequence fails the tests imposed by AND gate $G_1$ and the data presence circuit indicated by the dashed block **76**. The output of flip-flop **110** is connected through conductor **112** to a first input of AND gate $G_2$ and as will be apparent from the foregoing description of the count inhibit circuit indicated by the dashed block **78**, a low logic level output therefrom indicates that no bit position has violated the tests imposed by AND gate $G_1$ and the data presence circuit indicated by dashed block **76** while a high logic level indicates that a bit position has failed such test and hence that the eight (**8**) bit character in which the bit resides must be disregarded as its information content is faulty.

AND gate $G_2$ and counter means **80** form a duration check circuit which tests that a character sequence which has passed a plurality of previous tests has been repeated a sufficient number of times to insure that it represents a key which was validly depressed rather than one being teased or touched inadvertently. More particularly, the counter means **80** may comprise a conventional eight (**8**) bit binary counter having its incrementing input connected to the output of AND gate $G_2$. Although an eight (**8**) bit binary counter has been specified, as this constitutes a readily available commercial size, only stages **4** and **5** of the counter means **90** have been indicated on FIG. **6B** as only these stages thereof are employed and hence it will be apparent that counters having fewer stages may be utilized. The output of stage **4** of the counter means **80** is applied to conductor **114** where it is employed, as shall be seen below, to enable the character content of the shift register means **74** to be read out to utilization apparatus therefor (not shown). The output of stage **5** of the counter means **80** is connectd through conductor **116** to a second input of AND gate $G_2$ where, as shall be seen below, it is employd to inhibit the incrementing action of this gate after a sufficeint number of repetitions of the character under test have been counted. The reset input R of the counter means **80** is connected through conductor **118** to the output of the character identity check circuit indicated by the dashed block **82**. The character identity check circuit indicated by the dashed block **82**, as will be seen below, resets the counter means **80** any time that the character information being read into shift register means **80** does not correspond identically to the character previously stored therein. This means that the counter means **80** is reset each time there is a transition from character information which has been repeatedly read into the shift register means **74** to the first eight (**8**) bit character representing a subsequently depressed key as well as any time a spurious readout of a character occurs.

The AND gate $G_2$ serves to increment the count of the counter means **80** at the completion of each eight (**8**) bit character read into the shift register means **74** if that character has passed all of the tests applied thereto and AND gate $G_2$ is not otherwise inhibited. The AND gate $G_2$ has inverting inputs as indicated in FIG. **6B** and thus produces a high logic level output which serves to increment counter means **80** when all of the inputs thereto are low; however, when any of the inputs to AND gate $G_2$ are high, no incrementing signal is produced. The timing for the incrementing action of AND gate $G_2$ is provided by the input thereto connected, as indicated, to output terminal $TP_9$ of the input circuit depicted in FIG. **6A**. Output terminal $TP_9$, it will be recalled, receives a negatively directed pulse after all of the drive lines **1–8** have been pulsed; therefore if all of the other inputs to AND gate $G_2$ are low, a high logic level incrementing pulse will be produced at the output of AND gate $G_2$ when a negatively directed pulse is applied to terminal $TP_9$ to coincide with the end of a character read sequence and such incrementing pulse will terminate prior to the next application of drive pulses to drive lines **1–8** of the printed circuit board **2**.

The input to AND gate $G_2$ connected to conductor **116** is normally held in a low condition but is raised to a high level to inhibit incrementing when the count of counter means **80** reaches stage **5** to indicate that no further incrementing for the repetitively read character then being written into a shift register means **74** is required. The input to AND gate $G_2$ connected to conductor **112**, as previously described, is normally held at a low logic level except under conditions when one bit position in the character being written into shift register means **74** has failed to pass the test imposed by AND gate $G_1$ and/or the test imposed by the data presence circuit indicated by dashed block **76**. The remaining input to AND gate $G_2$ is connected to the output of flip-flop $FF_1$ through conductor **120**. The flip-flop $FF_1$ is connected at the resetting input R thereto to output terminal $TP_0$, as indicated, of the input circuit depicted in FIG. **6A** while the data input D of flip-flop $FF_1$ is connected through conductor **122** to the output of the differential amplifier means **71** which is connected through conductor **84** to the input of shift register means **74**. The data input D of flip-flop $FF_1$ thereby receives each input pulse applied to the shift register means **74**, where each such pulse here represents a One (**1**) bit, and will cause flip-flop $FF_1$ to toggle, in the well-known manner, with each such pulse received. The flip-flop $FF_1$ serves in the role of performing a parity check on each character written into the shift register means **74** and acts to inhibit the incrementing action of AND gate $G_2$ whenever the parity check run on a given character is improper. Thus, as either even or odd parity may be arbitrarily selected for the coding of all of the eight (**8**) bit character information produced by the output keyboard arrangements according to the present invention, either the reset state of the flip-flop $FF_1$, as established prior to each character read cycle by the output at terminal $TP_0$, or the appropriate connection of conductor **120** to the direct or inverting output of flip-flop $FF_1$ may be relied upon to obtain a low level output from flip-flop $FF_1$ in response to the last changes in state therein caused by the series of input pulses on conductor **122** as applied by an eight (**8**) bit character having the proper parity selected. Therefore,

as will be appreciated by those of ordinary skill in the art, upon the receipt of the last bit in the eight (8) bit character being inserted into shift register means **74**, the flip-flop $FF_1$ will produce a low level output if the appropriate parity is present while producing a high level output to inhibit the incrementing action of AND gate $G_2$ if such character does not have the proper parity. Accordingly, assuming that the counter means **80** is initially reset, the AND gate $G_2$ will increment the counter means **80** at the end of each eight (8) bit character read cycle, when the negatively directed pulse on terminal $TP_9$ is produced, if the eight (8) bit character then being read into the shift register means **74** passes the parity test imposed by flip-flop $FF_1$, the rollover test imposed by AND gate $G_1$ and the data presence test imposed by the circuit indicated by dashed block **76**. When this character has been successfully repeated four (4) times, the state of the count of the counter means **80** will be such that a high level is present at stage **4** of the counter means **80** which enables the output of the shift register means **74** to be read out to utilization apparatus therefor in a manner described below. Upon the fifth application of this repetitively read character to the shift register means **74**, and assuming it again passes the three (3) tests imposed by the input circuitry connected to AND gate $G_2$, the state of the count in counter means **80** will be advanced to stage **5** and the enabling output at stage **4** will be removed. The high level now present at stage **5** of the counter means **80** will inhibit the incrementing action of AND gate $G_2$ and maintain it inhibited until the counter means **80** is reset which, as shall be seen below, occurs when differing character information representing a new key depression is applied to the shift register means **74**.

The output of stage **4** of counter means **80** is connected through conductor **114** to the set input of flip-flop $FF_2$ while the reset input thereof is connected to output terminal $TP_9$ of the input circuit depicted in FIG. **6A**. One output of flip-flop $FF_2$ is connected through conductor **124** to an enabling input for AND gate **88** while a second output of flip-flop $FF_2$ is connected, as indicated, to a data output level indicia and may be considered to set a flag or the like. Normally, flip-flop $FF_2$ is in a reset condition due to the negatively directed pulse applied to terminal $TP_9$ and hence the reset input at the end of each character read cycle. When, however, stage **4** of the counter means **80** goes high, flip-flop $FF_2$ is set whereby AND gate **88** is enabled by the high logic level applied to conductor **124** and the data output level is set to indicate to the utilization apparatus that an eight (8) bit character is to read out at the character output lines connected to AND gate **88**. Thereafter, the fourth repetitively read eight (8) bit character which is present in the shift register means **74** is read out as the fifth repetitively read character is inserted in the shift register means **74**. When the fifth stage of the counter means **80** goes high, further incrementing by AND gate $G_2$ is inhibited and the high logic level on conductor **114** is removed. This permits the next pulse on terminal $TP_9$ to reset flip-flop $FF_2$ to thereby disable AND gate **88** and drop the output level indicia on line **126**.

The character identity check circuit indicated by the dashed block **82** comprises an exclusive "OR" array which functions to compare each bit position in a character being inserted into the shift register means **74** with the corresponding bit position in the previously stored character being read therefrom and to reset the counter means **80** whenever a proper comparison is not obtained. Therefore, as an identity check between corresponding bit positions of a character being applied to the shift register means **74** and the character being read therefrom is performed by the character identity check circuit indicated by dashed block **82**, it will be seen that this circuit serves to reset counter means **80** at each transition between a repetitively read character and a new character as well as whenever spurious character information is received. The character identity check circuit indicated by dashed block **82** comprises first and second invertor means **128** and **130**, first and second AND gates **132** and **134** and OR gate **136**. The first and second invertor means **128** and **130** comprise conventional logic devices which act in the well-known manner to provide an inverted output signal with respect to the logical input level received thereby while AND gates **132** and **134** and Or gate **136** take the same form as mentioned above with respect to correspondingly designated structure. The output of differential amplifier means **71** and hence the input to the shift register means **74** is connected through conductor **138** directly to the lower input to AND gate **134** and through inverter **128** to the lower input of AND gate **132**. Similarly the output of shift register means **74** is connected through conductor **140** directly to the upper input of AND gate **132** and through inverter **130** to the upper input of AND gate **134**. Thus, as the first and second AND gates **132** and **134** will only produce a high level output when both of the inputs thereto are high, it will be seen that AND gate **132** will produce a high level output when the output from the shift register means **74** is high and the input thereto is low while AND gate **134** will produce a high level output when the output from the shift register means **74** is low and the input thereto is high. Neither AND gate **132** nor **134**, however, will produce a high level output when the input to shift register means **74** corresponds to the output thereof. The OR gate **136** will produce a high level output whenever either input thereto is high and hence whenever one of the first or second AND gates **132** or **134** produces a high level output; OR gate **136** will apply a high logic level to conductor **118** to reset counter means **80**.

In the description of the operation of the exemplary output circuit illustrated in FIG. **6B** which follows, it will be assumed that the initial cycle of an eight (8) bit character associated with a newly depressed key in the output keyboard arrangement according to the present invention is being applied to input terminals $S_B$ and $S_A$ of the differential amplifiers **71** and **72** as each of the drive lines **1–8** on the printed circuit board **2** is pulsed by the input circuit illustrated in FIG. **6A**. Under these assumed conditions, flip-flops $FF_1$ and **110** will be reset to their low output conditions when the leading edge of the first pulse produced by the input circuit depicted in FIG. **6A** appears at output terminal $TP_0$ and the shift register means **74** will contain a Zero (**0**) bit stored in each of eight (**8**) stages therein due to the preceding interval when no coding and coupling element $C_{11}$–$C_{N8}$ was in capacitive coupling relationship with the printed conductors $S_A$, **1–8** and $S_B$ on the printed circuit board **2** and hence, conductor **84** gives the appearance of having all Zero (**0**) bits applied thereto. Furthermore, the counter means **80** will be in a reset condition (a count of Zero) as it was reset by the character identity

check circuit indicated by the dashed block **82** when the all Zero (**0**) bit character was initially applied to the shift register means **74** and subsequent repeated applications of the all Zero (**0**) bit character would not pass the parity check imposed by the flip-flop $FF_1$ or the data presence check imposed by the circuit within dashed block **76**, as the Zeros (**0**'s) here loaded do not derive from pulses on line $S_A$ but rather an absence of pulses on conductor **84**, and hence these circuits would apply high level inputs to AND gate $G_2$ and prevent it from incrementing the counter means **80** at the end of each character read cycle.

After output terminal $TP_0$ is pulsed as aforesaid, so that the leading edge of the pulse applied thereto resets flip-flops $FF_1$ and **110** to their low output states, a coded bit in the form of a pulse on conductor $S_B$ which represents a One (**1**) or a pulse on conductor $S_A$ which represents a Zero (**0**) will be received for each pulse applied to output terminals $TP_1$-$TP_8$ and hence to drive lines **1–8** by the input circuit depicted in FIG. **6**A. As each pulse is received on the sense conductors $S_B$ and $S_A$, it is tested against the threshold level −V set at each of the differential amplifier means **71** and **72** and if the magnitude thereof exceeds the threshold level set it is raised to standard logic levels, inverted and applied to output conductors **84** and **86.** The conductors **84** and **86** are tested on a continuous basis by AND gate $G_2$ and the data presence circuit indicated by dashed block **76** and should the input conditions present on conductors **84** and **86** fail either of the tests imposed, AND gate $G_2$ is inhibited from incrementing the state of the counter means **80** for the full character cycle in which such failure occurred due to a high level input supplied on conductor **112.** Thus, AND gate $G_1$ performs an anti-rollover function in that it tests conductors **84** and **86** to determine whether or not pulses representing bit information are simultaneously present therein. This condition would be indicated, as aforesaid, by a high level being simultaneously applied to both inputs of AND gate $G_1$ on conductors **86** and **89.** When both of the inputs to AND gate $G_1$ go high, a high logic level will be produced by AND gate $G_1$ on conductor **90.** This high level will force the output of OR gate **108** high which in turn sets the flip-flop **110** in a high output state whereby a high level is applied to conductor **112** until the flip-flop **110** is subsequently reset by a pulse at terminal $TP_0$ at the beginning of the next character read cycle. Therefore, if more than one key in the instant embodiment of the keyboard arrangement according to the present invention is depressed, at least one bit position in the eight (**8**) bit character read will have both a One (**1**) and a Zero (**0**) pulse produced therefor. Upon the detection of this condition, a high level will be applied to conductor **112** to prevent AND gate $G_2$ from incrementing counter means **80**, which, as shall be seen below, prevents the improper character from being treated as a valid character code or being read out. Similarly, the data presence circuit indicated by the dashed block **76** tests conductors **84** and **86** to insure that a coded data pulse, a One (**1**) or a Zero (**0**), is produced for each drive pulse applied to drive conductors **1–8** from terminals $TP_1$–$TP_8$ and should a condition occur in which these requirements are not met, acts to inhibit AND gate $G_2$ from incrementing the state of the counter means **80** until the next character read cycle is initiated. NOR gate **96** tests the outputs of the differential amplifier means **71** and **72,** through its input conductors **92** and **94,** for a condition when no data bit, as indicated by a pulse, is present at either output. Thus, whenever no output pulse is present on conductors **84** and **86,** the output of NOR gate **96** will go high while it will be in a low output condition at all times when an output pulse is present on conductors **84** or **86.** The timing function associated with the test established by the data presence circuit indicated by the dashed block **76** is provided by the clock pulse generator means **100,** which, as aforesaid, will place a high logic level on conductor **104** each time a drive pulse is applied to drive conductors **1–8** from terminals $TP_1$–$TP_8$. Thus, whenever a high level is applied to both input conductors **102** and **104** of AND gate **98,** the condition sought to be determined by the data presence circuit indicated by dashed block **76** is present. When both inputs to AND gate **98** on conductors **102** and **104** go high, the output of AND gate **98** on conductor **106** goes high. This causes the output of OR gate **108** to go high whereby the flip-flop **110** is set to its high output state and places a high level on conductor **112** to inhibit AND gate $G_2$ from incrementing counter means **80** until the flip-flop **110** is again reset at the beginning of a new character read cycle by the pulse provided at terminal $TP_0$.

Each pulse representing a One (**1**) bit as produced at the output of the differential amplifier means **71** is applied to conductor **84** and hence to the data input of shift register means **74** while a clock pulse or shift input is applied to the C input thereof from clock pulse generator means **100** each time a drive pulse is applied to drive conductors **1–8** on the printed circuit board **2** from the output terminals $TP_1$–$TP_8$ in the input circuit depicted in FIG. **6**A. Therefore, each time a clock pulse is applied to the clock of the shift register means **74,** a One (**1**) bit will be written into the initial stage thereof if a pulse or high logic level is present on conductor **84** while a Zero (**0**) bit is written into the initial stage of shift register means **74** whenever a clock pulse is applied to the clock thereof and no pulse or high logic level is present on conductor **84.** Accordingly, in this manner, an eight (**8**) bit character is written in series into shift register means **74** for each character read cycle and a corresponding bit position in the previously loaded eight (**8**) bit character present in the shift register means **74** is read out on conductor **86** each time a corresponding bit position in the next character is written into shift register means **74.**

For the initial conditions assumed above, as the first eight (**8**) bit character for the key depressed is loaded a bit at a time into shift register means **74,** the previously loaded eight (**8**) bit character, which here consists of all Zero (**0**) bits as aforesaid, will be read out a bit at a time onto conductor **87.** As AND gate **88** has not yet been enabled, each of the Zero (**0**) bits being read out of shift register means **74** as the first eight (**8**) bit character representing the key depressed is loaded will not be applied to the character output terminal; however each of these Zero (**0**) bits is applied through conductor **140** to the upper input of AND gate **132** as a low level input, and inverted and applied as a high level input to the upper input of AND gate **134** within the character identity check circuit indicated by the dashed block **82.** In a similar manner, each bit of the first eight (**8**) bit character representing the key depressed is applied to the lower input of AND gate **134** within the character identity check circuit indicated by

dashed block **82** and inverted and applied to the lower input of AND gate **132.** In this manner, the content of the first bit position in the first eight (**8**) bit character representing the key depressed and being inserted into the shift register means **74** is compared with the Zero (**0**) in the first bit position of the all Zero (**0**) bit character being read out of the shift register means **74** and this operation is repeated for each succeeding bit position of the eight (**8**) bit characters being written into and read from the shift register means **78.** As the eight (**8**) bit character being read out of the shift register means **74** consists of all Zeros (**0**'s), as aforesaid, the first One (**1**) bit to appear in the eight (**8**) bit character being inserted into shift register means **74** will produce a high logic level output from the output of AND gate **134** which will cause the output of OR gate **136** to go high and reset counter means **80** through conductor **118** and this action will be repeated each time the bit being loaded in the first eight (**8**) bit character representing the key depressed is a One (**1**). In addition, each One (**1**) bit to appear in the eight (**8**) bit character being inserted into shift register means **74** will be applied through conductor **122** to the data input D of the flip-flop $FF_1$ to toggle this flip-flop.

After output terminal $TP_8$ has been pulsed by the input circuitry depicted in FIG. **6A**, the first eight (**8**) bit character representing the key depressed will be fully loaded into the shift register means **74** and the counter means **80** will be in its reset condition due to the action of the character identity check circuit indicated by the dashed block **82,** as aforesaid. Therefore, if it is assumed that this initially loaded character has passed the test imposed by the AND gate $G_1$ and the data presence circuit indicated by the dashed block **76,** and had the requisite number of One (**1**) bits present therein to toggle flip-flop $FF_1$ an odd or even number of times to pass the parity check imposed thereby, low level inputs will be present on the inputs to AND gate $G_2$ connected to input conductors **120** and **122** when the first eight (**8**) bit character representing the key depressed is fully loaded into the shift register means **74.** In addition, as the counter means **80** is in its reset condition, a low logic level will be applied from stage **5** thereof, through conductor **116** to the third input of AND gate $G_2$. Accordingly, when the input circuit illustrated in FIG. **6A** applies a negatively directed pulse to output terminal $TP_9$ to thereby indicate the completion of the character read cycle under discussion, all of the inputs to AND gate $G_2$ will be low to thereby meet the input conditions for this gate and hence the output of AND gate $G_2$ will go high to increment counter means **80** placing a high level in stage **1** thereof.

In the next character read cycle, the output on terminal $TP_0$ acts to reset flip-flop $FF_1$ and **110** and thereafter, as each of drive lines **1–8** is pulsed by output terminals $TP_1$–$TP_8$, the same eight (**8**) bit character as was previously inserted into shift register means **74** will be inserted for a second time thereinto, assuming that a spurious readout cycle does not occur. This, time, however, no resetting output should be produced on conductor **118** by the character identity check circuit indicated by dashed block **82** since the second application of an eight (**8**) bit character representing the key depressed should identically compare, on a bit for bit basis, with the first eight (**8**) bit character inserted therein as it represents the same information. Therefore, if it is assumed that the second reading of character information passes the three (**3**) tests imposed by the AND gate $G_1$, the data presence circuit indicated by dashed block **76** and the flip-flop $FF_1$; AND gate $G_2$ will again increment counter means **80** when the second eight (**8**) bit character is fully loaded into shift register means **74** and the second character read cycle is completed as indicated by a pulse on output $TP_9$. Thus, when the negatively directed pulse is applied from the terminal $TP_9$ to the AND gate $G_2$, the output of AND gate $G_2$ will go high incrementing counter means **80** whereby the high level which was present in stage **1** thereof is shifted into stage **2.** The foregoing operation will be repeated in the exemplary output circuit depicted in FIG. **6B** until the state of the counter means **80** is such that a high level is set in stage **4** thereof. Ordinarily, this would occur after four (**4**) repetitive read cycles for the eight (**8**) bit character associated with the key depressed; however, if in any character read cycle, the character information applied in sequence fails to pass any of the three (**3**) tests imposed, no incrementing of counter means **80** will take place in that cycle and the counter would, under most conditions of test failure be reset by the action of the character identity check circuit indicated by dashed block **82** because a character failing one of such three (**3**) tests would not ordinarily compare identically to a character which did. Furthermore, the character identity check circuit indicated by the dashed block **82** may operate independently of the test circuits to reset counter means **80** any time the eight (**8**) bit character being applied to the shift register means **74** does not identically correspond to the eight (**8**) bit character stored therein. At any rate, when a high level is shifted into stage **4** of the counter means **80,** at the completion of the fourth or subsequent reading of the eight (**8**) bit character representing the key depressed, this high level is applied through conductor **114** to flip-flop $FF_2$ to place this flip-flop in its set state and hence place a high or enabling level on the input to AND gate **88** connected to conductor **124** while a data output level is applied to conductor **126** to set a flag or the like. During the next character read out cycle the insertion of the fifth reading of the eight (**8**) bit character representing the key depressed causes the previously stored eight (**8**) bit character to be read out in series. Therefore, as AND gate **88** has now been enabled by the flip-flop $FF_2$, this previously read character is applied in serial format to the character output conductor indicated for application to utilization circuitry, not shown. At the completion of the fifth character read cycle, AND gate $G_2$ will again increment counter means **80** shifting the high level present in stage **4** thereof into stage **5.** This allows the output on terminal $TP_9$ to reset flip-flop $FF_2$ which disables AND gate **88** and removes the data output level from conductor **126.**

The high level now set in stage **5** of counter means **80,** inhibits AND gate $G_2$ from further incrementing of counter means **80** with succeeding character read cycles until the counter means **80** is subsequently reset. This means that although further repetitions of character information for the key depressed are loaded in sequence into the shift register means **74,** no further application thereof to the character output conductor or incrementing of the counter means **80** results. When the depressed key is released, coupling of the coding and coupling element associated with the key depressed terminates and a new all Zero (**0**) bit character is loaded into the shift register means **74.** This causes

the character identity check circuit indicated by dashed block **82** to reset counter means **80** and prepare the exemplary output circuitry depicted in FIG. **6B** for character information representing a newly depressed key.

For the exemplary rates of pulsing the drive conductors **1-8** discussed above in connection with FIG. **6A**, the readout of an eight (**8**) bit character associated with a single key depressed in keyboard arrangements according to the present invention may ordinarily be expected to be repeated from ten (10) to one hundred (100) times depending upon the nature of the application in which the exemplary keyboard arrangement is employed. Therefore, although the exemplary output circuit depicted in FIG. **6B** relies upon the repeated readout of character information to insure the accuracy and propriety of character information which is ultimately applied in serial format to utilization apparatus therefor, such reliance is in no way detrimental to the practical operational speeds of equipment employing the instant invention. Thus, when the exemplary output circuit depicted in FIG. **6B** is employed in conjunction with the exemplary keyboard arrangements according to the instant invention, the accuracy and propriety of the character information which is ultimately provided in series to utilization apparatus is assured. Although only a few exemplary data checks were provided in the output circuit depicted in FIG. **6B**, it will be appreciated by those of ordinary skill in the art that the testing techniques disclosed in conjunction therewith may be expanded to encompass other areas in which the testing of other aspects of the character content may be desired or alternative tests may be substituted for those specifically described above and this is particularly so in the area of parity.

FIGS. **7A** and **7B** illustrate another exemplary embodiment of signal translating keyboard arrangements according to the present invention. More particularly, in the exemplary keyboard arrangement depicted in FIG. **7A** and **7B** the interdigitated drive line coding and coupling elements are formed directly on the printed circuit board in an underlying relationship with the keys associated therewith and are directly connected to a pair of sense conductors, as illustrated in FIG. **7A**. The drive lines, in this embodiment of the instant invention, as shown in FIG. **7B**, take the form of an eight (**8**) conductor printed cable which is disposed beneath the keys in the exemplary keyboard arrangement and is adapted to be selectively placed into a capacitive coupling relationship with the interdigitated drive line coding and coupling element underlying a given key when that key is depressed. From a manufacturing standpoint, the instant embodiment of the present invention is somewhat more difficult to fabricate than the embodiment of the invention previously described due to the requirement that the drive line printed conductor must be rolled between individual keys in the keyboard arrangement so that selected portions thereof may be brought into a coupling relationship with the drive line coding and coupling elements on the printed circuit board; however, this embodiment of the instant invention has the advantage that more than one coding and coupling element may be provided for each key to allow a multi-function keyboard arrangement to be achieved whereby the resulting character codes obtained are a function of the physical position of the printed circuit board which may be selectively shifted. Thus, for instance, a single piece of keyboard equipment may selectively drive a printer or key punch apparatus depending on the position selected for the printed circuit board.

An exemplary arrangement for an appropriate printed circuit board for the embodiment of this invention illustrated in FIGS. **7A** and **7B** is shown in FIG. **7A**. The printed circuit board **140** shown in FIG. **7A** comprises a conventional printed circuit board having a plurality of sense conductors $S_{A\text{-}1}$–$S_{A\text{-}M}$ and $S_{B\text{-}1}$–$S_{B\text{-}M}$ and a plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ formed thereon. As none of the conductors present on the printed circuit board **140** is required to carry current, they need not be of high quality and may thus be formed by any of the techniques mentioned above in connection with FIG. **1**. The plurality of sense conductors $S_{A\text{-}1}$–$S_{A\text{-}M}$ and $S_{B\text{-}1}$ and $S_{B\text{-}M}$, as shown in FIG. **7A**, are disposed in parallel in an interleaved manner on the printed circuit board **140** so that a plurality of rows $1-(2M-1)$ are defined therebetween. In addition, each of the plurality of sense conductors $S_{A\text{-}1}$–$S_{A\text{-}M}$ and $S_{B\text{-}1}$ and $S_{B\text{-}M}$ has a plurality of connector segments $T_{A11}$–$T_{AMm}$ and $T_{B11}$–$T_{BMm}$ connected selectively thereto so that a plurality of columns $1-(2m-1)$ are defined therebetween on the printed circuit board **140**. The intersections between each of the plurality of rows $1-(2M-1)$ of sense conductors $S_A$ and $S_B$ and each of the plurality of columns $1-(2m-1)$ of connector segments $T_A$ and $T_B$ are locations at which each of the plurality of coding and coupling elements $C_{11}$–$C_{Nn}$ may be formed by selectively connecting drive line coupling segments **1'-8'** to the connector segments $T_A$ and $T_B$ located at that intersection so that the binary code sequence for that coding and coupling element is formed wherein sense conductor $S_A$ is again arbitrarily designated as the Zero (**0**) sense line while sense conductor $S_B$ is designated as the One (**1**) sense line. However, as it is preferable that some spacing be provided between at least the columns of coding and coupling elements on the printed circuit board **140** to practically accommodate the positioning of a key array thereon, only alternate columns $1-(2n-1)$ on the printed circuit board **140** will normally have coding and coupling elements $C_{11}$–$C_{Nn}$ formed therein, unless two (**2**) coding and coupling elements are to be associated with each key on a displacable printed circuit board in a manner to be described subsequently. Of course, as will be apparent to those of ordinary skill in the art, alternate rows between the plurality of horizontally disposed sensed conductors $S_{A\text{-}1}$–$S_{A\text{-}M}$ and $S_{B\text{-}1}$–$S_{B\text{-}M}$ could also be employed.

All of the plurality of Zero (**0**) sense conductors $S_{A\text{-}1}$–$S_{A\text{-}M}$ are connected in parallel through conductor **142** so that all pulses applied thereto which thus represent Zeros (**0**'s) are read out in series on sense line $S_A$. Similarly, all of the plurality of One (**1**) sense conductors $S_{B\text{-}1}$–$S_{B\text{-}M}$ are connected in parallel through conductor **144** so that all pulses applied thereto, which represent Ones (**1**'s), are read out in series on sense line $S_B$. Sense lines $S_A$ and $S_B$ are connected, as indicated in FIG. **7A**, to the inputs of a differential amplifier means **146**. The differential amplifier means **146** may take the same form and function in the same manner as the differential amplifier means **46**, described in conjunction with FIG. **4B**, and thus serves to provide a bipolar output from the printed circuit board **140** in response to the application of positive pulses representing Ones

(1's) on sense line $S_B$ and positive pulses representing Zeros (0's) on sense line $S_A$. Although an output circuit in the form of a simple differential amplifier means **146** has been illustrated in FIG. 7A, it will be apparent to those of ordinary skill in the art that the output circuit depicted in FIG. 6B could also be employed as could any conventional form of output arrangement. The printed circuit board **140** is disposed on a high quality ground plane, not shown, which may take the same form as the ground plane discussed in conjunction with FIG. 1. It should be noted, however, that the ground plane is even more important in this embodiment of the invention than in the FIG. 1 embodiment because as each of the coding and coupling elements $C_{11}$–$C_{Nn}$ are connected directly to sense lines $S_A$ and $S_B$ the antenna-like characteristics thereof are substantially enhanced.

FIG. 7B is a side view of the instant embodiment of the keyboard arrangement according to the present invention and is employed to illustrate the relationship between the printed circuit board **140** and the drive lines therefor. As shown in FIG. 7B, a row of keys $K_{11}$ and $K_{1m}$ are disposed above the surface of the printed circuit board **140** and are physically positioned to overlie coding and coupling elements $C_{11}$ and $C_{1n}$ as indicated by the column indications in FIG. 7B. The keys $K_{11}$ and $K_{1m}$ are only schematically illustrated in FIG. 7B; however, it will be appreciated that they may take the same form as the key means illustrated in FIG. 3 except that no coding and coupling printed circuit spot is fixedly mounted to the underside of cushioning pad **38.** Furthermore, although only two keys $K_{11}$ and $K_{1m}$ are illustrated in FIG. 7B, it will be understood that in actual keyboard arrangements according to this embodiment of the instant invention as many keys as are present in a row or column of a usual keyboard for the equipment being considered would be employed with succeeding rows $2-(2M-1)$ of keys being physically positioned behind keys $K_{11}$ and $K_{1m}$ and overlying rows $2-(2M-1)$ on the printed circuit board **140.**

A printed conductor **148** or another conventional form of flat, ribbon-like cable having, in this case, eight (8) parallel, printed conductors therein is wound back and forth in the serpentine fashion illustrated in FIG. 1 beneath each row of keys so that the printed conductor **148** is oppositely directed beneath adjacent rows of keys to thereby reduce noise. With respect to each individual row of keys, as shown in FIG. 7B, the printed conductor **148** is fixedly positioned to be flat across the underside of each key, as may be achieved by fixedly mounting these portions of the printed conductors **148** to the key bottom or cushioning pad **38** with adhesive or the like, and is rolled between adjacent keys $K_{11}$ and $K_{1m}$ so that a loop-like or U-shaped segment is formed intermediate adjacent keys. Although the dimension of the U-shaped segment intermediate adjacent keys is not critical, a sufficient length of the printed conductor **148** must be contained within the loop formed so that a key may be fully displaced in the downward direction, bringing the surface of the printed conductor thereunder into what is tantamount to physical contact with its underlying coding and coupling element on the printed circuit board **140,** without fully exhausting the material in the loops on either side of that key so that adjacent keys are not displaced. Each of the eight (8) parallel conductors within the printed conductor **148,** as will by now be apparent to those of ordinary skill in the art, are adapted to be pulsed in sequence in the same manner as described for printed conductors **1–8** in FIG. **1** by input circuits similar to those shown in FIG. **4A** or **6A** or the like so that the leading edge of the drive pulses thereby applied to the drive conductors within the printed conductor **148** may be capacitively coupled in sequence to drive line coupling segments **1′–8′** on a selected coding and coupling element $C_{11}$–$C_{Nn}$ when the key associated therewith is depressed. Once the drive pulses applied in sequence to the eight (8) parallel conductors within the printed conductor **148** are capacitively coupled in sequence to the drive line coupling segments **1′–8′** on an underlying coding and coupling element $C_{11}$–$C_{Nn}$ selected by the depression of a key on the keyboard, the capacitively coupled bit information is coded by the connection sequence of the drive line coupling segments **1′–8′** to the sense conductors $S_A$ and $S_B$ on that coding and coupling element and applied to the inputs of the differential amplifier means **146** as a series of pulses representing Ones (1's) and Zeros (0's) in the same manner as illustrated in FIG. **5** for the embodiment of this invention there considered. The differential amplifier means **146** transforms the One (1) and Zero (0) pulses received into a bipolar waveform as indicated in FIG. 7A whereby a direct serial readout of an eight (8) bit character for the key depressed is again obtained.

The printed circuit board **140** may be overcoated by a thin layer of insulating material **150** to avoid the possibility of shorting and is mounted, as aforesaid, on a high quality ground plane **152** made of conductive material. In the embodiment of the keyboard arrangement depicted in FIGS. 7A and 7B, the lumped capacitance of the sense lines $S_A$ and $S_B$ on the printed circuit board **140** is much larger than that exhibited by the embodiment of the invention depicted in FIG. **1** due to the substantial increase in the length of the sense lines caused by the interdigitated coding and coupling element $C_{11}$–$C_{Nn}$ which in this case are directly connected to sense conductors $S_A$ and $S_B$ and hence form a part thereof. This means that the signals on one sense line will tend to be coupled to the other sense line and therefore, it may be desirable to reduce the impedance exhibited by each sense line $S_A$ and $S_B$ by placing a capacitor, having a value for example of one hundred picofarads (100 pf), in parallel therewith by connecting such capacitor between the sense line and ground. In the embodiment of the invention depicted in FIGS. 7A and 7B, capacitive coupling between the drive lines in the printed conductor **148** and the drive line coupling segments **1′–8′** on the coding and coupling elements $C_{11}$–$C_{Nn}$ will not generally occur until a key has been sufficiently depressed to bring them within about a quarter of a millimeter of each other. Although, eight (8) bit characters have again been employed in the instant invention, it will be apparent to those of ordinary skill in the art, that more or less coding bits may be obtained by increasing or decreasing the number of parallel drive conductors in printed conductor **148** and correspondingly, increasing or decreasing the number of drive line coupling segments **1′–8′** in each coding and coupling element $C_{11}$–$C_{Nn}$.

The embodiment of this invention illustrated in FIGS. 7A and 7B readily lends itself to multi-purpose keyboard arrangements. For instance, should it be desired to provide a keyboard arrangement capable of selectively driving a printer and keypunch apparatus, columns **1,** $(2m-1)$ etc. may be provided with coding and

coupling elements whose codes are suited for application to a printer while columns **2**, **2m**, etc. are provided with coding and coupling elements whose codes provide character information especially suited for application to keypunch apparatus. A function switch on the keyboard housing for selectively enabling the printer or keypunch modes of operation would then merely be provided with means for selectively displacing the printed circuit board **140** and ground plane **152**, as shown in FIG. 7B, to the left for keypunch operation so that columns **2** and **2m** underlie keys $K_{11}$ and $K_{1m}$, respectively, and to the right for printer operation so that columns **1** and $(2m - 1)$ underlie keys $K_{11}$ and $K_{1m}$ in the manner shown for printer operation. Therefore, as all that is being selectively displaced is the self-contained printed circuit board **140** and the ground plane **152**, this could easily be accomplished. Similarly, these functions could also be achieved by placing the keys on ¾ inch centers while the coding and coupling elements $C_{11}$–$C_{Nn}$ are placed on ⅜ inch centers. Furthermore, as will be apparent to those of ordinary skill in the art, four (**4**) way selectivity may readily be obtained by extending the foregoing techniques to alternate rows as well as columns. Thus, if means for selective front to back displacement of the printed circuit board **140** and ground plane **152** were provided, any coding and coupling element present at any of the intersections between rows **1** and **2** and columns **1** and **2** in FIG. 7A could be placed beneath key $K_{11}$ with similar results for all of the other keys on the keyboard arrangement. Accordingly, the embodiment of the instant invention depicted in FIGS. 7A and 7B provides a highly versatile keyboard arrangement while incidentally avoiding the need for ground conductor isolation between the drive lines.

The foregoing description of the instant invention will render it manifest that the keyboard signal translating methods and apparatus taught by the present invention not only provides for the direct encoding of input information to a keyboard and the direct output of coded information in a serial format therefrom, but in addition thereto, allows simplified printed circuit configurations to completely replace the relatively complex structure heretofore required in output keyboard arrangements. Thus, not only is the need for the independent switches for each key or group of keys, the electrical connections to the switches, the complex mechanical or electrical encoding means, and electrical connections to such encoding means, and the parallel to series converting arrangements so prevalent in the prior art completely avoided in the employment of the instant invention but manufacturing costs are greatly reduced because all mechanical parts such as key structure are the same while printed circuit techniques are employed to form specialized components such as the coding and coupling elements. Accordingly, the signal translating techniques taught by the instant invention result in output keyboard arrangements which are highly simplified and directly provide an output which is fully conversant with the state of the art utilization circuitry. Furthermore, the keyboard signal translating methods and apparatus taught by the present invention readily admit of provision with additional and/or specialized keys and associated character outputs without any substantial departure from the structure which might be employed in the formation of a keyboard arrangement for a conventional application and the repetitive character output available readily allows data processing techniques to be directed to the function of checking the accuracy and propriety of the character information obtained prior to its application to utilization circuitry therefor. In addition, the signal translating techniques disclosed herein are fully reversible and hence should it be desired to obtain output information in a parallel bit format, it would only be necessary to apply drive signals to one or both of the sense conductors while properly coded bit information could be obtained from the drive conductors.

Although the present invention has been described in association with several exemplary embodiments, it will be apparent that many modifications and variations with respect to the specific teachings contained herein are available and may be readily practiced by those of ordinary skill in the art without deviating from the inventive concepts presented herein. For instance, although capacitive coupling techniques were described, it will be apparent to those of ordinary skill in the art that inductive coupling techniques could be similarly employed to achieve the desired result. Furthermore, although the exemplary embodiments of the invention disclosed herein employed capacitive coupling configurations wherein either the drive lines and sense lines were formed on a printed circuit board and the coding and coupling elements were separately provided on the keys or where the coding and coupling elements were jointly formed with the sense conductors on the printed circuit board while the drive lines were associated with the keys; other arrangements are available so long as the requisite coupling relationships obtain between the drive lines and sense conductors and are established through the coding and coupling elements. Thus, for instance, the sense conductors and the drive conductors could be present in printed conductors associated with the keys as could the combination of the sense conductors and coding and coupling elements; however, these arrangements would tend to be more noisy and more difficult to fabricate. Further, although in the exemplary embodiments of this invention disclosed herein, the drive lines and sense lines were generally disposed in parallel, additional noise reduction may be obtained by disposing the drive conductors and sense conductors transversely to avoid linkage therebetween and having the coding and coupling elements arranged so that drive lines coupling segments therein are in a parallel relationship with respect to the drive lines and have other portions suitably disposed for direct or capacitive coupling to the sense conductors. This arrangement would be particularly easy to achieve in embodiments of this invention similar to that depicted in FIGS. 7A and 7B. It should also be noted that although two sense conductor outputs were employed in each of the exemplary embodiments disclosed herein so that the validity of both One (**1**) and Zero (**0**) pulse information could always be ascertained, it is also possible to rely upon a single sense conductor. In this case, One (**1**) or Zero (**0**) pulse information would be selectively applied to such single sense conductor while the other form of binary information, i.e. Zero (**0**) or One (**1**) information, would not be applied to any sense line whereby its presence would be indicated by the absence of information on the single sense conductor at times when the drive lines are pulsed.

In addition, although several specific structures and circuits were disclosed herein in an effort to acquaint

the reader with practical means which might reasonably be expected to accomplish the requisite functions within this invention of selectively establishing a desired capacitive relationship, applying drive pulses to the drive lines and accepting the output of the sense conductors, such specific structure and circuits admit of wide variation and hence should be deemed to have been set forth only for purposes of illustration and not by way of limitation. For instance, although specialized structure capable of being easily fabricated and placed within a housing while providing appropriate touch characteristics was disclosed in conjunction with FIG. **3**, it will be appreciated that any plunger type key structure could be employed. Similarly, although specific input circuits for applying specialized drive pulses in sequence to the drive conductors was disclosed in conjunction with FIGS. **4A** and **6A**, it will be appreciated that any input circuit capable of applying a pulse having a rapidly rising or rapidly falling leading or trailing edge in sequence to each of the drive conductors may be employed and that specialized additional pulses are only required to the extent that they provide necessary inputs to the output circuitry. Furthermore, although only unipolar pulses of specified waveform were considered in detail above, waveforms of any shape may be employed so long as the requisite leading and/or trailing edges are present and under certain circumstances bursts of an alternating waveform might be preferred for application to the drive lines due to the unique signature of such bursts when viewed from the standpoint of signals applied to the sense lines. In like manner, although specific output circuits for the sense lines were described in conjunction with FIGS. **4B** and **6B**, any output circuitry might be employed therefor. Thus, if it were desired to maintain a two (**2**) line logic configuration individual sense amplifiers could be employed while if a testing output configuration were desired, the output configuration described in conjunction with FIG. **6B** could be altered to add or delete selected ones of the tests carried out therein or alternate logical testing arrangements could be added. For example, in the output arrangement described in conjunction with FIG. **6A**, if a pulse is simultaneously detected on both the One (**1**) and Zero (**0**) sense lines, the anti-rollover function provided by AND gate $G_1$ inhibits for a full character cycle to allow the duration detection associated with the counter to merely skip that cycle. If the condition persists, the logic must wait for one of the keys to be raised so that it may operate on the remaining valid sequel. If desired, the anti-rollover function could be modified to check for noise by delaying its inhibiting function for a brief interval to ascertain whether one input subsides. Alternatively, by the addition of another character register, it is possible to determine the character code for the second key by subtracting the codes previously stored in the shift register from the new signal.

Furthermore, although not specifically mentioned above, keyboard arrangements according to the present invention may readily be provided with specialized functions which are desirable in the application in which such keyboard arrangement is employed. For example, in typewriter and calculator applications, it is often desirable to provide one or more keys in the keyboard arrangement formed which automatically repeat the printing of the character associated therewith if such key is held depressed with more than the usual pressure, i.e. in a typewriter, for instance, the keys associated with the "x," dash, underscore, space, back space and carriage return normally have this function. As the printed circuit boards employed in the instant invention are normally flexible structures even as mounted on a ground plane, the repeat function may be accomplished by placing repeat contacts beneath the printed circuit board in such manner that when a predetermined additional pressure is applied to the key, the printed circuit board will be flexed in the downward direction to close the repeat contacts and cause the character associated with the key depressed to be repeatedly read out to utilization apparatus therefore. This may readily be accomplished because key character information is applied to the sense lines as long as the key is depressed and hence the repeat contacts need only be employed to repeatedly enable gating circuitry. Alternatively, the printed circuit board and ground plane could be mounted on a spring platform which could be depressed, upon added pressure to the key, to close a set of key contacts located on the platform beneath the ground plane. Another approach to achieving the same result would be a repeat conductor on the printed circuit board in registration with a raised contact on the key. In this case, the repeat contacts would not be closed until sufficient pressure is applied to the key to fully compress the cushioning pad on which the coding and coupling element or drive line conductor is located.

While the invention has been described in connection with several exemplary embodiments thereof, it will be understood that many modifications will be readily apparent to those of ordinary skill in the art; and that this application is intended to cover any adaptions or variations thereof. Therefore, it is manifestly intended that this invention be only limited by the claims and the equivalents thereof.

What is claimed is:

**1.** Output keyboard apparatus comprising:

a plurality of key means for designating, when actuated, predetermined inputs to said output keyboard;

first and second sense conductor means for receiving coded bit information to form characters representing said predetermined inputs;

a plurality of drive line means for sequentially receiving drive pulses to be selectively encoded into said bit information, each of said plurality of drive line means adapted to receive at least one drive pulse and each drive pulse received being adapted to be encoded to form bit information in at least one bit position of said characters representing said predetermined inputs; and

a plurality of coding and coupling means for selectively receiving drive pulses in sequence from each of said plurality of drive line means and applying each drive pulse received to one of said first and second sense conductor means according to a preselected coding sequence, at least one of said plurality of coding and coupling means being associated with each of said plurality of key means and defining said character representing said predetermined input designated thereby, each of said plurality of coding and coupling means acting to selectively receive said drive pulses from said plurality of drive line means and apply each drive pulse received to one of said first and second sense conduc-

tor means only when said key means associated therewith is activated.

2. The output keyboard apparatus according to claim 1 wherein said plurality of drive line means comprise a plurality of individual drive conductor means disposed in parallel on a surface, said plurality of key means comprises depressible key means disposed over said surface and said plurality of coding and coupling means each comprise a conductor arrangement mounted on an underside of each of said depressible key means in an overlying relationship with respect to said plurality of individual drive conductor means on said surface and adapted to be brought into a coupling relationship therewith when said key means is depressed.

3. The output keyboard apparatus according to claim 2 wherein each mounted conductor arrangement forming one of said plurality of coding and coupling means comprises:

first means for applying received drive pulses to one of said first and second sense conductor means;

second means for applying received drive pulses to another of said first and second sense conductor means; and

a plurality of drive line coupling segments disposed in parallel with said plurality of individual drive conductor means, one of said plurality of drive line coupling segments being in an overlying relationship with respect to each of said individual drive conductor means disposed on said surface and effective to receive drive pulses present therein when said conductor arrangement is placed into a coupling relationship therewith, said plurality of drive line coupling segments being selectively connected to said first and second means to encode drive pulses received by said plurality of drive line coupling segments into said coded bit information.

4. The output keyboard apparatus according to claim 3 wherein said first and second sense conductor means comprise individual sense conductor means disposed on said surface in parallel with said plurality of individual drive conductor means, said first and second means for applying received drive pulses comprise first and second sense conductor coupling segments disposed in parallel with said individual sense conductor means, said first sense conductor coupling segment being in an overlying relationship with respect to one of said individual sense conductor means disposed on said surface and said second sense conductor coupling segment being in an overlying relationship with respect to another of said individual sense conductor means disposed on said surface, said first and second sense conductor coupling segments acting to apply said coded bit information to their underlying sense conductor means when said conductor arrangement is placed into a coupling relationship therewith.

5. The output keyboard apparatus according to claim 4 wherein the surface upon which said plurality of individual drive conductor means and individual sense conductor means are disposed is proximate an underlying ground plane.

6. The output keyboard apparatus according to claim 5 wherein said conductor arrangement comprises printed conductors formed on a printed circuit board.

7. The output keyboard apparatus according to claim 6 additionally comprising isolating conductor means maintained at a reference potential positioned intermediate said individual sense conductor means and said plurality of individual drive conductor means disposed in parallel on said surface.

8. The output keyboard apparatus according to claim 7 wherein said individual sense conductor means, said isolating conductor means and said plurality of individual drive conductor means comprise printed conductors formed on a printed circuit board, said printed circuit board being disposed on a conductive plate acting as ground plate.

9. The output keyboard apparatus according to claim 8 wherein at least one set of printed conductors being brought into said coupling relationship is insulated.

10. The output keyboard apparatus according to claim 9 wherein said plurality of key means having said conductor arrangements mounted to said undersides thereof are arranged in columns and rows, said individual sense conductor means and plurality of drive conductor means disposed in parallel being arranged in a serpentine configuration so as to underlie all of said plurality of key means passing in a first direction beneath one of said columns and rows and in a second, opposite direction beneath adjacent ones of said columns and rows.

11. The output keyboard apparatus according to claim 10 additionally comprising means for equalizing cross-talk between each of said individual sense conductor means and said plurality of drive conductor means.

12. The output keyboard apparatus according to claim 11 wherein all of said coupling is capacitive coupling.

13. The output keyboard apparatus according to claim 1 wherein each of said plurality of coding and coupling means comprise a conductive arrangement defining a plane and all of said conductive arrangements reside in substantially the same plane, said plurality of key means comprising depressible key means disposed over said plane in an arrangement wherein each of said plurality of key means overlies said at least one of said plurality of coding and coupling means associated therewith, said plurality of drive line means comprising individual drive conductor means disposed in parallel with succeeding parallel portions thereof mounted upon an underside of each of said depressible key means in an overlying relationship with respect to said conductor arrangements, said individual drive conductor means being adapted to be brought into a coupling relationship with an individual one of said conductor arrangements when said key means associated therewith is depressed.

14. The output keyboard apparatus according to claim 13 wherein each conductor arrangement defining a plane comprises:

first means for applying received drive pulses to one of said first and second sense conductor means;

second means for applying received drive pulses to another of said first and second sense conductor means; and

a plurality of drive line coupling segments disposed in said plane in parallel with an individual one of said succeeding parallel portions of individual drive conductor means disposed in parallel, one of said plurality of drive line coupling segments being in an underlying relationship with respect to each of said parallelly disposed individual drive conductor means and effective to receive drive pulses present therein when said individual drive conductor

means are placed into a coupling relationship therewith, said plurality of drive line coupling segments being selectively connected to said first and second means to encode drive pulses received by said plurality of drive line coupling segments into said coded bit information.

**15.** The output keyboard apparatus according to claim **14** wherein said first and second sense conductor means comprise individual sense conductor means disposed in parallel in said plane, said first means for applying received drive pulses comprises conductor means directly connected to one of said individual sense conductor means and said second means for applying received drive pulses comprises conductor means directly connected to another of said individual sense conductor means.

**16.** The output keyboard apparatus according to claim **15** wherein said individual sense conductor means and said plurality of coding and coupling elements formed by said conductor arrangements are disposed in an underlying ground plane.

**17.** The output keyboard apparatus according to claim **16** wherein said individual drive conductor means disposed in parallel are present in a ribbon-like multi-conductor cable means, said ribbon-like multi-conductor cable means having succeeding portions thereof mounted upon an underside of each of said depressible key means with the portions thereof intermediate adjacent keys being formed into U-shaped loops to allow for the selective depression of said depressible key means.

**18.** The output keyboard apparatus according to claim **17** wherein said individual sense conductor means and said plurality of coding and coupling elements formed by said conductor arrangements comprise printed conductors formed on a printed circuit board, said printed circuit being disposed on a conductive plate acting as said ground plane.

**19.** The output keyboard apparatus according to claim **18** wherein at least one set of printed conductors being brought into said coupling relationship is insulated.

**20.** The output keyboard apparatus according to claim **19** wherein said plurality of key means having said ribbon-like multi-conductor cable means mounted to the undersides thereof are arranged in columns and rows, said ribbon-like multi-conductor cable means being arranged in a serpentine configuration so as to underlie all of said plurality of key means passing in a first direction beneath one of said columns and rows and in a second, opposite direction beneath adjacent ones of said columns and rows.

**21.** The output keyboard apparatus according to claim **20** wherein all of said coupling is capacitive coupling.

**22.** The output keyboard apparatus according to claim **1** additionally comprising means connected to said first and second sense conductor means for algebraically subtracting said coded bit information present on one of said first and second sense conductor means from coded bit information present on another of said first and second sense conductor means to form said characters representing said predetermined inputs.

**23.** The output keyboard apparatus according to claim **22** wherein said means for algebraically subtracting comprises differential amplifier means producing a bipolar output waveform to form said characters representing said predetermined inputs.

**24.** The output keyboard apparatus according to claim **23** wherein said coded bit information takes the form of pulses and said characters include at least one pulse for each of said plurality of drive line means which are present.

**25.** The output keyboard apparatus according to claim **1** additionally comprising commutator means for applying a drive pulse to each of said plurality of drive line means in sequence, the time interval required for said commutator means to apply one drive pulse to all of said plurality of drive line means being defined as a character read cycle.

**26.** The output keyboard apparatus according to claim **25** additionally comprising first testing means for ascertaining if coded bit information is simultaneously present on said first and second sense conductor means, said first testing means being connected to receive bit information present on each of said first and second sense conductor means.

**27.** The output keyboard apparatus according to claim **25** additionally comprising second testing means for ascertaining if coded bit information is absent on both of said first and second sense conductor means each time a drive pulse is applied to one of said plurality of drive line means by said commutator means, said second testing means being connected to receive bit information present on each of said first and second sense conductor means.

**28.** The output keyboard apparatus according to claim **25** wherein a plurality of character cycles occur each time one of said plurality of key means is actuated and additionally comprising third testing means for ascertaining that the same bit information is produced a predetermined number of times for each plurality of character read cycles which occur each time one of said plurality of key means is actuated.

**29.** The output keyboard apparatus according to claim **25** additionally comprising:

first and second threshold detector means connected to said first and second sense conductor means for detecting coded bit information present thereon and providing an output only under conditions where said detected code bit information exceeds a predetermined threshold level;

shift register means connected to receive said output from one of said first and second threshold detector means; and

shift pulse generator means for producing a shift pulse each time a drive pulse is applied to one of said plurality of drive line means by said commutator means, said shift pulse generator means being connected to a shift input of said shift register means and causing a binary code bit to be inserted therein each time a shift pulse is generated, a first form of binary code bit being inserted whenever an output is received from said one of said first and second threshold detector means and a second form of binary code bit being inserted whenever an output is not received from said one of said first and second threshold detector means.

**30.** The output keyboard apparatus according to claim **29** additionally comprising first testing means for ascertaining if coded bit information is simultaneously present on said first and second sense conductor means, said first testing means being connected to re-

ceive bit information present on each of said first and second sense conductor means.

**31.** The output keyboard apparatus according to claim **30** additionally comprising second testing means for ascertaining if coded bit information is absent on both of said first and second sense conductor means each time a drive pulse is applied to one of said plurality of drive line means by said commutator means, said second testing means being connected to receive bit information present on each of said first and second sense conductor means.

**32.** The output keyboard apparatus according to claim **31** wherein a plurality of character read cycles occur each time one of said plurality of key means is actuated and additionally comprising third testing means for ascertaining that the same bit information is produced a predetermined number of times for each plurality of character read cycles which occur each time one of said plurality of key means is actuated.

**33.** The output keyboard apparatus according to claim **32** wherein said third testing means comprises:

counter means for counting the number of times that said same bit information is produced for each plurality of character read cycles which occur each time one of said plurality of key means is actuated;

means connected to said counter means for incrementing said counter means at the completion of each character read cycle; and

means for monitoring an input and output of said shift register means to determine if corresponding bit positions in character information present therein is the same, said last-named means resetting said counter means whenever said corresponding bit positions do not contain the same information.

**34.** The output keyboard apparatus according to claim **33** additionally comprising gating means for receiving binary coded bit information in series from said shift register means and selectively applying said binary coded bit information in series to output terminal means when said gating means is selectively enabled;

means for selectively enabling said gating means whenever said counter means reaches a predetermined count; and

means for inhibiting said incrementing means whenever at least one of said first and second testing means indicates that the condition which it seeks to ascertain is present.

**35.** The output keyboard apparatus according to claim **12** additionally comprising commutator means for applying a drive pulse to each of said plurality of drive line means in sequence, the time interval required for said commutator means to apply one drive pulse to all of said plurality of drive line means being defined as a character read cycle.

**36.** The output keyboard apparatus according to claim **35** additionally comprising:

first and second threshold detector means connected to said first and second sense conductor means for detecting coded bit information present thereon and providing an output only under conditions where said detected code bit information exceeds a predetermined threshold level;

shift register means connected to receive said output from one of said first and second threshold detector means; and

shift pulse generator means for producing a shift pulse each time a drive pulse is applied to one of said plurality of drive line means by said commutator means, said shift pulse generator means being connected to a shift input of said shift register means and causing a binary code bit to be inserted therein each time a shift pulse is generated, a first form of binary code bit being inserted whenever an output is received from said one of said first and second threshold detector means and a second form of binary code bit being inserted whenever an output is not received from said one of said first and second threshold detector means.

**37.** The output keyboard apparatus according to claim **36** additionally comprising first testing means for ascertaining if coded bit information is simultaneously present on said first and second sense conductor means, said first testing means being connected to receive bit information present on each of said first and second sense conductor means.

**38.** The output keyboard apparatus according to claim **37** additionally comprising second testing means for ascertaining if coded bit information is not present on at least one of said first and second sense conductor means each time a drive pulse is applied to one of said plurality of drive line means by said commutator means, said second testing means being connected to receive bit information present on each of said first and second sense conductor means.

**39.** The output keyboard apparatus according to claim **38** wherein a plurality of character read cycles occur each time one of said plurality of key means is actuated and additionally comprising third testing means for ascertaining that the same bit information is produced a predetermined number of times for each plurality of character read cycles which occur each time one of said plurality of key means is actuated.

**40.** The output keyboard apparatus according to claim **39** wherein said third testing means comprises:

counter means for counting the number of times that said same bit information is produced for each plurality of character read cycles which occur each time one of said plurality of key means is actuated;

means connected to said counter means for incrementing said counter means at the completion of each character read cycle; and

means for monitoring an input and output of said shift register means to determine if corresponding bit positions in character information therein is the same, said last-named means resetting said counter means whenever said corresponding bit positions do not contain the same information.

**41.** In output keyboards having a plurality of key means for designating predetermined inputs, the method of signal translation comprising the steps of:

providing sense conductor means for receiving coded bit information to form characters representing said predetermined inputs;

providing a plurality of drive conductors in an underlying relationship with respect to each of said plurality of key means;

applying drive pulses to each of said plurality of drive conductor means in sequence; and

coupling selected ones of said drive pulses, upon an actuation of one of said plurality of key means from said plurality of drive conductor means to said sense conductor means in accordance with a binary

code assigned to said actuated one of said plurality of key means.

**42.** The method of output keyboard signal translation according to claim **41** wherein said sense conductor means comprises first and second sense lines and said step of coupling selected ones of said drive pulses, upon an actuation of one of said plurality of key means, is performed by coupling selected ones of said drive pulses to one of said first and second sense lines and coupling the remaining ones of said drive pulses applied in sequence to said plurality of drive conductors to another of said first and second sense lines in accordance with a binary code assigned to said actuated one of said plurality of key means.

**43.** In output keyboard apparatus having a plurality of actuatable key means for designating predetermined inputs, the improvement comprising:

sense conductor means for receiving coded bit information in the form of characters representing said predetermined inputs;

a plurality of drive line means for sequentially receiving drive pulses to be selectively encoded into said bit information, each of said plurality of drive lines adapted to receive at least one drive pulse and each drive pulse received being adapted to be encoded to form bit information in at least one bit position of said characters representing said predetermined inputs; and

a plurality of coding and coupling means for selectively receiving drive pulses in sequence from said plurality of drive line means and applying at least selected ones of said received drive pulses to said sense conductor means according to a preselected coding sequence, at least one of said plurality of coding and coupling means being associated with each of said pluraty of actuatable key means and defining said character representing said predetermined input designated thereby, each of said plurality of coding and coupling means acting to selectively receive said drive pulses from said plurality of drive line means and apply at least selected ones of said received drive pulses to said sense conductor means only when said key means associated therewith is actuated.

**44.** In output keyboard apparatus having a plurality of actuatable key means for designating predetermined inputs, the improvement comprising:

a plurality of sense conductor means for receiving coded bit information in the form of characters representing said predetermined inputs;

drive line means for receiving drive pulses to be selectively encoded into said bit information to form said characters, said drive line means being adapted to receive at least one drive pulse for each character read and each drive pulse received being adapted to be encoded to form bit information in at least one bit position of said character representing said predetermined inputs; and

a plurality of coding and coupling means for selectively receiving said drive pulses from said drive line means and selectively applying each drive pulse received to at least a predetermined one of said plurality of sense conductor means according to a preselected coding sequence, at least one of said plurality of coding and coupling means being associated with each of said plurality of actuatable key means and defining said character representing said predetermined input designated thereby, each of said plurality of coding and coupling means selectively receiving said at least one drive pulse from said drive line means and applying each drive pulse received to at least a predetermined one of said plurality of sense conductor means in accordance with said preselected coding sequence only when said key means associated therewith is actuated.

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