



(51) International Patent Classification:
H01L 27/146 (2006.01)

(21) International Application Number:
PCT/US2009/006401

(22) International Filing Date:
7 December 2009 (07.12.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/122,860 16 December 2008 (16.12.2008) US
12/616,208 11 November 2009 (11.11.2009) US

(71) Applicant (for all designated States except US): **EASTMAN KODAK COMPANY** [US/US]; 343 State Street, Rochester, NY 14650-2201 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **SUMMA, Joseph, R.** [US/US]; 343 State Street, Rochester, NY 14650-2201 (US). **MCCARTEN, John, P.** [US/US]; 343 State Street, Rochester, NY 14650-2201 (US).

(74) Common Representative: **EASTMAN KODAK COMPANY**; 343 State Street, Rochester, NY 14650-2201 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: IMAGE SENSOR WITH THREE-DIMENSIONAL INTERCONNECT AND CCD

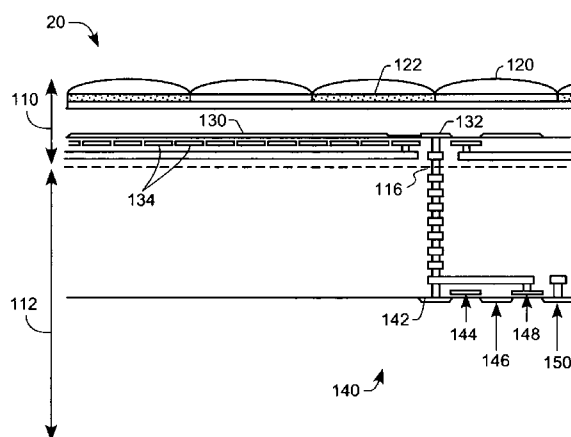


FIG. 3

(57) Abstract: An image sensor and associated image capture device and method include a sensing wafer with a plurality of charge storage elements. One or more floating diffusions are associated with the plurality of charge storage elements, and charge is transferred among the charge storage elements to the one or more floating diffusions. The one or more floating diffusions on the sensing wafer are electrically connected to support circuitry on a circuit wafer.

**IMAGE SENSOR WITH THREE-DIMENSIONAL INTERCONNECT AND
CCD**

TECHNICAL FIELD

5 The invention relates generally to the field of image sensors, and more particularly to a stacked image sensor construction.

BACKGROUND

10 A typical image sensor has an image sensing portion that includes a photosensitive area or charge collection area for collecting a charge in response to incident light and a transfer gate for transferring charge from the photosensitive area to a transfer mechanism. Usually, the sensing portion is fabricated within the same material layer and with similar processes as the control circuitry for the image sensor. In an effort to increase the number of pixels provided in an image
15 sensor, pixel size has been decreasing. However, as the pixel size shrinks, the illuminated area of the photodetector is also typically reduced, in turn decreasing the captured signal level and degrading performance.

 Stacked image sensor structures are known that consist of a sensor-only wafer over one (or more) circuit wafers. A stacked structure such as this
20 requires electrical interconnects between the wafers to be able to operate the sensor as well as read out the collected charges. The interconnects require the use of areas on the sensor and circuit wafers that could otherwise be used for charge collection and storage or support circuitry. Some interconnects also have the potential to cause noise in adjacent pixels.

25 Thus, a need exists for an improved stacked image sensor structure.

SUMMARY

 An image sensor and associated image capture device and method include a sensing wafer with a plurality of charge storage elements. A floating diffusion is associated with the plurality of charge storage elements, and a charge
30 is transferred among the charge storage elements to the floating diffusion. The floating diffusion is electrically connected to support circuitry of a circuit wafer.

The present invention thus provides the advantage of an improved image sensor structure.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Figure 1 is a block diagram illustrating an embodiment of an image capture device;

 Figure 2 is a perspective view conceptually illustrating an embodiment of image sensor;

 Figure 3 is a section view conceptually illustrating aspects of the
10 embodiment of the image sensor illustrated in Figure 2;

 Figure 4 is a block diagram conceptually illustrating further aspects of embodiments of the disclosed image sensor'

 Figure 5 is a top view conceptually illustrating an array of charge storage elements in accordance with disclosed embodiments;

15 Figure 6 is a block diagram conceptually illustrating an embodiment of a front illuminated image sensor; and

 Figure 7 schematically illustrates portions of an embodiment of a sensing wafer of an image sensor.

DETAILED DESCRIPTION

20 In the following Detailed Description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. In this regard, directional terminology, such as "top," "bottom," "front," "back," "leading," "trailing," etc., is used with reference to the orientation of the Figure(s)
25 being described. Because components of embodiments of the present invention can be positioned in a number of different orientations, the directional terminology is used for purposes of illustration and is in no way limiting. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention.
30 The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

Turning now to Figure 1, a block diagram of an image capture device shown as a digital camera embodying aspects of the present disclosure is illustrated. Although a digital camera is illustrated and described, the present invention is clearly applicable to other types of image capture devices. In the disclosed camera, light 10 from a subject scene is input to an imaging stage 11, where the light is focused by a lens 12 to form an image on an image sensor 20. The image sensor 20 converts the incident light to an electrical signal for each picture element (pixel).

The amount of light reaching the sensor 20 is regulated by an iris block 14 that varies the aperture and the neutral density (ND) filter block 13 that includes one or more ND filters interposed in the optical path. Also regulating the overall light level is the time that the shutter block 18 is open. The exposure controller block 40 responds to the amount of light available in the scene as metered by the brightness sensor block 16 and controls all three of these regulating functions.

This description of a particular camera configuration will be familiar to one skilled in the art, and it will be apparent to such a skilled person that many variations and additional features are present. For example, an autofocus system is added, or the lens is detachable and interchangeable. It will be understood that the present disclosure applies to various types of digital cameras where similar functionality is provided by alternative components. For example, the digital camera is a relatively simple point and shoot digital camera, where the shutter 18 is a relatively simple movable blade shutter, or the like, instead of the more complicated focal plane arrangement. Aspects of the present invention can also be practiced on imaging components included in non-camera devices such as mobile phones and automotive vehicles.

An analog signal from the image sensor 20 is processed by an analog signal processor 22 and applied to an analog to digital (A/D) converter 24. A timing generator 26 produces various clocking signals to select rows and pixels and synchronizes the operation of the analog signal processor 22 and the A/D converter 24. The image sensor stage 28 includes the image sensor 20, the analog

signal processor 22, the A/D converter 24, and the timing generator 26. The components of the image sensor stage 28 can be separately fabricated integrated circuits, or they could be fabricated as a single integrated circuit as is commonly done with CMOS image sensors. The resulting stream of digital pixel values from the A/D converter 24 is stored in a memory 32 associated with the digital signal processor (DSP) 36.

The digital signal processor 36 is one of three processors or controllers in the illustrated embodiment, in addition to a system controller 50 and an exposure controller 40. Although this partitioning of camera functional control among multiple controllers and processors is typical, these controllers or processors are combined in various ways without affecting the functional operation of the camera and the application of the present invention. These controllers or processors can comprise one or more digital signal processor devices, microcontrollers, programmable logic devices, or other digital logic circuits. Although a combination of such controllers or processors has been described, it should be apparent that one controller or processor can be designated to perform all of the needed functions. All of these variations can perform the same function and fall within the scope of this invention, and the term "processing stage" will be used as needed to encompass all of this functionality within one phrase, for example, as in processing stage 38 in Figure 1.

In the illustrated embodiment, the DSP 36 manipulates the digital image data in its memory 32 according to a software program permanently stored in program memory 54 and copied to the memory 32 for execution during image capture. The DSP 36 executes the software necessary for practicing image processing. The memory 32 includes of any type of random access memory, such as SDRAM. A bus 30 comprising a pathway for address and data signals connects the DSP 36 to its related memory 32, A/D converter 24 and other related devices.

The system controller 50 controls the overall operation of the camera based on a software program stored in the program memory 54, which can include Flash EEPROM or other nonvolatile memory. This memory can also be

used to store image sensor calibration data, user setting selections and other data which must be preserved when the camera is turned off. The system controller 50 controls the sequence of image capture by directing the exposure controller 40 to operate the lens 12, ND filter 13, iris 14, and shutter 18 as previously described, directing the timing generator 26 to operate the image sensor 20 and associated elements, and directing the DSP 36 to process the captured image data. After an image is captured and processed, the final image file stored in memory 32 is transferred to a host computer via an interface 57, stored on a removable memory card 64 or other storage device, and displayed for the user on an image display 88.

A bus 52 includes a pathway for address, data and control signals, and connects the system controller 50 to the DSP 36, program memory 54, system memory 56, host interface 57, memory card interface 60 and other related devices. The host interface 57 provides a high speed connection to a personal computer (PC) or other host computer for transfer of image data for display, storage, manipulation or printing. This interface is an IEEE1394 or USB2.0 serial interface or any other suitable digital interface. The memory card 64 is typically a Compact Flash (CF) card inserted into a socket 62 and connected to the system controller 50 via a memory card interface 60. Other types of storage that are utilized include, for example, PC-Cards, MultiMedia Cards (MMC), or Secure Digital (SD) cards.

Processed images are copied to a display buffer in the system memory 56 and continuously read out via a video encoder 80 to produce a video signal. This signal is output directly from the camera for display on an external monitor, or processed by the display controller 82 and presented on an image display 88. This display is typically an active matrix color liquid crystal display (LCD), although other types of displays are used as well.

The user interface, including all or any combination of viewfinder display 70, exposure display 72, status display 76 and image display 88, and user inputs 74, is controlled by a combination of software programs executed on the exposure controller 40 and the system controller 50. User inputs 74 typically include some combination of buttons, rocker switches, joysticks, rotary dials or

touchscreens. The exposure controller 40 operates light metering, exposure mode, autofocus and other exposure functions. The system controller 50 manages the graphical user interface (GUI) presented on one or more of the displays, for example, on the image display 88. The GUI typically includes menus for making
5 various option selections and review modes for examining captured images.

The exposure controller 40 accepts user inputs selecting exposure mode, lens aperture, exposure time (shutter speed), and exposure index or ISO speed rating and directs the lens and shutter accordingly for subsequent captures. The brightness sensor 16 is employed to measure the brightness of the scene and
10 provide an exposure meter function for the user to refer to when manually setting the ISO speed rating, aperture and shutter speed. In this case, as the user changes one or more settings, the light meter indicator presented on viewfinder display 70 tells the user to what degree the image will be over or underexposed. In an automatic exposure mode, the user changes one setting and the exposure
15 controller 40 automatically alters another setting to maintain correct exposure. For example, for a given ISO speed rating when the user reduces the lens aperture, the exposure controller 40 automatically increases the exposure time to maintain the same overall exposure.

Figure 2 conceptually illustrates an embodiment of the image
20 sensor 20. The image sensor 20 includes a sensing wafer 110 and a circuit wafer 112. The sensing wafer 110 has an array of pixels 114 that collect charges in response to incident light 100. The charges are sensed by the circuit wafer 112 by wafer interconnections 116. The circuit wafer 112 has support circuitry, including circuitry to read-out the charges collected by the pixels 114.

25 With known stacked image sensor structures, the wafer interconnections require the use of areas on the sensor and circuit wafers that could otherwise be used for charge collection and storage or support circuitry. Some interconnects also have the potential to cause noise in adjacent pixels. It is thus desirable to minimize the number of interconnects.

30 Embodiments of the disclosed image sensor 20 incorporate a charge transfer element into the sensor wafer that enables charge to be moved

across several pixels to an interconnect node 116 that need not be immediately adjacent to the charge collection point. This reduces the number of interconnects 116 required, preserving wafer area for other uses.

Figure 3 is a cross-section view conceptually illustrating further aspects of an embodiment of the image sensor 20. A micro lens 120 and a color filter array (CFA) 122 are situated over the sensing wafer 110. The pixels 114 include a plurality of charge transfer elements 130 and a floating diffusion 132 associated with the charge storage elements 130. The charge storage elements 130 illustrated in the embodiment shown in Figure 3 are charge coupled devices (CCD), which are operatively coupled to a photodetector, such as a photodiode, that collects a charge in response to received light. Figure 4 conceptually illustrates a photodiode 136 coupled to a CCD 130.

In another embodiment in accordance with the invention, the charge storage elements 130 are CCDs, with one or more of the CCDs configured as light-sensitive CCDs. The light-sensitive CCDs collect charge in response to received light.

A CCD array is typically composed of an array of closely spaced gates 134 that are used to effect transfer of charge in the CCD. The illustrated embodiment uses micro gaps between a single polycrystalline silicon (polysilicon) level to allow multiple adjacent gates on the same poly level.

A charge is transferred among the charge storage elements 130 to the floating diffusion 132, which is electrically connected to support circuitry 140 of the circuit wafer 112. In some embodiments, the support circuitry 140 includes a floating diffusion 142 that is electrically connected to the floating diffusion 132 on the sensing wafer 112 by the interconnects 116. In addition to the floating diffusion 142, the support circuitry can include, for example, a reset transistor connected to the floating diffusion 142, with the reset transistor including a reset gate 144, a V_{DD} voltage supply 146, and a source follower transistor coupled to V_{DD} and having input and output terminals 148, 150. In other embodiments, an input to the source follower transistor is coupled to the floating diffusion 132 on the sensing wafer 110, allowing an amplified signal to be transferred to the circuit

wafer 112. Figure 7 conceptually illustrates portions of the sensing wafer 110 including a source follower transistor 147 coupled to V_{DD} 146 with the source follower input 148 coupled to the floating diffusion 132 and the source follower output 150 coupled to the support circuitry on the circuit wafer 112 (not shown).

5 In the illustrated embodiments, the charge storage elements 130 are arranged in an array of rows and columns. Figure 5 illustrates an example of the array 160 of storage elements 130. The charge storage elements 130 are grouped into subsets 162 within each row with a respective floating diffusion 132 associated with each subset 162. Thus, the floating diffusions 132 in the sensing
10 wafer 110 each substitute for, or take the place of, one of the charge storage elements 130 in an embodiment in accordance with the invention. In another embodiment in accordance with the invention, each floating diffusion 132 substitutes for a portion of one charge storage element 130. A charge 164 is transferred horizontally to a respective floating diffusion node 132. Charge 164
15 can be transferred in either direction as illustrated in Figure 5.

 In yet another embodiment in accordance with the invention, the charge storage elements 130 are arranged in an array of rows and columns and the floating diffusions 132 are all disposed in one column at the edge or border of the array or within the array. Each row of charge storage elements has a floating
20 diffusion associated with the entire row. Charge is transferred among the charge storage elements in each row to the floating diffusion associated with the entire row.

 In some embodiments, such as the embodiment illustrated in Figure 3, the sensing wafer 110 is a back side illuminated sensor, where exposed light is
25 projected towards the back side surface of the sensing wafer 110. The photodetectors or light sensitive CCDs of the pixels 114 are located on a front side of the sensing wafer, which is thin enough so that light projected towards the backside of the substrate can reach the pixels. In other embodiments, the sensing wafer 110 is a front side illuminated sensor, where light is projected towards the
30 front side surface of the wafer. Figure 6 conceptually illustrates a front side

illuminated sensor 110, in which light 100 is projected through the associated metal and interconnect layers 163 towards the photodetectors or light sensitive CCDs in the pixels 114. The pixels are located above the substrate 164.

5 The invention has been described in detail with particular reference to certain preferred embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention. Additionally, even though specific embodiments of the invention have been described herein, it should be noted that the application is not limited to these embodiments. In particular, any features described with respect to one
10 embodiment may also be used in other embodiments, where compatible. And the features of the different embodiments may be exchanged, where compatible.

PARTS LIST

	10	light
	11	imaging stage
	12	lens
5	13	ND filter block
	14	iris block
	16	brightness sensor block
	18	shutter block
	20	image sensor
10	22	analog signal processor
	24	analog to digital (A/D) converter
	26	timing generator
	28	image sensor stage
	30	bus
15	32	memory
	36	digital signal processor (DSP)
	38	processing stage
	40	exposure controller
	50	system controller
20	52	bus
	54	program memory
	56	system memory
	57	host interface
	60	memory card interface
25	62	socket
	64	memory card
	70	viewfinder display
	72	exposure display
	74	user inputs
30	76	status display
	80	video encoder

	82	display controller
	88	image display
	100	light
	110	sensing wafer
5	112	circuit wafer
	114	pixels
	116	wafer interconnections
	120	lens
	122	color filter array
10	130	charge transfer elements/CCD
	132	floating diffusion
	134	CCD gates
	136	photodiode
	140	support circuitry
15	142	floating diffusion
	144	reset gate
	146	VDD
	147	source follower transistor
	148	source follower input
20	150	source follower output
	160	array
	162	array subsets
	163	metal and interconnect layers
	164	substrate

CLAIMS:

1. An image sensor, comprising:
a sensing wafer including a plurality of charge storage elements and one or
5 more floating diffusions associated with the plurality of charge
storage elements, wherein charge is transferred among the charge
storage elements to the one or more floating diffusions; and
a circuit wafer including support circuitry for the sensing wafer, wherein
the one or more floating diffusions are electrically connected to the
10 support circuitry.
2. The image sensor of claim 1, wherein the charge storage elements
are arranged in an array of rows and columns, and wherein the charge storage
elements are grouped into subsets within each row with a respective floating
15 diffusion associated with each subset.
3. The image sensor of claim 1 or claim 2, wherein at least one
floating diffusion substitutes for a charge storage element on the sensing wafer.
- 20 4. The image sensor of any one of claims 1 through 3, wherein the
support circuitry includes one or more floating diffusions that each are electrically
connected to respective floating diffusions on the sensing wafer.
5. The image sensor of claim 4, wherein the support circuitry includes
25 a reset gate coupled to at least one floating diffusion, a voltage supply, and a
source follower transistor.
6. The image sensor of any one of claims 1 through 3, further
comprising a source follower transistor coupled to at least one floating diffusion
30 on the sensing wafer.

7. The image sensor of any one of claims 1 through 6, wherein each charge storage element comprises a charge coupled device.

5 8. The image sensor of claim 7, wherein the charge coupled device is operatively connected to a photodetector.

9. An image capture device, comprising:
an imaging stage configured to receive light forming an image;
10 an image sensor receiving light from the imaging stage, the image sensor including:
a sensing wafer including a plurality of charge storage elements
and one or more floating diffusions associated with the
plurality of charge storage elements, wherein charge is
15 transferred among the charge storage elements to the one or more floating diffusions; and
a circuit wafer including support circuitry for the sensing wafer,
wherein each floating diffusion on the sensing wafer is
electrically connected to the support circuitry; and
20 a memory configured to store the received image.

10. The image capture device of claim 9, wherein the charge storage elements are arranged in an array of rows and columns, and wherein the charge storage elements are grouped into subsets within each row with a respective
25 floating diffusion associated with each subset.

11. The image capture device of claim 9 or claim 10, wherein at least one floating diffusion on the sensing wafer substitutes for a charge storage element.

12. The image capture device of any one of claims 9 through 11, wherein the support circuitry includes one or more floating diffusions that are each electrically connected to respective floating diffusions on the sensing wafer.

5

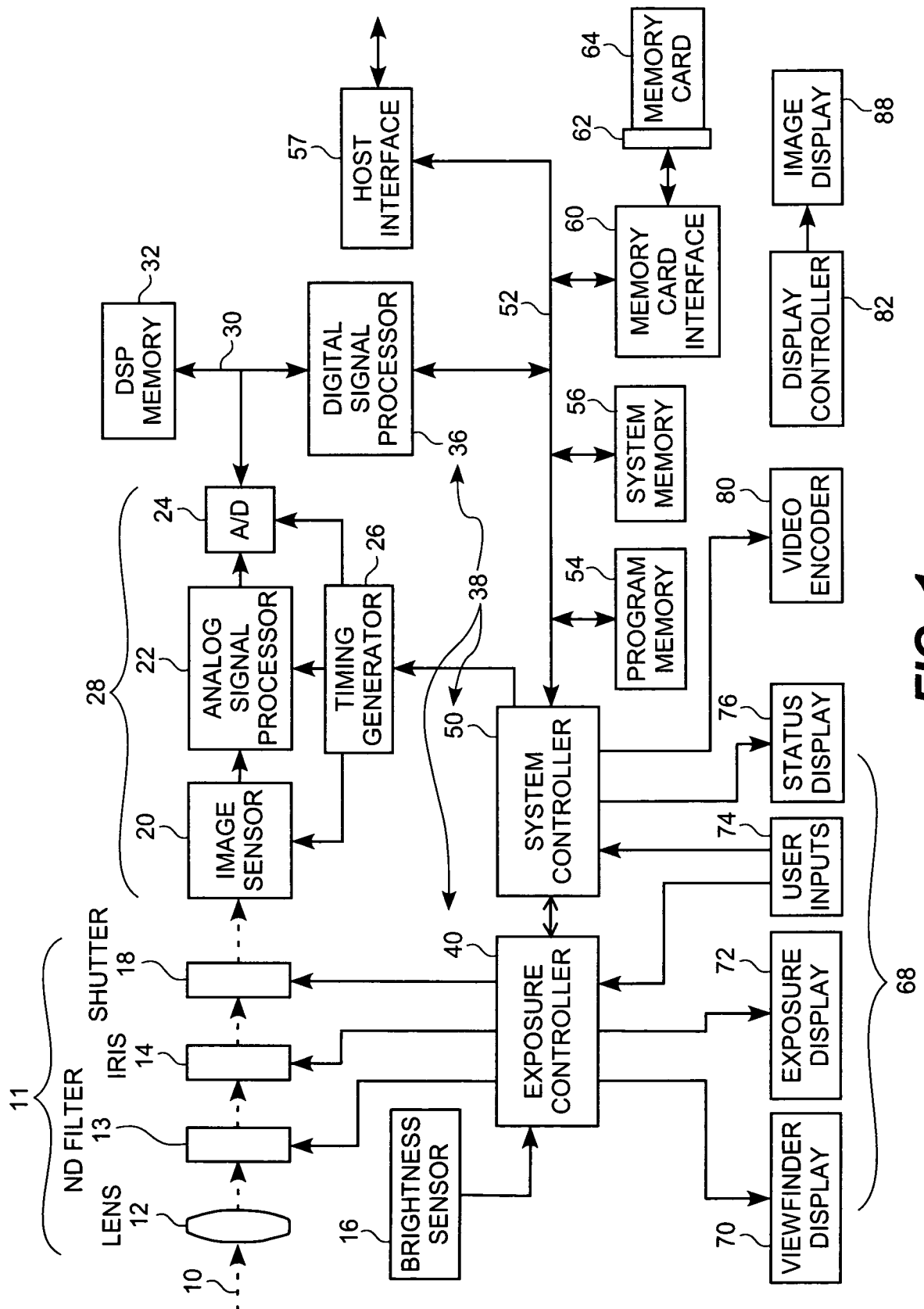
13. An image sensing method, comprising:
collecting a charge in response to received light;
transferring the charge among a plurality of charge storage elements to one or more floating diffusions on a sensor wafer; and
10 sensing the charge using support circuitry on a circuit wafer electrically connected to the sensing wafer.

14. The method of claim 13, wherein the charge storage elements are arranged in an array of rows and columns and the charge storage elements are
15 grouped into subsets within each row with a respective floating diffusion associated with each subset, and wherein transferring the charge among the plurality of charge storage elements includes transferring the charge in either a first or second direction within the rows.

20 15. The method of claim 13 or claim 14, wherein sensing the charge using support circuitry includes sensing the charge on the one or more floating diffusions on the sensing wafer using respective floating diffusions on the circuit wafer.

25

1/3

**FIG. 1**

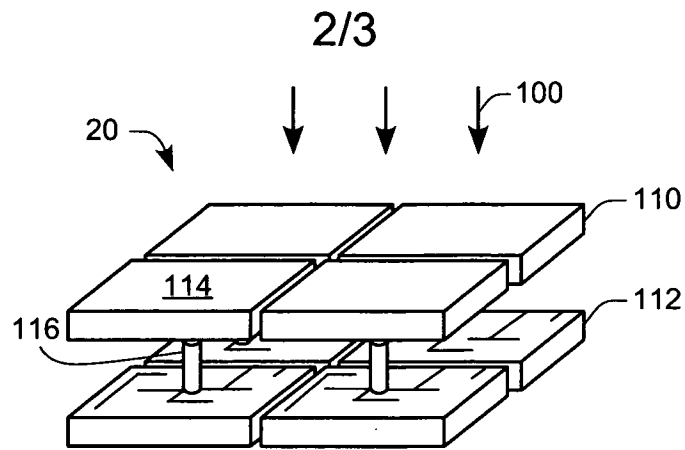


FIG. 2

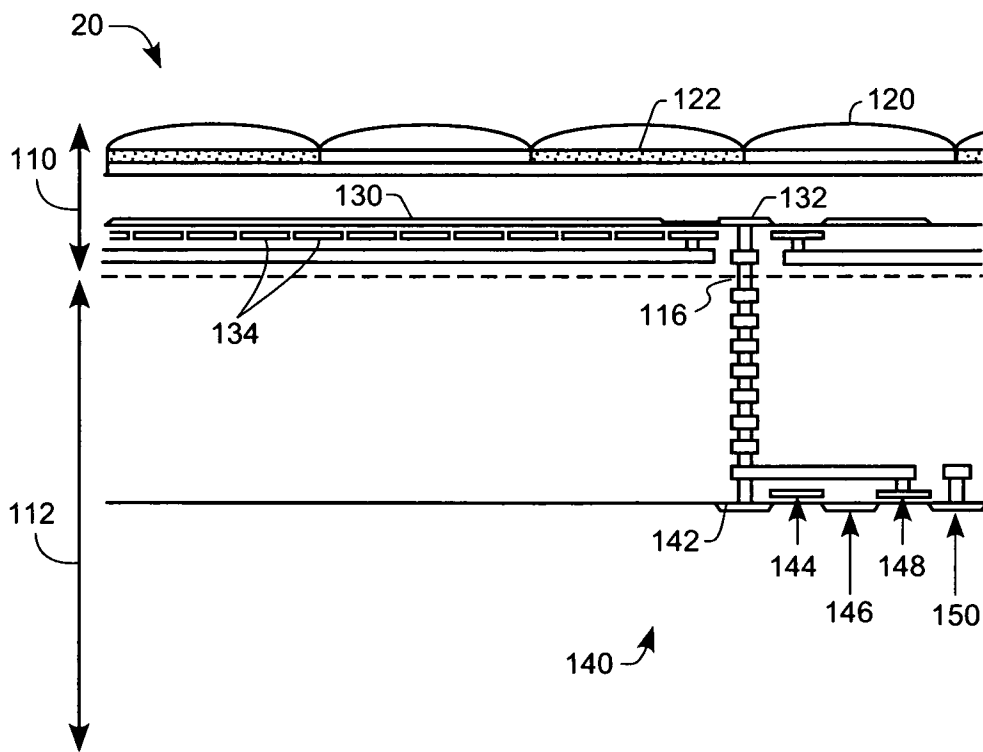


FIG. 3

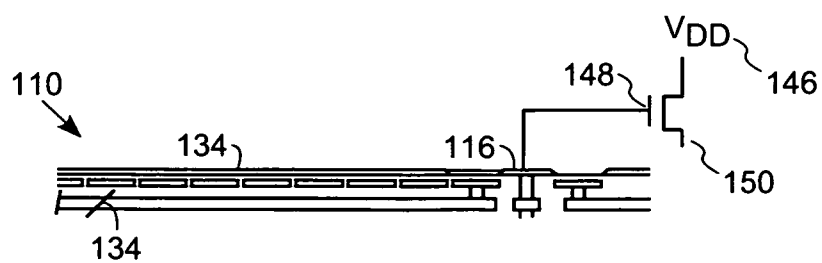
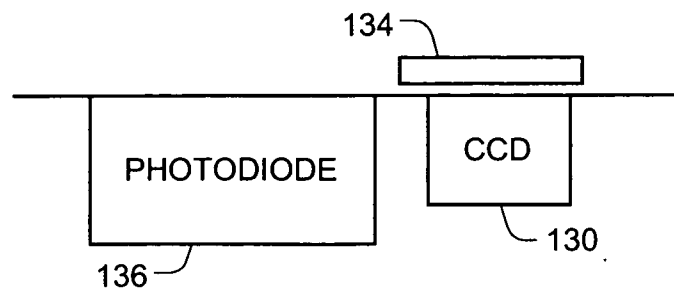
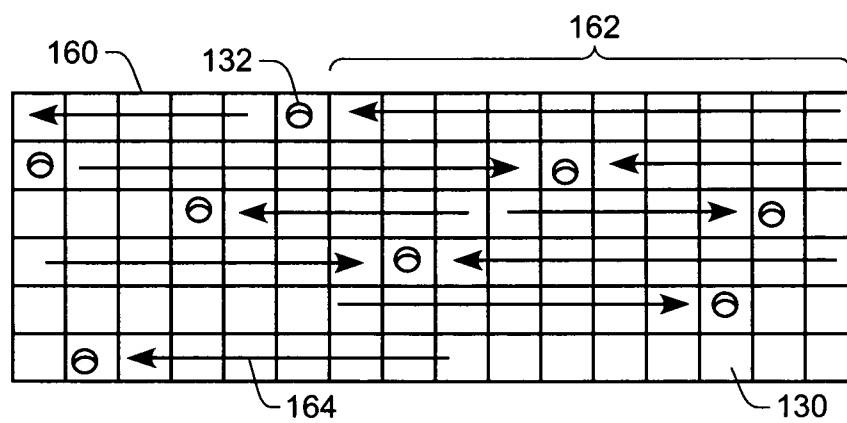
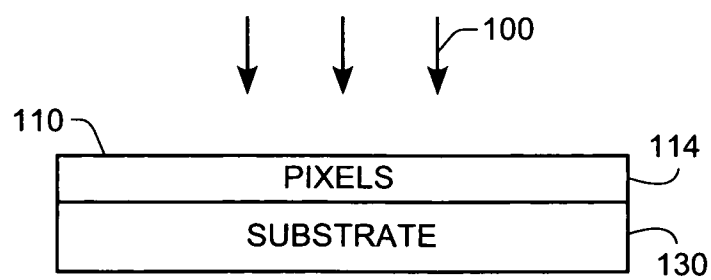


FIG. 3A

3/3

**FIG. 4****FIG. 5****FIG. 6**

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/006401

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/146

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 2009/230287 A1 (ANDERSON TODD J [US] ET AL) 17 September 2009 (2009-09-17) paragraphs [0021], [0035] - [0048]; figures 1-4	1-15
X,P	US 2009/242950 A1 (MCCARTEN JOHN P [US] ET AL) 1 October 2009 (2009-10-01) paragraphs [0022] - [0030]; figures 2-4	1-3, 6-11, 13-15
X	FR 2 888 989 A1 (ST MICROELECTRONICS SA [FR]) 26 January 2007 (2007-01-26) page 9, line 9 - page 16, line 13; figures 1-5	1-15
X	WO 2007/105478 A1 (KOYANAGI MITSUMASA [JP]) 20 September 2007 (2007-09-20) the whole document	1-15
	-/--	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

5 March 2010

Date of mailing of the international search report

17/03/2010

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Ley, Marc

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/006401

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/083939 A1 (GUIDASH ROBERT M [US]) 10 April 2008 (2008-04-10) paragraphs [0029] - [0061]; figures 1-7 -----	1-15
X	WO 2006/109937 A1 (SILICONFILE TECHNOLOGIES INC [KR]; LEE DO YOUNG [KR]) 19 October 2006 (2006-10-19) paragraphs [0025] - [0063]; figure 11 -----	1-15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2009/006401

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009230287 A1	17-09-2009	W0 2009117046 A1	24-09-2009
US 2009242950 A1	01-10-2009	W0 2009123693 A1	08-10-2009
FR 2888989 A1	26-01-2007	US 2007018075 A1	25-01-2007
W0 2007105478 A1	20-09-2007	JP 2007228460 A	06-09-2007
US 2008083939 A1	10-04-2008	EP 2067171 A2	10-06-2009
		KR 20090077904 A	16-07-2009
		W0 2008045356 A2	17-04-2008
W0 2006109937 A1	19-10-2006	CN 101151730 A	26-03-2008
		EP 1869706 A1	26-12-2007
		JP 2008536330 T	04-09-2008
		KR 20060108378 A	18-10-2006
		US 2008251823 A1	16-10-2008