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(54) Title: BIFACIAL SOLAR CELLS WITH OVERLAID BACK GRID SURFACE

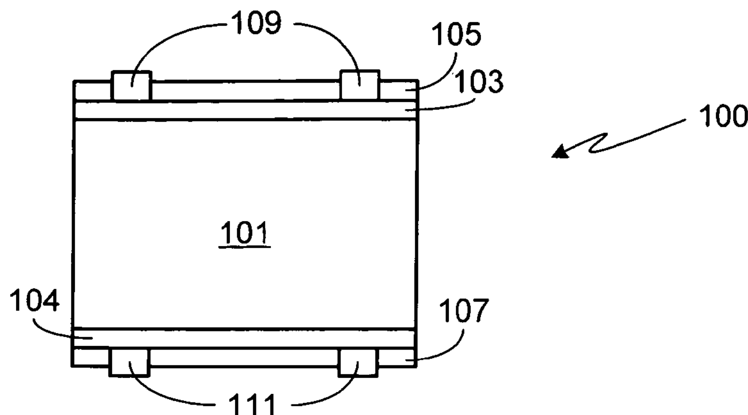

FIG. 1

(57) Abstract: A simplified manufacturing process and the resultant bifacial solar cell (BSC) are provided, the simplified manufacturing process reducing manufacturing costs. The BSC includes an active region (103) located on the front surface of the substrate (101), formed for example by a phosphorous diffusion step. After removing the PSG, assuming phosphorous diffusion, and isolating the front junction, dielectric layers (105/107) are deposited on the front and back surfaces. Contact grids (109/111) are formed, for example by screen printing. Prior to depositing the back surface dielectric, a metal grid may be applied to the back surface, the back surface contact grid registered to, and alloyed to, the metal grid during contact firing.

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BIFACIAL SOLAR CELLS WITH OVERLAID BACK GRID SURFACE

FIELD OF THE INVENTION

[001] The present invention relates generally to solar cells and, in particular, to an improved structure and manufacturing process for a bifacial solar cell.

BACKGROUND OF THE INVENTION

[002] Bifacial solar cells (BSC) may use any of a variety of different designs to achieve higher efficiencies than those typically obtained by a conventional, monofacial solar cell. One such design is shown in U.S. Patent No. 5,665,175 which discloses a BSC configuration with first and second active regions formed on the front and back surfaces of the BSC, respectively, the two regions separated by a distance λ. The distance λ allows a leakage current to flow between the first and second active regions, thus allowing a solar cell panel utilizing such bifacial cells to continue to operate even if one or more individual solar cells become shaded or defective.

[003] U.S. Patent No. 7,495,167 discloses an n^+pp^+ structure and a method of producing the same. In the disclosed structure, the p^+ layer, formed by boron diffusion, exhibits a lifetime close to that of the initial level of the substrate. In order to achieve this lifetime, the '167 patent teaches that after phosphorous gettering, the cell must be annealed at a temperature of 600° C or less for one hour or more. In order to retain the lifetime recovered by the phosphorous and low-temperature born gettering steps, the cell then undergoes a final heat treatment step in which the cell is fired at a temperature of around 700° C or less for one minute or less.

[004] U.S. Patent Application Publication No. 2005/0056312 discloses an alternative technique for achieving two or more p-n junctions in a single solar cell, the disclosed technique using transparent substrates (e.g., glass or quartz substrates). In one disclosed embodiment, the BSC includes two thin-film polycrystalline or amorphous cells formed on opposing sides of a transparent substrate. Due to the design of the cell, the high temperature deposition of the absorber layers can be completed before the low temperature deposition of the window layers, thus avoiding degradation or destruction of the p-n junctions.

[005] Although there are a variety of BSC designs and techniques for fabricating the same, these designs and techniques tend to be relatively complex, and thus expensive. Accordingly, what is needed is a solar cell design that achieves the benefits associated

with bifacial solar cells while retaining the manufacturing simplicity of a monofacial solar cell. The present invention provides such a design.

SUMMARY OF THE INVENTION

[006] The present invention provides a simplified manufacturing process and the resultant bifacial solar cell (BSC), the simplified manufacturing process reducing manufacturing costs. In at least one embodiment of the invention, the manufacturing method is comprised of the steps of simultaneously diffusing phosphorous onto the front surface of a silicon substrate to form an n^+ layer and a front surface junction and onto the back surface of the silicon substrate to form an n^+ layer and a back surface junction, removing the phosphor-silicate glass formed during the diffusion step (e.g., by etching with HF), depositing passivation and AR dielectric layers on the front and back surfaces, applying front and back surface contact grids, and firing the front and back surface contact grids. The front and back surface contact grid firing steps may be performed simultaneously. Alternately, the back surface contact grid applying and firing steps may be performed prior to, or after, the front surface contact grid applying and firing steps. The method may further include the step of firing the back surface contact grid through the back junction, leaving a floating junction. The method may further include the step of removing the back surface junction and isolating the front surface junction, this step performed prior to depositing the back surface dielectric. A back surface metal grid may be applied, for example by screen printing or deposition using a shadow mask, after removing the back surface junction and prior to depositing the dielectric layer on the back surface.

[007] In at least one embodiment of the invention, the manufacturing method is comprised of the steps of depositing a dielectric layer on the back surface of a silicon substrate, diffusing phosphorous onto the front surface of the substrate to form an n^+ layer and a front surface junction, removing the phosphor-silicate glass formed during the diffusion step (e.g., by etching with HF), isolating the front surface junction using a laser scriber, depositing a front surface passivation and AR dielectric layer, applying front and back surface contact grids, firing the front and back surface contact grids, and isolating the front surface junction, for example using a laser scriber. The front and back surface contact grid firing steps may be performed simultaneously. Alternately, the back surface contact grid applying and firing steps may be performed prior to, or after, the front surface contact grid applying and firing steps.

[008] In at least one embodiment of the invention, a bifacial solar cell (BSC) is provided that is comprised of a silicon substrate with a front surface active region of a first conductivity type, dielectric layers deposited on the front surface active region and on the back surface of the silicon substrate, a front surface contact grid applied to the front surface dielectric, and a back surface contact grid applied to the back surface dielectric, where the front surface contact grid alloys through the front surface dielectric to the active region during firing, and where the back surface contact grid alloys through the back surface dielectric to the back surface of the silicon substrate during firing. The silicon substrate may be comprised of p-type silicon, the active region may be comprised of n^+ material resulting from a phosphorous diffusion step, and the dielectric layers may be comprised of silicon nitride, silicon oxide and/or silicon oxynitride. The BSC may further comprise a floating back surface junction of the first conductivity type. The BSC may further comprise a metal grid pattern deposited directly on the back surface of the silicon substrate, where the back surface screen printed contact grid fires through the back surface dielectric and makes electrical contact with the metal grid pattern during firing. The BSC may further comprise a groove on the front surface of the silicon substrate, the groove isolating the front surface junction.

[009] A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Fig. 1 illustrates a preferred embodiment of a BSC in accordance with the invention;

[0011] Fig. 2 illustrates the process flow for the BSC of Fig. 1;

[0012] Fig. 3 illustrates an alternate process flow for the BSC of Fig. 1;

[0013] Fig. 4 illustrates an alternate embodiment of a BSC in accordance with the invention;

[0014] Fig. 5 illustrates the process flow for the BSC of Fig. 4;

[0015] Fig. 6 illustrates an alternate process flow for the BSC of Fig. 4;

[0016] Fig. 7 illustrates an alternate embodiment of a BSC in accordance with the invention; and

[0017] Fig. 8 illustrates the process flow for the BSC of Fig. 7.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

[0018] Fig. 1 illustrates a cross-sectional view of a preferred bifacial solar cell (BSC) structure fabricated in accordance with the procedure described in Fig. 2. Silicon substrate 101 may be of either p- or n-type. In the illustrated device and process of Figs. 1 and 2, a p-type substrate is used.

[0019] Initially, substrate 101 is prepared using any of a variety of well-known substrate preparatory processes (step 201). In general, during step 201 saw and handling induced damage is removed via an etching process, for example using a nitric and hydrofluoric (HF) acid mixture. After substrate preparation, phosphorous is diffused onto the front surface of substrate 101, creating n^+ layer 103 and a p-n junction at the interface of substrate 101 and n^+ layer 103. During this step, phosphorous is also diffused onto the back surface of substrate 101, creating n^+ layer 104 and a floating junction. Preferably n^+ layer 103 is formed using phosphoryl chloride ($POCl_3$) with a diffusion temperature in the range of 825° C to 890° C, preferably at a temperature of approximately 850° C, for 10 to 20 minutes in a nitrogen atmosphere (step 203). The phosphor-silicate glass (PSG) formed during diffusion step 203 is then etched away, preferably using an HF etch at or near room temperature for 1 to 5 minutes (step 205). In the preferred embodiment, the front and back surface junctions have a depth of 0.3 to 0.6 microns and a surface doping concentration of about $8 \times 10^{21}/cm^3$.

[0020] In step 207, a front surface passivation and anti-reflection (AR) dielectric layer 105 is deposited as well as a back surface passivation and AR dielectric layer 107, each layer preferably being approximately 76 nanometers thick. In the exemplary embodiment, layers 105 and 107 are comprised of silicon nitride with an index of refraction of 2.07. In an alternate embodiment, layers 105 and 107 are comprised of silicon oxynitride. In another alternate embodiment, layers 105 and 107 are comprised of a stack of two layers of different composition, for example 10 nanometers of silicon dioxide and 70 nanometers of silicon nitride. Layers 105 and 107 are preferably deposited at a temperature of 300° C to 400° C.

[0021] After deposition of the dielectric layers, contact grids are applied to the front and back surfaces of BSC 100 (step 209), for example using a screen printing process. In the exemplary embodiment, front contact grid 109 is comprised of silver while back contact grid 111 is comprised of aluminum. In the preferred embodiment, both the front and back contact grids are aligned and use the same contact size and

spacing, with electrodes being approximately 100 microns wide, 15 microns thick and spaced approximately 2.5 millimeters apart. In at least one alternate embodiment, the back contact grid uses a finer spacing in order to lessen resistance losses from lateral current flow in the substrate. Lastly, a contact firing step 211 is performed, preferably at a peak temperature of 750° C for 3 seconds in air. As a result of this process, contacts 109 alloy through passivation and AR dielectric coating 105 to n^+ layer 103. Contacts 111 alloy through passivation and AR dielectric coating 107 and back diffused layer 104 to form contact to substrate 101. As aluminum is a p-type dopant, a diode forms between back diffused layer 104 and contact 111 so that current does not flow from the back diffused layer into the contact and the back diffusion is floating. This isolates the back surface from the bulk 101 since there is zero current into a floating junction.

[0022] Fig. 3 illustrates an alternate process for fabricating cell 100. As illustrated, in this process the front surface and back surface contact grids are applied and fired separately, thereby allowing different firing conditions to be used for each grid. Preferably contact grid 111 is applied (step 301) and fired (step 303) first, followed by the application of contact grid 109 (step 305) and firing of the front contact grid (step 307).

[0023] Figs. 4 and 5 illustrate an alternate embodiment in which the floating junction on the back surface of the substrate is removed. In structure 400, after formation of the front junction and PSG etching, the back surface of substrate 101 is etched (step 501), thereby removing the back surface junction and providing isolation for the front junction. In a preferred embodiment, step 501 uses an isotropic wet silicon etch such as a mixture of nitric acid and HF acid. After removal of the back surface floating junction, the process continues as previously described relative to either Figs. 2 and 3. Preferably in this embodiment the back surface contact grid is comprised of an aluminum-silver mixture.

[0024] Fig. 6 illustrates an alternate process for fabricating cell 400. In this process, after preparation of substrate 101 (step 201), dielectric layer 107 is applied to the back surface of substrate 101 (step 601). As previously described, preferably dielectric layer 107 is comprised of silicon nitride or silicon oxynitride. Applying dielectric layer 107 prior to diffusing the front surface n^+ layer 103 (step 203) prevents the formation of a back surface junction. After the front surface diffusion (step 203) and the PSG etch (step 205), the front surface passivation and AR dielectric layer 105 is deposited (step 603), followed by application (step 209) and firing (step 211) of the contact grids. Lastly, the

front junction is isolated (step 605), for example using a laser scriber to form a groove on the front cell surface around the periphery of the cell. This embodiment can also separate the screen printing and firing of the front and back surface contact grids as described relative to Fig. 3.

[0025] Figs. 7 and 8 illustrate a variation of BFC 400. As shown in the BFC cross-sectional view of BFC 700, a metal grid 701 is applied directly onto the back surface of cell 101 (step 801), thereby reducing contact resistance. Step 801 is preferably performed after the back surface of substrate 101 has been etched to remove the back surface junction and isolate the front junction (step 501). Step 801 is performed using either a deposition process with a shadow mask, or using a screen printing process. Preferably, metal grid 701 is comprised of aluminum. After depositing dielectric layers 105 and 107 (step 207), contact grids 109 and 111 are applied and fired, either together as shown in Fig. 6 and described relative to Fig. 2, or separately as described relative to Fig. 3. Regardless of whether the contact formation process follows that shown in Fig. 2 or Fig. 3, it will be understood that back surface contact grid 111 is registered to metal grid 501. During the firing step, contact grid 111 alloys to metal grid 501.

[0026] As will be understood by those familiar with the art, the present invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. Accordingly, the disclosures and descriptions herein are intended to be illustrative, but not limiting, of the scope of the invention.

WHAT IS CLAIMED IS:

1. A method of fabricating a bifacial solar cell, the method comprising the steps of:

diffusing phosphorous onto a front surface of a silicon substrate to form a front surface junction and onto a back surface of said silicon to form a back surface junction;

removing a phosphor-silicate glass (PSG) formed during said phosphorous diffusing step;

depositing a front surface passivation and anti-reflection (AR) dielectric layer onto said n^+ layer and a back surface passivation and AR dielectric layer onto said back surface of said silicon substrate;

applying a back surface contact grid;

applying a front surface contact grid;

firing said back surface contact grid; and

firing said front surface contact grid.

2. The method of claim 1, wherein said step of applying said back surface contact grid further comprises the step of screen printing said back surface contact grid, and wherein said step of applying said front surface contact grid further comprises the step of screen printing said front surface contact grid.

3. The method of claim 1, wherein said step of firing said back surface contact grid further comprises the step of firing said back surface grid through said back surface passivation and AR dielectric layer and through said back surface junction to form a floating back surface junction.

4. The method of claim 1, further comprising the steps of removing said back surface junction and isolating said front surface junction.

5. The method of claim 4, wherein said back surface junction removing step further comprises the step of etching said back surface.

6. The method of claim 4, further comprising the step of applying a back surface metal grid onto said back surface of said silicon substrate, wherein said back

surface metal grid applying step is performed after said back surface junction removing step and before said back surface passivation and AR dielectric layer depositing step, and wherein the method of claim 1 further comprises the step of aligning said back surface contact grid with said back surface metal grid.

7. The method of claim 6, wherein said back surface metal grid applying step further comprises the step of depositing said back surface metal grid through a shadow mask onto said back surface of said silicon substrate.

8. The method of claim 6, wherein said back surface metal grid applying step further comprises the step of screen printing said back surface metal grid onto said back surface of said silicon substrate.

9. The method of claim 6, wherein said step of firing said back surface contact grid is performed prior to said step of applying said front surface contact grid.

10. The method of claim 1, wherein said steps of firing said back and front surface contact grids are performed simultaneously.

11. The method of claim 1, wherein said step of firing said back surface contact grid is performed prior to said step of applying said front surface contact grid.

12. The method of claim 1, wherein said PSG removing step further comprises the step of etching said front surface with a hydrofluoric acid etch.

13. A method of fabricating a bifacial solar cell, the method comprising the steps of:

depositing a dielectric layer onto a back surface of a silicon substrate;

diffusing phosphorous onto a front surface of said silicon substrate to form an n^+ layer and a front surface junction;

removing a phosphor-silicate glass (PSG) formed during said phosphorous diffusing step;

depositing a front surface passivation and anti-reflection (AR) dielectric layer onto said n^+ layer;

applying a back surface contact grid;
applying a front surface contact grid;
firing said back surface contact grid;
firing said front surface contact grid; and
isolating said front surface junction.

14. The method of claim 13, wherein said step of applying said back surface contact grid further comprises the step of screen printing said back surface contact grid, and wherein said step of applying said front surface contact grid further comprises the step of screen printing said front surface contact grid.

15. The method of claim 13, wherein said step of isolating said front surface junction is performed using a laser scriber.

16. The method of claim 13, wherein said steps of firing said back and front surface contact grids are performed simultaneously.

17. The method of claim 13, wherein said step of firing said back surface contact grid is performed prior to said step of applying said front surface contact grid.

18. The method of claim 13, wherein said PSG removing step further comprises the step of etching said front surface with a hydrofluoric etch.

19. A bifacial solar cell, comprising:

a silicon substrate with a front surface and a back surface;

an active region of a first conductivity type located on at least a portion of said front surface of said silicon substrate;

a first dielectric layer deposited on said active region;

a second dielectric layer deposited on said back surface of said silicon substrate;

a first contact grid applied to said first dielectric layer, said first contact grid comprised of a first metal, wherein after a firing step said first contact grid is alloyed through said first dielectric layer to said active region; and

a second contact grid applied to said second dielectric layer, said second contact grid comprised of a second metal, wherein after said firing step said second

contact grid is alloyed through said second dielectric layer to said back surface of said silicon substrate.

20. The bifacial solar cell of claim 19, further comprising a floating junction of said first conductivity type located on at least a portion of said back surface of said silicon substrate.

21. The bifacial solar cell of claim 19, wherein said silicon substrate is comprised of a p-type silicon, said active region is comprised of n^+ material resulting from a phosphorous diffusion step, and said first and second dielectric layers are selected from the group consisting of silicon nitride, silicon oxide and silicon oxynitride.

22. The bifacial solar cell of claim 19, further comprising a grid pattern of a third metal deposited directly on said back surface of said silicon substrate and interposed between said back surface of said silicon substrate and said second dielectric layer, wherein said second screen printed contact grid is registered to said grid pattern, and wherein after said firing step said second screen printed contact grid is alloyed through said second dielectric layer to said grid pattern of said third metal.

23. The bifacial solar cell of claim 19, further comprising a groove on said front surface of said silicon substrate, said groove isolating a front junction formed by said active region and said silicon substrate.

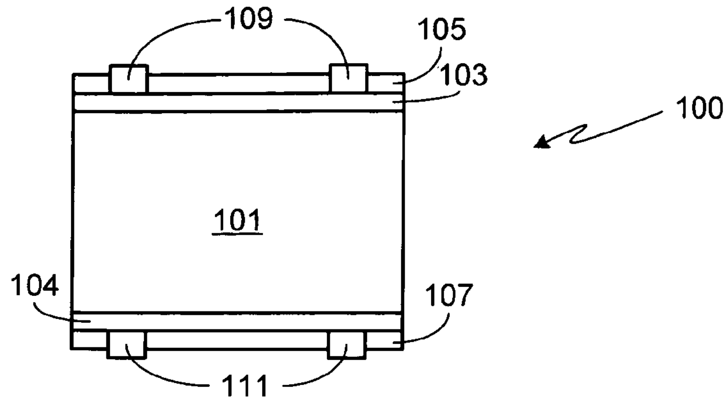

FIG. 1

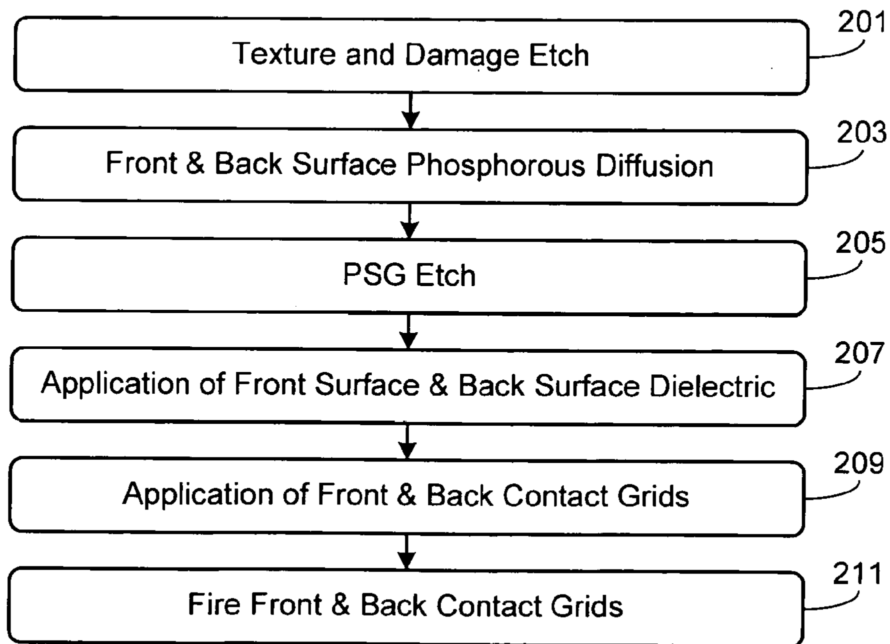

FIG. 2

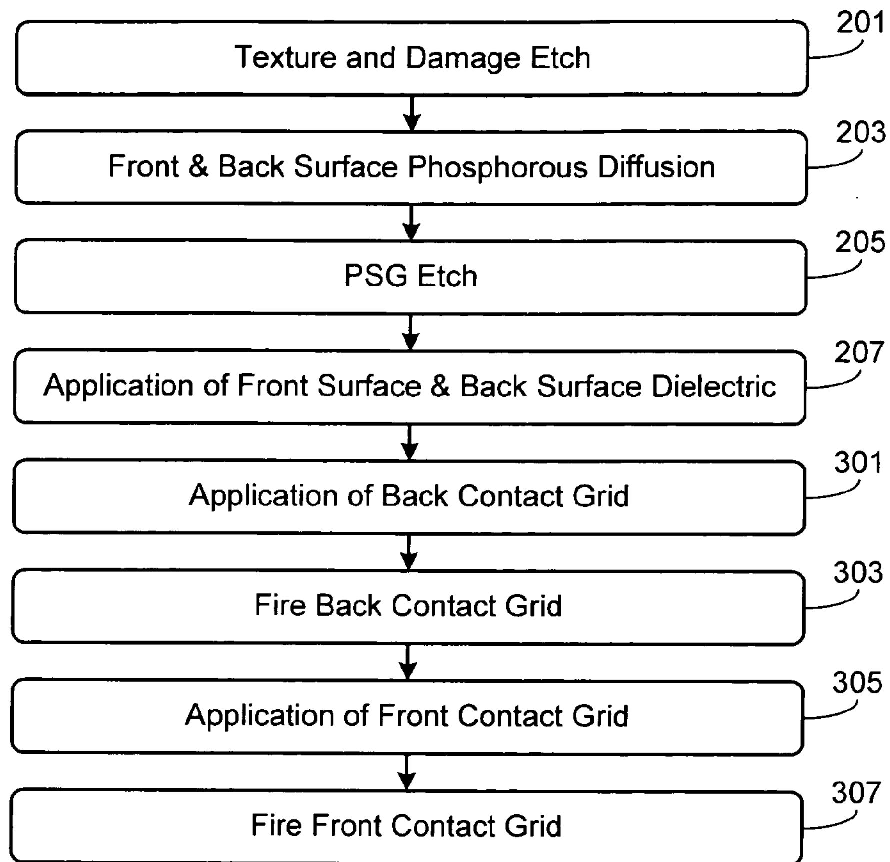

FIG. 3

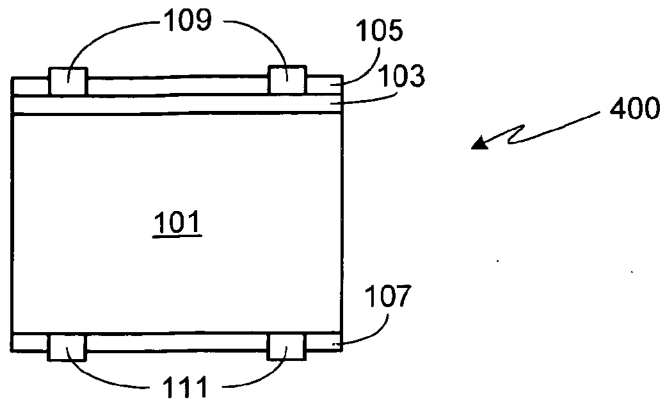

FIG. 4

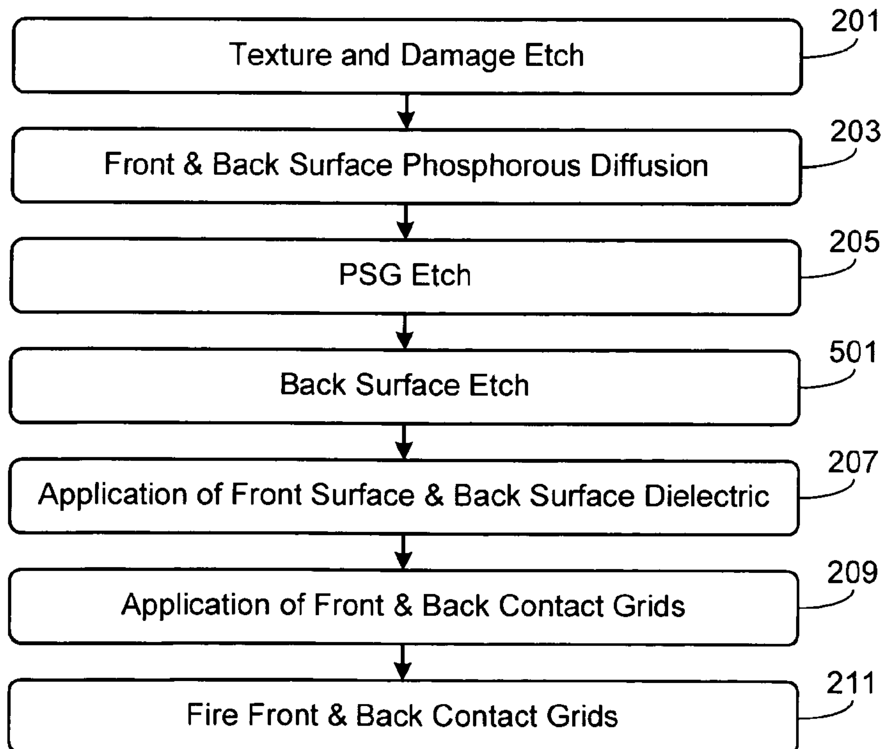

FIG. 5

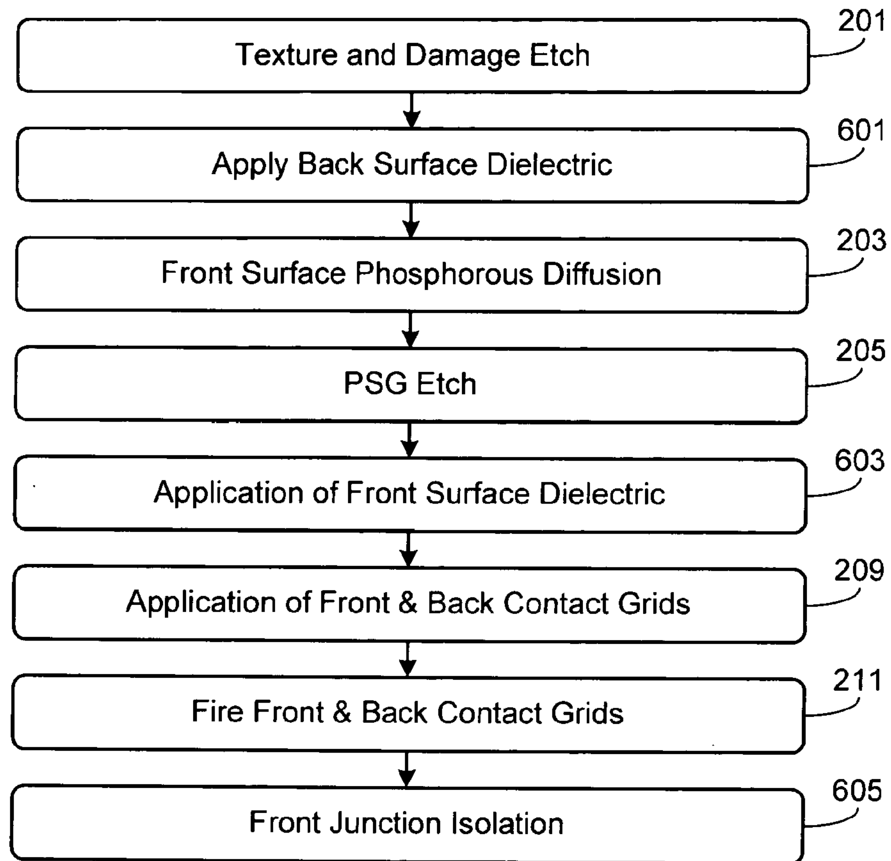

FIG. 6

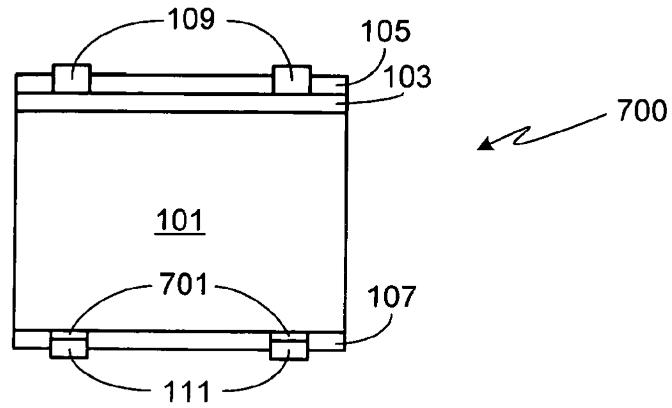

FIG. 7

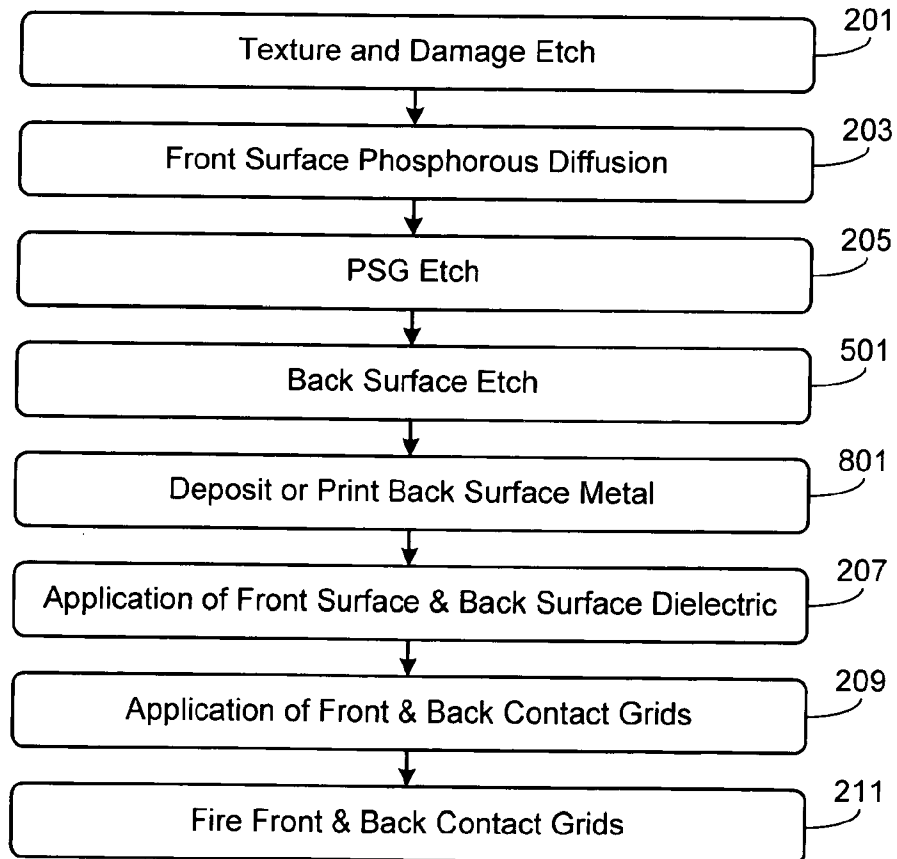

FIG. 8