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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors; and

(71) Applicants: **MAJHI, Prashant** [IN/US]; 1754 Indigo Oak Lane, San Jose, California 95121 (US). **DOYLE, Brian S.** [IE/US]; 11156 NW Montreux Lane, Portland, Oregon 97229 (US). **SHARMA, Abhishek A.** [IN/US]; 1091 NE Orenco Station Parkway E317, Hillsboro, Oregon 97124 (US). **KARPOV, Elijah V.** [US/US]; 3964 NW Brookview Way, Portland, Oregon 97229 (US). **OGUZ, Kaan** [TR/US]; 210 NW 209th Avenue, Beaverton, Oregon 97006 (US). **O'BRIEN, Kevin P.** [US/US]; 1846 SE 36th Avenue, Portland, Oregon 97214 (US). **AHMED, Khaled** [US/US]; 2366 W Broadway, Anaheim, California 92804 (US).

(74) Agent: **BRASK, Justin, K.** et al.; Schwabe, Williamson & Wyatt, 1211 SW 5th Ave., Suite 1900, Portland, OR 97204 (US).

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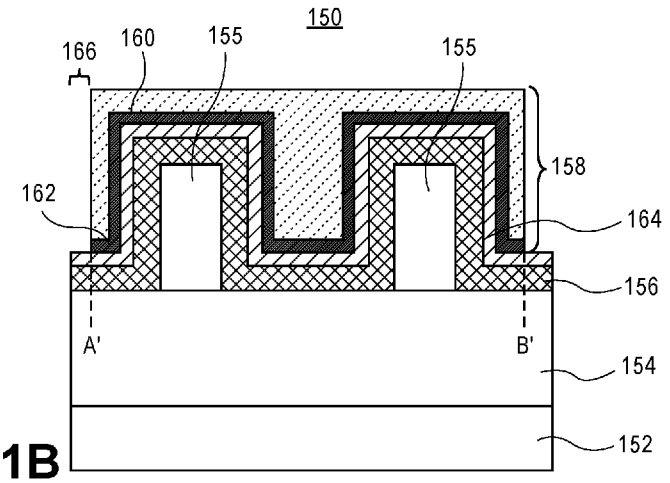


FIG. 1B

(57) Abstract: Thin film transistors having relatively increased width are described. In an example, an integrated circuit structure includes an insulator structure above a substrate. The insulator structure has a topography that varies along a plane parallel with a global plane of the substrate. A semiconducting oxide material is on the insulator structure. The semiconducting oxide material is conformal with the topography of the insulator structure. A gate electrode is over a first portion of the semiconducting oxide material on the insulator structure. The gate electrode has a first side opposite a second side. A first conductive contact is adjacent the first side of the gate electrode. A second conductive contact is adjacent the second side of the gate electrode.

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THIN FILM TRANSISTORS HAVING RELATIVELY INCREASED WIDTH

TECHNICAL FIELD

Embodiments of the disclosure are in the field of integrated circuit structures and, in particular, thin film transistors having relatively increased width.

BACKGROUND

For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips.

For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant. In the manufacture of integrated circuit devices, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. In conventional processes, tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and compatibility with the existing high-yielding bulk silicon substrate infrastructure. Scaling multi-gate transistors has not been without consequence, however. As the dimensions of these fundamental building blocks of microelectronic circuitry are reduced and as the sheer number of fundamental building blocks fabricated in a given region is increased, the constraints on the semiconductor processes used to fabricate these building blocks have become overwhelming.

The performance of a thin-film transistor (TFT) may depend on a number of factors. For example, the efficiency at which a TFT is able to operate may depend on the sub threshold swing of the TFT, characterizing the amount of change in the gate-source voltage needed to achieve a given change in the drain current. A smaller sub threshold swing enables the TFT to turn off to a lower leakage value when the gate-source voltage drops below the threshold voltage of the TFT. The conventional theoretical lower limit at room temperature for the sub threshold swing of the TFT is 60 millivolts per decade of change in the drain current.

Variability in conventional and state-of-the-art fabrication processes may limit the possibility to further extend them into the, e.g. 10 nm or sub-10 nm range. Consequently, fabrication of the functional components needed for future technology nodes may require the introduction of new methodologies or the integration of new technologies in current fabrication

processes or in place of current fabrication processes.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A illustrates a cross-sectional view taken along a gate "width" of a conventional thin film integrated circuit structure.

Figure 1B illustrates a cross-sectional view taken along a gate "width" of a thin film integrated circuit structure having relatively increased width, in accordance with an embodiment of the present disclosure.

Figures 1C, 1D, and 1E illustrate angled and direct cross-sectional views of a thin film integrated circuit structure having relatively increased width, in accordance with an embodiment of the present disclosure.

Figure 2A illustrates an angled three-dimensional view of another thin film integrated circuit structure having relatively increased width, in accordance with another embodiment of the present disclosure.

Figure 2B illustrates a top-down view of a portion of the thin film integrated circuit structure of Figure 2A, in accordance with another embodiment of the present disclosure.

Figure 3 illustrates an angled three-dimensional view of another thin film integrated circuit structure having relatively increased width, in accordance with another embodiment of the present disclosure.

Figures 4A-4H illustrate cross-sectional and plan views of various stages in a method of fabricating a thin film integrated circuit structure having relatively increased width, in accordance with an embodiment of the present disclosure.

Figures 5A and 5B are top views of a wafer and dies that include one or more thin film transistors having relatively increased width, in accordance with one or more of the embodiments disclosed herein.

Figure 6 is a cross-sectional side view of an integrated circuit (IC) device that may include one or more thin film transistors having relatively increased width, in accordance with one or more of the embodiments disclosed herein.

Figure 7 is a cross-sectional side view of an integrated circuit (IC) device assembly that may include one or more thin film transistors having relatively increased width, in accordance with one or more of the embodiments disclosed herein.

Figure 8 illustrates a computing device in accordance with one implementation of an embodiment of the disclosure.

DESCRIPTION OF THE EMBODIMENTS

Thin film transistors having relatively increased width are described. In the following description, numerous specific details are set forth, such as specific material and tooling regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as single or dual damascene processing, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale. In some cases, various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as "upper", "lower", "above", "below," "bottom," and "top" refer to directions in the drawings to which reference is made. Terms such as "front", "back", "rear", and "side" describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

Embodiments described herein may be directed to front-end-of-line (FEOL) semiconductor processing and structures. FEOL is the first portion of integrated circuit (IC) fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are patterned in the semiconductor substrate or layer. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers. Following the last FEOL operation, the result is typically a wafer with isolated transistors (e.g., without any wires).

Embodiments described herein may be directed to back end of line (BEOL) semiconductor processing and structures. BEOL is the second portion of IC fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are interconnected with wiring on the wafer, e.g., the metallization layer or layers. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections. In the BEOL part of the fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed. For modern IC processes, more than 10 metal layers may be added in the BEOL.

Embodiments described below may be applicable to FEOL processing and structures,

BEOL processing and structures, or both FEOL and BEOL processing and structures. In particular, although an exemplary processing scheme may be illustrated using a FEOL processing scenario, such approaches may also be applicable to BEOL processing. Likewise, although an exemplary processing scheme may be illustrated using a BEOL processing scenario, such approaches may also be applicable to FEOL processing.

One or more embodiments described herein are directed to structures and architectures for fabricating BEOL thin film transistors (TFTs) having relatively increased width relative to TFTs of conventional geometry. Embodiments may include or pertain to one or more of back end transistors, IGZO, semiconducting oxide materials, thin film transistors, and system-on-chip (SoC) technologies. One or more embodiments may be implemented to realize high performance backend transistors to potentially increase monolithic integration of backend logic plus memory in SoCs of future technology nodes.

To provide context, there is increased need for advanced SoCs to include monolithically integrated BEOL transistors for logic functionality at higher metal layers. Such BEOL transistors typically have a lower thermal budget than front end transistors due to increased thermal sensitivity of backend materials. Also, the performance of such transistors may be severely hampered due to low channel mobility for BEOL-compatible channel materials such as IGZO (indium gallium zinc oxide).

In accordance with one or more embodiments described herein, non-planar BEOL-compatible thin film transistors (TFTs) are fabricated by effectively increasing the transistor width (and hence the drive strength and performance) for a given projected area. A TFT fabricated using such an architecture may exhibit an increase in gate control, stability, and performance of thin film transistors. Applications of such systems may include, but are not limited to, back end (BEOL) logic, memory, or analog applications. Embodiments described herein may include non-planar structures that effectively increase transistor width (relative to a planar device) by integrating the devices in unique architectures.

To provide a benchmark, Figure 1A illustrates a cross-sectional view taken along a gate "width" of a conventional thin film integrated circuit structure.

Referring to Figure 1A, a planar TFT 100 is formed above a substrate 102, e.g., on an insulating layer 104 above a substrate, as is shown. The planar TFT 100 includes a channel material 106, such as a semiconducting oxide material. A gate electrode 108 is formed on a gate dielectric layer 114 formed on the channel material 106. The gate electrode 108 may include a fill material 110 on a workfunction layer 112, as is depicted. The gate electrode 108 may expose regions 116 of the channel material 106 and the gate dielectric layer 114, as is depicted. Alternatively, the channel material 106 and the gate dielectric layer 114 have a same lateral

dimension as the gate electrode 108. It is to be appreciated that source/drain regions are into and out of the page of the view of Figure 1A.

The planar TFT 100 has an effective gate width that is the length of the planar channel material 106 between locations A and B, as depicted in Figure 1A. The TFT 100 may be referred to herein as a planar BEOL field effect transistor (FET).

As a first example of a structure having relative increase in transistor width (e.g., relative to the structure of Figure 1A), Figure 1B illustrates a cross-sectional view taken along a gate "width" of a thin film integrated circuit structure having relatively increased width, in accordance with an embodiment of the present disclosure.

Referring to Figure 1B, a non-planar TFT 150 is formed above a substrate 152, e.g., on an insulating layer 154 above a substrate, as is shown. A pair of dielectric fins 155 is on the insulating layer 154. The non-planar TFT 150 includes a semiconducting oxide material 156, or similarly suitable channel material. The semiconducting oxide material 156 is conformal with the pair of dielectric fins 155 and with exposed portions of the insulating layer 154 between the pair of dielectric fins 155. A gate electrode 158 is formed on a gate dielectric layer 164 formed on the semiconducting oxide material 156. The gate electrode 158 may include a fill material 160 on a workfunction layer 162, as is depicted. The gate electrode 158 may expose regions 166 of the semiconducting oxide material 156 and the gate dielectric layer 164, as is depicted. Alternatively, the semiconducting oxide material 156 and the gate dielectric layer 164 have a same lateral dimension as the gate electrode 158. It is to be appreciated that source/drain regions are into and out of the page of the view of Figure 1B.

The non-planar TFT 150 has an effective gate width that is the length of the conformal semiconducting oxide material 156 between locations A' and B', i.e., the full length including undulating portions over the tops and sidewalls of the dielectric fins 155, as is depicted in Figure 1B. The TFT 150 may be referred to herein as a non-planar BEOL field effect transistor (FET). In comparison to Figure 1A, the structure of Figure 1B highlights the advantage of a non-planar architecture to increase effective gate width, referred to herein as a relatively increased width.

To highlight other aspects of a non-planar TFT topography, Figures 1C, 1D, and 1E illustrate angled and direct cross-sectional views of a thin film integrated circuit structure having relatively increased width, in accordance with an embodiment of the present disclosure. It is to be appreciated that one dielectric fin is illustrated in Figures 1C-1E for simplification. Embodiments may include a single device fabricated over one (Figure 1C), two (Figure 1B) or more such dielectric fins.

Referring to Figures 1C-1E, an integrated circuit structure 170 includes a dielectric fin 155 on an insulator layer 154 above a substrate 152. The dielectric fin 155 has a top and

sidewalls. A semiconducting oxide material 156, or similarly suitable channel material, is on the top and sidewalls of the dielectric fin 155. A gate electrode 158 is over a first portion of the semiconducting oxide material 156 on the top and sidewalls of the dielectric fin 155. The gate electrode 158 has a first side opposite a second side. A first conductive contact (left 174) is adjacent the first side of the gate electrode 158, over a second portion of the semiconducting oxide material 156 on the top and sidewalls of the dielectric fin 155. A second conductive contact (right 174) is adjacent the second side of the gate electrode 158, over a third portion of the semiconducting oxide material 156 on the top and sidewalls of the dielectric fin 155.

In an embodiment, the integrated circuit structure 170 further includes a gate dielectric layer 164 between the gate electrode 158 and the first portion of the semiconducting oxide material 156 on the top and sidewalls of the dielectric fin 155, as is depicted in Figures 1C-1E. In an embodiment, the integrated circuit structure 170 further includes a first dielectric spacer (left 172) between the first conductive contact 174 and the first side of the gate electrode 158, the first dielectric spacer 172 over a fourth portion of the semiconducting oxide material 156 on the top and sidewalls of the dielectric fin 155. A second dielectric spacer (right 172) is between the second conductive contact 174 and the second side of the gate electrode 158, the second dielectric spacer 172 over a fifth portion of the second semiconducting oxide material 156 on the top and sidewalls of the dielectric fin 155, as is depicted in Figures 1C and 1E. In one such embodiment, the gate dielectric layer 164 is further along the first and second dielectric spacers 172, as is also depicted in Figures 1C and 1E.

Referring collectively to Figures 1B-1E, in accordance with an embodiment of the present invention, an integrated circuit structure 150 or 170 includes an insulator structure 155 above a substrate 152. The insulator structure 155 has a topography that varies along a plane (ab) parallel with a global plane of the substrate 152. A semiconducting oxide material 156 is on the insulator structure 155. The semiconducting oxide material 156 is conformal with the topography of the insulator structure 155. A gate electrode 158 is over a first portion of the semiconducting oxide material 156 on the insulator structure 155. The gate electrode 158 has a first side opposite a second side. A first conductive contact (left 174) is adjacent the first side of the gate electrode 158. The first conductive contact 174 is over a second portion of the semiconducting oxide material 156 on the insulator structure 155. A second conductive contact (right 174) is adjacent the second side of the gate electrode 158. The second conductive contact 174 is over a third portion of the semiconducting oxide material 156 on the insulator structure 155.

In an embodiment, the insulator structure 150 or 170 includes one or more fins 155. Individual ones of the fins 155 have a top and sidewalls. The semiconducting oxide material 156 is on the top and sidewalls of the individual ones of the fins 155. In an embodiment, the

insulator structure 155 (such as fin or fins 155) is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride. In an embodiment, the insulator structure 155 is composed of a low-k dielectric material.

In an embodiment, dielectric fins described herein may be fabricated as a grating structure, where the term "grating" is used herein to refer to a tight pitch grating structure. In one such embodiment, the tight pitch is not achievable directly through conventional lithography. For example, a pattern based on conventional lithography may first be formed, but the pitch may be halved by the use of spacer mask patterning, as is known in the art. Even further, the original pitch may be quartered by a second round of spacer mask patterning. Accordingly, the grating-like patterns described herein may have dielectric fins spaced at a constant pitch and having a constant width. The pattern may be fabricated by a pitch halving or pitch quartering, or other pitch division, approach. In an embodiment, the dielectric fin or fins 155 each have squared-off (as shown) or rounder corners.

In an embodiment, a gate dielectric layer 164 is between the gate electrode 158 and the first portion of the semiconducting oxide material 156 on the insulator structure 155, as is depicted. In one such embodiment, the gate dielectric layer 164 includes a layer of a high-k dielectric material directly on the semiconducting oxide material 156.

In an embodiment, a first dielectric spacer (first 172) is between the first conductive contact (first 174) and the first side of the gate electrode 158, the first dielectric spacer (first 172) over a fourth portion of the semiconducting oxide material 156 on the insulator structure 155. A second dielectric spacer (second 172) is between the second conductive contact (second 174) and the second side of the gate electrode 158, the second dielectric spacer (second 172) over a fifth portion of the semiconducting oxide material 156 on the insulator structure 155. In one such embodiment, a gate dielectric layer 164 is between the gate electrode 158 and the first portion of the semiconducting oxide material 156 on the insulator structure 155. The gate dielectric layer 164 is further along the first dielectric spacer (first 172) and the second dielectric spacer (second 172). In a specific such embodiment, the gate dielectric layer 164 includes a layer of a high-k dielectric material directly on the semiconducting oxide material 156.

In an embodiment, the semiconducting oxide material 156 includes indium gallium zinc oxide (IGZO). In an embodiment, the semiconducting oxide material 156 includes a material selected from the group consisting of tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide and tungsten oxide. In an embodiment, the gate dielectric layer 164 includes a layer of a high-k dielectric material directly on the semiconducting oxide material 156. In an alternative embodiment, the channel material is not a semiconducting oxide material but is rather a layer of

polycrystalline silicon.

As a second example of a structure having relative increase in transistor width, Figure 2A illustrates an angled three-dimensional view of another thin film integrated circuit structure having relatively increased width, in accordance with another embodiment of the present disclosure. Figure 2B illustrates a top-down view of a portion of the thin film integrated circuit structure of Figure 2A.

Referring to Figures 2A and 2B, an integrated circuit structure 200 includes an insulator structure 250 above a substrate 202. The insulator structure 250 may be formed on an insulator layer 204, as is depicted. The insulator structure 250 has a first trench 252 therein, the first trench 252 having sidewalls and a bottom. A semiconducting oxide material 206, or similarly suitable channel material, is in the first trench 252 in the insulator structure 250. The semiconducting oxide material 206 is conformal with the sidewalls and bottom of the first trench 252. A gate dielectric layer 214 is on the semiconducting oxide material 206 in the first trench 252. The gate dielectric layer 214 is conformal with the semiconducting oxide material 206 conformal with the sidewalls and bottom of the first trench 252. A gate electrode 208 is on the gate dielectric layer 214 in the first trench 252. The gate electrode 208 has a first side opposite a second side and has an exposed top surface. A first conductive contact (left 254) is laterally adjacent the first side of the gate electrode 208. The first conductive contact (left 254) is on a first portion of the semiconducting oxide material 206 conformal with the sidewalls of the first trench 252. A second conductive contact (right 254) is laterally adjacent the second side of the gate electrode 208. The second conductive contact (right 254) is on a second portion of the semiconducting oxide material 206 conformal with the sidewalls of the first trench 252. It is to be appreciated that the conductive contacts 254 are shown only at the front portion of trench 252 for clarity of the drawing. In an embodiment, the conductive contacts 254 extend all the way, or substantially all the way along the trench 252 for maximized source/drain contact area and maintain a relatively small effective gate length.

In an embodiment, the insulator structure 250 is a single layer of ILD material, as is depicted. In another embodiment, the insulator structure 250 is a stack of alternating dielectric layers, such as described in association with Figures 4A-4H.

In an embodiment, a third conductive contact 258 is over and in contact with the exposed top surface of the gate electrode 208, as is depicted. In an embodiment, the first conductive contact (left 254) is in a second trench 270 in the insulator structure 250, and the third conductive contact (right 254) is in a third trench 272 in the insulator structure 250, as is depicted. In an embodiment, the third conductive contact 258 is coupled to a conductive line 260, which may be a word line, as is depicted. In an embodiment, the first and second conductive contacts 254 are

coupled corresponding conductive lines 256, as is depicted.

Referring again to Figure 2, in an embodiment, a non-planar back-end FET architecture uses the vertical length (depth) of the trench 252 to increase effective width of the transistor. That is, the depth of the trench 252 is the Z of the TFT, where the effective width (Weff) is relatively increased by setting Z to the depth of the trench.

In an embodiment, the semiconducting oxide material 206 includes indium gallium zinc oxide (IGZO). In an embodiment, the semiconducting oxide material 206 includes a material selected from the group consisting of tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide and tungsten oxide. In an embodiment, the gate dielectric layer 214 includes a layer of a high-k dielectric material directly on the semiconducting oxide material 206. In an alternative embodiment, the channel material is not a semiconducting oxide material but is rather a layer of polycrystalline silicon.

As a third example of a structure having relative increase in transistor width, Figure 3 illustrates an angled three-dimensional view of another thin film integrated circuit structure having relatively increased width, in accordance with another embodiment of the present disclosure.

Referring to Figure 3, an integrated circuit structure 300 includes an insulator structure 350 above a substrate 302. The insulator structure 350 may be formed on an insulator layer 304, as is depicted. The insulator structure 350 has a first trench 352 therein, the first trench 352 having sidewalls and a bottom. The insulator structure 350 has a topography that varies along a plane normal with a global plane of the substrate 302. In one such embodiment, the insulator structure 350 has a corrugated topography that varies along a plane normal with a global plane of the substrate 302, as is depicted. In a specific such embodiment, the corrugated topography is within a single layer of ILD material, as is depicted. In another specific such embodiment, the corrugated topography is within an arrangement of alternating dielectric layers, such as described in association with Figures 4A-4H.

A semiconducting oxide material 306, or similarly suitable channel material, is in the first trench 352 in the insulator structure 350. The semiconducting oxide material 306 is conformal with the sidewalls and bottom of the first trench 352, i.e., conformal with the topography of the insulator structure 350. A gate dielectric layer 314 is on the semiconducting oxide material 306 in the first trench 352. The gate dielectric layer 314 is conformal with the semiconducting oxide material 306 conformal with the sidewalls and bottom of the first trench 352. A gate electrode 308 is on the gate dielectric layer 314 in the first trench 352. The gate electrode 308 has a first side opposite a second side and has an exposed top surface. A first conductive contact (left 354)

is laterally adjacent the first side of the gate electrode 308. The first conductive contact (left 354) is on a first portion of the semiconducting oxide material 306 conformal with the sidewalls of the first trench 352. A second conductive contact (right 354) is laterally adjacent the second side of the gate electrode 308. The second conductive contact (right 354) is on a second portion of the semiconducting oxide material 306 conformal with the sidewalls of the first trench 352. In an embodiment, the conductive contacts 354 extend all the way, or substantially all the way along the trench 352 for maximized source/drain contact area and maintain a relatively small effective gate length.

In an embodiment, a third conductive contact 358 is over and in contact with the exposed top surface of the gate electrode 308, as is depicted. In an embodiment, the first conductive contact (left 354) is in a second trench 370 in the insulator structure 350, and the third conductive contact (right 354) is in a third trench 372 in the insulator structure 350, as is depicted. In an embodiment, the third conductive contact 358 is coupled to a conductive line 360, which may be a word line, as is depicted. In an embodiment, the first and second conductive contacts 354 are coupled corresponding conductive lines 356, as is depicted.

Referring again to Figure 3, in an embodiment, a non-planar back-end FET architecture uses the vertical length (depth) of the trench 352, including the additional length provided by the corrugation, to increase effective width of the transistor. That is, the length of the corrugated trench 352 is the Z of the TFT, where the effective width (Weff) is relatively increased by setting Z to the depth or length along the corrugated trench 352.

In an embodiment, the semiconducting oxide material 306 includes indium gallium zinc oxide (IGZO). In an embodiment, the semiconducting oxide material 306 includes a material selected from the group consisting of tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide and tungsten oxide. In an embodiment, the gate dielectric layer 314 includes a layer of a high-k dielectric material directly on the semiconducting oxide material 306. In an alternative embodiment, the channel material is not a semiconducting oxide material but is rather a layer of polycrystalline silicon.

In accordance with an embodiment of the present disclosure, the above TFT non-planar architectures 150, 170, 200 and 300 provide for higher effective widths for a transistor for a scaled projected area. In an embodiment, the drive strength and performance of such transistors are improved over state-of-the-art planar BEOL transistors.

As an exemplary processing scheme, Figures 4A-4H illustrate cross-sectional and plan views of various stages in a method of fabricating a thin film integrated circuit structure having relatively increased width, in accordance with an embodiment of the present disclosure.

Referring to Figure 4A, a stack 404 of dielectric layers is formed above a substrate 400 and, possibly, on an insulating layer 402 formed on or above the substrate 400. The stack 404 of dielectric layers includes alternating dielectric layers 404A and 404B of differing composition. In one embodiment, the stack 404 of dielectric layers is a stack of alternating silicon dioxide and silicon nitride layers.

Referring to Figure 4B, openings 406 are formed in the stack 404 of dielectric layers to form a once-patterned stack 404' of dielectric layers. In one embodiment, the structure of Figure 4B is used without the process described below in association with Figure 4C in order to arrive at a structure such as TFT 200.

Referring to Figure 4C, corrugation is achieved to form corrugated openings 408 by exposing the structure of Figure 4B to an etch process that recesses layers 404B selective to layers 404A. The selective etching process provides twice-patterned stack 404'' of dielectric layers. The twice-patterned stack 404'' of dielectric layers may be used in order to arrive at a structure such as TFT 300.

Referring to Figure 4D, conductive contacts 410, such as source/drain contacts, are formed in the openings 408 of the structure of Figure 4C. Conductive contacts may be formed, e.g., by a deposition or growth process.

Referring to Figure 4E, an opening 412 is formed between the conductive contacts 410 to form thrice-patterned stack 404''' of dielectric layers. The opening 412 exposes a corrugated surface of the conductive contacts 410.

Referring to Figure 4F, a semiconducting oxide layer 306, or other suitable channel material, is formed in opening 412 along the exposed surfaces of the conductive contacts 410. In an embodiment, the semiconducting oxide layer 306 is formed conformal with the corrugated surface of the conductive contacts 410, as is depicted.

Referring to Figure 4G, a gate dielectric layer 314 is formed in opening 412. The gate dielectric layer is on and conformal with the semiconducting oxide layer 306.

Referring to Figure 4H, a gate electrode 308 is formed within opening 412. The gate electrode is on and conformal with the gate dielectric layer 314. The structure of Figure 4G may be included as a portion of the TFT 300 described in association with Figure 3.

It is to be appreciated that the layers and materials described in association with embodiments herein are typically formed on or above an underlying semiconductor substrate 152, 202, 302 or 400, e.g., as FEOL layer(s). In other embodiments, the layers and materials described in association with embodiments herein are typically formed on or above underlying device layer(s) of an integrated circuit, e.g., as BEOL layer(s) above an underlying semiconductor substrate 152, 202, 302 or 400. In an embodiment, an underlying semiconductor

substrate represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. Furthermore, although not depicted, structures described herein may be fabricated on underlying lower level back end of line (BEOL) interconnect layers.

In the case that an insulator layer 154, 204, 304 or 402 is optionally used, the insulator layer 154, 204, 304 or 402 may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, portions of a gate structure from an underlying bulk substrate or interconnect layer. For example, in one embodiment, the insulator layer 154, 204, 304 or 402 is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride. In a particular embodiment, the insulator layer 154, 204, 304 or 402 is a low-k dielectric layer of an underlying BEOL layer.

In an embodiment, the semiconducting oxide material 156, 206 or 306 and, hence, channel material of a TFT includes an IGZO layer that has a gallium to indium ratio of 1:1, a gallium to indium ratio greater than 1 (e.g., 2:1, 3:1, 4:1, 5:1, 6:1, 7:1, 8:1, 9:1, or 10:1), or a gallium to indium ratio less than 1 (e.g., 1:2, 1:3, 1:4, 1:5, 1:6, 1:7, 1:8, 1:9, or 1:10). A low indium content IGZO may refer to IGZO having more gallium than indium (e.g., with a gallium to indium ratio greater than 1:1), and may also be referred to as high gallium content IGZO. Similarly, low gallium content IGZO may refer to IGZO having more indium than gallium (e.g., with a gallium to indium ratio less than 1:1), and may also be referred to as high indium content IGZO. In another embodiment, the semiconducting oxide material 156, 206 or 306 is or includes a material such as tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide, or tungsten oxide. In an alternative embodiment, polycrystalline silicon is used as the channel material instead of a semiconducting oxide material. In an embodiment, no matter the composition, the channel material has a thickness between 5 nanometers and 30 nanometers

In an embodiment, the semiconducting oxide material 156, 206 or 306 is an amorphous, crystalline, or semi crystalline oxide semiconductor, such as an amorphous, crystalline, or semi crystalline oxide semiconductor IGZO layer. The semiconducting oxide material 156, 206 or 306 may be formed using a low-temperature deposition process, such as physical vapor deposition (PVD) (e.g., sputtering), atomic layer deposition (ALD), or chemical vapor deposition

(CVD). The ability to deposit the semiconducting oxide material 156, 206 or 306 at temperatures low enough to be compatible with back-end manufacturing processes represents a particular advantage. The semiconducting oxide material 156, 206 or 306 may be deposited on sidewalls or conformably on any desired structure to a precise thickness, allowing the manufacture of transistors having any desired geometry.

In an embodiment, gate electrode 158, 208 or 308 includes at least one P-type work function metal or N-type work function metal, depending on whether the integrated circuit device 150, 170, 200 or 300 is to be included in a P-type transistor or an N-type transistor. For a P-type transistors, metals that may be used for the gate electrode 158, 208 or 308 may include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides (e.g., ruthenium oxide). For an N-type transistor, metals that may be used for the gate electrode 158, 208 or 308 include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals (e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide). In some embodiments, the gate electrode includes a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as to act as a barrier layer. In some implementations, the gate electrode 158, 208 or 308 may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

In an embodiment, gate dielectric layer 164, 214 or 314 is composed of a high-K material. For example, in one embodiment, the gate dielectric layer 164, 214 or 314 is composed of a material such as, but not limited to, hafnium oxide, hafnium oxy-nitride, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, or a combination thereof. In some implementations, the gate dielectric 164, 214 or 314 may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate, as is depicted in Figures 1C and

1E.

In some embodiments, the semiconducting oxide material 156, 206 or 306 is in contact with the gate dielectric layer 164, 214 or 314, respectively, an arrangement which may put an IGZO layer in contact with a high-k metal oxide layer. In other embodiments, an intermediate material is disposed between the semiconducting oxide material 156, 206 or 306 and the gate dielectric layer 164, 214 or 314. In some embodiments, an IGZO layer includes multiple regions of IGZO having different material properties. For example, an IGZO layer may include low indium content IGZO close to (e.g., in contact with) a high-k gate dielectric layer, and a high indium content IGZO close to (e.g., in contact with) the higher mobility semiconducting oxide channel material. High indium content IGZO may provide higher mobility and poorer interface properties relative to low indium content IGZO, while low indium content IGZO may provide a wider band gap, lower gate leakage, and better interface properties, although a lower mobility, relative to high indium content IGZO.

In an embodiment, dielectric spacers 172 are formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In some embodiments, a plurality of spacer pairs may be used. For example, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate electrode 172.

In an embodiment, conductive contacts 174, 254 or 354 act as contacts to source/drain regions of a TFT, or act directly as source/drain regions of the TFT. The conductive contacts 174, 254, 258 or 354 may be spaced apart by a distance that is the gate length of the transistor 150, 170, 200 or 300. In an embodiment, conductive contacts 258 or 358 directly contact a gate electrode. In some embodiments, the gate length is between 7 and 30 nanometers. In an embodiment, the conductive contacts 174, 254, 258, 354 or 358 include one or more layers of metal and/or metal alloys. In a particular embodiment, the conductive contacts 174, 254, 258, 354 or 358 are composed of aluminum or an aluminum-containing alloy.

In an embodiment, interconnect lines (and, possibly, underlying via structures), such as interconnect lines 256, 260, 356 or 360, described herein are composed of one or more metal or metal-containing conductive structures. The conductive interconnect lines are also sometimes referred to in the art as traces, wires, lines, metal, interconnect lines or simply interconnects. In a particular embodiment, each of the interconnect lines includes a barrier layer and a conductive fill material. In an embodiment, the barrier layer is composed of a metal nitride material, such as tantalum nitride or titanium nitride. In an embodiment, the conductive fill material is composed of a conductive material such as, but not limited to, Cu, Al, Ti, Zr, Hf, V, Ru, Co, Ni, Pd, Pt, W,

Ag, Au or alloys thereof.

Interconnect lines described herein may be fabricated as a grating structure, where the term "grating" is used herein to refer to a tight pitch grating structure. In one such embodiment, the tight pitch is not achievable directly through conventional lithography. For example, a pattern based on conventional lithography may first be formed, but the pitch may be halved by the use of spacer mask patterning, as is known in the art. Even further, the original pitch may be quartered by a second round of spacer mask patterning. Accordingly, the grating-like patterns described herein may have conductive lines spaced at a constant pitch and having a constant width. The pattern may be fabricated by a pitch halving or pitch quartering, or other pitch division, approach.

In an embodiment, ILD materials described herein, such as ILD materials 250 or 350, are composed of or include a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO_2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

In one aspect, a gate electrode and gate dielectric layer, e.g., gate electrode 158, 208 or 308 and gate dielectric layer 164, 214 or 314 may be fabricated by a replacement gate process. In such a scheme, dummy gate material such as polysilicon or silicon nitride pillar material, may be removed and replaced with permanent gate electrode material. In one such embodiment, a permanent gate dielectric layer is also formed in this process, as opposed to being carried through from earlier processing. In an embodiment, dummy gates are removed by a dry etch or wet etch process. In one embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a dry etch process including use of SF_6. In another embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a wet etch process including use of aqueous NH_4OH or tetramethylammonium hydroxide. In one embodiment, dummy gates are composed of silicon nitride and are removed with a wet etch including aqueous phosphoric acid.

In an embodiment, one or more approaches described herein contemplate essentially a dummy and replacement gate process in combination with a dummy and replacement contact process to arrive at structures described herein. In one such embodiment, the replacement contact process is performed after the replacement gate process to allow high temperature anneal of at least a portion of the permanent gate stack. For example, in a specific such embodiment, an anneal of at least a portion of the permanent gate structures, e.g., after a gate dielectric layer is

formed. The anneal is performed prior to formation of the permanent contacts.

It is to be appreciated that not all aspects of the processes described above need be practiced to fall within the spirit and scope of embodiments of the present disclosure. For example, in one embodiment, dummy gates need not ever be formed prior to fabricating gate contacts over active portions of the gate stacks. The gate stacks described above may actually be permanent gate stacks as initially formed. Also, the processes described herein may be used to fabricate one or a plurality of semiconductor devices. One or more embodiments may be particularly useful for fabricating semiconductor devices at a 10 nanometer (10 nm) or smaller technology node.

In an embodiment, as is also used throughout the present description, lithographic operations are performed using 193nm immersion lithography (i193), extreme ultra-violet (EUV) and/or electron beam direct write (EBDW) lithography, or the like. A positive tone or a negative tone resist may be used. In one embodiment, a lithographic mask is a trilayer mask composed of a topographic masking portion, an anti-reflective coating (ARC) layer, and a photoresist layer. In a particular such embodiment, the topographic masking portion is a carbon hardmask (CHM) layer and the anti-reflective coating layer is a silicon ARC layer.

In another aspect, the performance of a thin film transistor (TFT) may depend on the carrier mobility of the components in the TFT. For example, a material with a higher carrier mobility enables carriers to move more quickly in response to a given electric field than a material with a lower carrier mobility. Accordingly, high carrier mobilities may be associated with improved performance. Although shown and described above as single semiconducting oxide layers, in accordance with embodiments described herein, a layer of a semiconducting oxide, such as a layer of IGZO, is between a high-k gate dielectric material and a higher mobility semiconducting oxide channel material. Although IGZO has a relatively low mobility (approximately 10 cm^2/V-s), the sub threshold swing of IGZO may be close to the conventional theoretical lower limit. In some embodiments, a thin layer of IGZO may directly border a channel material of choice, and may be sandwiched between the channel material and the high-k dielectric. The use of IGZO at the interface between the gate stack and the channel may achieve one or more of a number of advantages. For example, an IGZO interface may have a relatively small number of interface traps, defects at which carriers are trapped and released that impede performance. A TFT that includes an IGZO layer as a second semiconducting oxide material may exhibit desirably low gate leakage. When IGZO is used as an interface to a non-IGZO semiconducting oxide channel material (e.g., a thin film oxide semiconductor material having a higher mobility than IGZO), the benefits of the higher mobility channel material may be realized simultaneously with the good gate oxide interface properties provided by the IGZO. In

accordance with one or more embodiments described herein, a gate-channel arrangement based on a dual semiconducting oxide layer channel enables the use of a wider array of thin film transistor channel materials, while achieving desirable gate control, than realizable using conventional approaches.

In an embodiment, the addition of a second thin film semiconductor around a first TFT material can provide one or more of mobility enhancement, improved short channel effects (SCEs) particularly if all conduction occurs in the second material. The second TFT material may be selected for strong oxygen bond capability in order to stabilize the TFT when exposed to downstream processing. In accordance with one embodiment, a higher mobility semiconducting oxide material is effectively wrapped in a lower mobility material semiconducting oxide that is more oxygen stable. The resulting structure may limit the negative effects of downstream high temperature processing operations or aggressive operations on the inner TFT material by having the highly stable outer material. An increased set of materials that can be chosen to maximize stability and mobility simultaneously may be achieved using such a dual material architecture.

In another aspect, the integrated circuit structures described herein may be included in an electronic device. As a first example of an apparatus that may include one or more of the TFTs disclosed herein, Figures 5A and 5B are top views of a wafer and dies that include one or more thin film transistors having relatively increased width, in accordance with any of the embodiments disclosed herein.

Referring to Figures 5A and 5B, a wafer 500 may be composed of semiconductor material and may include one or more dies 502 having integrated circuit (IC) structures formed on a surface of the wafer 500. Each of the dies 502 may be a repeating unit of a semiconductor product that includes any suitable IC (e.g., ICs including one or more structures such as structures 150, 170, 200 or 300). After the fabrication of the semiconductor product is complete (e.g., after manufacture of structures 150, 170, 200 or 300), the wafer 500 may undergo a singulation process in which each of the dies 502 is separated from one another to provide discrete "chips" of the semiconductor product. In particular, devices that include TFT as disclosed herein may take the form of the wafer 500 (e.g., not singulated) or the form of the die 502 (e.g., singulated). The die 502 may include one or more transistors and/or supporting circuitry to route electrical signals to the transistors, as well as any other IC components. In some embodiments, the wafer 500 or the die 502 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., an AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 502. For example, a memory array formed by multiple memory devices may be formed on a same die 502 as a processing device or other logic that is configured to store

information in the memory devices or execute instructions stored in the memory array.

Figure 6 is a cross-sectional side view of an integrated circuit (IC) device that may include one or more thin film transistors having relatively increased width, in accordance with one or more of the embodiments disclosed herein.

Referring to Figure 6, an IC device 600 is formed on a substrate 602 (e.g., the wafer 500 of Figure 5A) and may be included in a die (e.g., the die 502 of Figure 5B), which may be singulated or included in a wafer. Although a few examples of materials from which the substrate 602 may be formed are described above in association with substrate 152, 202, 302 or 400, any material that may serve as a foundation for an IC device 600 may be used.

The IC device 600 may include one or more device layers, such as device layer 604, disposed on the substrate 602. The device layer 604 may include features of one or more transistors 640 (e.g., TFTs described above) formed on the substrate 602. The device layer 604 may include, for example, one or more source and/or drain (S/D) regions 620, a gate 622 to control current flow in the transistors 640 between the S/D regions 620, and one or more S/D contacts 624 to route electrical signals to/from the S/D regions 620. The transistors 640 may include additional features not depicted for the sake of clarity, such as device isolation regions, gate contacts, and the like. The transistors 640 are not limited to the type and configuration depicted in Figure 6 and may include a wide variety of other types and configurations such as, for example, planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include Fin-based transistors, such as double-gate transistors or tri-gate transistors, and wrap-around or all-around gate transistors, such as nanoribbon and nanowire transistors. In particular, one or more of the transistors 640 take the form of the transistors 150, 170, 200 or 300. Thin-film transistors such as 100 or 300 may be particularly advantageous when used in the metal layers of a microprocessor device for analog circuitry, logic circuitry, or memory circuitry, and may be formed along with existing complementary metal oxide semiconductor (CMOS) processes.

Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or from the transistors 640 of the device layer 604 through one or more interconnect layers disposed on the device layer 604 (illustrated in Figure 6 as interconnect layers 606-610). For example, electrically conductive features of the device layer 604 (e.g., the gate 622 and the S/D contacts 624) may be electrically coupled with the interconnect structures 628 of the interconnect layers 606-610. The one or more interconnect layers 606-610 may form an interlayer dielectric (ILD) stack 619 of the IC device 600.

The interconnect structures 628 may be arranged within the interconnect layers 606-610 to route electrical signals according to a wide variety of designs (in particular, the arrangement is

not limited to the particular configuration of interconnect structures 628 depicted in Figure 6). Although a particular number of interconnect layers 606-610 is depicted in Figure 6, embodiments of the present disclosure include IC devices having more or fewer interconnect layers than depicted.

In some embodiments, the interconnect structures 628 may include trench structures 628a (sometimes referred to as "lines") and/or via structures 628b filled with an electrically conductive material such as a metal. The trench structures 628a may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of the substrate 602 upon which the device layer 604 is formed. For example, the trench structures 628a may route electrical signals in a direction in and out of the page from the perspective of Figure 6. The via structures 628b may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the substrate 602 upon which the device layer 604 is formed. In some embodiments, the via structures 628b may electrically couple trench structures 628a of different interconnect layers 606-610 together.

The interconnect layers 606-610 may include a dielectric material 626 disposed between the interconnect structures 628, as shown in Figure 6. In some embodiments, the dielectric material 626 disposed between the interconnect structures 628 in different ones of the interconnect layers 606-610 may have different compositions; in other embodiments, the composition of the dielectric material 626 between different interconnect layers 606-610 may be the same. In either case, such dielectric materials may be referred to as inter-layer dielectric (ILD) materials.

A first interconnect layer 606 (referred to as Metal 1 or "M1") may be formed directly on the device layer 604. In some embodiments, the first interconnect layer 606 may include trench structures 628a and/or via structures 628b, as shown. The trench structures 628a of the first interconnect layer 606 may be coupled with contacts (e.g., the S/D contacts 624) of the device layer 604.

A second interconnect layer 608 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 606. In some embodiments, the second interconnect layer 608 may include via structures 628b to couple the trench structures 628a of the second interconnect layer 608 with the trench structures 628a of the first interconnect layer 606. Although the trench structures 628a and the via structures 628b are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 608) for the sake of clarity, the trench structures 628a and the via structures 628b may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual-damascene process) in some embodiments.

A third interconnect layer 610 (referred to as Metal 3 or "M3") (and additional

interconnect layers, as desired) may be formed in succession on the second interconnect layer 608 according to similar techniques and configurations described in connection with the second interconnect layer 608 or the first interconnect layer 606.

The IC device 600 may include a solder resist material 634 (e.g., polyimide or similar material) and one or more bond pads 636 formed on the interconnect layers 606-610. The bond pads 636 may be electrically coupled with the interconnect structures 628 and configured to route the electrical signals of the transistor(s) 640 to other external devices. For example, solder bonds may be formed on the one or more bond pads 636 to mechanically and/or electrically couple a chip including the IC device 600 with another component (e.g., a circuit board). The IC device 600 may have other alternative configurations to route the electrical signals from the interconnect layers 606-610 than depicted in other embodiments. For example, the bond pads 636 may be replaced by or may further include other analogous features (e.g., posts) that route the electrical signals to external components.

Figure 7 is a cross-sectional side view of an integrated circuit (IC) device assembly that may include one or more thin film transistors having relatively increased width, in accordance with one or more of the embodiments disclosed herein.

Referring to Figure 7, an IC device assembly 700 includes components having one or more integrated circuit structures described herein. The IC device assembly 700 includes a number of components disposed on a circuit board 702 (which may be, e.g., a motherboard). The IC device assembly 700 includes components disposed on a first face 740 of the circuit board 702 and an opposing second face 742 of the circuit board 702. Generally, components may be disposed on one or both faces 740 and 742. In particular, any suitable ones of the components of the IC device assembly 700 may include a number of the TFT structures 150, 170, 200 or 300 disclosed herein.

In some embodiments, the circuit board 702 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 702. In other embodiments, the circuit board 702 may be a non-PCB substrate.

The IC device assembly 700 illustrated in Figure 7 includes a package-on-interposer structure 736 coupled to the first face 740 of the circuit board 702 by coupling components 716. The coupling components 716 may electrically and mechanically couple the package-on-interposer structure 736 to the circuit board 702, and may include solder balls (as shown in Figure 7), male and female portions of a socket, an adhesive, an underfill material, and/or any

other suitable electrical and/or mechanical coupling structure.

The package-on-interposer structure 736 may include an IC package 720 coupled to an interposer 704 by coupling components 718. The coupling components 718 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 716. Although a single IC package 720 is shown in Figure 7, multiple IC packages may be coupled to the interposer 704. It is to be appreciated that additional interposers may be coupled to the interposer 704. The interposer 704 may provide an intervening substrate used to bridge the circuit board 702 and the IC package 720. The IC package 720 may be or include, for example, a die (the die 502 of Figure 5B), an IC device (e.g., the IC device 600 of Figure 6), or any other suitable component. Generally, the interposer 704 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 704 may couple the IC package 720 (e.g., a die) to a ball grid array (BGA) of the coupling components 716 for coupling to the circuit board 702. In the embodiment illustrated in Figure 7, the IC package 720 and the circuit board 702 are attached to opposing sides of the interposer 704. In other embodiments, the IC package 720 and the circuit board 702 may be attached to a same side of the interposer 704. In some embodiments, three or more components may be interconnected by way of the interposer 704.

The interposer 704 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some implementations, the interposer 704 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 704 may include metal interconnects 708 and vias 710, including but not limited to through-silicon vias (TSVs) 706. The interposer 704 may further include embedded devices 714, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 704. The package-on-interposer structure 736 may take the form of any of the package-on-interposer structures known in the art.

The IC device assembly 700 may include an IC package 724 coupled to the first face 740 of the circuit board 702 by coupling components 722. The coupling components 722 may take the form of any of the embodiments discussed above with reference to the coupling components 716, and the IC package 724 may take the form of any of the embodiments discussed above with reference to the IC package 720.

The IC device assembly 700 illustrated in Figure 7 includes a package-on-package structure 734 coupled to the second face 742 of the circuit board 702 by coupling components 728. The package-on-package structure 734 may include an IC package 726 and an IC package 732 coupled together by coupling components 730 such that the IC package 726 is disposed between the circuit board 702 and the IC package 732. The coupling components 728 and 730 may take the form of any of the embodiments of the coupling components 716 discussed above, and the IC packages 726 and 732 may take the form of any of the embodiments of the IC package 720 discussed above. The package-on-package structure 734 may be configured in accordance with any of the package-on-package structures known in the art.

Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

Figure 8 illustrates a computing device 800 in accordance with one implementation of the disclosure. The computing device 800 houses a board 802. The board 802 may include a number of components, including but not limited to a processor 804 and at least one communication chip 806. The processor 804 is physically and electrically coupled to the board 802. In some implementations the at least one communication chip 806 is also physically and electrically coupled to the board 802. In further implementations, the communication chip 806 is part of the processor 804.

Depending on its applications, computing device 800 may include other components that may or may not be physically and electrically coupled to the board 802. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 806 enables wireless communications for the transfer of data to

and from the computing device 800. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 806 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 800 may include a plurality of communication chips 806. For instance, a first communication chip 806 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 806 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 804 of the computing device 800 includes an integrated circuit die packaged within the processor 804. In some implementations of the disclosure, the integrated circuit die of the processor includes one or more thin film transistors having relatively increased width, in accordance with implementations of embodiments of the disclosure. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 806 also includes an integrated circuit die packaged within the communication chip 806. In accordance with another implementation of embodiments of the disclosure, the integrated circuit die of the communication chip includes one or more thin film transistors having relatively increased width, in accordance with implementations of embodiments of the disclosure.

In further implementations, another component housed within the computing device 800 may contain an integrated circuit die that includes one or more thin film transistors having relatively increased width, in accordance with implementations of embodiments of the disclosure.

In various implementations, the computing device 800 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 800 may be any other electronic

device that processes data.

Thus, embodiments described herein include thin film transistors having relatively increased width.

The above description of illustrated implementations of embodiments of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Example embodiment 1: An integrated circuit structure includes an insulator structure above a substrate. The insulator structure has a topography that varies along a plane parallel with a global plane of the substrate. A semiconducting oxide material is on the insulator structure. The semiconducting oxide material is conformal with the topography of the insulator structure. A gate electrode is over a first portion of the semiconducting oxide material on the insulator structure. The gate electrode has a first side opposite a second side. A first conductive contact is adjacent the first side of the gate electrode. The first conductive contact is over a second portion of the semiconducting oxide material on the insulator structure. A second conductive contact is adjacent the second side of the gate electrode. The second conductive contact is over a third portion of the semiconducting oxide material on the insulator structure.

Example embodiment 2: The integrated circuit structure of example embodiment 1, wherein the insulator structure includes one or more fins. Individual ones of the fins have a top and sidewalls. The semiconducting oxide material is on the top and sidewalls of the individual ones of the fins.

Example embodiment 3: The integrated circuit structure of example embodiment 1 or 2, wherein the semiconducting oxide material includes indium gallium zinc oxide.

Example embodiment 4: The integrated circuit structure of example embodiment 1, 2 or 3, wherein the semiconducting oxide material includes a material selected from the group consisting of tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide and tungsten oxide.

Example embodiment 5: The integrated circuit structure of example embodiment 1, 2, 3

or 4, further including a gate dielectric layer between the gate electrode and the first portion of the semiconducting oxide material on the insulator structure.

Example embodiment 6: The integrated circuit structure of example embodiment 5, wherein the gate dielectric layer includes a layer of a high-k dielectric material directly on the semiconducting oxide material.

Example embodiment 7: The integrated circuit structure of example embodiment 1, 2, 3, 4, 5 or 6, further including a first dielectric spacer between the first conductive contact and the first side of the gate electrode, the first dielectric spacer over a fourth portion of the semiconducting oxide material on the insulator structure. A second dielectric spacer is between the second conductive contact and the second side of the gate electrode, the second dielectric spacer over a fifth portion of the semiconducting oxide material on the insulator structure.

Example embodiment 8: The integrated circuit structure of example embodiment 7, further including a gate dielectric layer between the gate electrode and the first portion of the semiconducting oxide material on the insulator structure, wherein the gate dielectric layer is further along the first dielectric spacer and the second dielectric spacer.

Example embodiment 9: The integrated circuit structure of example embodiment 8, wherein the gate dielectric layer includes a layer of a high-k dielectric material directly on the semiconducting oxide material.

Example embodiment 10: An integrated circuit structure includes an insulator structure above a substrate. The insulator structure has a trench therein, the trench having sidewalls and a bottom. A semiconducting oxide material is in the trench in the insulator structure, the semiconducting oxide material conformal with the sidewalls and bottom of the trench. A gate dielectric layer is on the semiconducting oxide material in the trench, the gate dielectric layer conformal with the semiconducting oxide material conformal with the sidewalls and bottom of the trench. A gate electrode is on the gate dielectric layer in the trench, the gate electrode having a first side opposite a second side and having an exposed top surface. A first conductive contact is laterally adjacent the first side of the gate electrode, the first conductive contact on a first portion of the semiconducting oxide material conformal with the sidewalls of the trench. A second conductive contact is laterally adjacent the second side of the gate electrode, the second conductive contact on a second portion of the semiconducting oxide material conformal with the sidewalls of the trench.

Example embodiment 11: The integrated circuit structure of example embodiment 10, further including a third conductive contact over and in contact with the exposed top surface of the gate electrode.

Example embodiment 12: The integrated circuit structure of example embodiment 10 or

11, wherein the first conductive contact is in a second trench in the insulator structure, and the third conductive contact is in a third trench in the insulator structure.

Example embodiment 13: The integrated circuit structure of example embodiment 10, 11 or 12, wherein the semiconducting oxide material includes indium gallium zinc oxide.

Example embodiment 14: The integrated circuit structure of example embodiment 10, 11, 12 or 13, wherein the semiconducting oxide material includes a material selected from the group consisting of tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide and tungsten oxide.

Example embodiment 15: The integrated circuit structure of example embodiment 10, 11, 12, 13 or 14, wherein the gate dielectric layer includes a layer of a high-k dielectric material directly on the semiconducting oxide material.

Example embodiment 16: An integrated circuit structure includes an insulator structure above a substrate. The insulator structure has a topography that varies along a plane normal with a global plane of the substrate. A semiconducting oxide material is on the insulator structure. The semiconducting oxide material is conformal with the topography of the insulator structure. A gate electrode is laterally adjacent to a portion of the semiconducting oxide material on the insulator structure. The gate electrode has a first side opposite a second side. A first conductive contact is adjacent the first side of the gate electrode. A second conductive contact is adjacent the second side of the gate electrode.

Example embodiment 17: The integrated circuit structure of example embodiment 16, wherein the insulator structure includes a corrugated arrangement of alternating dielectric layers.

Example embodiment 18: The integrated circuit structure of example embodiment 17, wherein the insulator structure has a trench therein, the trench having sidewalls and a bottom.

Example embodiment 19: The integrated circuit structure of example embodiment 18, wherein at least one of the sidewalls of the trench includes the corrugated arrangement of alternating dielectric layers.

Example embodiment 20: The integrated circuit structure of example embodiment 16, 17, 18 or 19, further including a third conductive contact over and in contact with an exposed top surface of the gate electrode.

Example embodiment 21: The integrated circuit structure of example embodiment 16, 17, 18, 19 or 20, wherein the semiconducting oxide material includes indium gallium zinc oxide.

Example embodiment 22: The integrated circuit structure of example embodiment 16, 17, 18, 19, 20 or 21, wherein the semiconducting oxide material includes a material selected from the group consisting of tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium

oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide and tungsten oxide.

Example embodiment 23: The integrated circuit structure of example embodiment 16, 17, 18, 19, 20, 21 or 22, further including a gate dielectric layer between the gate electrode and the portion of the semiconducting oxide material on the insulator structure.

Example embodiment 24: The integrated circuit structure of example embodiment 23, wherein the gate dielectric layer includes a layer of a high-k dielectric material directly on the semiconducting oxide material.

CLAIMS

What is claimed is:

1. An integrated circuit structure, comprising:

an insulator structure above a substrate, the insulator structure having a topography that varies along a plane parallel with a global plane of the substrate;

a semiconducting oxide material on the insulator structure, the semiconducting oxide material conformal with the topography of the insulator structure;

a gate electrode over a first portion of the semiconducting oxide material on the insulator structure, the gate electrode having a first side opposite a second side;

a first conductive contact adjacent the first side of the gate electrode, the first conductive contact over a second portion of the semiconducting oxide material on the insulator structure; and

a second conductive contact adjacent the second side of the gate electrode, the second conductive contact over a third portion of the semiconducting oxide material on the insulator structure.

2. The integrated circuit structure of claim 1, wherein the insulator structure comprises one or more fins, individual ones of the fins having a top and sidewalls, the semiconducting oxide material on the top and sidewalls of the individual ones of the fins.

3. The integrated circuit structure of claim 1, wherein the semiconducting oxide material comprises indium gallium zinc oxide.

4. The integrated circuit structure of claim 1, wherein the semiconducting oxide material comprises a material selected from the group consisting of tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide and tungsten oxide.

5. The integrated circuit structure of claim 1, further comprising:

a gate dielectric layer between the gate electrode and the first portion of the semiconducting oxide material on the insulator structure.

6. The integrated circuit structure of claim 5, wherein the gate dielectric layer comprises a layer of a high-k dielectric material directly on the semiconducting oxide material.

7. The integrated circuit structure of claim 1, further comprising:

a first dielectric spacer between the first conductive contact and the first side of the gate electrode, the first dielectric spacer over a fourth portion of the semiconducting oxide material on the insulator structure; and

a second dielectric spacer between the second conductive contact and the second side of the gate electrode, the second dielectric spacer over a fifth portion of the semiconducting oxide material on the insulator structure.

8. The integrated circuit structure of claim 7, further comprising:

a gate dielectric layer between the gate electrode and the first portion of the semiconducting oxide material on the insulator structure, wherein the gate dielectric layer is further along the first dielectric spacer and the second dielectric spacer.

9. The integrated circuit structure of claim 8, wherein the gate dielectric layer comprises a layer of a high-k dielectric material directly on the semiconducting oxide material.

10. An integrated circuit structure, comprising:

an insulator structure above a substrate, the insulator structure having a trench therein, the trench having sidewalls and a bottom;

a semiconducting oxide material in the trench in the insulator structure, the semiconducting oxide material conformal with the sidewalls and bottom of the trench;

a gate dielectric layer on the semiconducting oxide material in the trench, the gate dielectric layer conformal with the semiconducting oxide material conformal with the sidewalls and bottom of the trench;

a gate electrode on the gate dielectric layer in the trench, the gate electrode having a first side opposite a second side and having an exposed top surface;

a first conductive contact laterally adjacent the first side of the gate electrode, the first conductive contact on a first portion of the semiconducting oxide material conformal with the sidewalls of the trench; and

a second conductive contact laterally adjacent the second side of the gate electrode, the second conductive contact on a second portion of the semiconducting oxide material conformal with the sidewalls of the trench.

11. The integrated circuit structure of claim 10, further comprising:

a third conductive contact over and in contact with the exposed top surface of the gate electrode.

12. The integrated circuit structure of claim 10, wherein the first conductive contact is in a second trench in the insulator structure, and the third conductive contact is in a third trench in the insulator structure.

13. The integrated circuit structure of claim 10, wherein the semiconducting oxide material comprises indium gallium zinc oxide.

14. The integrated circuit structure of claim 10, wherein the semiconducting oxide material comprises a material selected from the group consisting of tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide and tungsten oxide.

15. The integrated circuit structure of claim 10, wherein the gate dielectric layer comprises a layer of a high-k dielectric material directly on the semiconducting oxide material.

16. An integrated circuit structure, comprising:

an insulator structure above a substrate, the insulator structure having a topography that varies along a plane normal with a global plane of the substrate;

a semiconducting oxide material on the insulator structure, the semiconducting oxide material conformal with the topography of the insulator structure;

a gate electrode laterally adjacent to a portion of the semiconducting oxide material on the insulator structure, the gate electrode having a first side opposite a second side;

a first conductive contact adjacent the first side of the gate electrode; and

a second conductive contact adjacent the second side of the gate electrode.

17. The integrated circuit structure of claim 16, wherein the insulator structure comprises a corrugated arrangement of alternating dielectric layers.

18. The integrated circuit structure of claim 17, wherein the insulator structure has a trench therein, the trench having sidewalls and a bottom.

19. The integrated circuit structure of claim 18, wherein at least one of the sidewalls of the

trench comprises the corrugated arrangement of alternating dielectric layers.

20. The integrated circuit structure of claim 16, further comprising:

a third conductive contact over and in contact with an exposed top surface of the gate electrode.

21. The integrated circuit structure of claim 16, wherein the semiconducting oxide material comprises indium gallium zinc oxide.

22. The integrated circuit structure of claim 16, wherein the semiconducting oxide material comprises a material selected from the group consisting of tin oxide, antimony oxide, indium oxide, indium tin oxide, titanium oxide, zinc oxide, indium zinc oxide, gallium oxide, titanium oxynitride, ruthenium oxide and tungsten oxide.

23. The integrated circuit structure of claim 16, further comprising:

a gate dielectric layer between the gate electrode and the portion of the semiconducting oxide material on the insulator structure.

24. The integrated circuit structure of claim 23, wherein the gate dielectric layer comprises a layer of a high-k dielectric material directly on the semiconducting oxide material.

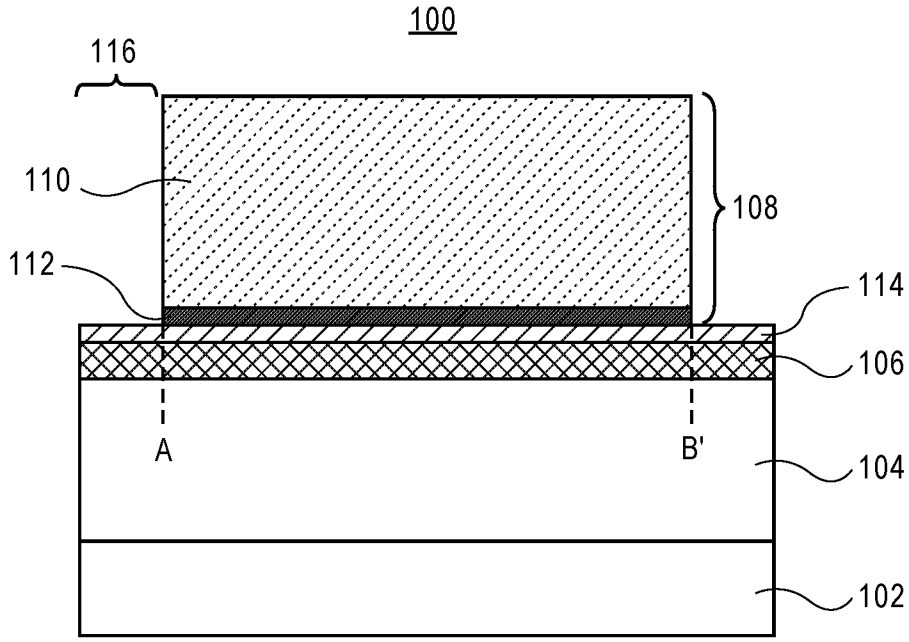

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FIG. 1A

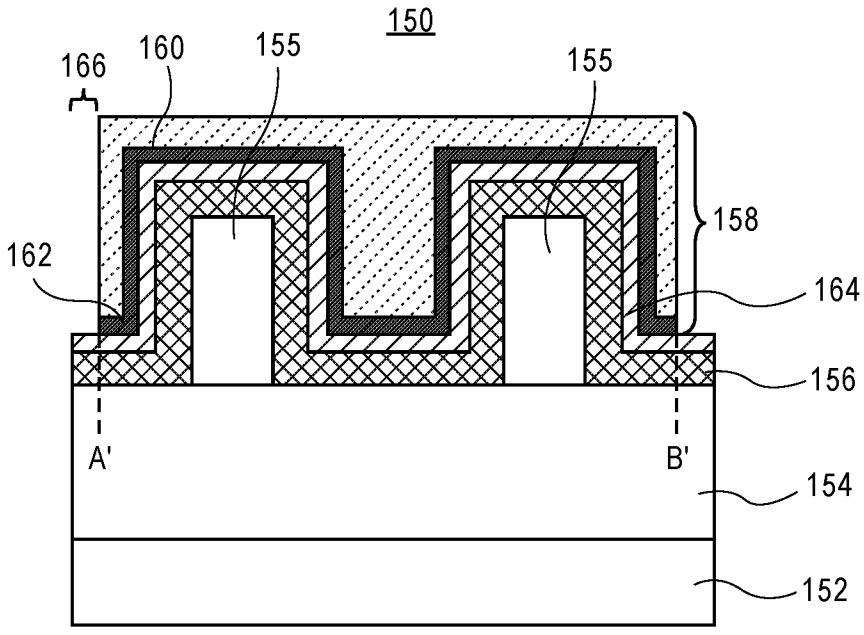

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FIG. 1B

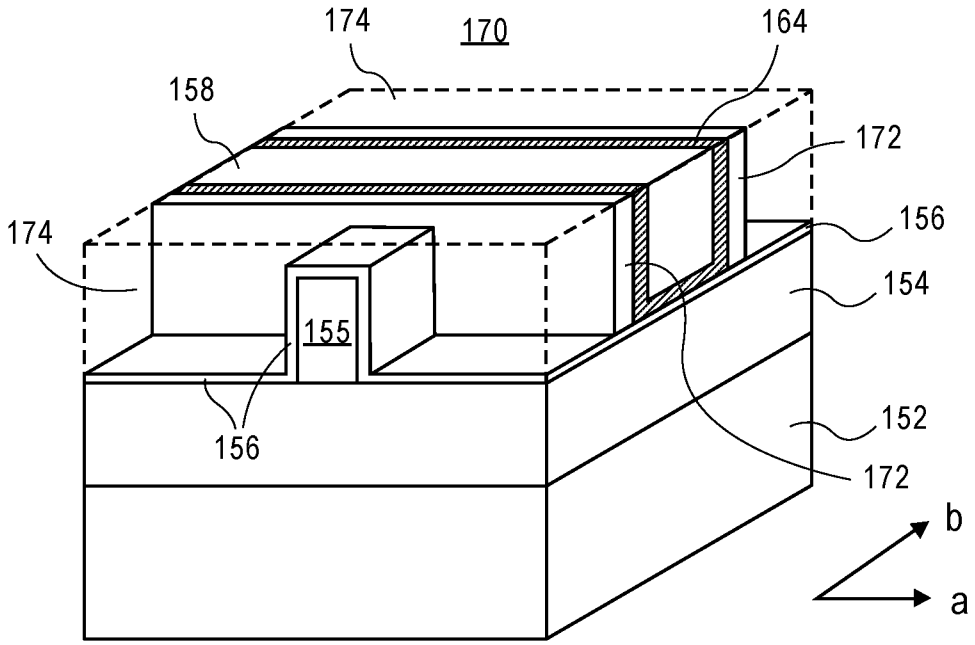


FIG. 1C

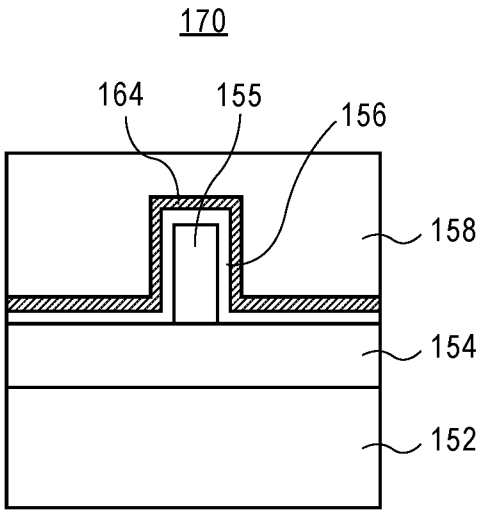


FIG. 1D

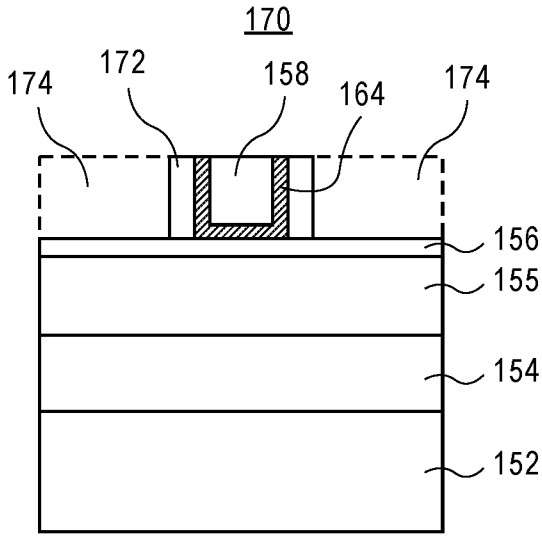


FIG. 1E

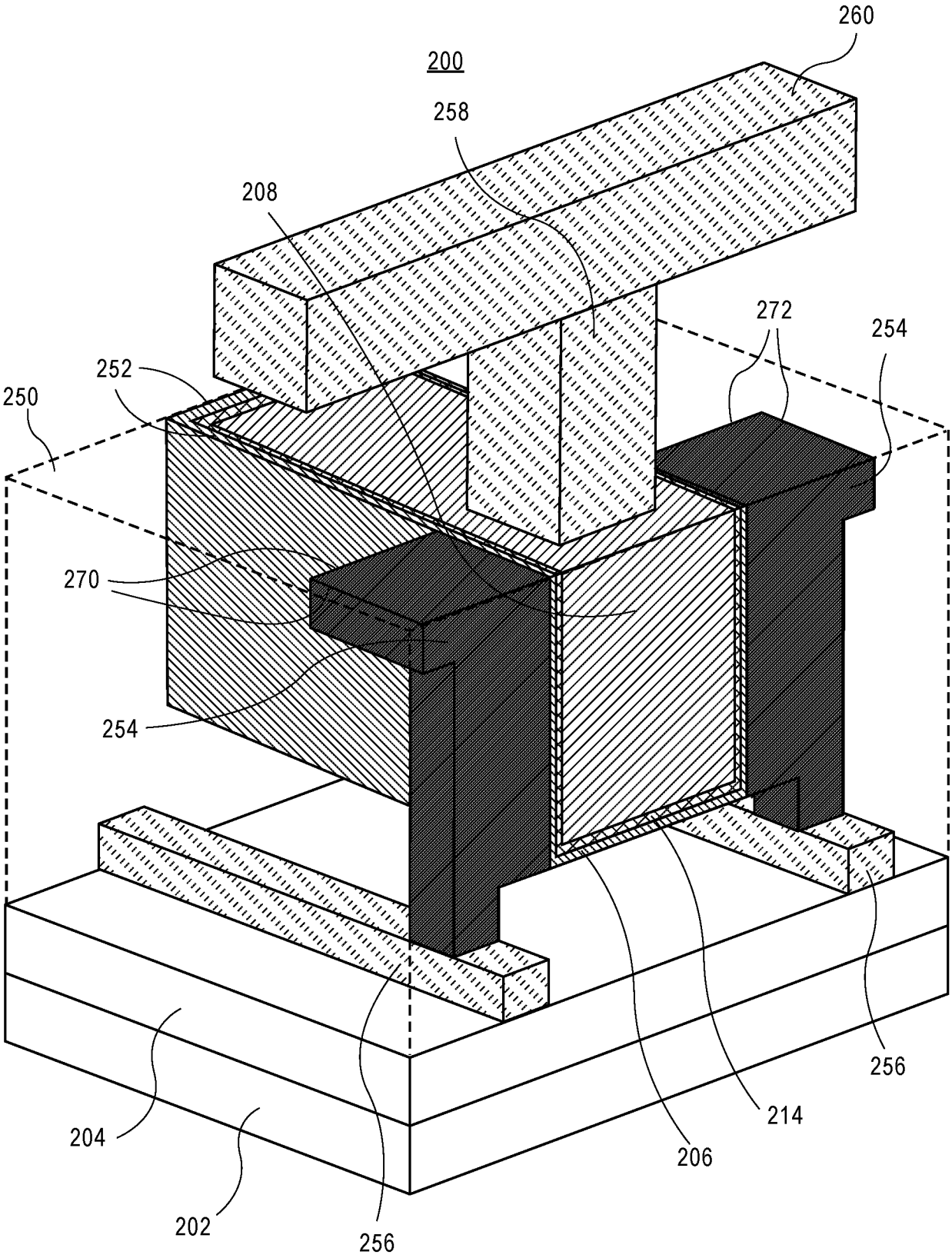


FIG. 2A

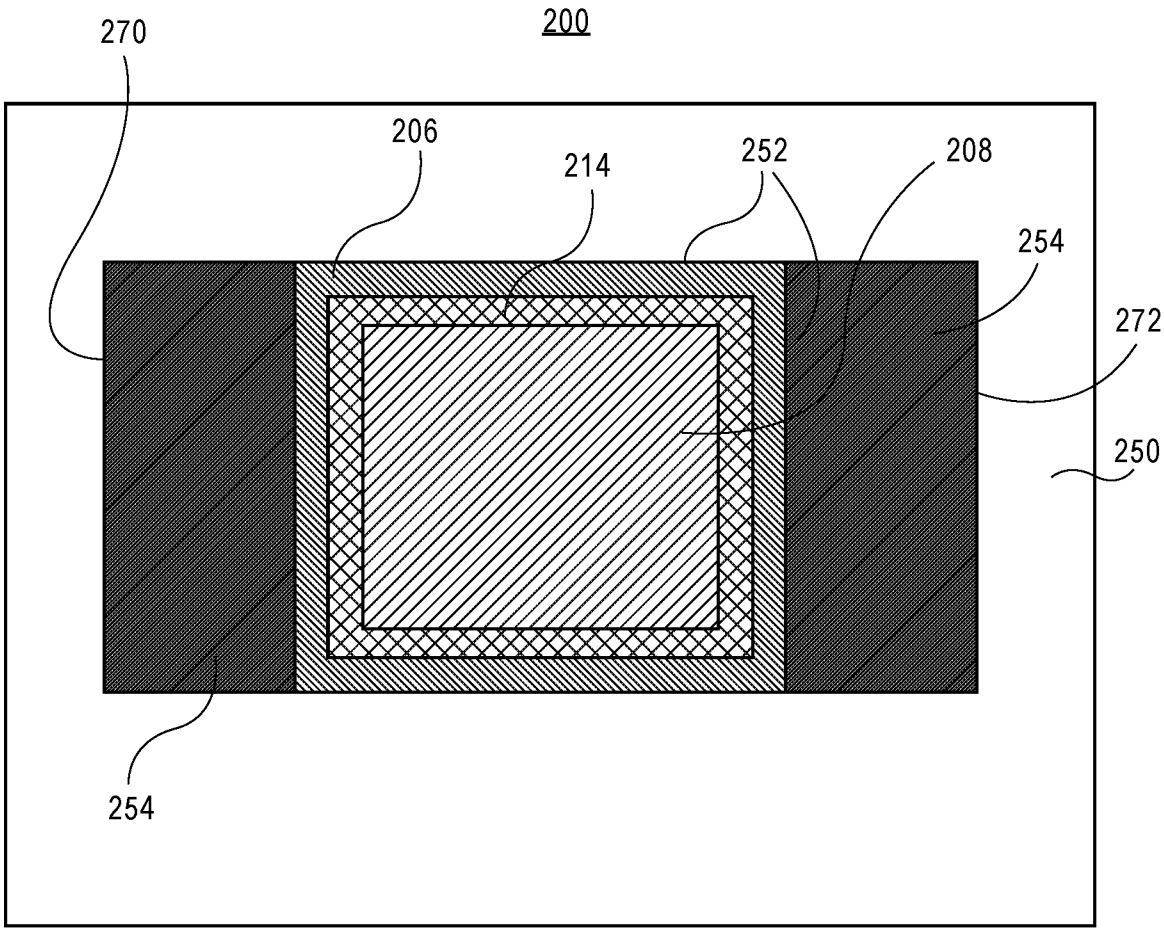


FIG. 2B

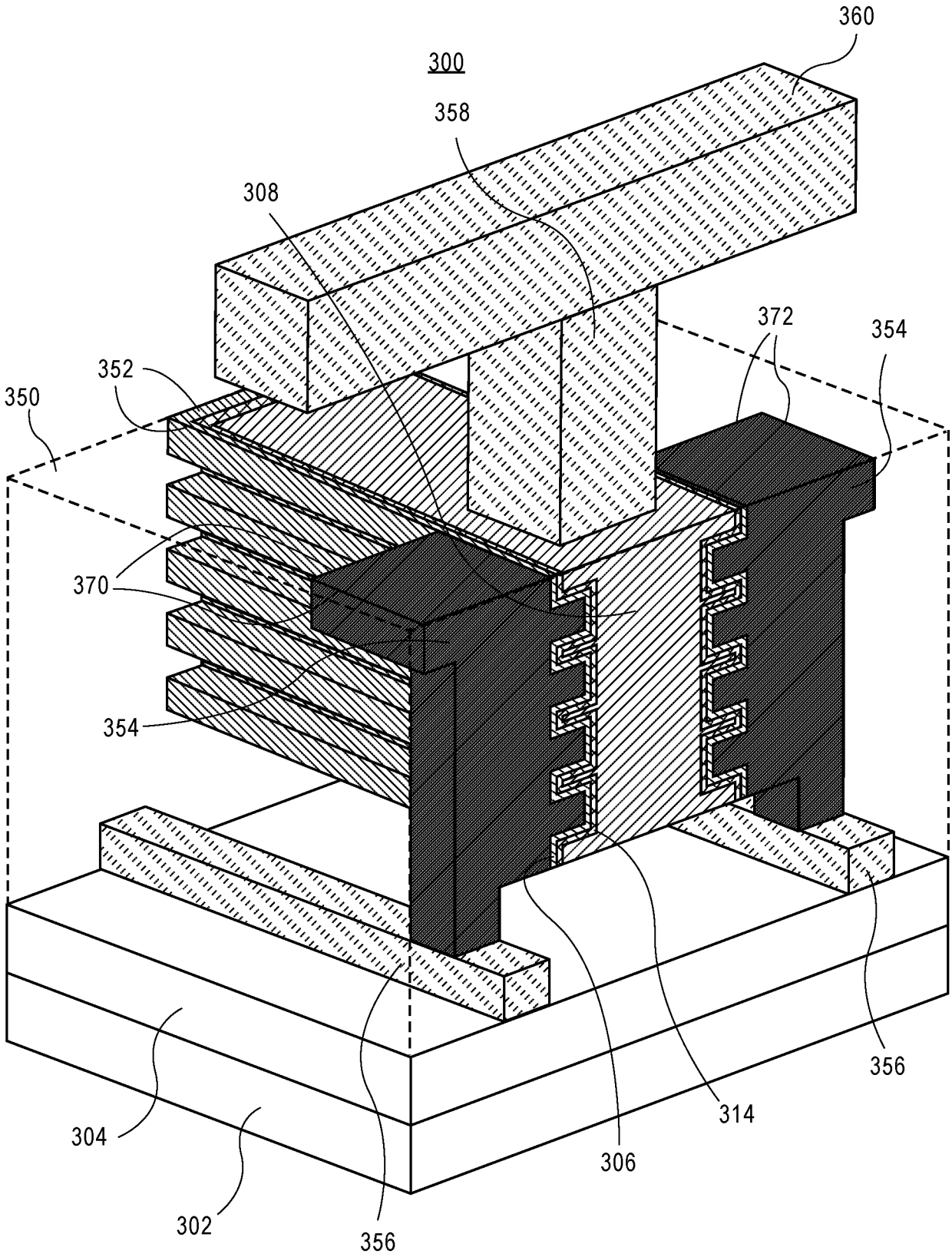


FIG. 3

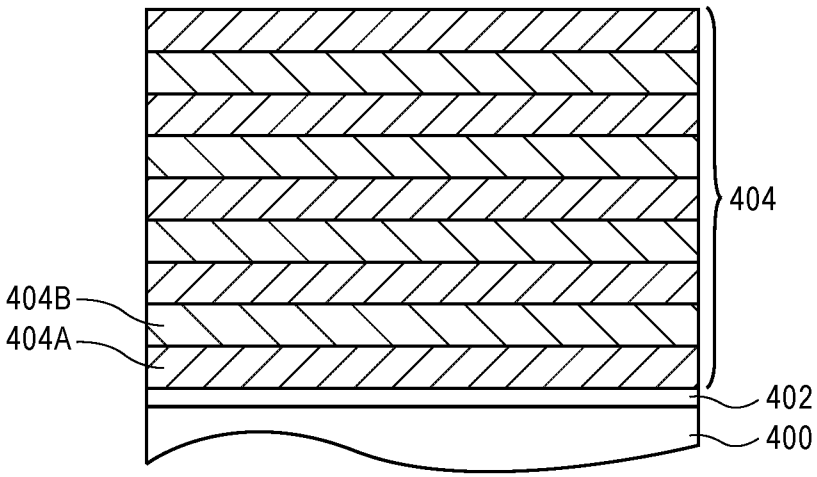


FIG. 4A

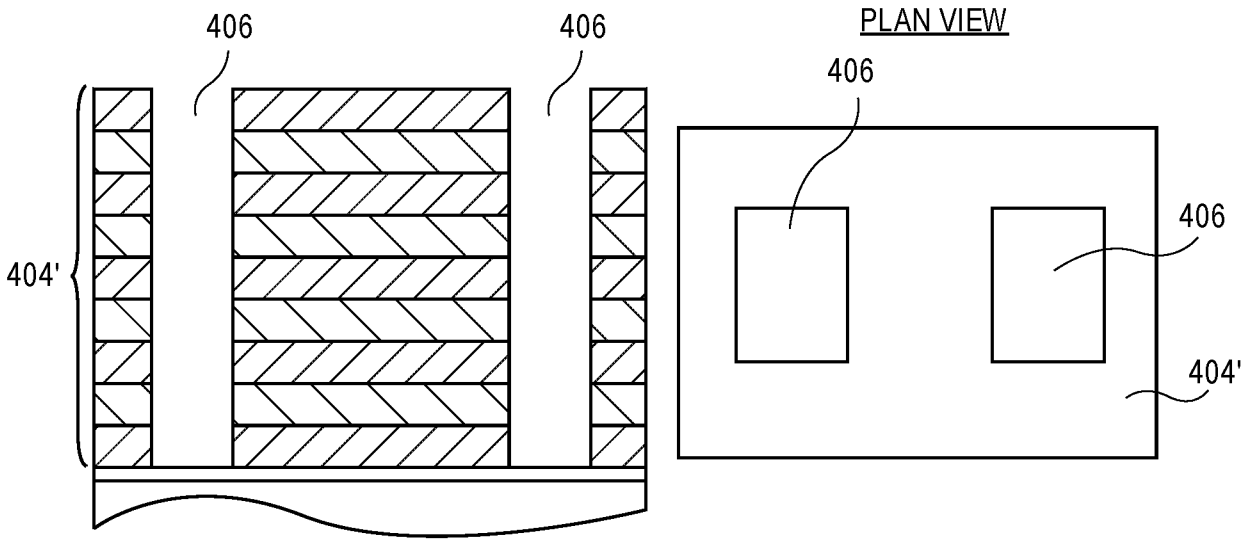


FIG. 4B

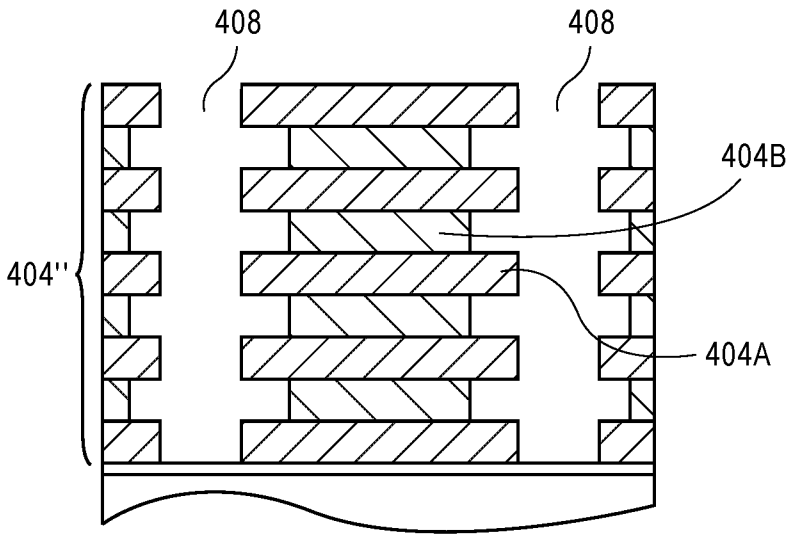


FIG. 4C

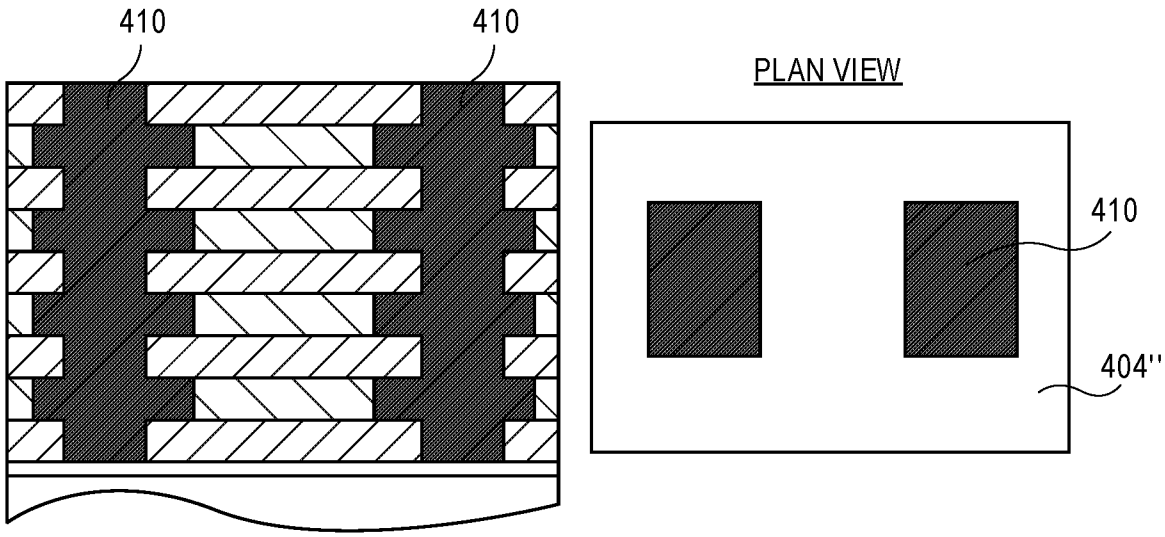


FIG. 4D

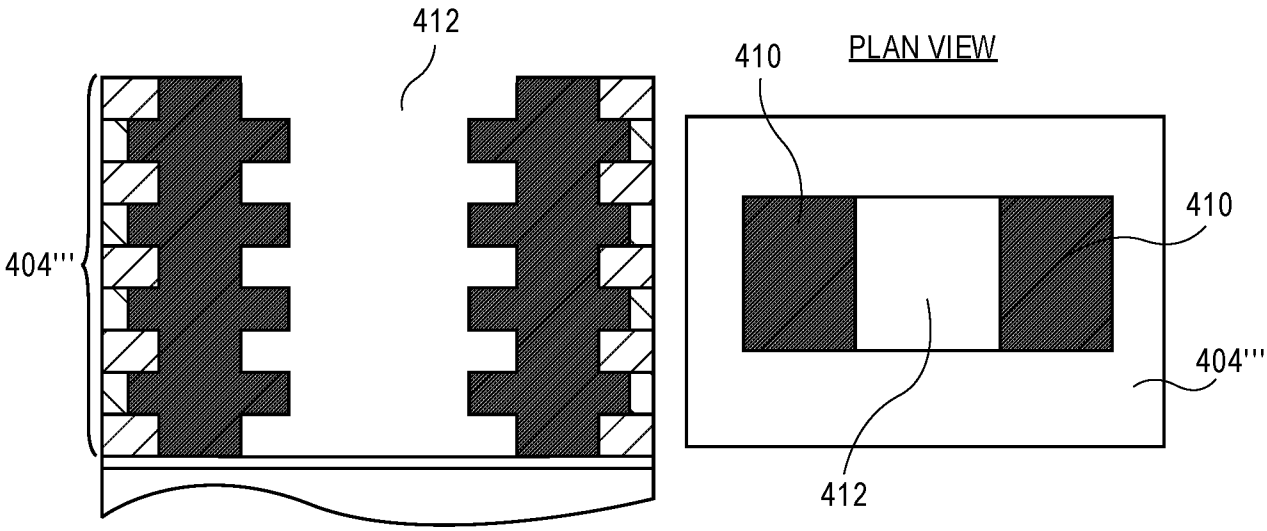


FIG. 4E

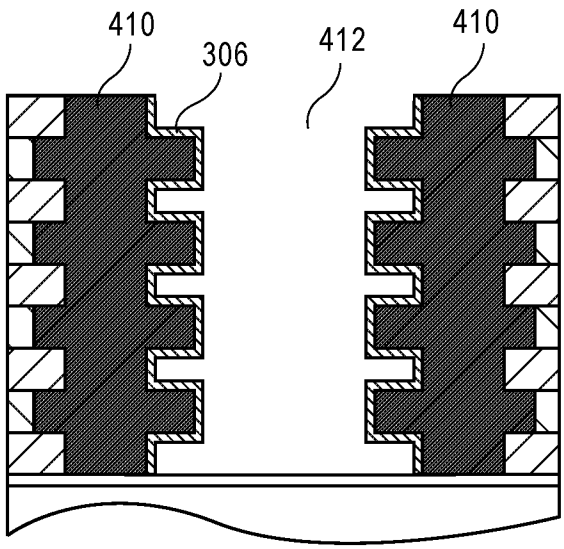


FIG. 4F

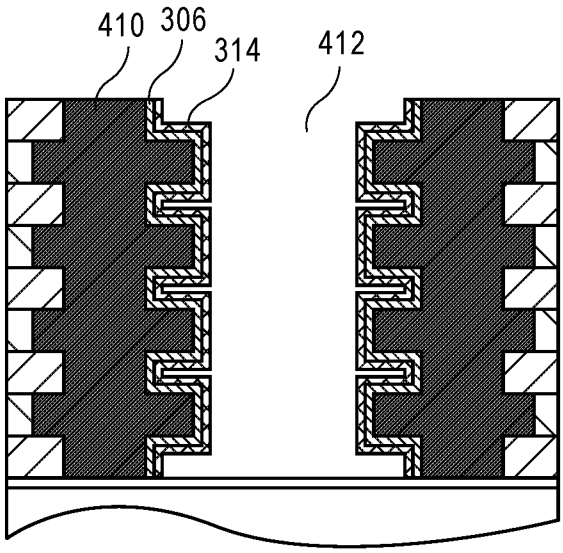

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FIG. 4G

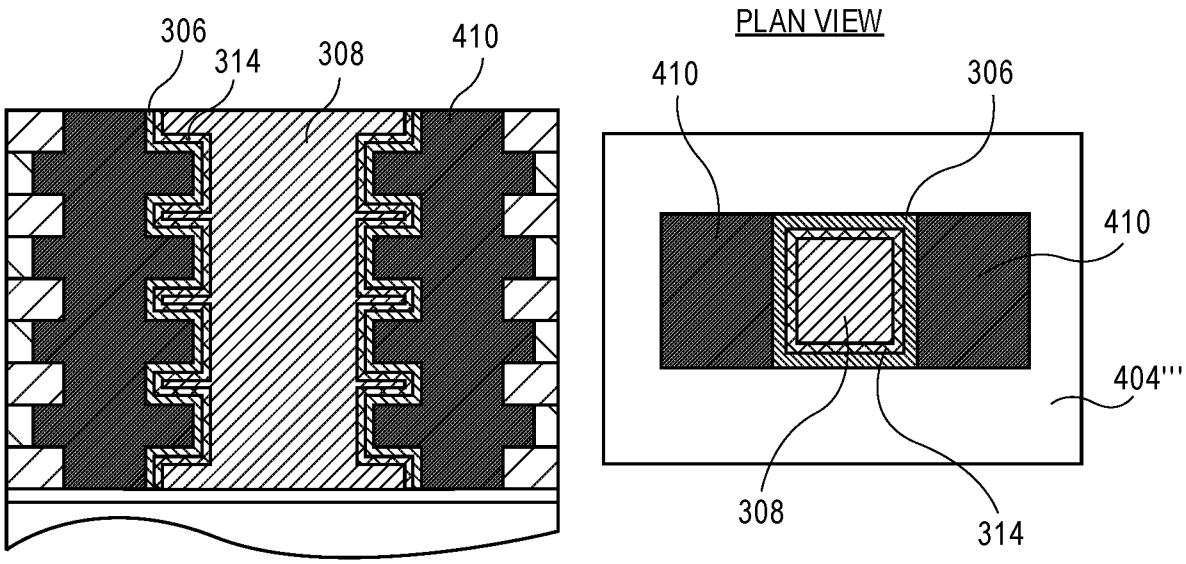

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PLAN VIEW
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FIG. 4H

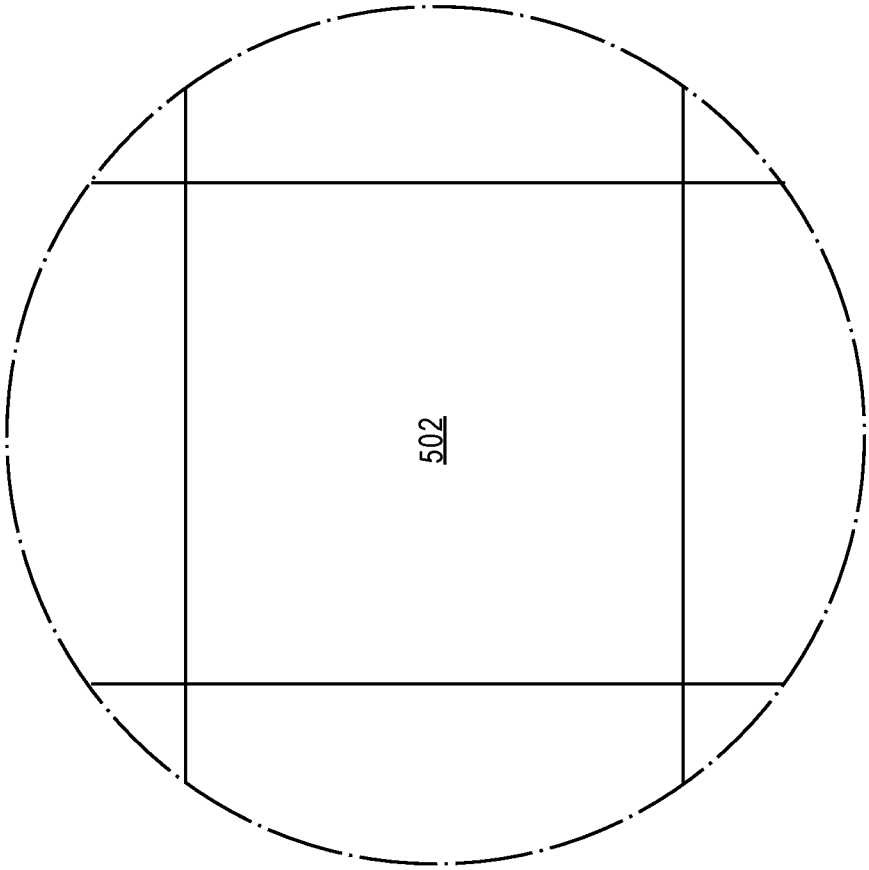


FIG. 5B

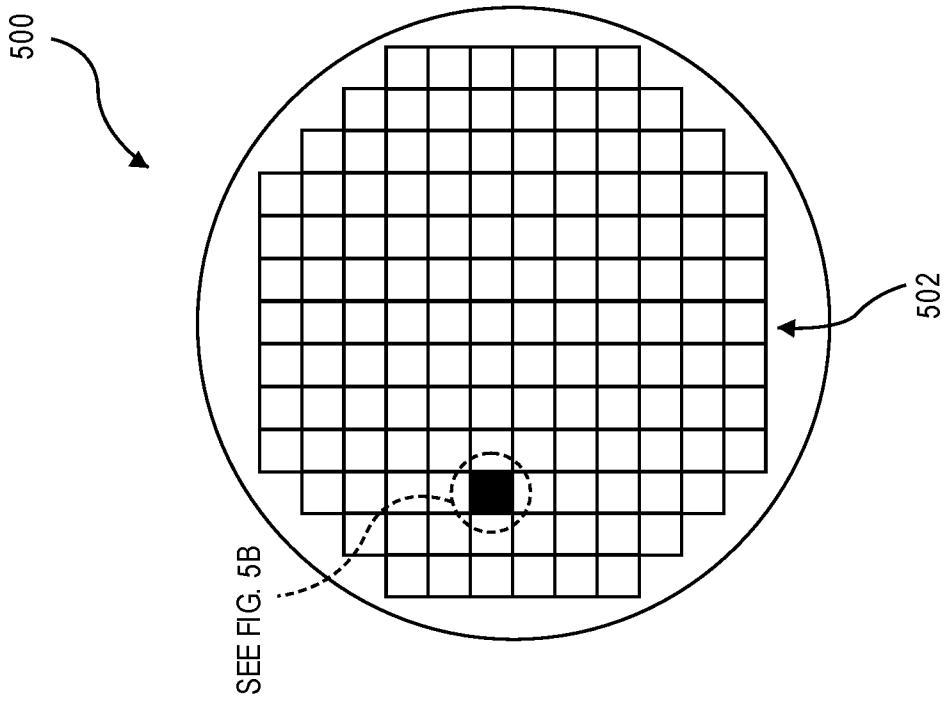


FIG. 5A

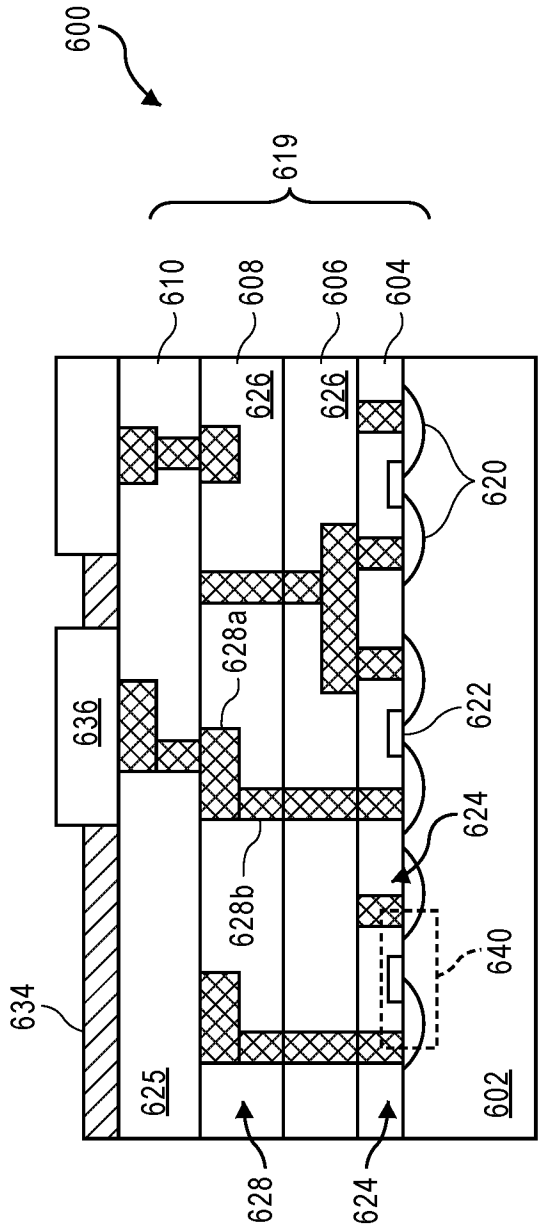

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FIG. 6

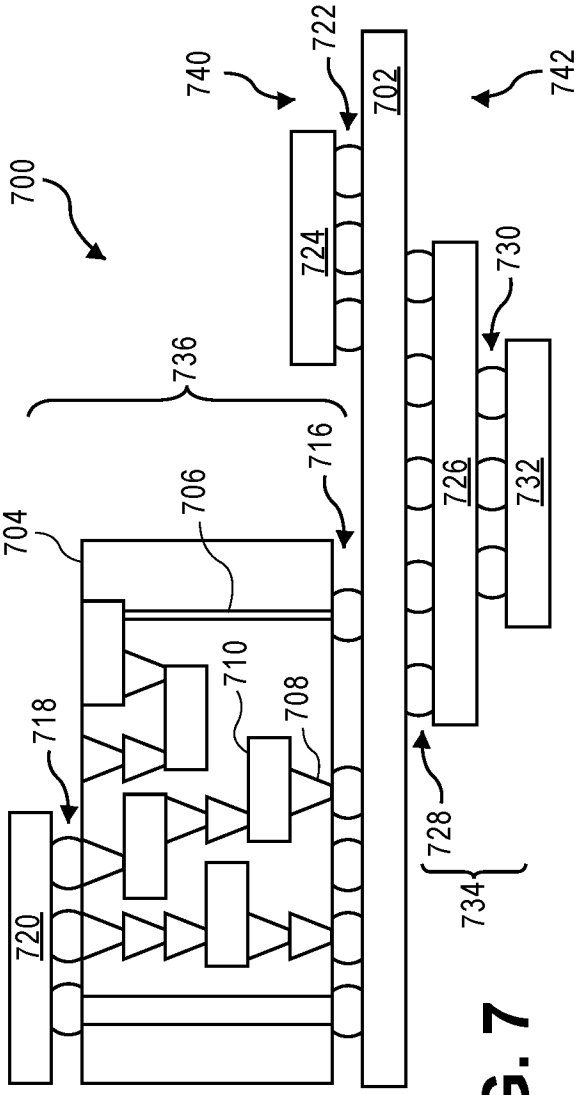

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FIG. 7

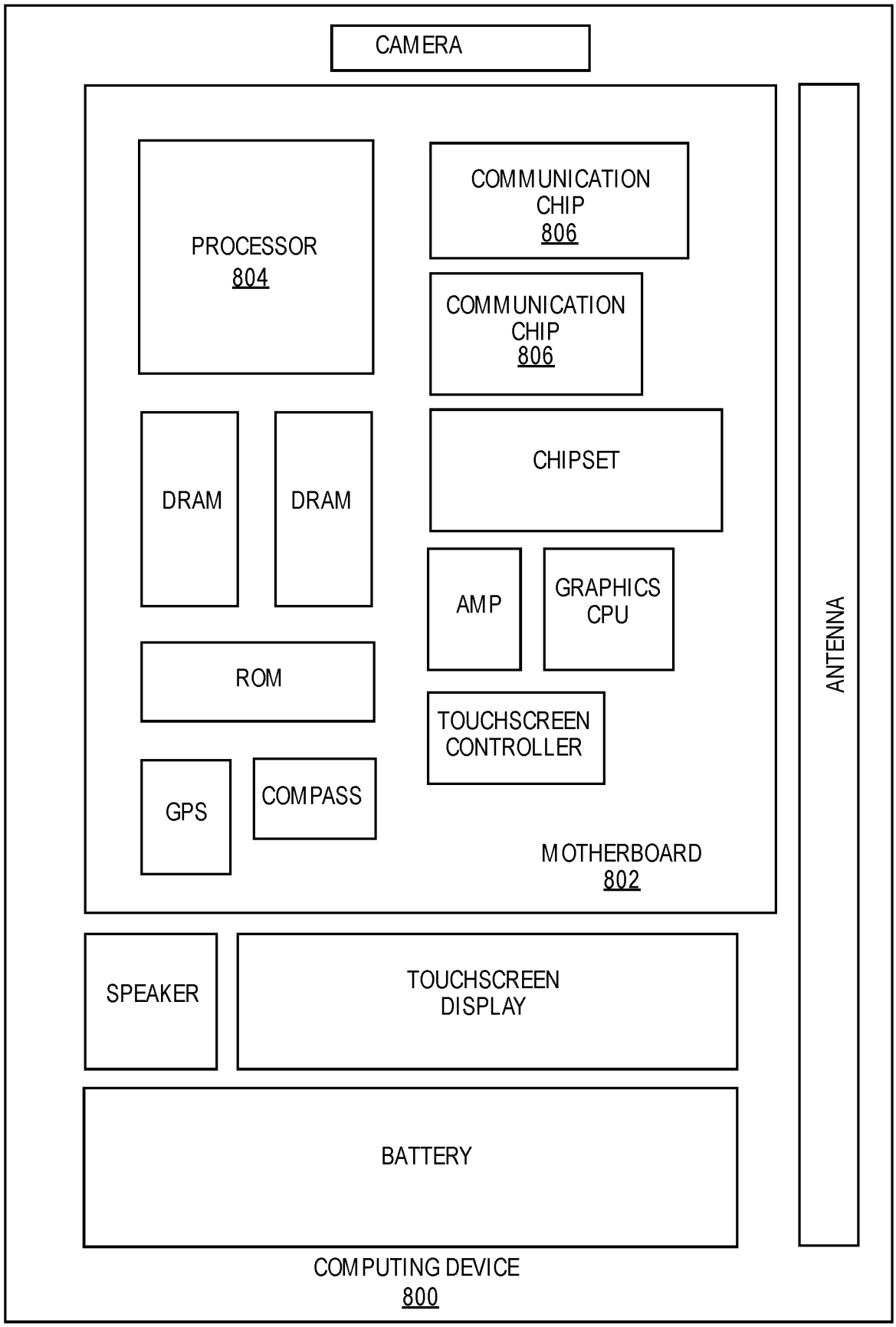

CAMERA
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COMMUNICATION
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COMMUNICATION
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AMP
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CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD
802
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE
800

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/038383

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/786(2006.01)i, H01L 29/78(2006.01)i, H01L 21/768(2006.01)i, H01L 29/423(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/786; H01L 21/336; H01L 29/78; H01L 29/94; H01L 21/02; H01L 21/768; H01L 29/423

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: thin film transistor, tft, fin-structure, semiconducting oxides, contact, gate, electrode

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2016-0359043 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 08 December 2016 See paragraphs [0012]-[0034]; claim 1; and figures 2-5.	1-9
A		10-24
Y	US 2013-0175530 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 11 July 2013 See paragraphs [0049], [0071], [0167]; claim 1; and figures 1D, 10A.	1-15
Y	US 8603881 B1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 10 December 2013 See column 3, line 8-column 9 line 29; claim 1; and figures 1, 5, 7, 12-13.	10-24
Y	US 2013-0119371 A1 (CHIU et al.) 16 May 2013 See paragraphs [0008], [0017], [0033]; and figures 1A-2B.	16-24
A	US 2006-0249777 A1 (FORBES et al.) 09 November 2006 See figure 1.	1-24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 February 2018 (13.02.2018)	**13 February 2018 (13.02.2018)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
Kim, Yeonkyung
Telephone No. +82-42-481-3325

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/038383

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2016-0359043 A1	08/12/2016	CN 106252231 A	21/12/2016
		KR 10-1799646 B1	20/11/2017
		KR 10-2016-0142750 A	13/12/2016
		TW 201643967 A	16/12/2016
		TW I588907 B	21/06/2017
US 2013-0175530 A1	11/07/2013	JP 2013-165260 A	22/08/2013
		JP 2017-092490 A	25/05/2017
		JP 6076097 B2	08/02/2017
		KR 10-2013-0082068 A	18/07/2013
		US 9012913 B2	21/04/2015
US 8603881 B1	10/12/2013	None	
US 2013-0119371 A1	16/05/2013	CN 102569415 A	11/07/2012
		CN 102569415 B	05/11/2014
		TW 201320338 A	16/05/2013
		TW I445175 B	11/07/2014
		US 8704220 B2	22/04/2014
US 2006-0249777 A1	09/11/2006	US 2001-0035549 A1	01/11/2001
		US 6025225 A	15/02/2000
		US 7084451 B2	01/08/2006
		US 7408216 B2	05/08/2008