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Szimmetrikus perforálás CQI/PCI jelentéshez HS-DPCCH-n

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(54) **SYMMETRIC PUNCTURING FOR CQI/PCI REPORTING ON THE HS-DPCCH**

SYMMETRISCHE PUNKTIERUNG FÜR CQI/PCI NACHRICHTEN AUF DEM HS-DPCCH KANAL
POINCONNAGE SYMÉTRIQUE POUR LES RAPPORTS CQI/PCI TRANSMIS PAR LE CANAL
HS-DPCCH

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Description

TECHNICAL FIELD

5 **[0001]** The present disclosure relates to multi antenna wireless communication systems.

BACKGROUND

10 **[0002]** Several new features are added to the long term High Speed Packet Access (HSPA) evolution in order to meet performance requirements set by the International Mobile Telecommunications Advanced (IMT-A). The main objective of these additional features is to increase average spectral efficiency. One possible technique for improving downlink spectral efficiency is to introduce support for four branch multiple-input multiple-output (MIMO), i.e. utilize up to four transmit and receive antennas to enhance the spatial multiplexing gains and to offer improved beamforming capabilities. Four branch MIMO provides up to 84 Mbps per 5 MHz carrier for high signal to noise ratio (SNR) users and improves
15 the coverage for low SNR users.

[0003] The current HSPA system (Release 7-10) supports 1 or 2 transmit antennas at the base station (e.g., NodeB). For these systems, from channel sounding, a user equipment (UE) (e.g., a mobile phone or any other wireless communication device) measures a channel and reports in one sub frame channel state information related to the measured channel. Typically, this report consists of a channel quality indicator (CQI), which explicitly indicates rank indicator (RI),
20 and precoding control indicator (PCI). The UE sends this report periodically for every subframe (TTI). The NodeB uses this report in scheduling the UE.

[0004] Introduction of 4-branch MIMO will require a new feedback channel structure to send the CQI/PCI information to the NodeB. To reduce the signaling overhead at downlink and uplink, it was recommended to use two codewords for four branch MIMO. For the uplink signalling channel (HS-DPCCH), it was agreed to use a structure similar to that of 2
25 Antenna MIMO (Release -7), where the CQI, PCI are sent in one subframe. Hence in total 14 bits are used to report: CQI (8 bits), RI (2 bits) and PCI (4 bits). Since the total number of bits is different compared to that of Release 7 structure of 10 bits, a new encoding scheme is needed to transmit these bits. Hence to encode these 14 bits in one subframe a convolutional code with 1/3 code rate has been proposed. Unfortunately the puncturing pattern chosen for this scheme is not optimal in terms of packet error performance.

30 3GPP Tdoc R1-123565 "Remaining issues on HS-SCCH design for Four Branch Downlink MIMO" discuss different channel coding and puncturing schemes and simulation results of such schemes for HS-SCCH design of four branch downlink MIMO.

 3GPP Tdoc R1-123816 "Further discussions on HS-SCCH design" discuss different convolutional coding and puncturing schemes and simulation results of such schemes for HS-SCCH design of four branch downlink MIMO.

35 3GPP Tdoc R1-123566 "Remaining issues on feedback design for Four Branch Downlink MIMO" discuss and compares simulation results for some CQI coding schemes using convolutional coding/puncturing and block codes respectively.

 3GPP Tdoc R1-99G51 "New puncturing scheme for convolutional codes" discuss different puncturing schemes for convolutional coding.

40 SUMMARY

[0005] According to the present invention a method for encoding control information and a user equipment are provided in independent claims 1 and 4, respectively.

45 **[0006]** A method for encoding control information generated by a user equipment (UE) is disclosed. The control information comprises a first bit sequence, a second bit sequence, and a third bit sequence. The method includes: arranging said bit sequences to produce a bit sequence X1; padding the bit sequence X1 with a bit sequence P1 to produce a bit sequence X1'; convolution encoding the bit sequence X1' to produce an encoded bit sequence Z1; and puncturing the bit sequence Z1 using a predefined puncturing pattern to produce a bit sequence R1, wherein the predefined puncturing pattern is a rotationally symmetric puncturing pattern.

50 **[0007]** The bit sequence Z1 may consist of 44 bits, and the predefined puncturing pattern may be [1 3 42 and 44]. Puncturing the bit sequence Z1 using the predefined puncturing pattern to produce the bit sequence R1 may consist of removing the first bit, the third bit, the forty-second bit, and the forty-fourth bit from the bit sequence Z1. The first bit sequence may be a channel quality indicator, CQI, value; the second bit sequence may be a precoding control indicator, PCI, value; and the third bit sequence is value identifying a preferred number of layers. The bit sequence X1 may consist
55 of fourteen bits, and the bit sequence P1 may consist of eight bits. Convolution encoding the bit sequence X1' to produce the encoded bit sequence Z1 may include convolution encoding the bit sequence X1' using rate 1/2 convolutional encoding.

[0008] A user equipment (UE) is disclosed. The UE is adapted to: generate control information, the control information

comprising a first bit sequence, a second bit sequence, and a third bit sequence; arrange said bit sequences to produce a bit sequence X1; pad the bit sequence X1 with a bit sequence P1 to produce a bit sequence X1'; convolution encode the bit sequence X1' to produce an encoded bit sequence Z1; and puncture bit sequence Z1 using a predefined puncturing pattern (700, 900) to produce a bit sequence R1. The predefined puncturing pattern is a rotationally symmetric puncturing pattern.

[0009] An apparatus for encoding control information is disclosed. The control information includes a first bit sequence, a second bit sequence, and a third bit sequence. The apparatus comprises: a multiplexor adapted to multiplex said bit sequences to produce a bit sequence X1; a padder adapted to pad the bit sequence X1 with a bit sequence P1 to produce a bit sequence X1'; a convolution encoder adapted to convolution encode the bit sequence X1' to produce an encoded bit sequence Z1; and a rate matcher adapted to puncture the bit sequence Z1 using a predefined puncturing pattern to produce a bit sequence R1. The predefined puncturing pattern is a rotationally symmetric puncturing pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010]

FIG. 1 illustrates an exemplary system.

FIG. 2 is a block diagram of an example base station.

FIG. 3 is a block diagram of an example UE.

FIG. 4 illustrates a message flow diagram.

FIG. 5A illustrates a structure of HS-DPCCH for a single carrier.

FIG. 5B illustrates another structure for HS-DPCCH.

FIG. 6 illustrates an example puncturing pattern.

FIG. 7 illustrates an example puncturing pattern.

FIG. 8 shows a BLER plot.

FIG. 9 illustrates an example puncturing pattern.

FIG. 10 illustrates an example puncturing pattern.

FIG. 11 shows a BLER plot.

FIG. 12 shows a BLER plot.

FIG. 13 illustrates an example puncturing pattern.

FIG. 14 illustrates an example puncturing pattern.

FIG. 15 shows a BLER plot.

FIG. 16 shows a BLER plot.

FIG. 17 is a functional block diagram of an example UE.

FIG. 18 is a flow chart illustrating a process according to some embodiments.

DETAILED DESCRIPTION OF EMBODIMENTS

[0011] In one aspect, this disclosure relates to an improved process for encoding control information transmitted from a UE to a base station in a MIMO system. In some embodiments, the process may begin with the UE selecting and/or

determining (i.e., "generating") control information to transmit to the base station. The generated control information may include: CQI, RI, and PCI, where each has a corresponding bit sequence. The bit sequences are arranged to produce a bit sequence X1, (in some embodiments X1 is fourteen bits). In some embodiments, the first portion of X1 (e.g., the first eight bits of X1) are for the CQI, the next portion of X1 (e.g., the next two bits) identify the RI (i.e., the bits identify a rank), and the last portion of X1 (e.g., the next four bits of X1) identify a PCI. Next, X1 is padded with bit sequence P1 (in some embodiments P1 is eight bits in length) to produce bit sequence X1'. Bit sequence X1' is convolution encoded to produce encoded bit sequence Z1. Depending on the length of X1' and on the rate of the convolutional encoder, Z1 may be, for example, 44 or 66 bits. For example, when X1' is 22 bits and the rate is $\frac{1}{2}$, then Z1=44bits and when X1' is 22 bits and the rate is $\frac{1}{3}$, then Z1=66bits. The encoded bits Z1 are then punctured by a rate matcher using a predefined rotationally symmetric puncturing pattern to produce bit sequence R1 (in some embodiments Z1 is punctured such that RI is 40 bits in length). In some embodiments, R1 is then spread by spreading factor 128, QPSK modulated, and transmitted using two slots.

[0012] In one particular embodiment, when the rate is $\frac{1}{3}$, the following puncturing pattern is used by the rate matcher: [1 2 3 4 5 6 7 8 9 10 11 12 13 54 55 56 57 58 59 60 61 62 63 64 65 66]. That is, bits 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, and 66 are removed from Z1 by rate matcher to produce R1.

[0013] In another particular embodiment, when the rate is $\frac{1}{2}$ and, the one of the following six puncturing patterns is used by the rate matcher: (1) [1 3 42 44]; (2) [1 2 43 44]; (3) [1 4, 41 44]; (4) [2 3 42 43]; (5) [2 4 41 43]; (6) [3 4 41 42]. That is, for example, if the first puncturing patterns is used, then bits 1, 3, 42 and 44 are removed from Z1 by rate matcher to produce R1.

[0014] Preferably, the puncturing pattern used is a "rotationally symmetric" pattern. That is, for each bit n included in the puncturing pattern there exists another bit n' that is also included in the puncturing pattern, wherein $n' = (N+1) - n$, where N is the bit length of encoded bit sequence Z1. For example, if the puncturing pattern is rotationally symmetric and includes bit 7 and N=66, then the puncturing pattern necessarily also includes bit 60 (i.e., $60 = 66+1-7$). Each of the above identified puncturing patterns is rotationally symmetric.

[0015] In another aspect, the disclosure relates to an improved UE for use in a MIMO system. In some embodiments, the improved UE includes a receiver for receiving data intended for the UE. The UE may further include a channel measuring unit for generating control information to send to the base station serving the UE. The generated control information may include: CQI bits (e.g., 8 bits), RI bits (e.g., 2 bits), and PCI bits (e.g., 4 bits). The UE may further include a multiplexor for multiplexing the CQI bits, RI bits, and PCI bits to produce a bit sequence X1. In some example embodiments, the first 8 bits of X1 are the CQI bits, the next two bits of X1 are the RI bits, and the last four bits of X1 are the PCI bits (in some embodiments X1 is fourteen bits). The UE may also include a padder that pads X1 with bit sequence P (in some embodiments P is eight bits in length) to produce bit sequence X1'. The UE also includes a convolutional encoder that convolution encodes X1' to produce encoded bit sequence Z1. Depending on the length of X1' and on the rate of the convolutional encoder, Z1 may be, for example, 44 or 66 bits. For example, when X1' is 22 bits and the rate is $\frac{1}{2}$, then Z1=44bits and when X1' is 22 bits and the rate is $\frac{1}{3}$, then Z1=66bits. The encoded bits Z1 are then punctured by a rate matcher using a predefined rotationally symmetric puncturing pattern to produce bit sequence RI (in some embodiments Z1 is punctured such that RI is 40 bits in length). The UE may also include modulator and transmitter that then spreads, modulates and transmits RI in one or more slots.

[0016] Referring now to FIG. 1, FIG. 1 illustrates schematically a universal mobile telecommunications system, UMTS, network 100 in which the present methods and apparatuses can be implemented. It should be noted, however, that the skilled person will readily be able to perform implementations in other similar communication systems involving transmission of coded data between nodes.

[0017] In FIG. 1 the UMTS network 100 comprises a core network 110 and a UMTS terrestrial radio access network, UTRAN, 103. The UTRAN 103 comprises a number of nodes in the form of radio network controllers (RNC) 105 (e.g., RNCs 105a,b), each of which is coupled to a set of neighbouring nodes in the form of one or more base stations 104 (e.g. NodeBs 104a,b). Each NodeB 104 is responsible for a given geographical radio cell and the controlling RNC 105 is responsible for routing user and signalling data between that NodeB 104 and the core network 110. All of the RNC's 105 may be coupled to one another. A general outline of the UTRAN 103 is given in 3GPP technical specification TS 25.401 V3.2.0.

[0018] FIG. 1 also illustrates communication devices 106 (a.k.a., user equipments (UEs) (e.g., UEs 106a, 106b) connected to a respective NodeB 104a, 104b in the UTRAN 103 via a respective air interface 111a, 111b. UEs served by one NodeB, such as UE 106a served by NodeB 104a, are located in a so-called radio cell. The core network 110 comprises a number of nodes represented by node 107 and provides communication services to the UE 106 via the UTRAN 103, for example when communicating with the Internet 109 where, schematically, a server 120 illustrates an entity with which the UEs 106 may communicate. As the skilled person realizes, the network 100 in FIG. 1 may comprise a large number of similar functional units in the core network 110 and the UTRAN 103, and in typical realizations of networks, the number of mobile devices may be very large. Furthermore, communication between the nodes in the UTRAN 103 and the UEs 106 may follow the protocols as specified by 3GPP HSPA specifications.

[0019] FIG. 2 is a functional block diagram schematically illustrating base station 104, according to some embodiments. In the embodiment of FIG. 2, the base station 104 represents a NodeB. The base station 104 comprises processing means, memory means and communication means in the form of a processor 202, a memory 204 and communication circuitry 206. The base station 104 communicates with other nodes via a first data path 208 and via a second data path 210. For example, the first data path 208 can be connected to a RNC and the second data path 210 can be connected to one or more antennas 212. The data paths 208, 210 can be any of uplink and downlink data paths, as the skilled person will realize.

[0020] FIG. 3 is a functional block diagram schematically illustrating UE 106, according to some embodiments. The UE 106 comprises processing means, memory means and communication means in the form of a processor 252, a memory 254 and radio circuitry 256. The UE 106 communicates with other nodes via a radio air interface with the use of one or more antennas 262. The UE 106 also comprises input/output circuitry 258 in the form of, e.g., a display, a keypad, a microphone, a camera etc.

[0021] The methods to be described below can be implemented in the base station 104 and the UE 106, respectively. In such embodiments, the method actions are realized by means of software instructions 205, 255 that are stored in the memory 204, 254 and are executable by the processor 202, 252. Such software instructions 205, 255 can be realized and provided in any suitable way, e.g. provided via the networks 110, 103 or being installed during manufacturing, as the skilled person will realize. Moreover, the memory 204, 254, the processor 202, 252, as well as the communication circuitry 206 and radio circuitry 256 comprise software and/or firmware that, in addition to being configured such that it is capable of implementing the methods to be described, is configured to control the general operation of the base station 104 and the UE 106, respectively, when operating in a cellular mobile communication system such as the system 100 in FIG. 1. However, for the purpose of avoiding unnecessary detail, no further description will be made in the present disclosure regarding this general operation.

[0022] Referring now to FIG. 4, FIG. 4 shows an example message exchange between a base station 104 (e.g., NodeB 104) and a UE 106 in a HSDPA system 100. As shown in FIG. 4, the NodeB 104 transmits a pilot signal on a common pilot channel (e.g., the CPICH) 402.

[0023] The pilot signal may be broadcast by the base station with constant power and of a known bit sequence. The UE receives the pilot signal and a channel measuring unit of the UE uses the pilot channel to determine a channel quality indicator (CQI) and a precoding channel indicator (PCI).

[0024] For two antennas, the CQI is computed as

$$CQI = \begin{cases} 15 \times CQI_1 + CQI_2 + 31 & \text{when 2 transport blocks are preferred by the user equipment} \\ CQI_S & \text{when 1 transport block is preferred by the user equipment} \end{cases}$$

where the CQI is the channel quality per individual layer. CQI_S is the CQI value in the case of Rank = 1. CQI₁ and CQI₂ are the individual CQI values for each stream in the case of Rank = 2.

[0025] It can be observed that if the CQI is less than 31, the rank information is 1, otherwise the rank information is 2. The PCI is the precoding information bits selected in the subset of the codebook corresponding to the rank information.

[0026] The CQI and PCI along with other information (e.g., hybrid automatic repeat request (HARQ) acknowledgement/negative acknowledgement (ACK/NAK)) is reported to the NodeB using, for example a high speed dedicated physical control channel (HS-DPCCH) 404. In some embodiments, the periodicity of HS-DPCCH is one subframe (2msec). The structure of HS-DPCCH for a single carrier is shown in FIG. 5a.

[0027] Once the NodeB receives this information, it allocates the required channelization codes, modulation and coding, precoding channel index to the UE after scheduling. This information 406 is conveyed to UE by shared control channel (HS-SCCH). Once the UE detects the HS-SCCH, downlink transmission 408 starts through data traffic channel using Physical Downlink Shared Channel (HS-PDSCH).

[0028] For a 4 branch MIMO, the UE transmits, to the base station via the HS-DPCCH, the following information: HARQ ACK information (same structure that of Release-7); CQI (8 bits); RI (i.e., information indicating the number of layers the UE prefers) (2bits); and PCI (Precoding Control Index in the RI) (4 bits). Hence if we compare the structure with respect to Release 7 MIMO, we need to add additional bits for reporting PCI and RI. From a structure that has been proposed, the reporting is shown in FIG. 5B.

[0029] It can be observed from FIG. 5B that the HARQ ACK is transmitted in a first slot (10 bits) as per Release 7 structure. CQI, RI and PCI are transmitted in the 2nd and 3rd slots with 40 bits. A convolutional code of 1/3 code rate with puncturing pattern identifying 26 bits is recommended to encode the 14 CQI/RI/PCI information bits to 40 bits. A puncturing pattern selected per the rules in 3GPP TS 25.212 v10.2.0 results in the following puncturing pattern: [1 3 6 8 11 13 16 18 21 23 26 28 31 34 36 39 41 44 46 49 51 54 56 59 61 64]. This pattern is referred to herein as an "R99" puncturing pattern and is illustrated in FIG. 6. This puncturing pattern is not optimal.

Design Options for Rate Matching

Option1: Convolution code with 1/3 code rate and "end" puncturing

[0030] FIG. 7 shows a puncturing pattern 700 that is rotationally symmetric and uses "end" puncturing, i.e. only beginning bits (e.g., bits 1-21) and ending bits (e.g. bits 46-66) are punctured, but not middle bits. Hence in this method all the bits are equally protected. Puncturing pattern 700 provides better results than the R99 puncturing pattern shown in FIG. 6. FIG. 8 shows the BLER plot for these two patterns. It can be seen that pattern 700 performs better than the R99 puncturing by 0.25 dB. Hence we propose that a convolutional code of rate 1/3 with the puncturing pattern [1 2 3 4 5 6 7 8 9 10 11 12 13 54 55 56 57 58 59 60 61 62 63 64 65 66] should be used, as shown in FIG. 7.

Option2: Convolution code with 1/2 code rate and "end" puncturing

[0031] In this option we use convolutional code with rate $\frac{1}{2}$ and also use end puncturing. FIG. 9 shows an example puncturing pattern 900 according to option 2. As shown in FIG. 9 the puncturing patterns is [1 3 42 44]. Like puncturing pattern 700, puncturing pattern 900 is rotationally symmetric (i.e., for every bit n that is included in the pattern there is also included in the pattern a corresponding bit n' , where $n' = N+1-n$, where N is the length of the bit sequence that is to be punctured, which in this case is 44). For a point of comparison, FIG. 10 shows an R99 puncturing pattern 1000 (i.e., a puncturing pattern using the principles outlined in 3GPP TS 25.212 v10.2.0). Puncturing pattern 1000 is not rotationally symmetric (e.g., bit 1 is included in the pattern, but bit 1's corresponding bit (i.e., bit 44) is not included). FIG. 11 shows the BLER plot for these patterns 900 and 1000. It can be seen that puncturing pattern 900 performs better than the R99 puncturing pattern 1000. Alternative end puncturing patterns for $\frac{1}{2}$ code rate are also contemplated. For example, the following five alternative puncturing patterns provide the same (or nearly the same) result as puncturing pattern 900: (1) [1 2 43 44], (2) [1 4 41 44], (3) [2 3 42 43], (4) [2 4 41 43] and (5) [3 4 41 42]. Like pattern 700, these alternative patterns are also rotationally symmetric.

[0032] Upon a comparison of option 1 and option 2, it can be observed that the best performance is achieved using $\frac{1}{2}$ code rate and using an end puncturing pattern that is rotationally symmetric. See e.g., FIG. 12, which shows the BLER plot for the above described options.

[0033] For the sake of comparison, the simulation results achieved using non symmetric puncturing pattern is compared with simulation results achieved using rotationally symmetric puncturing pattern. FIG. 13 and 14 shows two example non-symmetric puncturing patterns, and FIGs. 15 and 16 show the BLER for these two respective patterns (also plotted are the result with rotationally symmetric end puncturing pattern). From the plots shown in FIG. 15 and 16, it can be argued that a puncturing pattern with rotationally symmetry gives the best performance rather than a puncturing pattern arbitrarily punctured at the beginning and the end of the code sequence. This is because with a rotationally symmetric pattern there is an equal amount of puncturing at both the ends.

[0034] An advantage of at least some of the preferred embodiments discussed herein includes requiring less power for control channel hence more throughputs for UL data traffic.

[0035] Referring now to FIG. 17, FIG. 17 illustrates functional components of UE 106, according to some embodiment. As shown in FIG. 17, UE 106 may include a channel measuring unit 800 for generating control information comprising a first bit sequence, a second bit sequence and a third bit sequence (e.g., CQI, RI, and PCI) to send to the base station serving the UE based on a pilot signal transmitted from the base station. The UE 106 also includes a multiplexer 801 for multiplexing the CQI, RI and PCI bits to produce bit sequence X_1 (14 bits) (i.e., a fourth bit sequence). X_1 is then padded by padder 802 with bit sequence P_1 ($P_1=8$ bits) to produce bit sequence X_1' ($X_1'=22$ bits) (i.e., a fifth bit sequence). X_1' is then encoded by a convolutional encoder 804 to convolutionally encode X_1' to produce encoded bits Z_1 (i.e., a sixth bit sequence). Depending on the rate of the convolutional encoder 804, Z_1 may be 44 or 66, for example. For instance, when the rate is $\frac{1}{2}$, $Z_1=44$ bits and when the rate is $\frac{1}{3}$, then $Z_1=66$ bits. The encoded bits Z_1 are then punctured by a rate matcher 806 according to a pre-defined puncturing pattern to produce bit sequence R_1 (i.e., a seventh bit sequence), where R_1 is 40 bits in length. R_1 is then spread by spreading factor 128, QPSK modulated, and transmitted. Further details are provided below.

[0036] In one embodiment, when the rate is $\frac{1}{2}$, the following puncturing pattern is used by the rate matcher 806: [1 3 42 44]. That is, bits 1, 3, 42 and 44 are removed ("punctured") from Z_1 by rate matcher 806 to produce R_1 .

[0037] In another embodiment, when the rate is $\frac{1}{2}$ one of the following puncturing patterns is used by the rate matcher 806: [1 2 43 44], [1 4 41 44], [2 3 42 43], [2 4 41 43] or [3 4 41 42].

[0038] In yet another embodiment, when the rate is $\frac{1}{3}$ and, the following puncturing pattern is used by the rate matcher 806: [1 2 3 4 5 6 7 8 9 10 11 12 13 54 55 56 57 58 59 60 61 62 63 64 65 66].

[0039] Referring now to FIG. 18, FIG. 18 is a flow chart illustrating a process 1800 according to some embodiments, which process may be performed by UE 106. Process 1800 may begin in step 1802, where UE 106 receives a pilot signal.

[0040] In step 1804, the UE uses pilot signal to generate CQI, PCI and RI bits (i.e. three bit sequences).

[0041] In step 1806, the CQI, PCI and RI bits are arranged to produce a bit sequence X1, i.e., a fourth bit sequence, (in some embodiments X1 is fourteen bits). In some embodiments, the first portion of X1 (e.g., the first 8 bits of X1) identify a CQI, the next portion of X1 (e.g., the next 2 bits) identify an RI, and the last portion of X1 (e.g., the next four bits of X1) identify a PCI.

[0042] Next (step 1808), X1 is padded with bit sequence P1 (in some embodiments P1 is eight bits in length) to produce bit sequence X1' (i.e., a fifth bit sequence).

[0043] Next (step 1810) bit sequence X1' is convolution encoded to produce encoded bit sequence Z1 (i.e., a sixth bit sequence). Depending on the length of X1' and on the rate of the convolutional encoder, Z1 may be, for example, 44 or 66 bits, for example. For instance, when X1' is 22 bits and the rate is $\frac{1}{2}$, then Z1=44bits and when X1' is 22 bits and the rate is $\frac{1}{3}$, then Z1=66bits.

[0044] Next (step 1812) the encoded bits Z1 are then punctured by a rate matcher using a predefined rotationally symmetric puncturing pattern to produce bit sequence RI (i.e., a seventh bit sequence) (in some embodiments Z1 is punctured such that RI is 40 bits in length).

[0045] RI is then spread (e.g., by spreading factor 188), modulated (e.g., QPSK modulated), and transmitted (step 1816).

[0046] While various embodiments have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of this disclosure should not be limited by any of the above-described exemplary embodiments. Moreover, any combination of the above-described elements in all possible variations thereof is encompassed by the disclosure unless otherwise indicated herein or otherwise clearly contradicted by context.

[0047] Additionally, while the processes described above and illustrated in the drawings are shown as a sequence of steps, this was done solely for the sake of illustration. Accordingly, it is contemplated that some steps may be added, some steps may be omitted, the order of the steps may be re-arranged, and some steps may be performed in parallel.

Claims

1. A method for encoding control information generated by a user equipment, UE (106a,106b), the control information comprising a first bit sequence, a second bit sequence, and a third bit sequence, the method comprising:

arranging (1806) said bit sequences to produce a bit sequence X1;
padding (1808) the bit sequence X1 with a bit sequence P1 to produce a bit sequence X1';
convolution (1810) encoding the bit sequence X1' to produce an encoded bit sequence Z1 ; and
puncturing (1812) the bit sequence Z1 using a predefined puncturing pattern (700, 900) to produce a bit sequence R1, wherein
convolution encoding the bit sequence X1' to produce the encoded bit sequence Z1
comprises convolution encoding the bit sequence X1' using rate 1/2 convolutional encoding,
the bit sequence X1 consists of fourteen bits,
the bit sequence P1 consists of eight bits,
the bit sequence Z1 consists of 44 bits, and
the predefined puncturing pattern is [1 3 42 and 44].

2. The method of any of claim 1, wherein
the first bit sequence is a channel quality indicator, CQI, value;
the second bit sequence is a precoding control indicator, PCI, value.

3. The method of claim 2, wherein the third bit sequence is a value identifying a preferred number of layers.

4. A user equipment, UE, (106a,106b) adapted to:

generate control information, the control information comprising a first bit sequence, a second bit sequence, and a third bit sequence;
arrange said bit sequences to produce a bit sequence X1;
pad the bit sequence X1 with a bit sequence P1 to produce a bit sequence X1';
convolution encode the bit sequence X1' to produce an encoded bit sequence Z1; and
puncture bit sequence Z1 using a predefined puncturing pattern (700, 900) to produce a bit sequence R1, wherein the UE is adapted to convolution encode the bit sequence X1' to produce the encoded bit sequence Z1 by convolution encoding the bit sequence X1' using rate 1/2 convolutional encoding,

the bit sequence X1 consists of fourteen bits,
the bit sequence P1 consists of eight bits,
the bit sequence Z1 consists of 44 bits, and
the predefined puncturing pattern is [1 3 42 and 44].

- 5 5. The UE of claim 4, wherein
the first bit sequence is a channel quality indicator, CQI, value;
the second bit sequence is a precoding control indicator, PCI, value.
- 10 6. The UE of claim 5, wherein the third bit sequence is value identifying a preferred number of layers.

Patentansprüche

- 15 1. Verfahren zum Codieren von durch eine Benutzereinrichtung, UE (106a, 106b), erzeugten Steuerinformationen, wobei die Steuerinformationen eine erste Bitfolge, eine zweite Bitfolge und eine dritte Bitfolge umfassen, wobei das Verfahren Folgendes umfasst:

Anordnen (1806) der Bitfolgen zum Herstellen einer Bitfolge X1;
20 Auffüllen (1808) der Bitfolge X1 mit einer Bitfolge P1 zum Herstellen einer Bitfolge X1';
Faltungscodieren (1810) der Bitfolge X1' zum Herstellen einer codierten Bitfolge Z1; und
Punktieren (1812) der Bitfolge Z1 unter Verwendung eines vordefinierten Punktierungsmusters (700, 900) zum
Herstellen einer Bitfolge R1, wobei
Faltungscodieren der Bitfolge X1' zum Herstellen der codierten Bitfolge Z1 ein Faltungscodieren der Bitfolge
25 X1' unter Verwendung von Faltungscodieren mit einer Rate von 1/2 umfasst,
die Bitfolge X1 aus vierzehn Bits besteht,
die Bitfolge P1 aus acht Bits besteht,
die Bitfolge Z1 aus 44 Bits besteht, und
das vordefinierte Punktierungsmuster [1 3 42 und 44] ist.

- 30 2. Verfahren nach einem von Anspruch 1, wobei
die erste Bitfolge ein Wert für einen Kanalqualitätsindikator, CQI, ist;
die zweite Bitfolge ein Wert für einen Vorcodierungssteuerungsindikator, PCI, ist.
- 35 3. Verfahren nach Anspruch 2, wobei die dritte Bitfolge ein Wert ist, der eine bevorzugte Anzahl von Schichten angibt.
4. Benutzereinrichtung, UE, (106a, 106b), die zu Folgendem angepasst ist:

Erzeugen von Steuerinformationen, wobei die Steuerinformationen eine erste Bitfolge, eine zweite Bitfolge und
40 eine dritte Bitfolge umfassen;
Anordnen der Bitfolgen zum Herstellen einer Bitfolge X1;
Auffüllen der Bitfolge X1 mit einer Bitfolge P1 zum Herstellen einer Bitfolge X1';
Faltungscodieren der Bitfolge X1' zum Herstellen einer codierten Bitfolge Z1; und
Punktieren der Bitfolge Z1 unter Verwendung eines vordefinierten Punktierungsmusters (700, 900) zum Her-
45 stellen einer Bitfolge R1, wobei
die UE zum Faltungscodieren der Bitfolge X1' zum Herstellen der codierten Bitfolge Z1 angepasst ist, indem
sie die Bitfolge X1' unter Verwendung von Faltungscodieren mit einer Rate von 1/2 faltungscodiert,
die Bitfolge X1 aus vierzehn Bits besteht,
die Bitfolge P1 aus acht Bits besteht,
50 die Bitfolge Z1 aus 44 Bits besteht, und
das vordefinierte Punktierungsmuster [1 3 42 und 44] ist.

5. UE nach Anspruch 4, wobei
die erste Bitfolge ein Wert für einen Kanalqualitätsindikator, CQI, ist;
55 die zweite Bitfolge ein Wert für einen Vorcodierungssteuerungsindikator, PCI, ist.
6. UE nach Anspruch 5, wobei die dritte Bitfolge ein Wert ist, der eine bevorzugte Anzahl von Schichten angibt.

Revendications

1. Procédé pour coder des informations de commande générées par un équipement d'utilisateur, UE (106a, 106b), les informations de commande comprenant une première séquence de bits, une deuxième séquence de bits et une troisième séquence de bits, le procédé comprenant :

l'agencement (1806) desdites séquences de bits pour produire une séquence de bits X1 ;
 le remplissage (1808) de la séquence de bits X1 avec une séquence de bits P1 pour produire une séquence de bits X1' ;
 le codage par convolution (1810) de la séquence de bits X1' pour produire une séquence de bits codée Z1 ; et
 le poinçonnage (1812) de la séquence de bits Z1 utilisant un motif de poinçonnage prédéfini (700, 900) pour produire une séquence de bits R1, dans lequel
 le codage par convolution de la séquence de bits X1' pour produire la séquence de bits codée Z1 comprend un codage par convolution de la séquence de bits X1' utilisant un codage convolutionnel de rendement 1/2,
 la séquence de bits X1 est constituée de quatorze bits,
 la séquence de bits P1 est constituée de huit bits,
 la séquence de bits Z1 est constituée de 44 bits, et
 le motif de poinçonnage prédéfini est [1 3 42 et 44].

2. Procédé selon l'une quelconque de la revendication 1, dans lequel
 la première séquence de bits est une valeur d'indicateur de qualité de canal, CQI ;
 la deuxième séquence de bits est une valeur d'indicateur de commande de précodage, PCI.
3. Procédé selon la revendication 2, dans lequel la troisième séquence de bits est une valeur identifiant un nombre préféré de couches.
4. Équipement d'utilisateur, UE, (106a, 106b) adapté pour :

générer des informations de commande, les informations de commande comprenant une première séquence de bits, une deuxième séquence de bits et une troisième séquence de bits,
 agencer lesdites séquences de bits pour produire une séquence de bits X1 ;
 remplir la séquence de bits X1 avec une séquence de bits P1 pour produire une séquence de bits X1' ;
 coder par convolution la séquence de bits X1' pour produire une séquence de bits codée Z1 ; et
 poinçonner la séquence de bits Z1 en utilisant un motif de poinçonnage prédéfini (700, 900) pour produire une séquence de bits R1, dans lequel
 l'UE est adapté pour coder par convolution la séquence de bits X1' pour produire la séquence de bits codée Z1 en codant par convolution la séquence de bits X1' en utilisant un codage par convolution de rendement 1/2,
 la séquence de bits X1 est constituée de quatorze bits,
 la séquence de bits P1 est constituée de huit bits,
 la séquence de bits Z1 est constituée de 44 bits, et
 le motif de poinçonnage prédéfini est [1 3 42 et 44].

5. UE selon la revendication 4, dans lequel
 la première séquence de bits est une valeur d'indicateur de qualité de canal, CQI ;
 la deuxième séquence de bits est une valeur d'indicateur de commande de précodage, PCI.
6. UE selon la revendication 5, dans lequel la troisième séquence de bits est une valeur identifiant un nombre préféré de couches.

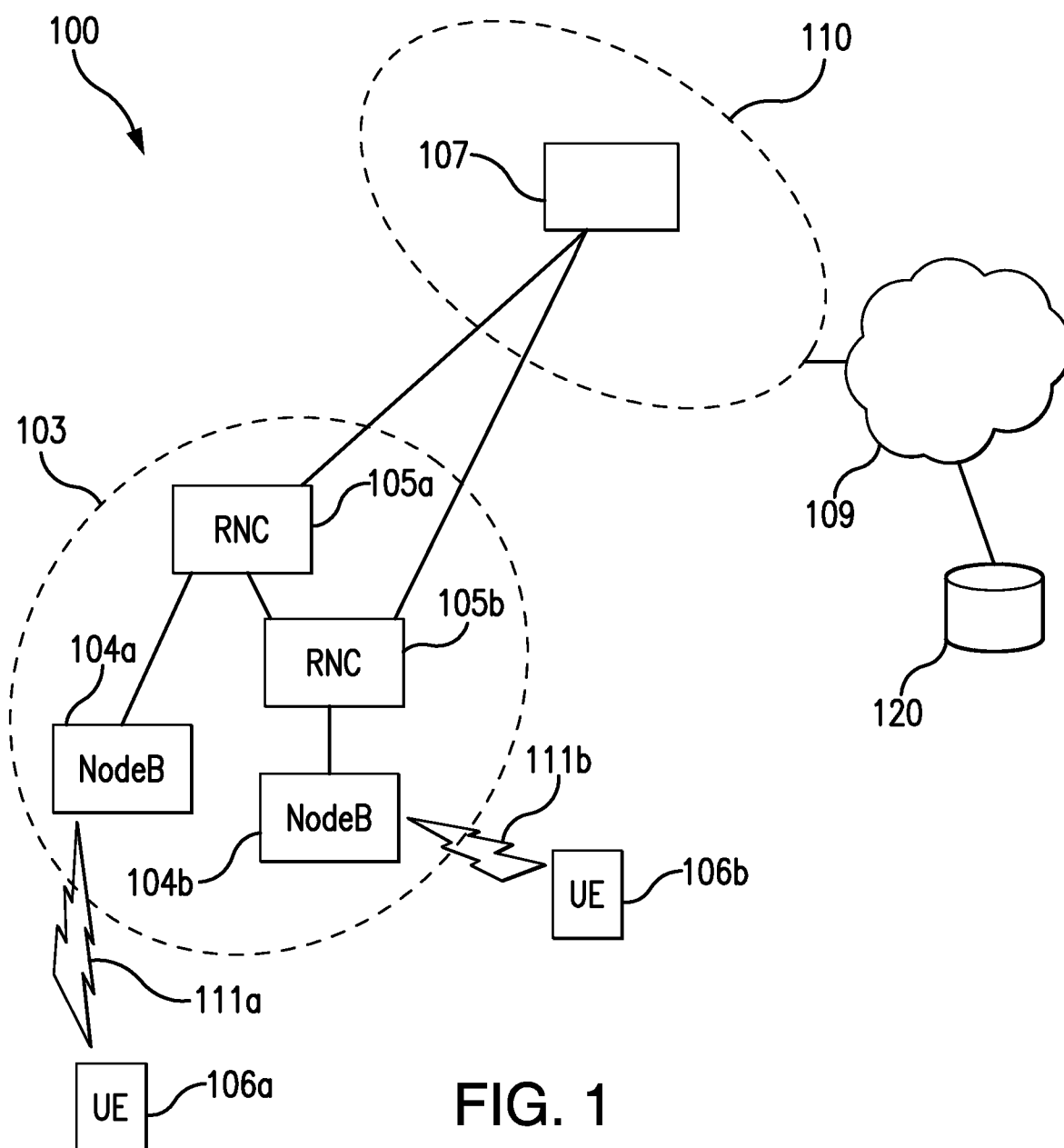


FIG. 1

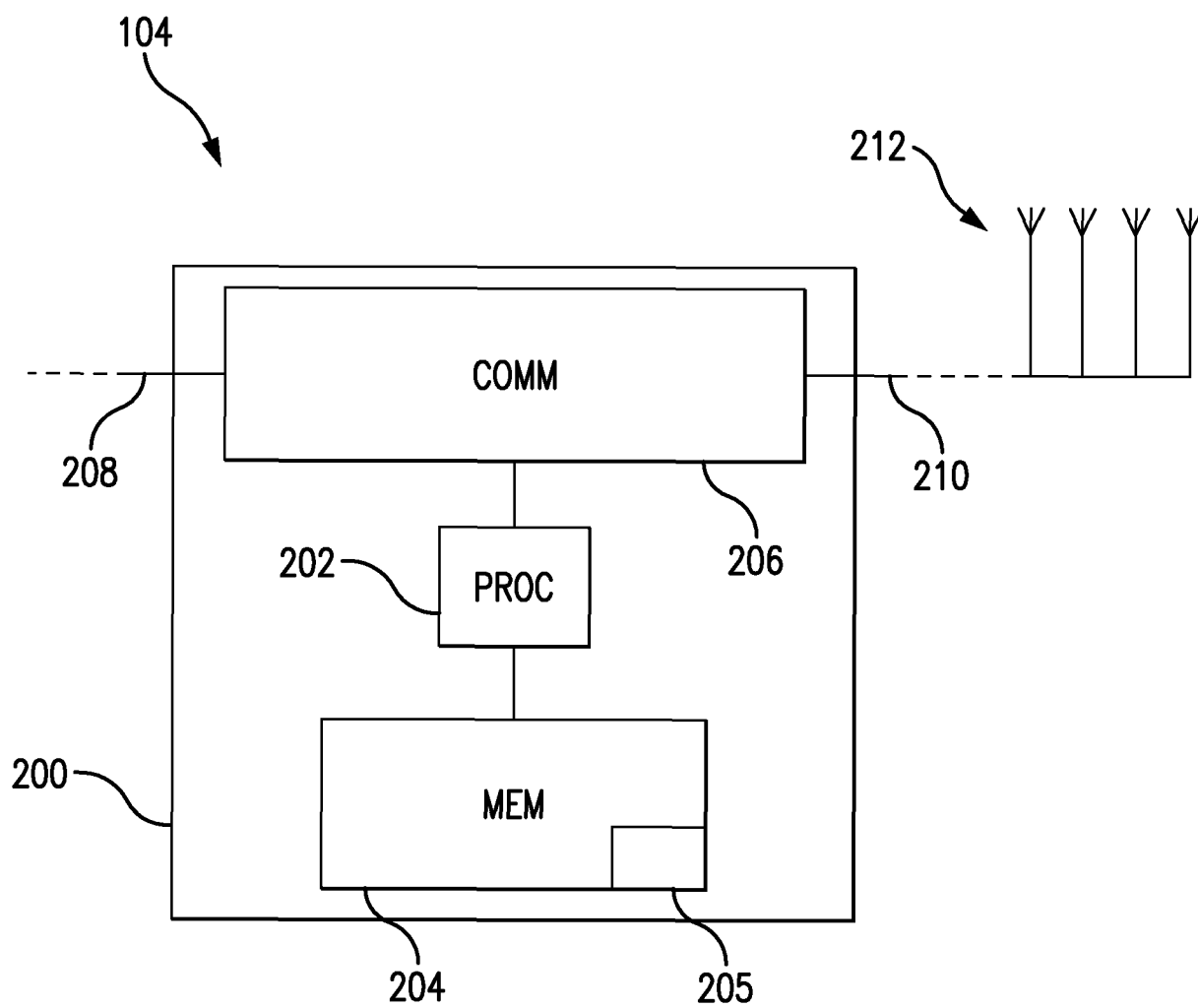


FIG. 2

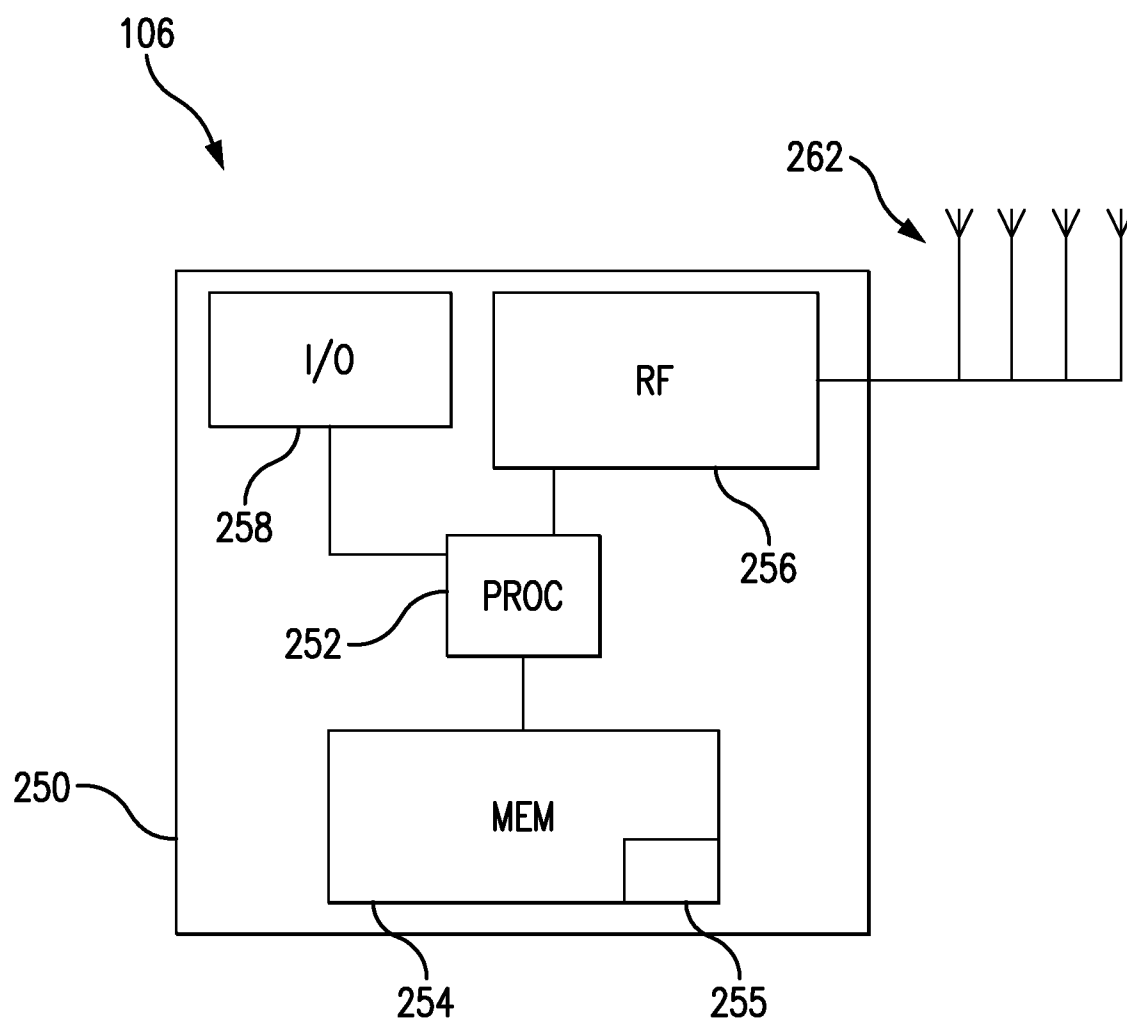


FIG. 3

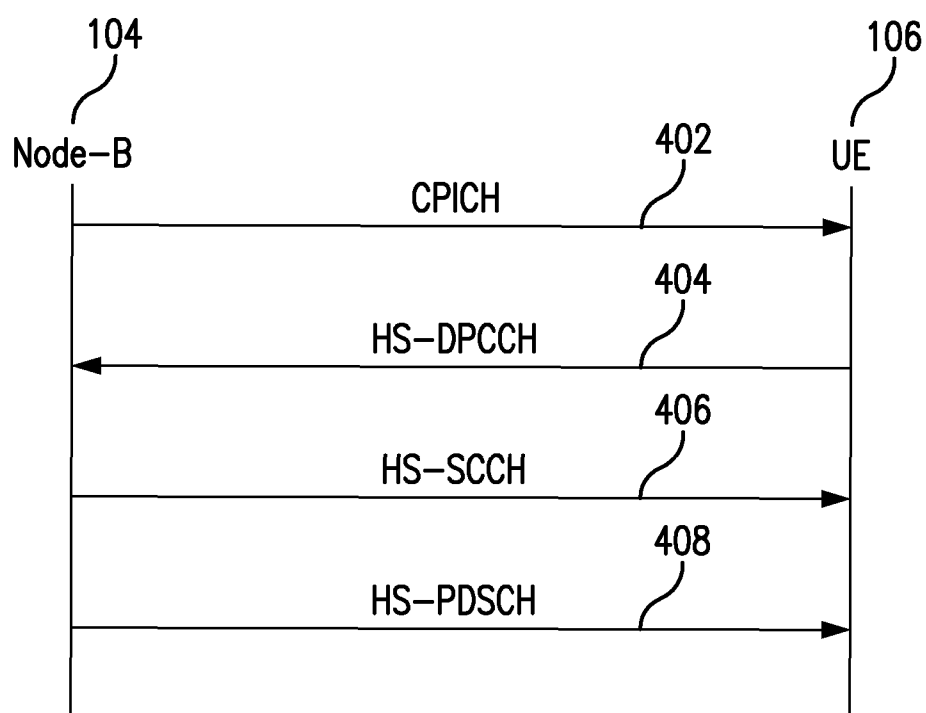


FIG. 4

HARQ ACK	CQI	PCI
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FIG. 5A

HARQ ACK	CQI	RI	PCI
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FIG. 5B

1	4	7	10	13	16	19	22	25	28	31	34	37	40	43	46	49	52	55	58	61	64
2	5	8	11	14	17	20	23	26	29	32	35	38	41	44	47	50	53	56	59	62	65
3	6	9	12	15	18	21	24	27	30	33	36	39	42	45	48	51	54	57	60	63	66

FIG. 6

700

1	4	7	10	13	16	19	22	25	28	31	34	37	40	43	46	49	52	55	58	61	64
2	5	8	11	14	17	20	23	26	29	32	35	38	41	44	47	50	53	56	59	62	65
3	6	9	12	15	18	21	24	27	30	33	36	39	42	45	48	51	54	57	60	63	66

FIG. 7

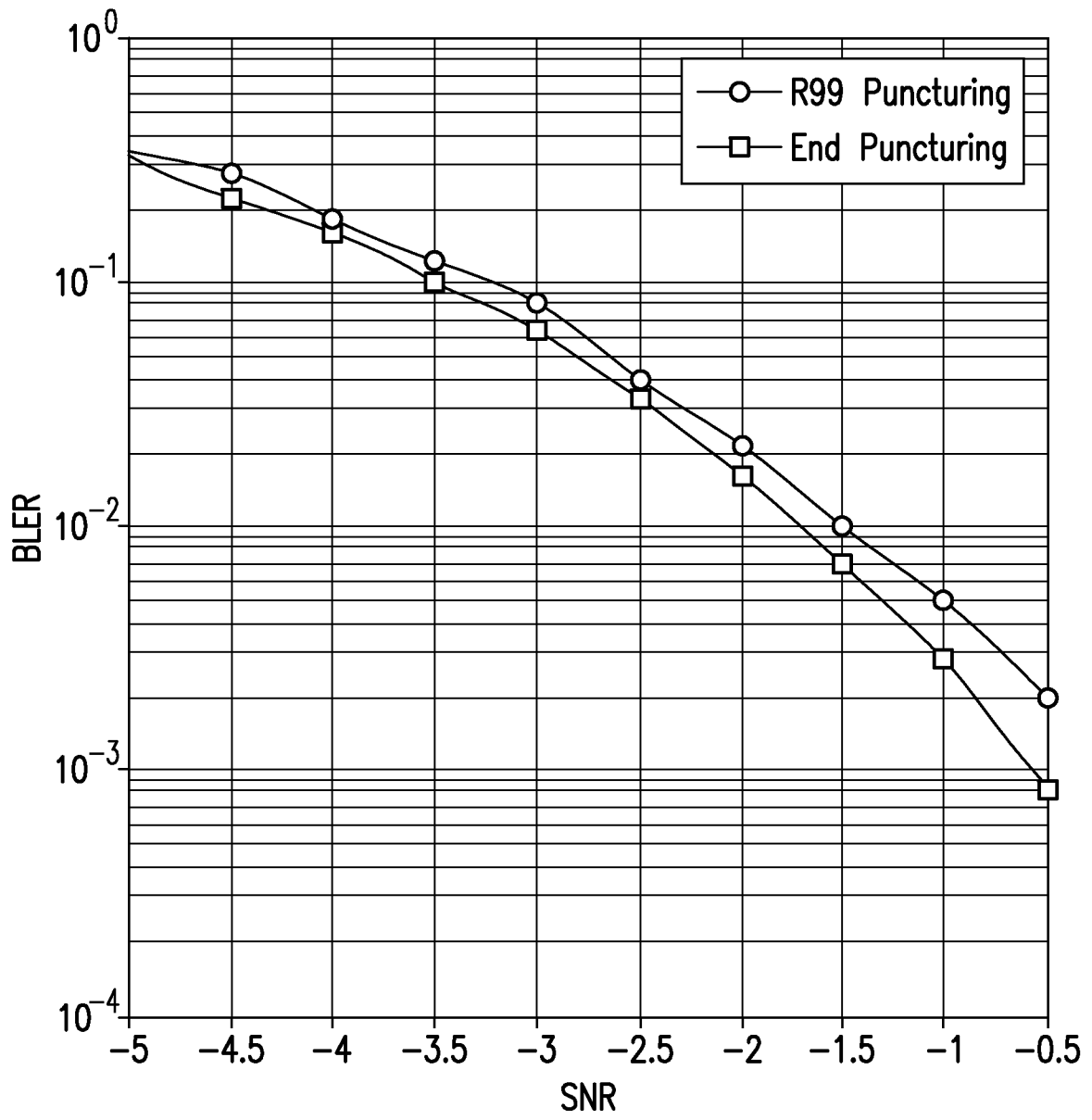


FIG. 8

900



1	5	9	13	17	21	25	29	33	37	41
2	6	10	14	18	22	26	30	34	38	42
3	7	11	15	19	23	27	31	35	39	43
4	8	12	16	20	24	28	32	36	40	44

FIG. 9

1	5	9	13	17	21	25	29	33	37	41
2	6	10	14	18	22	26	30	34	38	42
3	7	11	15	19	23	27	31	35	39	43
4	8	12	16	20	24	28	32	36	40	44

FIG. 10

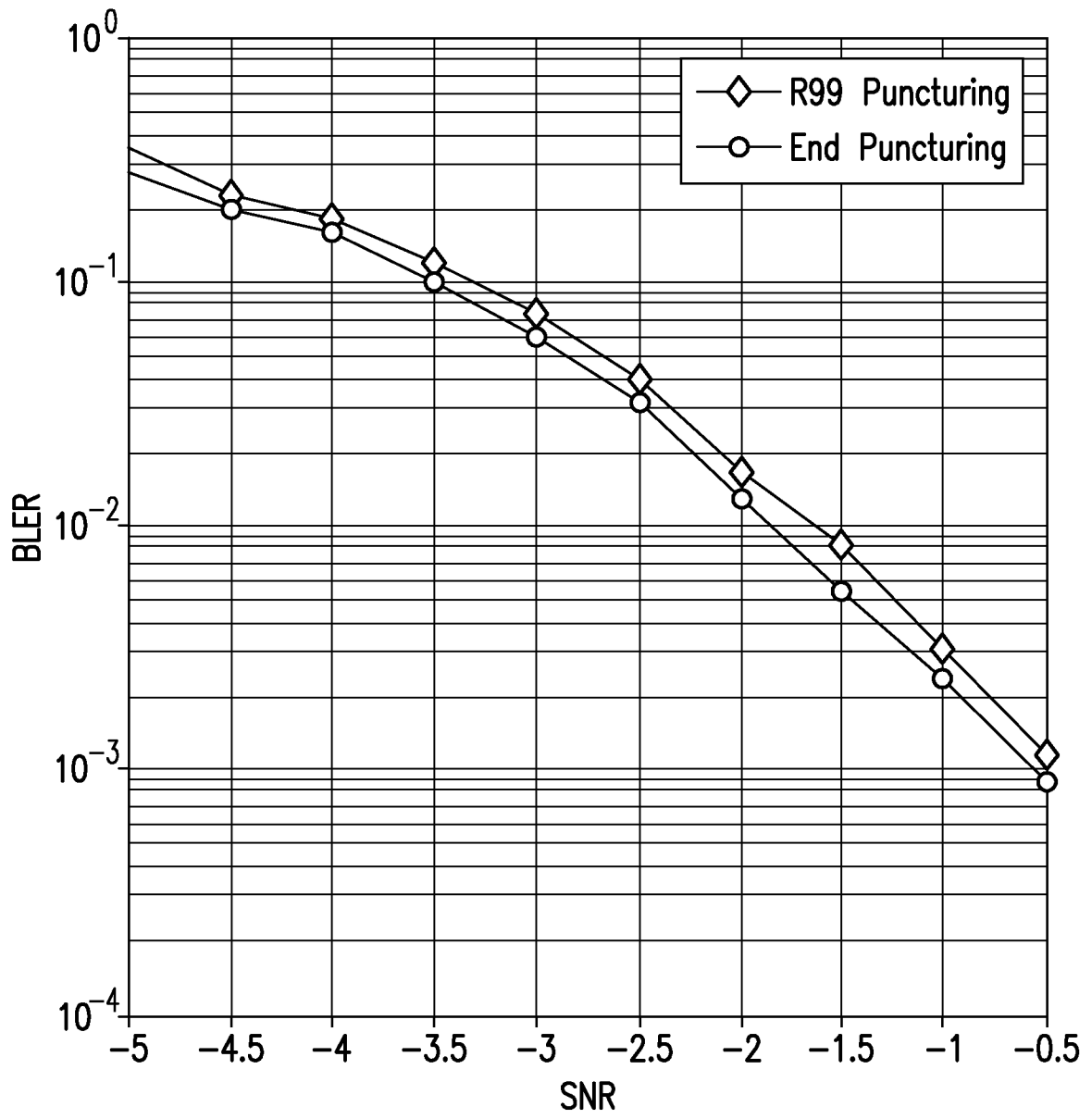


FIG. 11

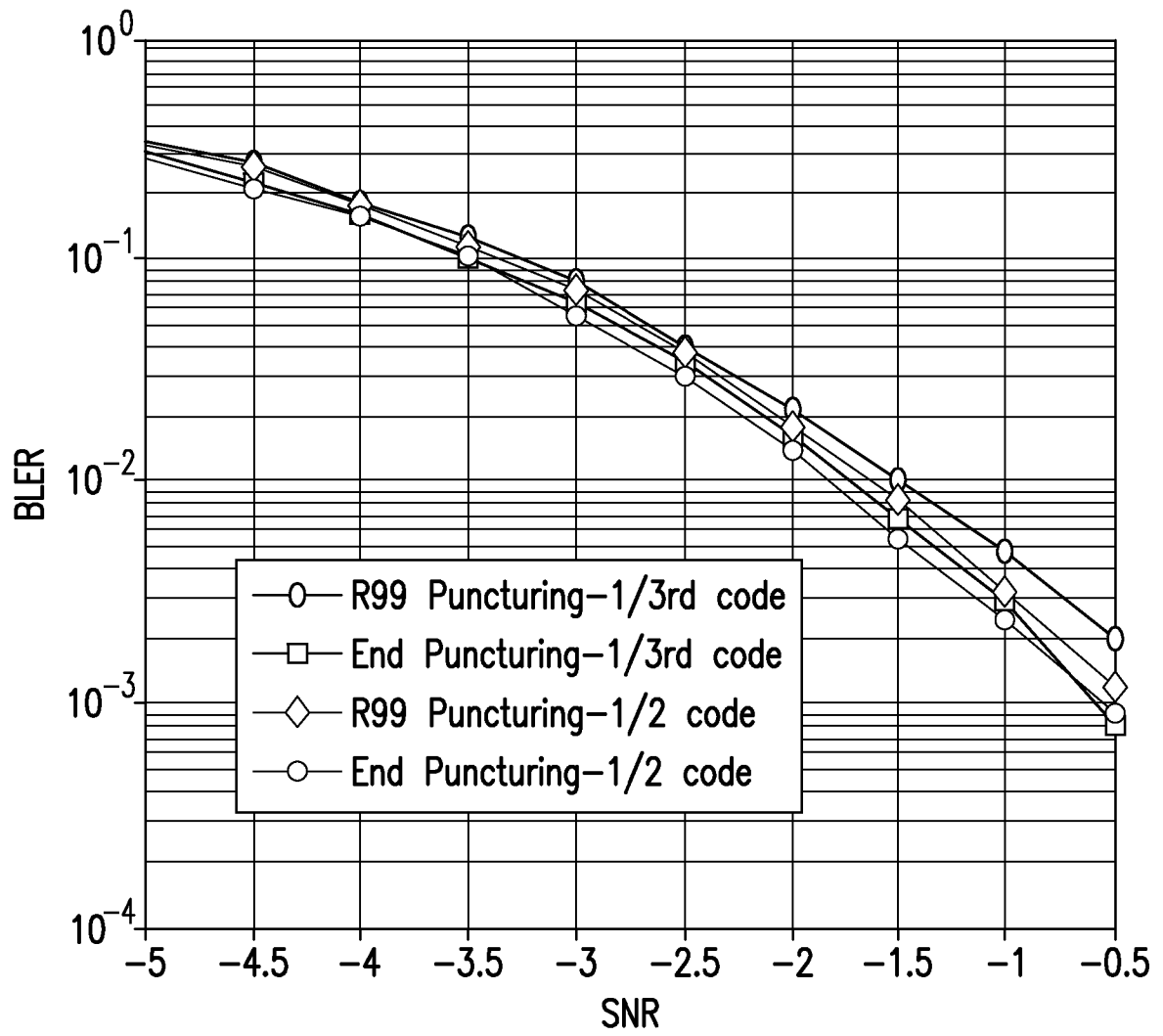


FIG. 12

1	5	9	13	17	21	25	29	33	37	41
2	6	10	14	18	22	26	30	34	38	42
3	7	11	15	19	23	27	31	35	39	43
4	8	12	16	20	24	28	32	36	40	44

FIG. 13

1	5	9	13	17	21	25	29	33	37	41
2	6	10	14	18	22	26	30	34	38	42
3	7	11	15	19	23	27	31	35	39	43
4	8	12	16	20	24	28	32	36	40	44

FIG. 14

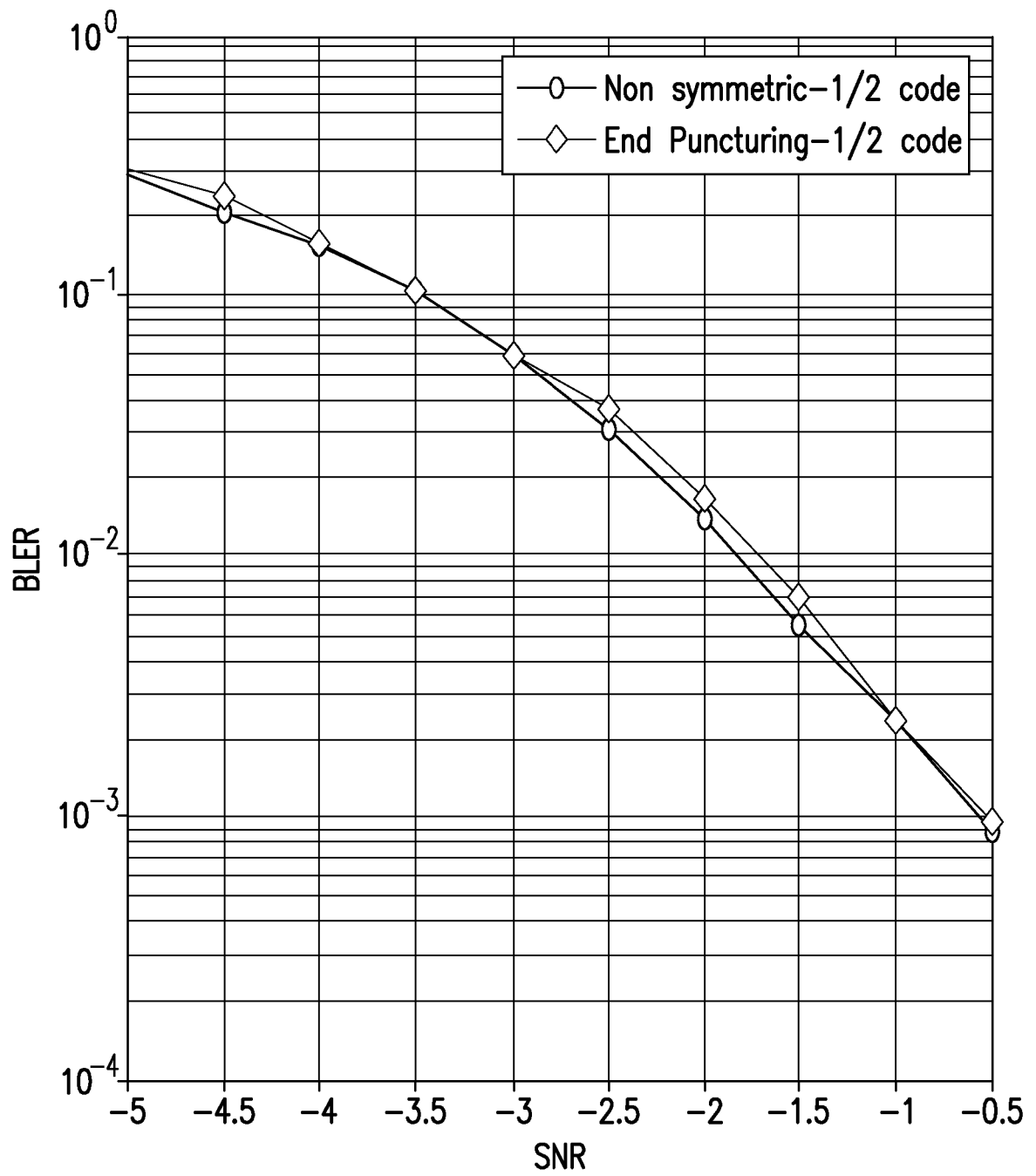


FIG. 15

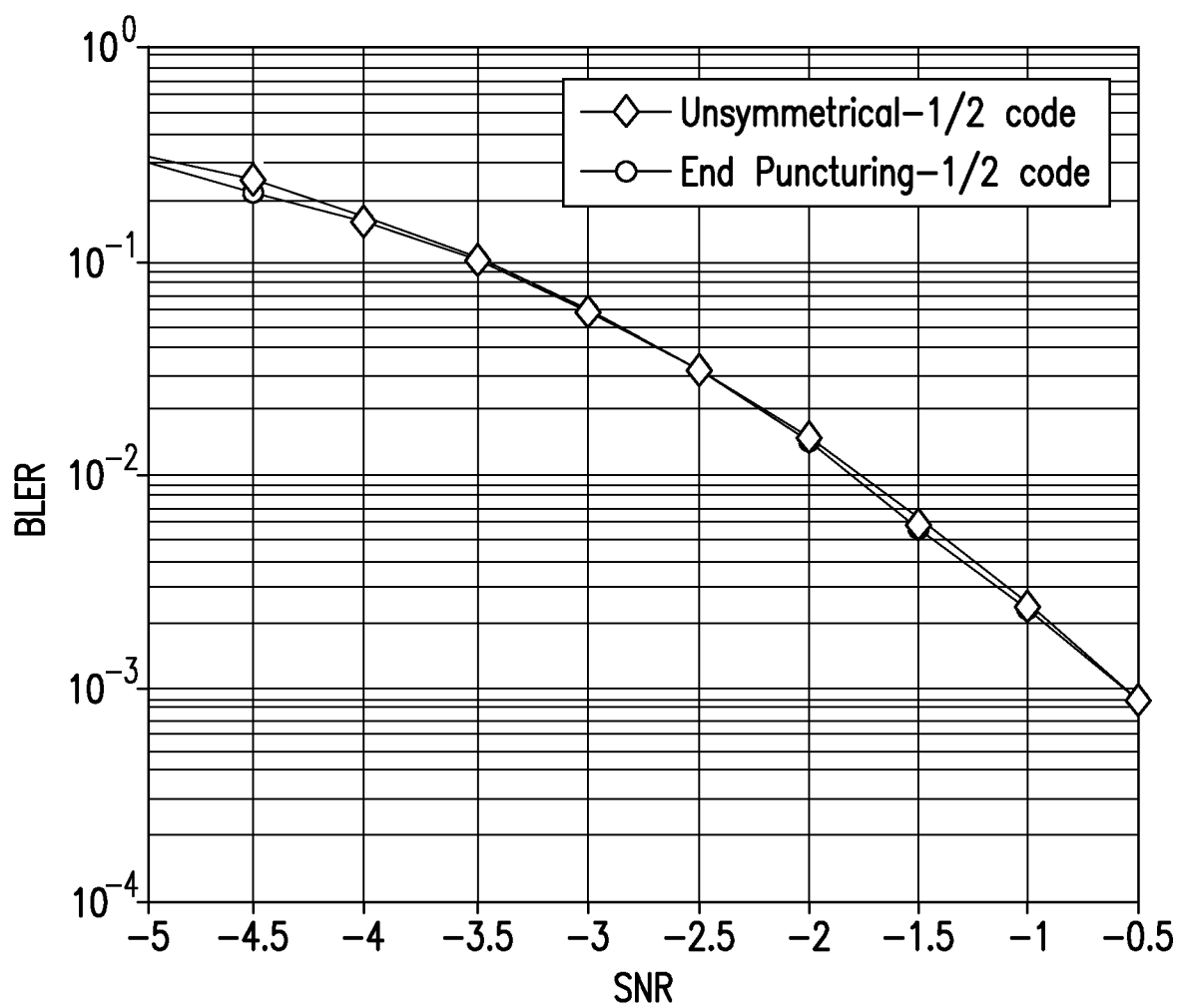


FIG. 16

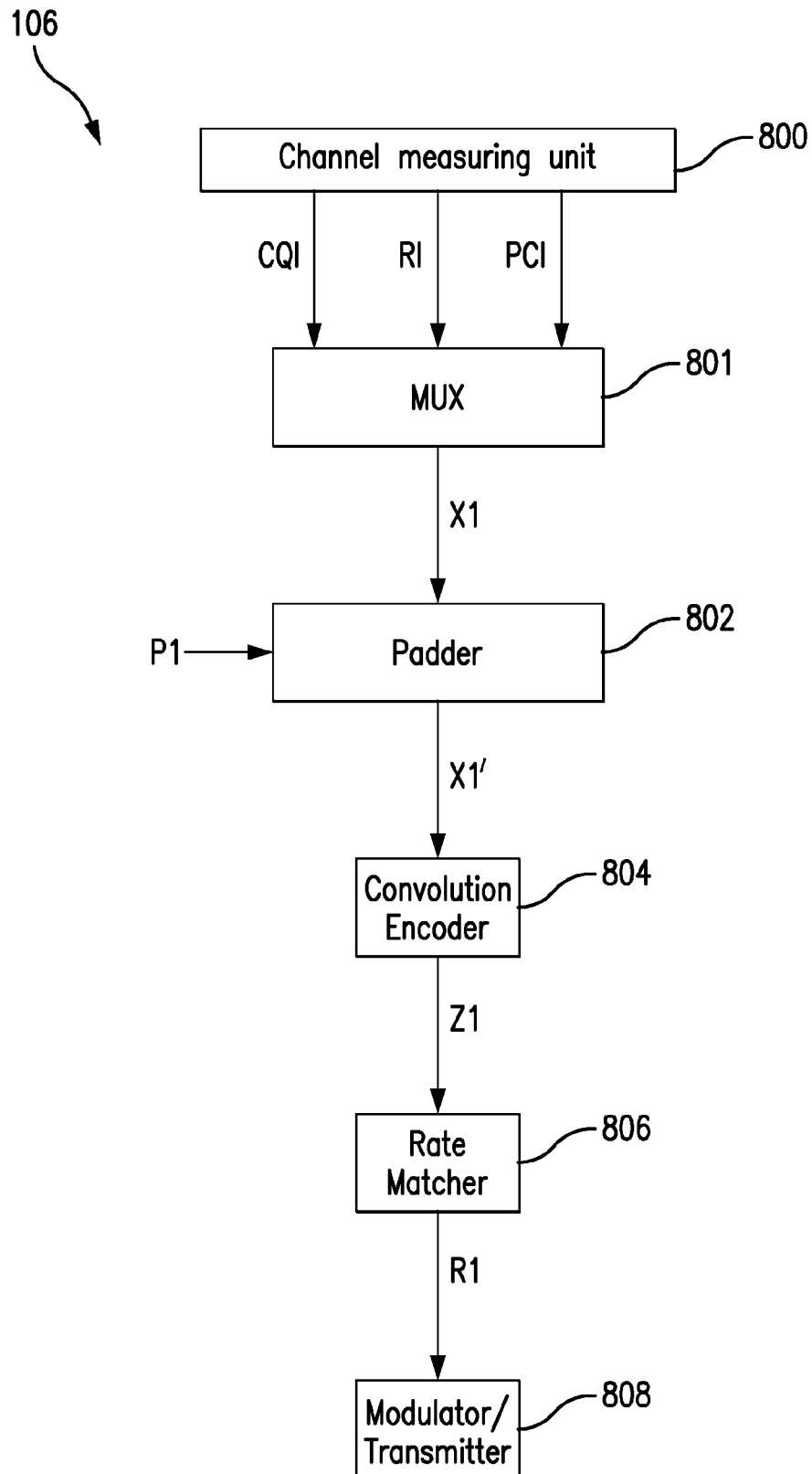


FIG. 17

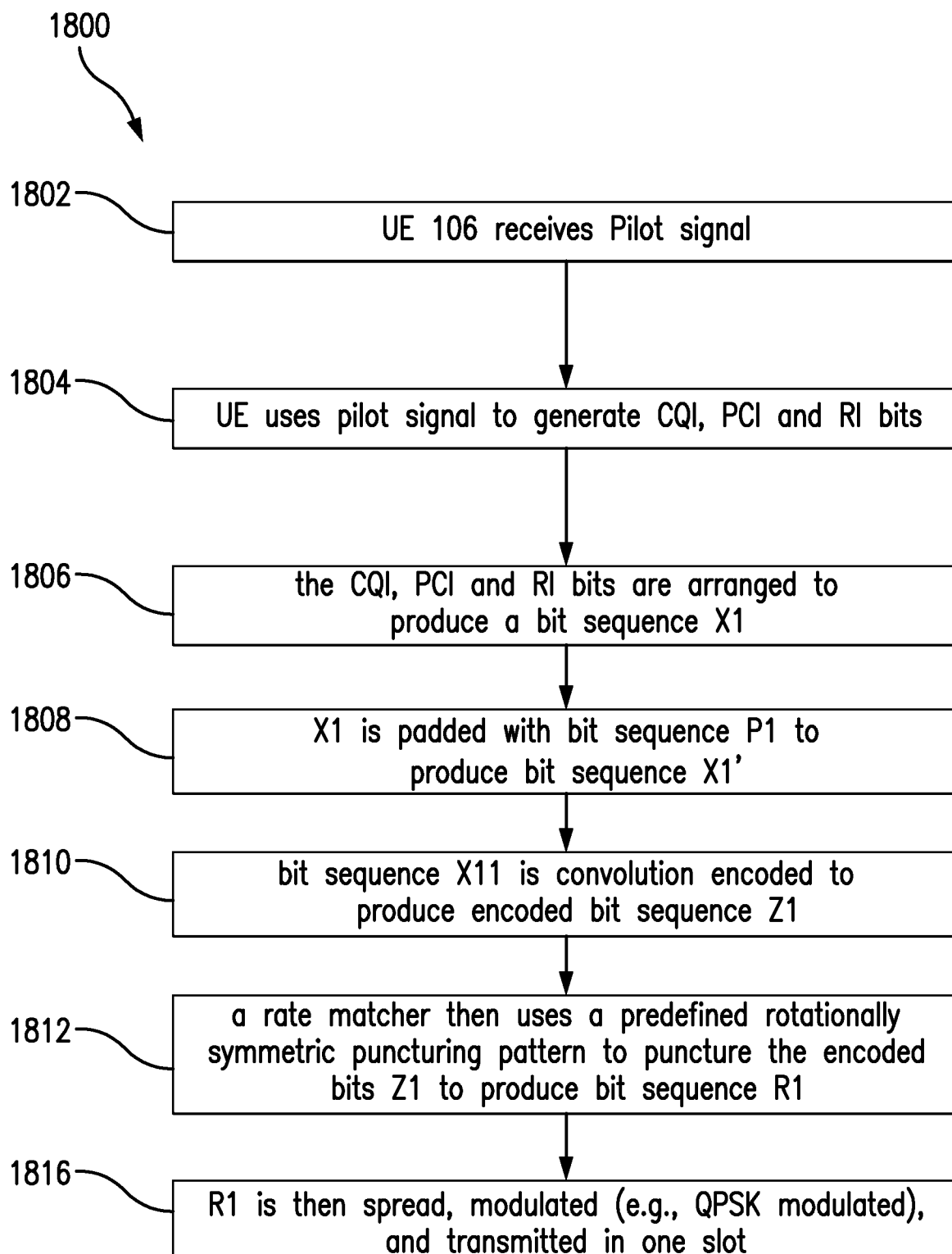


FIG. 18

SZIMMETRIKUS PERFORÁLÁS CQI/PCI JELENTÉSHEZ HS-DPCCH-N

Szabadalmi igénypontok

1. Eljárás UE felhasználói berendezés (106a, 106b) által előállított vezérlési információ kódolására, a vezérlési információ tartalmaz egy első bitsorozatot, egy második bitsorozatot és egy harmadik bitsorozatot, az eljárás a következőket tartalmazza:
 - a bitsorozatok elrendezése (1806) egy X1 bitsorozat előállítására;
 - az X1 bitsorozat kitöltése (1808) P1 bitsorozattal egy X1' bitsorozat előállítására;
 - az X1' bitsorozat csavart (1810) kódolása egy Z1 kódolt bitsorozat előállítására;
 - és
 - a Z1 bitsorozat perforálása (1812) előre meghatározott R1 bitsorozat perforálási minta (700, 900) segítségével egy R1 bitsorozat előállítására, ahol
 - az X1' bitsorozat csavart kódolása egy Z1 kódolt bitsorozat előállítására tartalmazza az X1' bitsorozat csavart kódolását 1/2 csavarásos kódolás segítségével,
 - az X1 bitsorozat tízennégy bitből áll,
 - a P1 bitsorozat nyole bitből áll,
 - a Z1 bitsorozat 44 bitből áll, és
 - az előre meghatározott minta [1 3 42 és 44].
2. Az 1. igénypont szerinti eljárás, ahol:
 - az első bitsorozat egy CQI csatornaminőség jelző érték,
 - a második bitsorozat egy PCI előkódoló vezérlésjelző érték.
3. A 2. igénypont szerinti eljárás, ahol a harmadik bitsorozat előnyben részesített számú réteget azonosító érték,
4. UE felhasználói berendezés (106a, 106b), amelyet a következőkre alkalmaznak:



vezérlési információ előállítása, a vezérlési információ tartalmaz egy első bitsorozatot, egy második bitsorozatot és egy harmadik bitsorozatot;
 a bitsorozatok elrendezése egy $X1$ bitsorozat előállítására;
 az $X1$ bitsorozat kitöltése $P1$ bitsorozattal egy $X1'$ bitsorozat előállítására;
 az $X1'$ bitsorozat csavart kódolása egy $Z1$ kódolt bitsorozat előállítására; és
 a $Z1$ bitsorozat perforálása előre meghatározott $R1$ bitsorozat perforálási minta (700, 900) segítségével egy $R1$ bitsorozat előállítására, ahol
 az UE-t az $X1'$ bitsorozat csavart kódolására alkalmazzák a $Z1$ kódolt bitsorozat előállítására az $X1'$ bitsorozat csavart kódolása által $1/2$ arányú csavarásos kódolás segítségével,
 az $X1$ bitsorozat tizennégy bitből áll,
 a $P1$ bitsorozat nyolc bitből áll,
 a $Z1$ bitsorozat 44 bitből áll, és
 az előre meghatározott minta [1 3 42 és 44].

5. A 4. igénypont szerinti UE, ahol:
 az első bitsorozat egy CQI csatamaminőség jelző érték,
 a második bitsorozat egy PCI előkódoló vezérlésjelző érték.
6. A 5. igénypont szerinti UE, ahol a harmadik bitsorozat előnyben részesített számú réteget azonosító érték.