United States Patent

[54] FLASH MEMORY CELL AND METHOD OF FABRICATING THE SAME

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[56] References Cited
U.S. PATENT DOCUMENTS
4,794,565 12/1988 Wu et al. 257/316
5,382,540 1/1995 Sharma et al. 438/259
5,397,724 3/1995 Nakajima et al. 438/257
5,587,332 12/1996 Chang et al. 257/315

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ABSTRACT
A flash memory cell includes a semiconductor substrate, source and drain regions in the semiconductor substrate, a channel region having first and second channel region between the source and drain regions, a field oxide layer at a field region of the semiconductor substrate, a first gate oxide layer on the semiconductor substrate including the source and rain regions, a floating gate having first and second sides on the first gate oxide layer, a first insulating layer having first and second sides on the floating gate, a control gate having first and second sides on the first insulating layer, a second insulating layer having first and second sides on the control gate, a third insulating layer on the second sides of the second insulating layer including the control gate and the first insulating layer, a fourth insulating layer on the second side of the floating gate and the first sides of the second insulating layer including the control gate and the first insulating layer, a selection gate on the fifth insulating layer, an erase gate on the fourth insulating layer including the third insulating layer, and a lightly-doped region in the semiconductor substrate, the lightly-doped region being partly overlapped with the floating gate.

11 Claims, 4 Drawing Sheets
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FLASH MEMORY CELL AND METHOD OF FABRICATING THE SAME

This application claims the benefit of Korean Patent Application No. 96-75711 filed on Dec. 28, 1996, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, and more particularly, to a flash memory cell and a method of fabricating the same. Although the present invention is suitable for a wide scope of applications, it is particularly suitable for suppressing undesirable leakage current caused by an over-erase.

2. Discussion of the Related Art

Generally, as a nonvolatile memory device, a flash memory cell having a laminated structure including a floating gate and a control gate maintains a high erasing rate by erasing memory array cells concurrently. The programming of the flash memory cell is carried out when hot electrons are injected into the floating gate from the channel by applying high voltage to the control gate. The ratio of the voltage applied to the floating gate to the voltage applied to the control gate is known as a coupling ratio. As the coupling ratio goes higher, the programming efficiency increases.

The erasure of the flash memory cell is achieved when high voltage is applied to a source region having a deep junction and electrons of the floating gate are injected into the source region or a substrate by the mechanism of Fowler-Nordheim tunneling. Generally, to enhance the erasing efficiency, the thickness of a gate oxide layer at the bottom part of the floating gate has to be reduced. However, the thin gate oxide layer may lower the voltage applied to the floating gate and thus reduce the coupling ratio. Therefore, it is required to maintain a higher coupling ratio to enhance the programming and erasure efficiencies without reducing the thickness of the gate oxide layer.

A conventional flash memory cell and a method of fabricating the same will now be explained with reference to FIG. 1.

FIG. 1 is a cross-sectional view of the conventional flash memory cell. As shown in FIG. 1, the conventional flash memory cell includes a semiconductor substrate 11, source and drain regions 24 and 23 in the substrate, a lightly-doped region 25 below the source region, a field oxide layer 13 at a field region of the substrate, a gate oxide layer 15 on the substrate 11 exclusive of a portion on the source and drain regions 24 and 23 and the field oxide layer 13, a floating gate 17 on the gate oxide layer 15, an interlevel insulating layer 19 on the floating gate 17, and a control gate 21 on the interlevel insulating layer.

FIGS. 2A through 2D are cross-sectional views illustrating the process steps for fabricating a conventional flash memory cell.

Referring to FIG. 2A, a field oxide layer 13 for defining an active region of a device is formed on the field region of a P-type substrate 11 using a LOCOS (Local Oxidation of Silicon) process. Then, thermal oxidation is performed on the exposed portion of the substrate 11 to form a gate oxide layer 15. After a polysilicon doped with impurity is deposited on the field oxide layer 13 and the gate oxide layer 15 by CVD (Chemical Vapor Deposition), a floating gate 17 is finally formed by patterning a deposited polysilicon into a stripe shape in a direction parallel to the substrate 11 using photolithography.
To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a method of fabricating a flash memory cell includes the steps of forming a first oxide layer on a substrate of a first conductivity type, forming a floating gate being in a stripe shape in a first direction on the first oxide layer, forming an interlevel insulating layer, a control gate and a cap oxide layer being in a stripe shape in a second direction so as to perpendicularly superpose on the floating gate, and having first and second lateral surfaces, forming a sidewall insulating layer on the second lateral surfaces of the interlevel insulating layer, the control gate and the cap oxide layer, forming a lightly-doped region of a first conductivity type on the substrate on the second lateral surfaces of the control gate and the cap oxide layer, forming a second oxide layer on the first and second lateral surfaces of the floating gate and the control gate, forming a selection gate and an erase gate being in a sidewall form on the first and second lateral surfaces of the floating gate and the control gate, and forming a heavily-doped region of a second conductivity type on the substrate by using the cap oxide layer, the selection gate and the erase gate as a mask.

In another aspect of the present invention, a flash memory cell includes a semiconductor substrate, source and drain regions in the semiconductor substrate, a channel region having first and second channel region between the source and drain regions, a field oxide layer at a field region of the semiconductor substrate, a first oxide layer on the semiconductor substrate including the source and drain regions, a floating gate having first and second sides on the first oxide layer, a first insulating layer having first and second sides on the floating gate, a control gate having first and second sides on the first insulating layer, a second insulating layer having first and second sides on the control gate, a third insulating layer on the second sides of the second insulating layer including the control gate and the first insulating layer, a fourth insulating layer on the second side of the floating gate and the first sides of the second insulating layer including the control gate and the first insulating layer, a selection gate on the fifth insulating layer, an erase gate on the fourth insulating layer including the third insulating layer, and a lightly-doped region in the semiconductor substrate, the lightly-doped region being partly overlapped with the floating gate.

In another aspect of the present invention, a method of fabricating a flash memory cell having a semiconductor substrate, the method includes the steps of forming a field oxide layer at a field region of the semiconductor substrate, forming a first oxide layer on the semiconductor substrate, forming a gate oxide layer on the semiconductor layer, forming a polysilicon layer on an exposed surface over the semiconductor substrate, forming a first insulating layer having first and second sides on the polysilicon layer, forming a control gate having first and second sides on the first insulating layer, forming a second insulating layer having first and second sides on the control gate, forming a third insulating layer on the first and second sides of the first insulating layer, the control gate, and the second insulating layer, forming a first photore sist layer on an exposed surface over the semiconductor substrate, removing a portion of the first photore sist layer to expose portions of the polysilicon layer including a portion of the third insulating layer on the first sides of the first insulating layer, the control gate, and the second insulating layer, removing the portions of the polysilicon layer exposed including the third insulating layer, removing the first photore sist layer, forming a second photore sist layer on an exposed surface over the semiconductor substrate exclusive of the polysilicon layer, removing the polysilicon layer to form a floating gate having first and second sides on the source and drain oxide layer, forming a lightly-doped region on the semiconductor substrate, forming selection gate and erase gate on the fourth insulating layer and the third insulating layer, respectively, and removing the second photore sist layer forming a fourth insulating layer on the first sides of the first insulating layer, the control gate, and the second insulating layer and on the first and second sides of the floating gate, forming source and drain region on the semiconductor substrate.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention:

In the drawings:

FIG. 1 is a cross-sectional view of a conventional flash memory cell.

FIGS. 2A through 2D are cross-sectional views illustrating the process steps for fabricating the conventional flash memory cell.

FIG. 3 is a cross-sectional view of a flash memory cell in accordance with a preferred embodiment of the present invention; and

FIGS. 4A through 4E are cross-sectional views illustrating the process steps for fabricating a flash memory cell in accordance with the preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the preferred embodiment of the present invention, examples of which are illustrated in the accompanying drawings.

Referring to FIG. 3, source and drain regions 57 and 58 are formed in a semiconductor substrate 31. A channel region 63 having first and second channel regions 60 and 62 are formed between the source and drain region 57 and 58.
A field oxide layer 33 is formed at a field region of the substrate 31. A first gate oxide layer 35 is formed on the substrate 31 excluding the field oxide layer 33. A floating gate 37 is formed having first and second sides is formed on the first gate oxide layer 35. An interlevel insulating layer 39 having first and second sides is formed on the floating gate 37. A lightly-doped region 51 is formed at the drain region to have a portion partly overlapping an edge of the floating gate 37.

A control gate 41 having first and second sides is then formed on the interlevel insulating layer 39. A cap oxide layer 43 having first and second sides is formed on the control gate 41. A sidewall insulating layer 45 having a thickness in the range of about 500 to 700 Å is formed on the second sides of the cap oxide layer 43, the control gate 41, and the interlevel insulating layer 39. A second gate oxide layer 52 is formed on the second side of the floating gate 37. PSG (Phosphor Silicate Glass), BSG (Boro Silicate Glass), and BPSG is also formed on the first sides of the floating gate 37, the interlevel insulating layer 39, the control gate 41, and the cap oxide layer 43. A selection gate 53 is formed on the second gate oxide layer on the first side of the floating gate 37. An erase gate 55 is formed on the second gate oxide layer 52 on the second side of the floating gate 37 and the sidewall insulating layer 45.

Referring to FIG. 4A, a field oxide layer 33 for defining active region of the device is formed on the field region of a p-type substrate 31 using a LOCOS process. An exposed portion of the substrate 31 is treated with thermal oxidation so as to form a first gate oxide layer 35 having a thickness of preferably 200 to 500 Å. A polysilicon 37 doped with an impurity for forming a floating gate is then deposited to have a thickness in the range of preferably 3000 to 4000 Å on the field oxide layer 33 and the first gate oxide layer 35 by CVD.

Referring to FIG. 4B, an interlevel insulating layer 39 of an ONO structure having a thickness in the range of preferably 200 to 500 Å is formed on the polysilicon 37. Then, a polysilicon layer doped with an impurity is deposited using CVD to have a thickness in the range of preferably 3000 to 4000 Å on the interlevel insulating layer 39. Subsequently, a silicon oxide layer is deposited using CVD on the polysilicon layer to have a thickness in the range of preferably 3000 to 4000 Å. The polysilicon and the silicon oxide are patterned in a stripe shape using photolithography to define a control gate 41 and a cap oxide layer 43 having first and second sides. Concurrently, the interlevel insulating layer 39 is also patterned in this process.

Subsequently, an insulating material having a etching rate different from the silicon oxide is deposited on the entire surface of the aforementioned structure using CVD. For example, PSG (Phosphor Silicate Glass), BSG (Boro Silicate Glass), and BPSG (Boro-Phosphor-Silicate Glass) can be used in this process. The deposited insulating material is then etched back by means of anisotropic etching, such as reactive ion etching, so as to expose the cap oxide layer 43 and the polysilicon layer 37. After this step, a sidewall insulating layer 45 having a thickness in the range of preferably 500 to 700 Å is formed on the first and second sides of the control gate 41 and the cap oxide layer 43. At this time, the cap oxide layer 43 is not etched because its etching rate is different from the etching rate of the insulating material used in the previous steps.

Referring to FIG. 4C, after depositing a first photore sist 47 on the entire surface of the above-described structure, one side of the polysilicon layer 37 including one of the sidewall insulating layer 45 on the first side of the control gate 41 and the cap oxide layer 43 is exposed by carrying out an exposure and development process on the first photore sist 47. Next, wet etching is performed to remove the exposed sidewall insulating layer 45 on the first sides of the control gate 41 and the cap oxide layer 43 by using the first photore sist 47 as a mask.

As shown in FIG. 4B, the first photore sist 47 is removed. The floating gate 37 is then formed by anisotropic etching the polysilicon layer 37 using the cap oxide layer 43 and a portion of the insulating layer 45 remaining on the second sides of the control gate 41 and the cap oxide layer 43 as masks. After depositing a second photore sist 49 on the entire surface over the substrate 31, the other side of the floating gate 37 is exposed by carrying out an exposure and development process on the second photore sist 49. Then, N-type impurities, such as phosphorus (P) or arsenic (As), are lightly implanted into the substrate to form a region 51. A lightly-doped region 51 is then formed by using the second photore sist 49 as a mask. The lightly-doped region 51 partially overlaps the edge of the floating gate 37.

Referring to FIG. 4E, the second photore sist 49 is removed. Then, oxidation is performed on the exposed first and second sides of the floating gate 37 and the control gate 41 to form a second gate oxide layer 52 having a thickness in the range of preferably 200 to 400 Å. A polysilicon doped with impurity is deposited by CVD on the exposed surfaces and etched back by means of anisotropic etching, such as reactive ion etching. Then, the exposed cap oxide layer 43 and the first gate oxide layer 35. Then, a selection gate 53 and an erase gate 55 are formed on the first and second sides of the floating gate 37 and the control gate 41. The erase gate 55 is formed to overlap the lightly-doped region 51.

Then, source and drain regions 57 and 58 are formed by heavily implanting N-type impurities such as phosphorus (P) or arsenic (As) on an exposed portion of the substrate 31 by using the cap oxide layer 43, the selection gate 53, and the erase gate 55 as masks. A portion of the lightly-doped region 51 that does not overlap the erase gate 55 overlaps the drain region 58. A channel 63 below the floating gate 37 and the selection gate 53 is formed between the source region 57 and the lightly-doped region 51. The channel 63 includes first and second channel regions 60 and 62 controlled by the selection gate 53 and the floating gate 37, respectively.

The flash memory cell according to the present invention includes the selection gate 53 for determining the selection of cells, the control gate 41 for controlling the programming and erasing of the cell, the floating gate 37 for storing electrons in programming, and the erase gate 55 for erasing the cell by tunneling the electrons stored in the floating gate 37 through the second gate oxide layer 52.

The flash memory cell is programmed by a source lateral injection of the hot electrons into the floating gate 37. In other words, after turning on the first channel region 60 by applying a low voltage over a threshold voltage to the selection gate 53, the hot electrons generated in the first channel region 60 are injected into the floating gate 37 when a high voltage is applied to the control gate 41 and the drain region 58. As a result, the cell is programmed. As described above, the source lateral injection of the hot electrons into the floating gate 37 increases the programming speed of the cell and the thick first gate oxide layer 35 improves the coupling effect, so that the programming efficiency of the cell is improved.
Contrary to the programming, the cell is erased when the electrons injected into the floating gate 37 are tunneled through the second gate oxide layer 52 to the erase gate 55 by the Fowler-Nordheim mechanism. In other words, the cell is erased when the control gate 41 and the drain region 58 are applied with a voltage higher than the voltage applied in programming the cell. Thus the electrons injected into the floating gate 37 are tunneled into the second gate oxide layer 52.

If a negative voltage is applied to the selection gate 53 and the control gate 41, the cell can be erased with a relatively low voltage. According to the present invention, the reliability of the first gate oxide layer can be improved due to the tunneling of the electrons injected into the floating gate 37 to the erase gate 55 through the thin second gate oxide layer 52. Further, when the negative voltage is applied to the selection gate 53 and thus turning-off the first channel region 60, the leakage current caused by an over-erasure is greatly suppressed.

It will be apparent to those skilled in the art that various modifications and variations can be made in the method of fabricating a flash memory cell in accordance with the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:
1. A flash memory cell comprising:
   a gate insulating layer formed on a substrate;
   a floating gate, a first insulating layer and a control gate formed on the gate insulating layer, the floating gate and the control gate each having a first side and a second side;
   a first sidewall insulating layer formed on the first side of the control gate;
   a second sidewall insulating layer formed on both the first side and the second side of the floating gate, on the second side of the control gate and on a portion of the first sidewall layer;
   an erase gate formed on the first and the second sidewall insulating layers on the first sides of the floating gate and the control gate;
   a selection gate formed on the second sidewall insulating layer on the second sides of the floating gate and the control gate; and
   a source and drain region formed in the substrate.

2. The flash memory cell according to claim 1, wherein the width of the floating gate is larger than that of the control gate.

3. The flash memory cell according to claim 1, wherein the drain region includes a lightly-doped region that partly overlaps with the floating gate and the erase gate.

4. The flash memory cell according to claim 1, further comprising a lightly-doped drain region formed in the substrate below the erase gate.

5. The flash memory cell according to claim 1, wherein the erase gate and the selection gate are polysilicon layers.

6. The flash memory cell according to claim 1, wherein the first and the second sidewall insulating layers are oxide layers.

7. The flash memory cell according to claim 1, wherein the first and the second sidewall insulating layers are one of the PSG, BSG and BPSG.

8. The flash memory cell according to claim 1, wherein a first side of the second sidewall insulating layer is covered by an upper portion of the first side of the floating gate.

9. The flash memory cell according to claim 1, wherein the floating gate and the control gate each has a thickness in the range of 3000 to 4000 Å.

10. The flash memory cell according to claim 1, wherein the second sidewall insulating layer has a thickness in the range of 200 to 400 Å.

11. The flash memory cell according to claim 1, wherein the first insulating layer includes an oxide/nitride/oxide.
UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,874,759
DATED : February 23, 1999
INVENTOR(S) : Eun-Jeong PARK

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 7, line 37, change “control gate” to --control gate;--.

Column 8, line 2, change “sidewall layer” to --sidewall insulating layer--.

Signed and Sealed this Tenth Day of August, 1999

Attesting Officer

Q. TODD DICKINSON
Acting Commissioner of Patents and Trademarks