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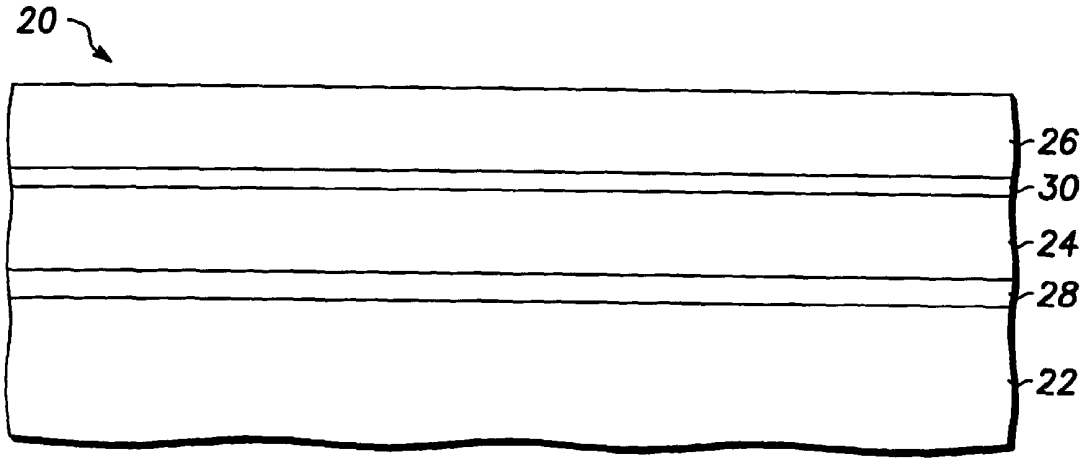

(57) **Abstract:** High quality epitaxial layers of compound semiconductor materials (26) can be grown overlying large silicon wafers (22) by first growing an accommodating buffer layer (24) on a silicon wafer. The accommodating buffer layer is a layer of monocrystalline oxide spaced apart from the silicon wafer by an amorphous interface layer of silicon oxide. The amorphous interface layer (28) dissipates strain and permits the growth of a high quality monocrystalline oxide accommodating buffer layer. Any lattice mismatch between the accommodating buffer layer and the underlying silicon substrate is taken care of by the amorphous interface layer.

WO 02/09186 A2

FIELD EFFECT TRANSISTOR

Field of the Invention

This invention relates generally to compound semiconductor structures and devices and to a method for their fabrication, and more specifically to field effect transistors fabricated at least partially within compound semiconductor structures and to the fabrication and use of semiconductor structures, devices, and integrated circuits that include a monocrystalline compound semiconductor material.

Background of the Invention

The vast majority of semiconductor discrete devices and integrated circuits are fabricated from silicon, at least in part because of the availability of inexpensive, high quality monocrystalline silicon substrates. Other semiconductor materials, such as the so called compound semiconductor materials, have physical attributes, including wider bandgap and/or higher mobility than silicon, or direct bandgaps that make these materials advantageous for certain types of semiconductor devices. Unfortunately, compound semiconductor materials are generally much more expensive than silicon and are not available in large wafers as is silicon. Gallium arsenide (GaAs), the most readily available compound semiconductor material, is available in wafers only up to about 150 millimeters (mm) in diameter. In contrast, silicon wafers are available up to about 300 mm and are widely available at 200 mm. The 150 mm GaAs wafers are many times more expensive than are their silicon counterparts. Wafers of other compound semiconductor materials are even less available and are more expensive than GaAs.

Because of the desirable characteristics of compound semiconductor materials, and because of their present generally high cost and low availability in bulk form, for many years attempts have been made to grow thin films of the compound semiconductor materials on a foreign substrate. To achieve optimal characteristics of the compound semiconductor material, however, a monocrystalline film of high crystalline quality is desired. Attempts have been made, for example, to grow layers of a monocrystalline compound semiconductor material on germanium, silicon, and various insulators. These attempts have generally been unsuccessful because lattice mismatches between the host crystal and the grown crystal have caused the resulting thin film of compound semiconductor material to be of low crystalline quality.

If a large area thin film of high quality monocrystalline compound semiconductor material was available at low cost, a variety of semiconductor devices could advantageously be fabricated in that film at a low cost compared to the cost of fabricating such devices on a bulk wafer of compound semiconductor material or in an epitaxial film of such material on a bulk wafer of compound semiconductor material. In addition, if a thin film of high quality monocrystalline compound semiconductor material could be realized on a bulk wafer such as a silicon wafer, an integrated device structure, including for example field effect transistors (FETs), could be achieved that took advantage of the best properties of both the silicon and the compound semiconductor material.

Accordingly, a need exists for a semiconductor structure that provides a high quality monocrystalline compound semiconductor film over another monocrystalline material and for a process for making such a structure.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIGS. 1 - 3 illustrate schematically, in cross section, device structures in accordance with various embodiments of the invention;

FIG. 4 illustrates graphically the relationship between maximum attainable film thickness and lattice mismatch between a host crystal and a grown crystalline overlayer;

FIG. 5 illustrates a high resolution Transmission Electron Micrograph of a structure including a monocrystalline accommodating buffer layer;

FIG. 6 illustrates an x-ray diffraction spectrum of a structure including a monocrystalline accommodating buffer layer;

FIG. 7 illustrates a high resolution Transmission Electron Micrograph of a structure including an amorphous oxide layer;

FIG. 8 illustrates an x-ray diffraction spectrum of a structure including an amorphous oxide layer;

FIG. 9 illustrates schematically, in cross-section, a semiconductor structure 90 including source and drain electrodes formed on a monocrystalline compound semiconductor layer and a gate electrode formed in a monocrystalline substrate;

FIG. 10 illustrates schematically, in cross-section, a semiconductor structure similar to that in FIG. 9, illustrating impurity doped source and drain regions;

FIG. 11 illustrates schematically, in cross-section, a semiconductor structure including impurity doped source and drain regions and a pair of gates;

FIG. 12 illustrates schematically, in cross-section, impurity doped source and drain regions in a monocrystalline semiconductor substrate, with an accompanying gate formed in a monocrystalline compound semiconductor layer;

FIG. 13 illustrates schematically, in cross-section, a semiconductor structure generally analogous to that shown in FIG. 12, further illustrating spaced apart source and drain electrodes formed in a monocrystalline compound semiconductor layer;

FIGS. 14-18 illustrate schematically, in cross-section, various additional embodiments of FET structures which further include an amorphous silicon oxide layer.

Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description of the Drawings

FIG. 1 illustrates schematically, in cross section, a portion of a semiconductor structure 20 in accordance with an embodiment of the invention. Semiconductor structure 20 includes a monocrystalline substrate 22, accommodating buffer layer 24 comprising a monocrystalline material, and a layer 26 of a monocrystalline compound semiconductor material. In this context, the term "monocrystalline" shall have the meaning commonly used within the semiconductor industry. The term shall refer to materials that are a single crystal or that are substantially a single crystal and shall include those materials having a relatively small number of defects such as dislocations

and the like as are commonly found in substrates of silicon or germanium or mixtures of silicon and germanium and epitaxial layers of such materials commonly found in the semiconductor industry.

In accordance with one embodiment of the invention, structure 20 also includes an amorphous intermediate layer 28 positioned between substrate 22 and accommodating buffer layer 24. Structure 20 may also include a template layer 30 between the accommodating buffer layer and compound semiconductor layer 26. As will be explained more fully below, the template layer helps to initiate the growth of the compound semiconductor layer on the accommodating buffer layer. The amorphous intermediate layer helps to relieve the strain in the accommodating buffer layer and by doing so, aids in the growth of a high crystalline quality accommodating buffer layer.

Substrate 22, in accordance with an embodiment of the invention, is a monocrystalline semiconductor wafer, preferably of large diameter. The wafer can be of a material from Group IV of the periodic table, and preferably a material from Group IVA. Examples of Group IV semiconductor materials include silicon, germanium, mixed silicon and germanium, mixed silicon and carbon, mixed silicon, germanium and carbon, and the like. Preferably substrate 22 is a wafer containing silicon or germanium, and most preferably is a high quality monocrystalline silicon wafer as used in the semiconductor industry. Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material epitaxially grown on the underlying substrate. In accordance with one embodiment of the invention, amorphous intermediate layer 28 is grown on substrate 22 at the interface between substrate 22 and the growing accommodating buffer layer by the oxidation of substrate 22 during the growth of layer 24. The amorphous intermediate layer serves to relieve

strain that might otherwise occur in the monocrystalline accommodating buffer layer as a result of differences in the lattice constants of the substrate and the buffer layer. As used herein, lattice constant refers to the distance between atoms of a cell measured in the plane of the surface. If such strain is not relieved by the amorphous intermediate layer, the strain may cause defects in the crystalline structure of the accommodating buffer layer. Defects in the crystalline structure of the accommodating buffer layer, in turn, would make it difficult to achieve a high quality crystalline structure in monocrystalline compound semiconductor layer 26.

Accommodating buffer layer 24 is preferably a monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying compound semiconductor material. For example, the material could be an oxide or nitride having a lattice structure substantially matched to the substrate and to the subsequently applied semiconductor material. Materials that are suitable for the accommodating buffer layer include metal oxides such as the alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be used for the accommodating buffer layer. Most of these materials are insulators, although strontium ruthenate, for example, is a conductor. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include at least two different

metallic elements. In some specific applications, the metal oxides or nitride may include three or more different metallic elements.

Amorphous interface layer 28 is preferably an oxide formed by the oxidation of the surface of substrate 22, and more preferably is composed of a silicon oxide. The thickness of layer 28 is sufficient to relieve strain attributed to mismatches between the lattice constants of substrate 22 and accommodating buffer layer 24. Typically, layer 28 has a thickness in the range of approximately 0.5-5 nm.

The compound semiconductor material of layer 26 can be selected, as needed for a particular semiconductor structure, from any of the Group IIIA and VA elements (III-V semiconductor compounds), mixed III-V compounds, Group II(A or B) and VIA elements (II-VI semiconductor compounds), and mixed II-VI compounds. Examples include gallium arsenide (GaAs), gallium indium arsenide (GaInAs), gallium aluminum arsenide (GaAlAs), indium phosphide (InP), cadmium sulfide (CdS), cadmium mercury telluride (CdHgTe), zinc selenide (ZnSe), zinc sulfur selenide (ZnSSe), and the like. Suitable template materials chemically bond to the surface of the accommodating buffer layer 24 at selected sites and provide sites for the nucleation of the epitaxial growth of the subsequent compound semiconductor layer 26. Appropriate materials for template 30 are discussed below.

FIG. 2 illustrates, in cross section, a portion of a semiconductor structure 40 in accordance with a further embodiment of the invention. Structure 40 is similar to the previously described semiconductor structure 20, except that an additional buffer layer 32 is positioned between accommodating buffer layer 24 and layer of monocrystalline compound semiconductor material 26. Specifically, the additional buffer layer is positioned

between template layer 30 and the overlying layer of compound semiconductor material. The additional buffer layer, formed of a semiconductor or compound semiconductor material, serves to provide a lattice compensation when the lattice constant of the accommodating buffer layer cannot be adequately matched to the overlying monocrystalline compound semiconductor material layer.

FIG. 3 schematically illustrates, in cross section, a portion of a semiconductor structure 34 in accordance with another exemplary embodiment of the invention. Structure 34 is similar to structure 20, except that structure 34 includes an amorphous layer 36, rather than accommodating buffer layer 24 and amorphous interface layer 28, and an additional semiconductor layer 38.

As explained in greater detail below, amorphous layer 36 may be formed by first forming an accommodating buffer layer and an amorphous interface layer in a similar manner to that described above. Monocrystalline semiconductor layer 38 is then formed (by epitaxial growth) overlying the monocrystalline accommodating buffer layer. The accommodating buffer layer is then exposed to an anneal process to convert the monocrystalline accommodating buffer layer to an amorphous layer. Amorphous layer 36 formed in this manner comprises materials from both the accommodating buffer and interface layers, which amorphous layers may or may not amalgamate. Thus, layer 36 may comprise one or two amorphous layers. Formation of amorphous layer 36 between substrate 22 and semiconductor layer 38 (subsequent to layer 38 formation) relieves stresses between layers 22 and 38 and provides a true compliant substrate for subsequent processing--*e.g.*, compound semiconductor layer 26 formation.

The processes previously described above in connection with FIGS. 1 and 2 are adequate for growing monocrystalline compound semiconductor layers over a

monocrystalline substrate. However, the process described in connection with FIG. 3, which includes transforming a monocrystalline accommodating buffer layer to an amorphous oxide layer, may be better for growing monocrystalline compound semiconductor layers because it allows any strain in layer 26 to relax.

Semiconductor layer 38 may include any of the materials described throughout this application in connection with either of compound semiconductor material layer 26 or additional buffer layer 32. For example, layer 38 may include monocrystalline Group IV or monocrystalline compound semiconductor materials.

In accordance with one embodiment of the present invention, semiconductor layer 38 serves as an anneal cap during layer 36 formation and as a template for subsequent semiconductor layer 26 formation. Accordingly, layer 38 is preferably thick enough to provide a suitable template for layer 26 growth (at least one monolayer) and thin enough to allow layer 38 to form as a substantially defect free monocrystalline semiconductor compound.

In accordance with another embodiment of the invention, semiconductor layer 38 comprises compound semiconductor material (*e.g.*, a material discussed above in connection with compound semiconductor layer 26) that is thick enough to form devices within layer 38. In this case, a semiconductor structure in accordance with the present invention does not include compound semiconductor layer 26. In other words, the semiconductor structure in accordance with this embodiment only includes one compound semiconductor layer disposed above amorphous oxide layer 36.

The following non-limiting, illustrative examples illustrate various combinations of materials useful in structures 20, 40, and 34 in accordance with various alternative embodiments of the invention. These examples

are merely illustrative, and it is not intended that the invention be limited to these illustrative examples.

Example 1

In accordance with one embodiment of the invention, monocrystalline substrate 22 is a silicon substrate oriented in the (100) direction. The silicon substrate can be, for example, a silicon substrate as is commonly used in making complementary metal oxide semiconductor (CMOS) integrated circuits having a diameter of about 200-300 mm. In accordance with this embodiment of the invention, accommodating buffer layer 24 is a monocrystalline layer of $Sr_zBa_{1-z}TiO_3$ where z ranges from 0 to 1 and the amorphous intermediate layer is a layer of silicon oxide (SiO_x) formed at the interface between the silicon substrate and the accommodating buffer layer. The value of z is selected to obtain one or more lattice constants closely matched to corresponding lattice constants of the subsequently formed layer 26. The accommodating buffer layer can have a thickness of about 2 to about 100 nanometers (nm) and preferably has a thickness of about 10 nm. In general, it is desired to have an accommodating buffer layer thick enough to isolate the compound semiconductor layer from the substrate to obtain the desired electrical and optical properties. Layers thicker than 100 nm usually provide little additional benefit while increasing cost unnecessarily; however, thicker layers may be fabricated if needed. The amorphous intermediate layer of silicon oxide can have a thickness of about 0.5-5 nm, and preferably a thickness of about 1.5-2.5 nm.

In accordance with this embodiment of the invention, compound semiconductor material layer 26 is a layer of gallium arsenide (GaAs) or aluminum gallium arsenide

(AlGaAs) having a thickness of about 1 nm to about 100 micrometers (μm) and preferably a thickness of about 0.5 μm to 10 μm. The thickness generally depends on the application for which the layer is being prepared. To facilitate the epitaxial growth of the gallium arsenide or aluminum gallium arsenide on the monocrystalline oxide, a template layer is formed by capping the oxide layer. The template layer is preferably 1-10 monolayers of Ti-As, Sr-O-As, Sr-Ga-O, or Sr-Al-O. By way of a preferred example, 1-2 monolayers of Ti-As or Sr-Ga-O have been shown to successfully grow GaAs layers.

Example 2

In accordance with a further embodiment of the invention, monocrystalline substrate 22 is a silicon substrate as described above. The accommodating buffer layer is a monocrystalline oxide of strontium or barium zirconate or hafnate in a cubic or orthorhombic phase with an amorphous intermediate layer of silicon oxide formed at the interface between the silicon substrate and the accommodating buffer layer. The accommodating buffer layer can have a thickness of about 2-100 nm and preferably has a thickness of at least 5 nm to ensure adequate crystalline and surface quality and is formed of a monocrystalline $SrZrO_3$, $BaZrO_3$, $SrHfO_3$, $BaSnO_3$ or $BaHfO_3$. For example, a monocrystalline oxide layer of $BaZrO_3$ can grow at a temperature of about 700 degrees C. The lattice structure of the resulting crystalline oxide exhibits a 45 degree rotation with respect to the substrate silicon lattice structure.

An accommodating buffer layer formed of these zirconate or hafnate materials is suitable for the growth of compound semiconductor materials in the indium

phosphide (InP) system. The compound semiconductor material can be, for example, indium phosphide (InP), indium gallium arsenide (InGaAs), aluminum indium arsenide, (AlInAs), or aluminum gallium indium arsenic phosphide (AlGaInAsP), having a thickness of about 1.0 nm to 10 μm. A suitable template for this structure is 1-10 monolayers of zirconium-arsenic (Zr-As), zirconium-phosphorus (Zr-P), hafnium-arsenic (Hf-As), hafnium-phosphorus (Hf-P), strontium-oxygen-arsenic (Sr-O-As), strontium-oxygen-phosphorus (Sr-O-P), barium-oxygen-arsenic (Ba-O-As), indium-strontium-oxygen (In-Sr-O), or barium-oxygen-phosphorus (Ba-O-P), and preferably 1-2 monolayers of one of these materials. By way of an example, for a barium zirconate accommodating buffer layer, the surface is terminated with 1-2 monolayers of zirconium followed by deposition of 1-2 monolayers of arsenic to form a Zr-As template. A monocrystalline layer of the compound semiconductor material from the indium phosphide system is then grown on the template layer. The resulting lattice structure of the compound semiconductor material exhibits a 45 degree rotation with respect to the accommodating buffer layer lattice structure and a lattice mismatch to (100) InP of less than 2.5%, and preferably less than about 1.0%.

Example 3

In accordance with a further embodiment of the invention, a structure is provided that is suitable for the growth of an epitaxial film of a II-VI material overlying a silicon substrate. The substrate is preferably a silicon wafer as described above. A suitable accommodating buffer layer material is $Sr_xBa_{1-x}TiO_3$, where x ranges from 0 to 1, having a thickness of about 2-100 nm

and preferably a thickness of about 5-15 nm. The II-VI compound semiconductor material can be, for example, zinc selenide (ZnSe) or zinc sulfur selenide (ZnSSe). A suitable template for this material system includes 1-10 monolayers of zinc-oxygen (Zn-O) followed by 1-2 monolayers of an excess of zinc followed by the selenidation of zinc on the surface. Alternatively, a template can be, for example, 1-10 monolayers of strontium-sulfur (Sr-S) followed by the ZnSeS.

Example 4

This embodiment of the invention is an example of structure 40 illustrated in FIG. 2. Substrate 22, monocrystalline oxide layer 24, and monocrystalline compound semiconductor material layer 26 can be similar to those described in example 1. In addition, an additional buffer layer 32 serves to alleviate any strains that might result from a mismatch of the crystal lattice of the accommodating buffer layer and the lattice of the monocrystalline semiconductor material. Buffer layer 32 can be a layer of germanium or a GaAs, an aluminum gallium arsenide (AlGaAs), an indium gallium phosphide (InGaP), an aluminum gallium phosphide (AlGaP), an indium gallium arsenide (InGaAs), an aluminum indium phosphide (AlInP), a gallium arsenide phosphide (GaAsP), or an indium gallium phosphide (InGaP) strain compensated superlattice. In accordance with one aspect of this embodiment, buffer layer 32 includes a $GaAs_xP_{1-x}$ superlattice, wherein the value of x ranges from 0 to 1. In accordance with another aspect, buffer layer 32 includes an $In_yGa_{1-y}P$ superlattice, wherein the value of y ranges from 0 to 1. By varying the value of x or y, as the case may be, the lattice constant is varied from bottom to top across the superlattice to create a match between lattice constants of the underlying

oxide and the overlying compound semiconductor material. The compositions of other materials, such as those listed above, may also be similarly varied to manipulate the lattice constant of layer 32 in a like manner. The superlattice can have a thickness of about 50-500 nm and preferably has a thickness of about 100-200 nm. The template for this structure can be the same of that described in example 1. Alternatively, buffer layer 32 can be a layer of monocrystalline germanium having a thickness of 1-50 nm and preferably having a thickness of about 2-20 nm. In using a germanium buffer layer, a template layer of either germanium-strontium (Ge-Sr) or germanium-titanium (Ge-Ti) having a thickness of about one monolayer can be used as a nucleating site for the subsequent growth of the monocrystalline compound semiconductor material layer. The formation of the oxide layer is capped with either a monolayer of strontium or a monolayer of titanium to act as a nucleating site for the subsequent deposition of the monocrystalline germanium. The monolayer of strontium or titanium provides a nucleating site to which the first monolayer of germanium can bond.

Example 5

This example also illustrates materials useful in a structure 40 as illustrated in FIG. 2. Substrate material 22, accommodating buffer layer 24, monocrystalline compound semiconductor material layer 26 and template layer 30 can be the same as those described above in example 2. In addition, a buffer layer 32 is inserted between the accommodating buffer layer and the overlying monocrystalline compound semiconductor material layer. The buffer layer, a further monocrystalline semiconductor material, can be, for example, a graded layer of indium

gallium arsenide (InGaAs) or indium aluminum arsenide (InAlAs). In accordance with one aspect of this embodiment, buffer layer 32 includes InGaAs, in which the indium composition varies from 0 to about 47%. The buffer layer preferably has a thickness of about 10-30 nm. Varying the composition of the buffer layer from GaAs to InGaAs serves to provide a lattice match between the underlying monocrystalline oxide material and the overlying layer of monocrystalline compound semiconductor material. Such a buffer layer is especially advantageous if there is a lattice mismatch between accommodating buffer layer 24 and monocrystalline compound semiconductor material layer 26.

Example 6

This example provides exemplary materials useful in structure 34, as illustrated in FIG. 3. Substrate material 22, template layer 30, and monocrystalline compound semiconductor material layer 26 may be the same as those described above in connection with example 1.

Amorphous layer 36 is an amorphous oxide layer which is suitably formed of a combination of amorphous intermediate layer materials (e.g., layer 28 materials as described above) and accommodating buffer layer materials (e.g., layer 24 materials as described above). For example, amorphous layer 36 may include a combination of SiO_x and $Sr_zBa_{1-z}TiO_3$ (where z ranges from 0 to 1),which combine or mix, at least partially, during an anneal process to form amorphous oxide layer 36.

The thickness of amorphous layer 36 may vary from application to application and may depend on such factors as desired insulating properties of layer 36, type of semiconductor material comprising layer 26, and the like. In accordance with one exemplary aspect of the present

embodiment, layer 36 thickness is about 2 nm to about 100 nm, preferably about 2-10 nm, and more preferably about 5-6 nm.

Layer 38 comprises a monocrystalline compound semiconductor material that can be grown epitaxially over a monocrystalline oxide material such as material used to form accommodating buffer layer 24. In accordance with one embodiment of the invention, layer 38 includes the same materials as those comprising layer 26. For example, if layer 26 includes GaAs, layer 38 also includes GaAs. However, in accordance with other embodiments of the present invention, layer 38 may include materials different from those used to form layer 26. In accordance with one exemplary embodiment of the invention, layer 38 is about 1 monolayer to about 100 nm thick.

Referring again to FIGS. 1 - 3, substrate 22 is a monocrystalline substrate such as a monocrystalline silicon substrate. The crystalline structure of the monocrystalline substrate is characterized by a lattice constant and by a lattice orientation. In similar manner, accommodating buffer layer 24 is also a monocrystalline material and the lattice of that monocrystalline material is characterized by a lattice constant and a crystal orientation. The lattice constants of the accommodating buffer layer and the monocrystalline substrate must be closely matched or, alternatively, must be such that upon rotation of one crystal orientation with respect to the other crystal orientation, a substantial match in lattice constants is achieved. In this context the terms "substantially equal" and "substantially matched" mean that there is sufficient similarity between the lattice constants to permit the growth of a high quality crystalline layer on the underlying layer.

FIG. 4 illustrates graphically the relationship of the achievable thickness of a grown crystal layer of high

crystalline quality as a function of the mismatch between the lattice constants of the host crystal and the grown crystal. Curve 42 illustrates the boundary of high crystalline quality material. The area to the right of curve 42 represents layers that tend to be polycrystalline. With no lattice mismatch, it is theoretically possible to grow an infinitely thick, high quality epitaxial layer on the host crystal. As the mismatch in lattice constants increases, the thickness of achievable, high quality crystalline layer decreases rapidly. As a reference point, for example, if the lattice constants between the host crystal and the grown layer are mismatched by more than about 2%, monocrystalline epitaxial layers in excess of about 20 nm cannot be achieved.

In accordance with one embodiment of the invention, substrate 22 is a (100) or (111) oriented monocrystalline silicon wafer and accommodating buffer layer 24 is a layer of strontium barium titanate. Substantial matching of lattice constants between these two materials is achieved by rotating the crystal orientation of the titanate material by 45° with respect to the crystal orientation of the silicon substrate wafer. The inclusion in the structure of amorphous interface layer 28, a silicon oxide layer in this example, if it is of sufficient thickness, serves to reduce strain in the titanate monocrystalline layer that might result from any mismatch in the lattice constants of the host silicon wafer and the grown titanate layer. As a result, in accordance with an embodiment of the invention, a high quality, thick, monocrystalline titanate layer is achievable.

Still referring to FIGS. 1 - 3, layer 26 is a layer of epitaxially grown monocrystalline material and that crystalline material is also characterized by a crystal

lattice constant and a crystal orientation. In accordance with one embodiment of the invention, the lattice constant of layer 26 differs from the lattice constant of substrate 22. To achieve high crystalline quality in this epitaxially grown monocrystalline layer, the accommodating buffer layer must be of high crystalline quality. In addition, in order to achieve high crystalline quality in layer 26, substantial matching between the crystal lattice constant of the host crystal, in this case, the monocrystalline accommodating buffer layer, and the grown crystal is desired. With properly selected materials this substantial matching of lattice constants is achieved as a result of rotation of the crystal orientation of the grown crystal with respect to the orientation of the host crystal. If the grown crystal is gallium arsenide, aluminum gallium arsenide, zinc selenide, or zinc sulfur selenide and the accommodating buffer layer is monocrystalline $Sr_xBa_{1-x}TiO_3$, substantial matching of crystal lattice constants of the two materials is achieved, wherein the crystal orientation of the grown layer is rotated by 45° with respect to the orientation of the host monocrystalline oxide. Similarly, if the host material is a strontium or barium zirconate or a strontium or barium hafnate or barium tin oxide and the compound semiconductor layer is indium phosphide or gallium indium arsenide or aluminum indium arsenide, substantial matching of crystal lattice constants can be achieved by rotating the orientation of the grown crystal layer by 45° with respect to the host oxide crystal. In some instances, a crystalline semiconductor buffer layer between the host oxide and the grown compound semiconductor layer can be used to reduce strain in the grown monocrystalline compound semiconductor layer that might result from small differences in lattice constants. Better crystalline

quality in the grown monocrystalline compound semiconductor layer can thereby be achieved.

The following example illustrates a process, in accordance with one embodiment of the invention, for fabricating a semiconductor structure such as the structures depicted in FIGS. 1 - 3. The process starts by providing a monocrystalline semiconductor substrate comprising silicon or germanium. In accordance with a preferred embodiment of the invention, the semiconductor substrate is a silicon wafer having a (100) orientation. The substrate is preferably oriented on axis or, at most, about 0.5° off axis. At least a portion of the semiconductor substrate has a bare surface, although other portions of the substrate, as described below, may encompass other structures. The term "bare" in this context means that the surface in the portion of the substrate has been cleaned to remove any oxides, contaminants, or other foreign material. As is well known, bare silicon is highly reactive and readily forms a native oxide. The term "bare" is intended to encompass such a native oxide. A thin silicon oxide may also be intentionally grown on the semiconductor substrate, although such a grown oxide is not essential to the process in accordance with the invention. In order to epitaxially grow a monocrystalline oxide layer overlying the monocrystalline substrate, the native oxide layer must first be removed to expose the crystalline structure of the underlying substrate. The following process is preferably carried out by molecular beam epitaxy (MBE), although other epitaxial processes may also be used in accordance with the present invention. The native oxide can be removed by first thermally depositing a thin layer of strontium, barium, a combination of strontium and barium, or other alkali earth metals or combinations of

alkali earth metals in an MBE apparatus. In the case where strontium is used, the substrate is then heated to a temperature of about 750° C to cause the strontium to react with the native silicon oxide layer. The strontium serves to reduce the silicon oxide to leave a silicon oxide-free surface. The resultant surface, which exhibits an ordered 2x1 structure, includes strontium, oxygen, and silicon. The ordered 2x1 structure forms a template for the ordered growth of an overlying layer of a monocrystalline oxide. The template provides the necessary chemical and physical properties to nucleate the crystalline growth of an overlying layer.

In accordance with an alternate embodiment of the invention, the native silicon oxide can be converted and the substrate surface can be prepared for the growth of a monocrystalline oxide layer by depositing an alkali earth metal oxide, such as strontium oxide, strontium barium oxide, or barium oxide, onto the substrate surface by MBE at a low temperature and by subsequently heating the structure to a temperature of about 750°C. At this temperature a solid state reaction takes place between the strontium oxide and the native silicon oxide causing the reduction of the native silicon oxide and leaving an ordered 2x1 structure with strontium, oxygen, and silicon remaining on the substrate surface. Again, this forms a template for the subsequent growth of an ordered monocrystalline oxide layer.

Following the removal of the silicon oxide from the surface of the substrate, in accordance with one embodiment of the invention, the substrate is cooled to a temperature in the range of about 200-800°C and a layer of strontium titanate is grown on the template layer by molecular beam epitaxy. The MBE process is initiated by opening shutters in the MBE apparatus to expose strontium,

titanium and oxygen sources. The ratio of strontium and titanium is approximately 1:1. The partial pressure of oxygen is initially set at a minimum value to grow stochiometric strontium titanate at a growth rate of about 0.3-0.5 nm per minute. After initiating growth of the strontium titanate, the partial pressure of oxygen is increased above the initial minimum value. The overpressure of oxygen causes the growth of an amorphous silicon oxide layer at the interface between the underlying substrate and the growing strontium titanate layer. The growth of the silicon oxide layer results from the diffusion of oxygen through the growing strontium titanate layer to the interface where the oxygen reacts with silicon at the surface of the underlying substrate. The strontium titanate grows as an ordered monocrystal with the crystalline orientation rotated by 45° with respect to the ordered 2x1 crystalline structure of the underlying substrate. Strain that otherwise might exist in the strontium titanate layer because of the small mismatch in lattice constant between the silicon substrate and the growing crystal is relieved in the amorphous silicon oxide intermediate layer.

After the strontium titanate layer has been grown to the desired thickness, the monocrystalline strontium titanate is capped by a template layer that is conducive to the subsequent growth of an epitaxial layer of a desired compound semiconductor material. For the subsequent growth of a layer of gallium arsenide, the MBE growth of the strontium titanate monocrystalline layer can be capped by terminating the growth with 1-2 monolayers of titanium, 1-2 monolayers of titanium-oxygen or with 1-2 monolayers of strontium-oxygen. Following the formation of this capping layer, arsenic is deposited to form a Ti-As bond, a Ti-O-As bond or a Sr-O-As. Any of these form an

appropriate template for deposition and formation of a gallium arsenide monocrystalline layer. Following the formation of the template, gallium is subsequently introduced to the reaction with the arsenic and gallium arsenide forms. Alternatively, gallium can be deposited on the capping layer to form a Sr-O-Ga bond, and arsenic is subsequently introduced with the gallium to form the GaAs.

FIG. 5 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the present invention. Single crystal $SrTiO_3$ accommodating buffer layer 24 was grown epitaxially on silicon substrate 22. During this growth process, amorphous interfacial layer 28 is formed which relieves strain due to lattice mismatch. GaAs compound semiconductor layer 26 was then grown epitaxially using template layer 30.

FIG. 6 illustrates an x-ray diffraction spectrum taken on structure including GaAs compound semiconductor layer 26 grown on silicon substrate 22 using accommodating buffer layer 24. The peaks in the spectrum indicate that both the accommodating buffer layer 24 and GaAs compound semiconductor layer 26 are single crystal and (100) orientated.

The structure illustrated in FIG. 2 can be formed by the process discussed above with the addition of an additional buffer layer deposition step. The buffer layer is formed overlying the template layer before the deposition of the monocrystalline compound semiconductor layer. If the buffer layer is a compound semiconductor superlattice, such a superlattice can be deposited, by MBE for example, on the template described above. If instead the buffer layer is a layer of germanium, the process above is modified to cap the strontium titanate monocrystalline layer with a final layer of either strontium or titanium and then by depositing germanium to

react with the strontium or titanium. The germanium buffer layer can then be deposited directly on this template.

Structure 34, illustrated in FIG. 3, may be formed by growing an accommodating buffer layer, forming an amorphous oxide layer over substrate 22, and growing semiconductor layer 38 over the accommodating buffer layer, as described above. The accommodating buffer layer and the amorphous oxide layer are then exposed to an anneal process sufficient to change the crystalline structure of the accommodating buffer layer from monocrystalline to amorphous, thereby forming an amorphous layer such that the combination of the amorphous oxide layer and the now amorphous accommodating buffer layer form a single amorphous oxide layer 36. Layer 26 is then subsequently grown over layer 38. Alternatively, the anneal process may be carried out subsequent to growth of layer 26.

In accordance with one aspect of this embodiment, layer 36 is formed by exposing substrate 22, the accommodating buffer layer, the amorphous oxide layer, and semiconductor layer 38 to a rapid thermal anneal process with a peak temperature of about 700°C to about 1000°C and a process time of about 10 seconds to about 10 minutes. However, other suitable anneal processes may be employed to convert the accommodating buffer layer to an amorphous layer in accordance with the present invention. For example, laser annealing or "conventional" thermal annealing processes (in the proper environment) may be used to form layer 36. When conventional thermal annealing is employed to form layer 36, an overpressure of one or more constituents of layer 30 may be required to prevent degradation of layer 38 during the anneal process. For example, when layer 38 includes GaAs, the anneal

environment preferably includes an overpressure of arsenic to mitigate degradation of layer 38.

As noted above, layer 38 of structure 34 may include any materials suitable for either of layers 32 or 26. Accordingly, any deposition or growth methods described in connection with either layer 32 or 26 may be employed to deposit layer 38.

FIG. 7 is a high resolution Transmission Electron Micrograph (TEM) of semiconductor material manufactured in accordance with the embodiment of the invention illustrated in FIG. 3. In Accordance with this embodiment, a single crystal $SrTiO_3$ accommodating buffer layer was grown epitaxially on silicon substrate 22. During this growth process, an amorphous interfacial layer forms as described above. Next, GaAs layer 38 is formed above the accommodating buffer layer and the accommodating buffer layer is exposed to an anneal process to form amorphous oxide layer 36.

FIG. 8 illustrates an x-ray diffraction spectrum taken on a structure including GaAs compound semiconductor layer 38 and amorphous oxide layer 36 formed on silicon substrate 22. The peaks in the spectrum indicate that GaAs compound semiconductor layer 38 is single crystal and (100) orientated and the lack of peaks around 40 to 50 degrees indicates that layer 36 is amorphous.

The process described above illustrates a process for forming a semiconductor structure including a silicon substrate, an overlying oxide layer, and a monocrystalline gallium arsenide compound semiconductor layer by the process of molecular beam epitaxy. The process can also be carried out by the process of chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), migration enhanced epitaxy (MEE), atomic layer epitaxy (ALE), physical vapor deposition (PVD), chemical solution deposition (CSD), pulsed laser deposition (PLD), or the

like. Further, by a similar process, other monocrystalline accommodating buffer layers such as alkaline earth metal titanates, zirconates, hafnates, tantalates, vanadates, ruthenates, and niobates, peroskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide can also be grown. Further, by a similar process such as MBE, other III-V and II-VI monocrystalline compound semiconductor layers can be deposited overlying the monocrystalline oxide accommodating buffer layer.

Each of the variations of compound semiconductor materials and monocrystalline oxide accommodating buffer layer uses an appropriate template for initiating the growth of the compound semiconductor layer. For example, if the accommodating buffer layer is an alkaline earth metal zirconate, the oxide can be capped by a thin layer of zirconium. The deposition of zirconium can be followed by the deposition of arsenic or phosphorus to react with the zirconium as a precursor to depositing indium gallium arsenide, indium aluminum arsenide, or indium phosphide respectively. Similarly, if the monocrystalline oxide accommodating buffer layer is an alkaline earth metal hafnate, the oxide layer can be capped by a thin layer of hafnium. The deposition of hafnium is followed by the deposition of arsenic or phosphorous to react with the hafnium as a precursor to the growth of an indium gallium arsenide, indium aluminum arsenide, or indium phosphide layer, respectively. In a similar manner, strontium titanate can be capped with a layer of strontium or strontium and oxygen and barium titanate can be capped with a layer of barium or barium and oxygen. Each of these depositions can be followed by the deposition of arsenic or phosphorus to react with the capping material to form a template for the deposition of a compound

semiconductor material layer comprising indium gallium arsenide, indium aluminum arsenide, or indium phosphide.

FIG. 9 illustrates schematically, in cross-section, a semiconductor structure 90 including a monocrystalline semiconductor substrate layer 92, an amorphous oxide layer 94 overlying the substrate, a monocrystalline compound semiconductor layer 98 overlying the amorphous oxide layer, a source terminal 100, a drain terminal 104, a channel 105, and a CMOS circuit 112 having a device region 114. Those skilled in the art will appreciate that source terminal 100, drain terminal 104, channel 105, and device region 114 function together to form a field effect transistor (FET). In a preferred embodiment, amorphous oxide layer 94 comprises any of the materials discussed above in connection with layer 36, such as an alkali earth metal oxide, for example $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1. Compound semiconductor layer 98 preferably comprises a material selected from the group consisting of: GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS. Alternatively, compound semiconductor layer 98 may be made from any suitable material selected from the group consisting of III-V compounds, II-VI compounds, and mixed II-VI compounds. CMOS circuit 112 may comprise a control circuit, digital logic, a digital integrated circuit, or virtually any other microelectronic structure fabricated within monocrystalline substrate layer 92. In a particularly preferred embodiment, monocrystalline semiconductor substrate 92 is a silicon substrate. Those skilled in the art will further appreciate that channel 105, source 100 and drain 104 are suitably configured such that current is conducted along channel 105 from drain 104 to source 100 (or vice versa) in accordance with the biasing of device region 114. More particularly, the extent of the current conductivity associated with channel 105 may be controlled, either in a linear fashion or in a

bi-stable fashion (*e.g.*, a switch) under the control of device region 114, typically a gate. Those skilled in the art will also appreciate that source terminal 100 and drain terminal 104 may comprise metal patterned on compound semiconductor layer 98.

FIG. 10 illustrates schematically, in cross-section, a semiconductor structure 120 generally analogous to semiconductor structure of FIG. 9, illustrating a source region 106 and a drain region 108 spaced apart therefrom, wherein the source and drain regions are impurity doped regions formed in compound semiconductor layer 98.

FIG. 11 illustrates schematically, in cross-section, a semiconductor structure 122 wherein source region 106 and drain region 108 are configured to cooperate with a gate 118 to form an FET, wherein the biasing of gate 118 controls the conductivity of channel 105. If desired, gate 118 may be formed as a metal electrode insulated from channel 105 by a gate dielectric 116. Gate 118 and/or gate dielectric 116 may be photolithographically patterned onto compound semiconductor layer 98.

With continued reference to FIG. 11, device region 114 may be configured to function as a second gate electrode which, in conjunction with gate 118, influences the conductivity of channel 105. For example, gate 118 could function as a "front" gate for source region 106 and drain region 108, while gate 114 functions as a "back" gate for the drain and source regions. In this way, by biasing one of the gates, the threshold voltage of the FET device could be effectively shifted from a first (*e.g.*, a higher voltage value) to a second (*e.g.*, a lower voltage value) threshold. Alternatively, by tying first gate 118 and second gate 114 together electrically, the transconductivity of the device could be significantly increased, for example, on the order of 2x.

In one embodiment, second gate 114 may comprise an impurity doped region of CMOS circuit 112 configured to receive a voltage signal. In an alternate embodiment, second gate electrode may comprise a conductive electrode associated with CMOS circuit 112 and configured to receive a voltage signal. Moreover, although circuit 112 is preferably a CMOS circuit, circuit 112 may comprise any desired microelectronic structure, which is at least partially fabricated within monocrystalline substrate layer 92.

FIG. 12 illustrates schematically, in cross-section, a semiconductor structure 142 including respective layers 92, 94 and 98 substantially as discussed above, including a source region 146 and a drain region 148 spaced apart from one another and formed within substrate layer 92, and a gate electrode 144 formed either partially within or patterned on top of compound semiconductor layer 98. In order to function as a FET, gate electrode 144 is suitably disposed in substantial alignment with source and drain regions 146 and 148. In this regard, gate 144, source region 146 and drain region 148 may suitably function as a metal semiconductor field effect transistor (MESFET).

Semiconductor structure 142 may also include, as desired, a source electrode 143 and a drain electrode 145, advantageously positioned in ohmic contact with corresponding impurity doped source and drain regions 147, 149, respectively, in monocrystalline compound semiconductor layer 198.

With continuing reference to FIG. 12, insulator layer 94 preferably comprises an insulator selected form the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates. In a particularly preferred embodiment, oxide layer 94 comprises $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1. Monocrystalline compound semiconductor structure 98

preferably comprises a material selected from the group consisting of: III-V compounds, mixed III-V compounds, II-VI compounds, and mixed II-VI compounds. In a particularly preferred embodiment, compound semiconductor layer 98 comprises a material selected from the group consisting of: GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS.

As briefly discussed above in connection with FIG. 3, alkali earth metal oxide layer 94 may comprise an amorphous oxide formed by heat treating a monocrystalline oxide. Alternatively, layer 94 may include a monocrystalline accommodating buffer layer and an amorphous interface as discussed in connection with FIGS. 1-2.

FIG. 14 illustrates schematically, in cross-section, a semiconductor structure 124 including a monocrystalline substrate 92 (*e.g.*, silicon), an alkali earth metal insulator layer 94 overlying substrate 92, an amorphous oxide layer 110 disposed between substrate 92 and insulator layer 94, a monocrystalline compound semiconductor layer 98 overlying insulator layer 94, a source electrode 100 and a drain electrode 104 spaced apart therefrom and formed on monocrystalline compound semiconductor 98, a channel region 126 extending between source electrode 100 and drain electrode 104, and a gate electrode 128 formed within substrate 92 generally in alignment with channel region 126. In this configuration, source electrode 100, drain electrode 104, channel region 126, and gate electrode 128 function as a FET.

Insulator layer 94 preferably comprises an insulator selected form the group consisting of alkali earth metal titanates, zirconates, hafnates, tantalates, ruthenates, niobates. In a particularly preferred embodiment, insulator layer 94 comprises $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1. With continued reference to FIG. 14,

monocrystalline compound semiconductor layer 98 preferably comprises a material selected from the group consisting of: III-V compounds, mixed III-V compounds, II-VI compounds, and mixed II-VI compounds. In a particularly preferred embodiment, compound semiconductor layer 98 is made from gallium arsenide, but may be any material consisting of AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS.

FIG. 15 illustrates schematically, in cross-section, a semiconductor structure 131 generally analogous to structure 124 of FIG. 14, further including a second gate electrode 102 formed on or at least partially within compound semiconductor layer 98, with second gate electrode 102 advantageously overlying channel region 126. In this configuration, source electrode 100, drain electrode 104, channel region 126 and second gate electrode 102 may function together as MESFET in accordance with generally known principles. Alternatively, source electrode 100, drain electrode 104, second gate electrode 102, and channel region 126 may form a high electron mobility transistor (HEMT). As discussed above in connection with FIG. 11, semiconductor structure 132, including first gate electrode 128 and second gate electrode 102, may also be configured to function as a single FET having two gates, such that one gate can be employed to modulate the threshold voltage for the other gate's electrode or, alternatively, both gate electrodes can be tied together to substantially increase the transconductance of the transistor.

FIG. 16 illustrates schematically, in cross-section, a semiconductor structure 134 generally analogous to structure 124 of FIG. 14, further illustrating a logic circuit, for example, a CMOS circuit 130 formed in substrate 92. Semiconductor 134 illustrates many of the advantages associated with growing a monocrystalline compound semiconductor layer 128 on a silicon substrate

92, which allows the monolithic integration of microelectronic structures associated with compound semiconductor layer 98 with microelectronic structures associated with substrate 92.

More particularly, FIG. 17 illustrates schematically, in cross-section, a semiconductor structure 136 generally analogous to structure 134 of FIG. 16, further illustrating gate electrode 128 being coupled to circuit 130, for example through an electrical interconnect 132. In this way, circuit 130 may be configured to apply a predetermined voltage to gate 128 to thereby turn on, turn off, or otherwise modulate the current between source terminal 100 and drain terminal 104.

In an alternate embodiment, FIG. 18 illustrates schematically, in cross-section, a semiconductor structure 138 generally analogous to semiconductor 134 of FIG. 16, illustrating an impurity doped region 140 formed in substrate 92 which effectively electrically couples circuit 130 with gate electrode 128. Many of the structures set forth in FIGS. 9-18 may be made in accordance with the following process parameters.

A semiconductor substrate 92 is initially provided. Thereafter, circuit 112 (FIG. 10), circuit 130 (FIG. 16), or any other desired microelectronic structure may be fabricated within the semiconductor substrate. If desired, the integrated circuit fabricated within the semiconductor substrate 92 may include a device region configured to receive a signal, for example a voltage signal, whereupon the device region is then employed to bias channel 105 which extends between source 100 and drain 104.

Thereafter, monocrystalline oxide layer 94 may be epitaxially grown overlying the semiconductor substrate. An amorphous oxide layer, for example, an amorphous oxide layer analogous to layer 110 in FIG. 14, may be formed

underlying monocrystalline oxide layer 94 during the foregoing step of epitaxially growing the monocrystalline layer. Monocrystalline compound semiconductor layer 98 may then be epitaxially grown overlying monocrystalline oxide layer 94, as discussed above in connection with FIGS. 1-3. Also, as discussed above in connection with FIG. 3, layer 94 may be exposed to an anneal process such that layer 94 structure changes from monocrystalline to amorphous. A semiconductor device, for example, one or more of source terminal 100, drain terminal 104, and channel region 105 (See FIG. 9), may then be formed within the monocrystalline compound semiconductor layer 98. As discussed above, source 100, drain 104, and channel 105 preferably function as a semiconducting device (*e.g.*, an FET), configured to change the conductivity of channel 105 in response to a voltage signal applied to the device region (*e.g.*, region 114 of FIG. 9) within substrate 92.

As briefly discussed above in connection with FIGS. 1-3, the aforementioned epitaxial growing steps may be implemented by any suitable process selected from the group consisting of MBE, MOCVD, MEE, and ALE. Moreover, the step of epitaxially growing a monocrystalline compound semiconductor layer may be implemented by first growing a seed layer of monocrystalline semiconductor material overlying the monocrystalline oxide layer, and thereafter growing a monocrystalline compound semiconductor device layer overlying the seed layer. Additionally, the compound semiconductor can be grown in two or more stages such that an anneal process can be performed between any two stages, wherein anneal process is configured to cause monocrystalline layer 94 to become amorphous.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without

departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

1. A semiconductor device structure comprising:

a monocrystalline substrate comprising silicon;

an alkali earth metal insulator overlying the substrate;

an amorphous silicon oxide layer between the substrate and the alkali earth metal insulator;

a monocrystalline compound semiconductor layer overlying the alkali earth metal insulator;

spaced apart source and drain electrodes formed on the monocrystalline compound semiconductor layer and defining a channel region therebetween; and

a first gate electrode formed in the substrate in alignment with the channel region.

2. The structure of claim 1 further comprising a second gate electrode formed on the monocrystalline compound semiconductor layer overlying the channel region.

3. The structure of claim 2 wherein the source electrode, drain electrode, channel region and second gate electrode form a MESFET.

4. The structure of claim 2 wherein the source electrode, drain electrode, channel region and second gate electrode form an HEMT.

5. The structure of claim 1 further comprising a CMOS circuit formed in the substrate.

6. The structure of claim 5 wherein the first gate electrode is coupled to the CMOS circuit.

7. The structure of claim 5 wherein the first gate electrode comprises an impurity doped region formed in the substrate and coupled to the CMOS circuit.

8. The structure of claim 5 wherein the first gate electrode comprises an electrical conductor coupled to the CMOS circuit.

9. The structure of claim 6 wherein the CMOS circuit is configured to selectively control a bias applied to the first gate electrode.

10. The structure of claim 1 wherein the alkali earth metal insulator comprises an insulator selected from the group consisting of alkali earth metal titanates, zirconates, hafantes, tantalates, ruthenates, and niobates.

11. The structure of claim 1 wherein the monocrystalline compound semiconductor layer comprises a material selected from the group consisting of: III-V compounds, mixed III-V compounds, II-VI compounds, and mixed II-VI compounds.

12. The structure of claim 1 wherein the monocrystalline compound semiconductor layer comprises a material selected from the group consisting of: GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS.

13. The structure of claim 12 wherein the alkali earth metal insulator comprises $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

14. A semiconductor device structure comprising:

a monocrystalline semiconductor substrate;

an alkali earth metal oxide overlying the substrate;

a monocrystalline compound semiconductor layer overlying the alkali earth metal oxide;

spaced apart source and drain regions formed in the substrate; and

a gate electrode formed in the monocrystalline compound semiconductor layer in alignment with the source and drain regions.

15. The device structure of claim 14 further comprising a MESFET formed in the monocrystalline compound semiconductor layer.

16. The device structure of claim 15 wherein the MESFET comprises:

spaced apart source and drain electrodes in ohmic contact with the monocrystalline compound semiconductor layer; and

a metallic gate electrode contacting the monocrystalline compound semiconductor layer and positioned between the source and drain electrodes.

17. The device structure of claim 16 wherein the source and drain electrodes contact impurity doped source and drain regions, respectively, in the monocrystalline compound semiconductor layer.

18. The structure of claim 14 wherein the alkali earth metal insulator comprises an insulator selected from the group consisting of alkali earth metal titanates, zirconates, hafantes, tantalates, ruthenates, and niobates.

19. The structure of claim 14 wherein the monocrystalline compound semiconductor layer comprises a material selected from the group consisting of: III-V compounds, mixed III-V compounds, II-VI compounds, and mixed II-VI compounds.

20. The structure of claim 14wherein the monocrystalline compound semiconductor layer comprises a material selected from the group consisting of: GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS.

21. The structure of claim 20 wherein the alkali earth metal insulator comprises $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

22. The structure of claim 14 wherein the alkali earth metal oxide comprises a monocrystalline oxide.

23. The structure of claim 14 wherein the alkali earth metal oxide comprises an amorphous oxide formed by heat treating a monocrystalline oxide.

24. A semiconductor device structure comprising:

a monocrystalline semiconductor substrate;

an amorphous oxide layer overlying the substrate;

a monocrystalline compound semiconductor layer overlying the amorphous oxide layer;

a field effect transistor having a source, a drain, a gate, and a channel, having a current conductivity, formed at least partially in the compound semiconductor layer; and

a CMOS circuit formed at least partially in the silicon substrate, the CMOS circuit comprising a device region configured to control the current conductivity of the channel.

25. The device structure of claim 24 wherein the amorphous oxide layer comprises an alkali earth metal oxide.

26. The device structure of claim 25 wherein the alkali earth metal oxide comprises $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

27. The device structure of claim 26 wherein the compound semiconductor layer comprises a material selected from the group consisting of: GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS.

28. The device structure of claim 24 wherein the compound semiconductor layer comprises a material selected from the group consisting of: III-V compounds, mixed III-V compounds, II-VI compounds, and mixed II-VI compounds.

29. The device structure of claim 24 wherein the CMOS circuit comprises a digital integrated circuit.

30. The device structure of claim 24 wherein the source and drain comprise spaced apart impurity doped regions formed in the compound semiconductor layer.

31. The device structure of claim 30 wherein the gate comprises a metal electrode formed on the compound semiconductor between the source and the drain.

32. The device structure of claim 30 wherein the gate comprises a metal electrode insulated from the channel by a gate dielectric.

33. The device structure of claim 24 wherein the device region comprises a second gate electrode.

34. The device structure of claim 33 wherein the second gate electrode comprises an impurity doped region of the CMOS circuit configured to receive a voltage signal.

35. The device structure of claim 33 wherein the second gate electrode comprises a conductive electrode of the CMOS circuit configured to receive a voltage signal.

36. The device structure of claim 24 wherein the monocrystalline semiconductor substrate comprises a silicon substrate.

37. A process for fabricating a semiconductor device structure comprising the steps of:

providing a semiconductor substrate;

forming an integrated circuit at least partially within the semiconductor substrate, the integrated circuit including a device region configured to receive a signal;

epitaxially growing a monocrystalline oxide layer overlying the semiconductor substrate;

forming an amorphous oxide layer underlying the monocrystalline oxide layer during the step of epitaxially growing a monocrystalline oxide layer;

epitaxially growing a monocrystalline compound semiconductor layer overlying the monocrystalline oxide layer; and

forming a semiconductor device at least partially within the monocrystalline semiconductor layer, the semiconductor device configured to alter its conductivity in response to the signal received by the device region.

38. The process of claim 37 wherein the semiconductor substrate comprises silicon.

39. The process of claim 38 wherein the step of forming an amorphous oxide comprises the step of growing a silicon oxide.

40. The process of claim 38 wherein the step of epitaxially growing a monocrystalline oxide comprises the step of epitaxially growing an oxide comprising a material selected from the group consisting of alkali earth metal titanates, alkali earth metal zirconates, alkali earth

metal hafantes, alkali earth metal tantalates, alkali earth metal ruthenates, and alkali earth metal niobates.

41. The process of claim 40 wherein the step of epitaxially growing a monocrystalline oxide comprises the step of epitaxially growing $Sr_xBa_{1-x}TiO_3$ where x ranges from 0 to 1.

42. The process of claim 40 wherein the step of epitaxially growing a monocrystalline oxide comprises the step of growing an oxide by a process selected from the group consisting of MBE, MOCVD, MEE, and ALE.

43. The process of claim 37 wherein the step of epitaxially growing a monocrystalline compound semiconductor layer comprises the steps of:

growing a seed layer of monocrystalline semiconductor material overlying the monocrystalline oxide layer; and

growing a monocrystalline compound semiconductor device layer overlying the seed layer.

44. The process of claim 43 further comprising the step of heat treating the monocrystalline oxide layer to convert the monocrystalline oxide layer to an additional amorphous oxide layer.

45. The process of claim 44 wherein the step of heat treating is carried out after the step of growing a seed layer.

46. The process of claim 44 wherein the step of heat treating is carried out after the step of growing a monocrystalline compound semiconductor device layer.

47. The process of claim 43 wherein the step of growing a monocrystalline compound semiconductor device layer comprises the step of growing a material from the group consisting of GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS.

48. The process of claim 43 wherein the step of growing a seed layer comprises the step of growing a material from the group consisting of germanium, and a superlattice of a material selected from $GaAs_xP_{1-x}$ where x ranges from 0 to 1, $In_yGa_{1-y}P$ where y ranges from 0 to 1, InGaAs, GaAs, AlGaAs, InGaP, AlInP, and AlInP.

49. The process of claim 37 wherein the step of epitaxially growing a monocrystalline compound semiconductor layer comprises the step of growing a material from the group consisting of GaAs, AlGaAs, InP, InGaAs, InGaP, ZnSe, and ZnSeS.

50. The process of claim 49 wherein the step of epitaxially growing a monocrystalline compound layer comprises the step of growing a compound semiconductor layer by a process selected from the group consisting of MBE, MOCVD, MEE, and ALE.

51. A process for fabricating a semiconductor device comprising the steps of:

providing a monocrystalline semiconductor substrate having a surface;

forming first spaced apart source and drain regions at the surface of the substrate, the source and drain

regions defining a first channel therebetween, the channel configured to carry an electrical current;

epitaxially growing a gate insulator overlying the surface;

epitaxially growing a layer of compound semiconductor material overlying the gate insulator;

forming a gate electrode in the layer of compound semiconductor material, the gate electrode configured to control the electrical current through the channel region;

forming second spaced apart source and drain regions in the layer of compound semiconductor material, the second spaced apart source and drain regions aligned relative to the first source and drain regions and defining a second channel region in the compound semiconductor material therebetween, the second channel configured to conduct a second channel current; and

forming a second gate electrode overlying the channel region, the second gate electrode configured to control the second channel current.

52. The process of claim 50 wherein the second channel is configured to influence the electrical current through the first channel in response to electrical signals applied to the second spaced apart source and drain regions.

53. The process of claim 50 wherein the first drain region is configured to influence the flow of current through the second channel in response to an electrical signal applied to first drain region.

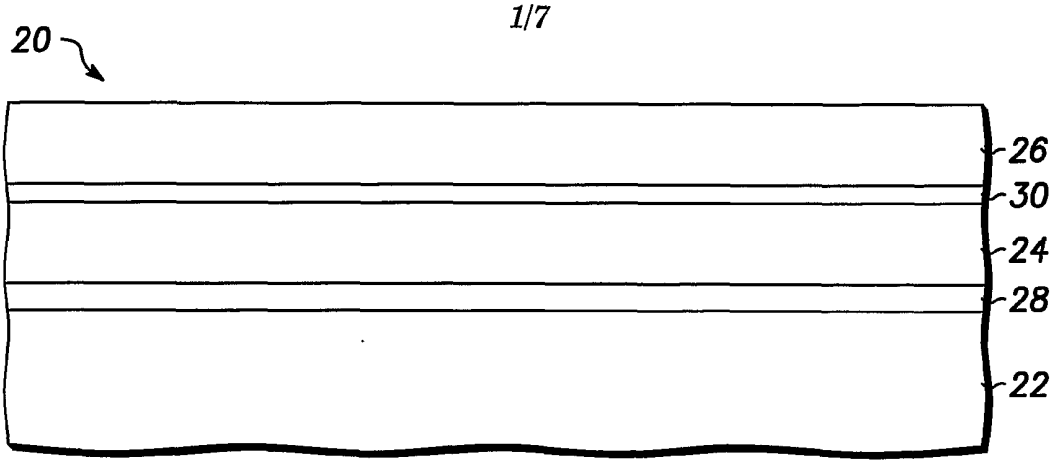

FIG. 1

FIG. 2

FIG. 3

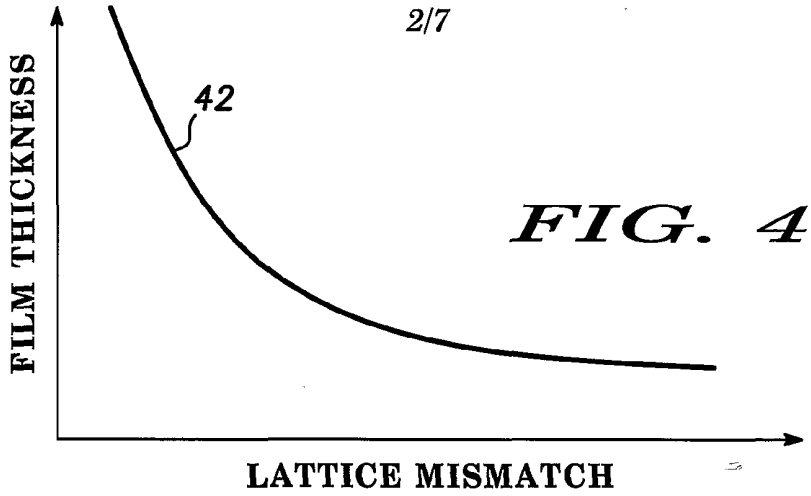

FIG. 4

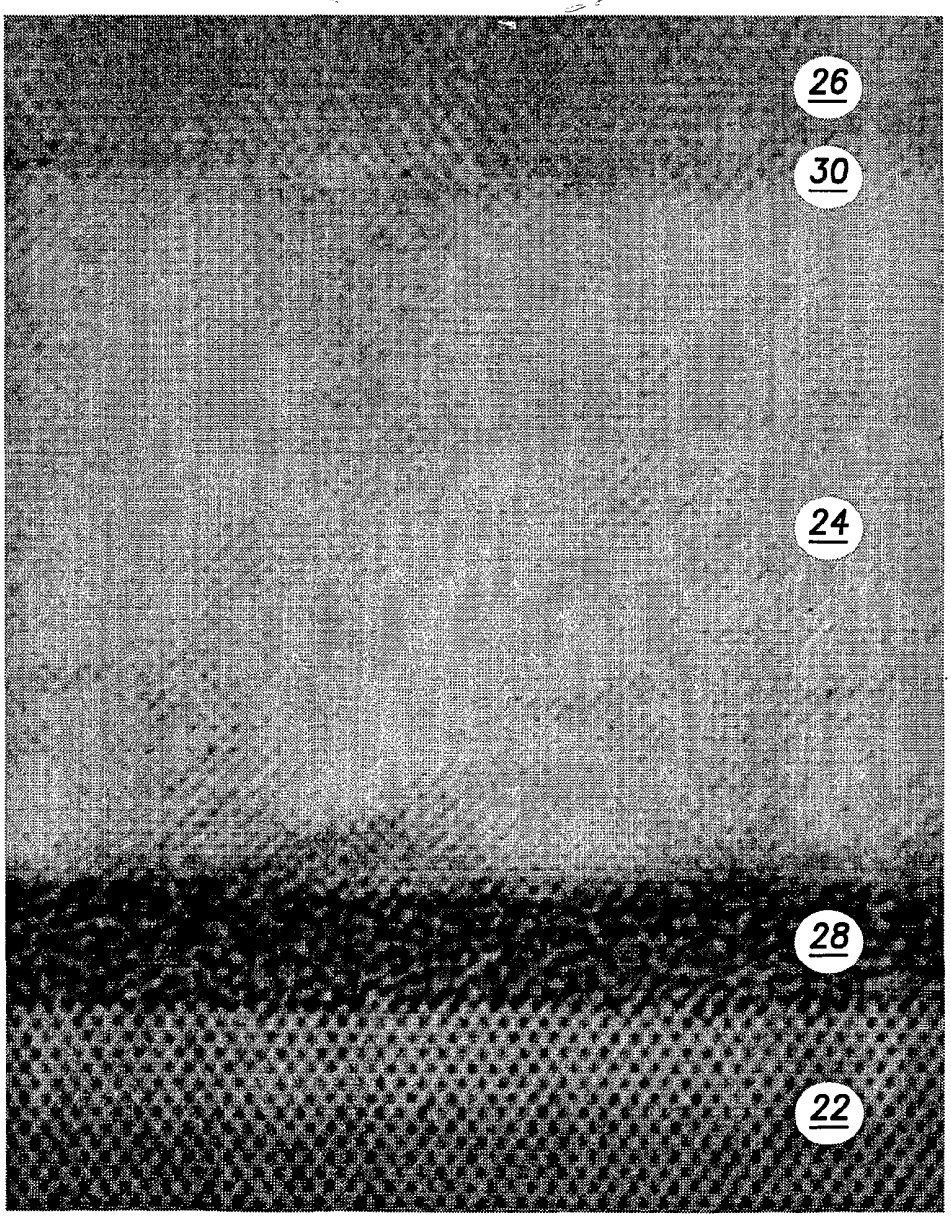

FIG. 5

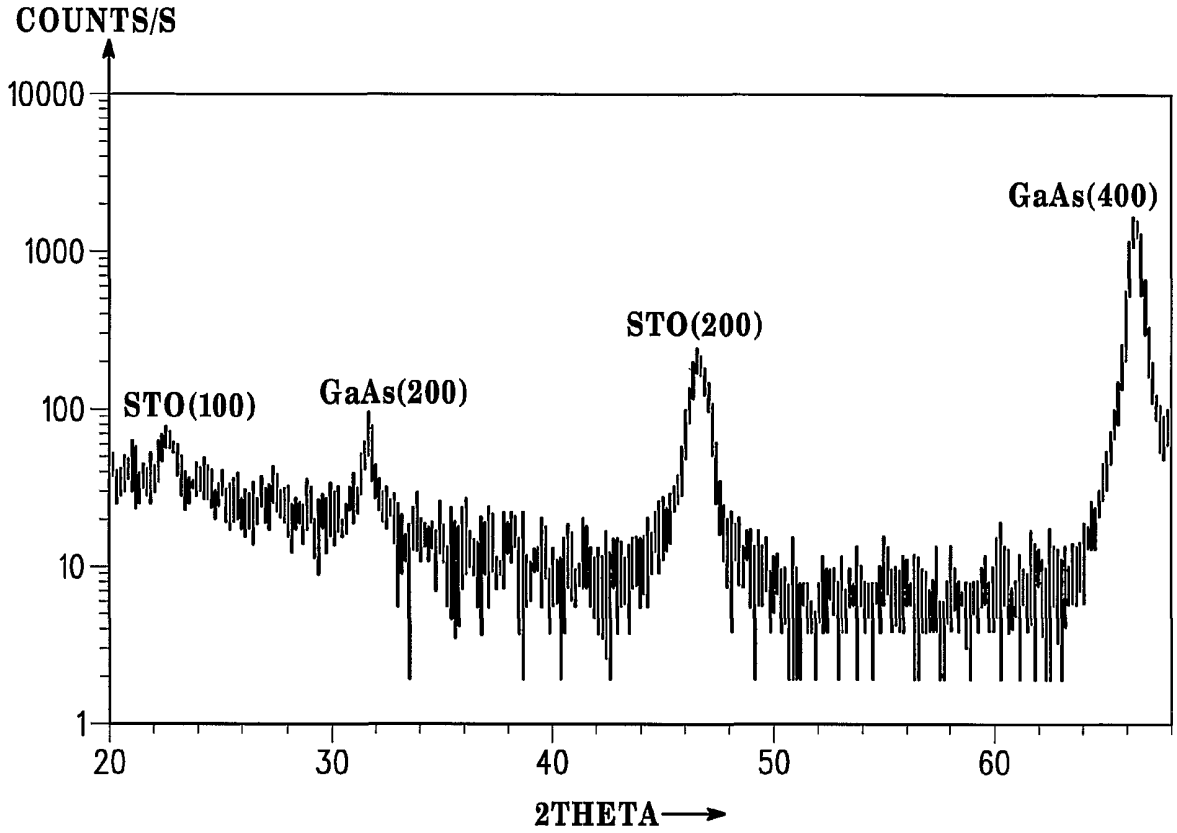
COUNTS/S
10000
1000
100
10
1
20
30
40
50
60
2THETA
STO(100)
GaAs(200)
STO(200)
GaAs(400)

FIG. 6

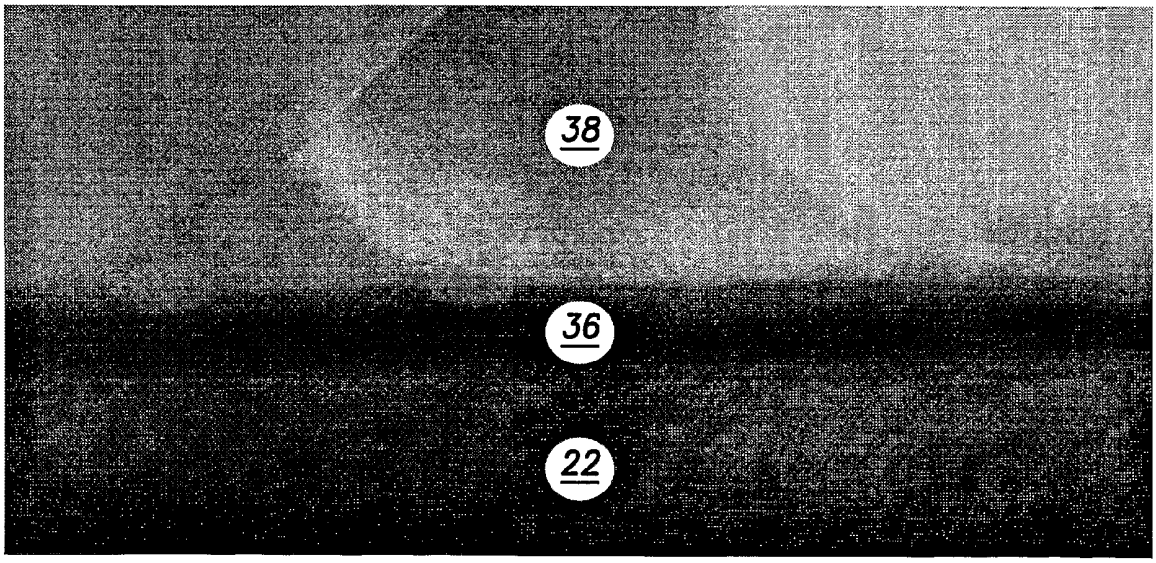
38
36
22

FIG. 7

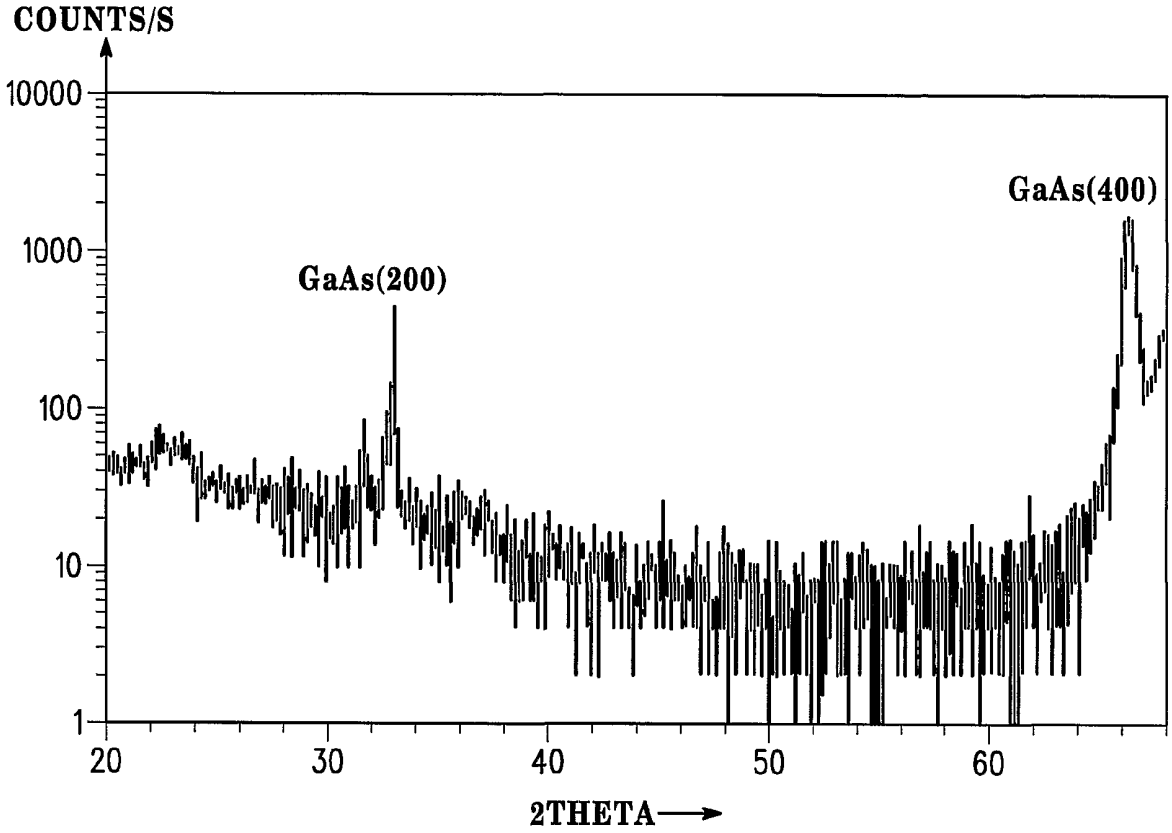
COUNTS/S
10000
1000
100
10
1
GaAs(200)
GaAs(400)
20
30
40
50
60
2THETA

FIG. 8

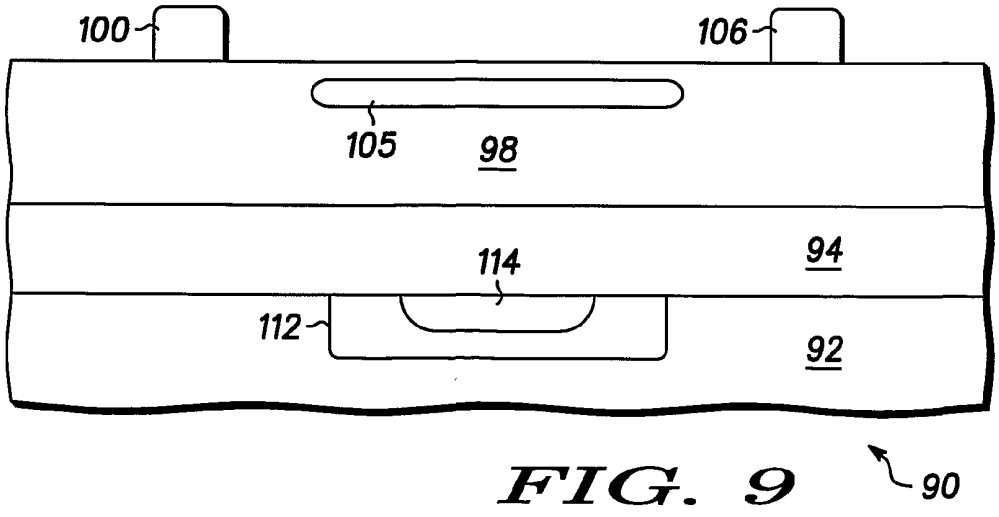
100
106
105
98
114
94
112
92
90

FIG. 9

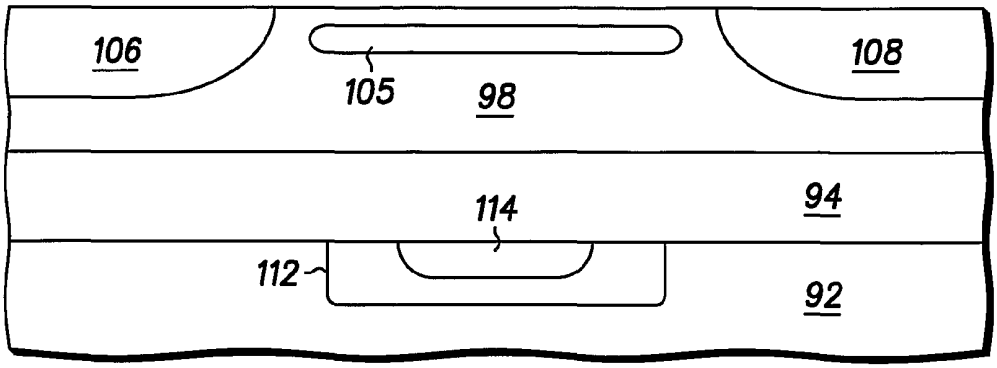

FIG. 10

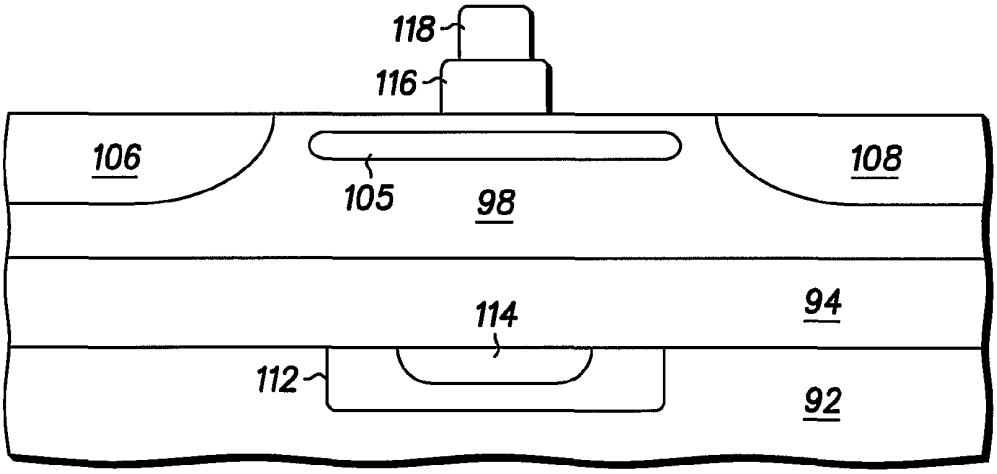

FIG. 11

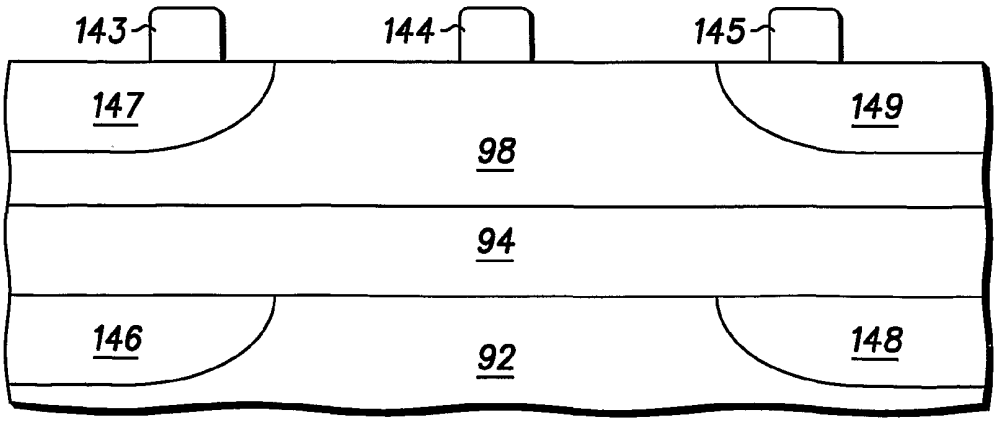

FIG. 12

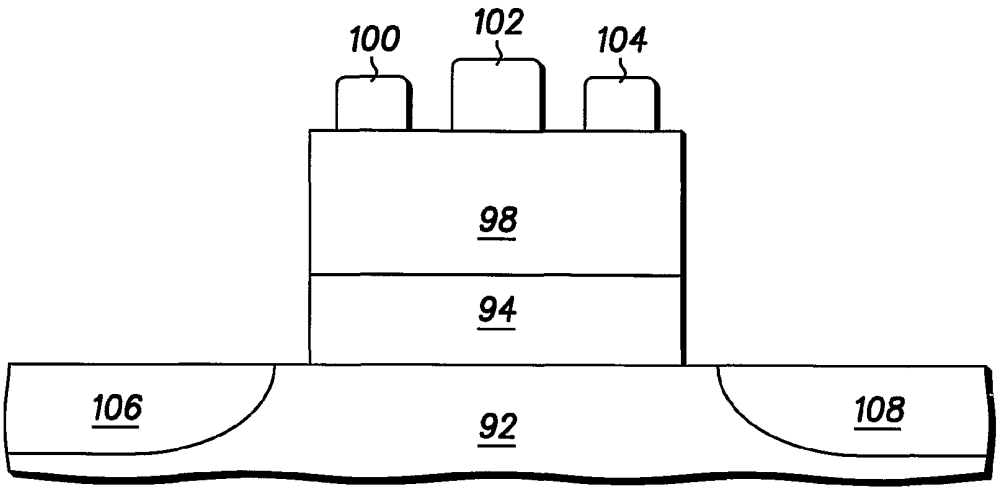

FIG. 13

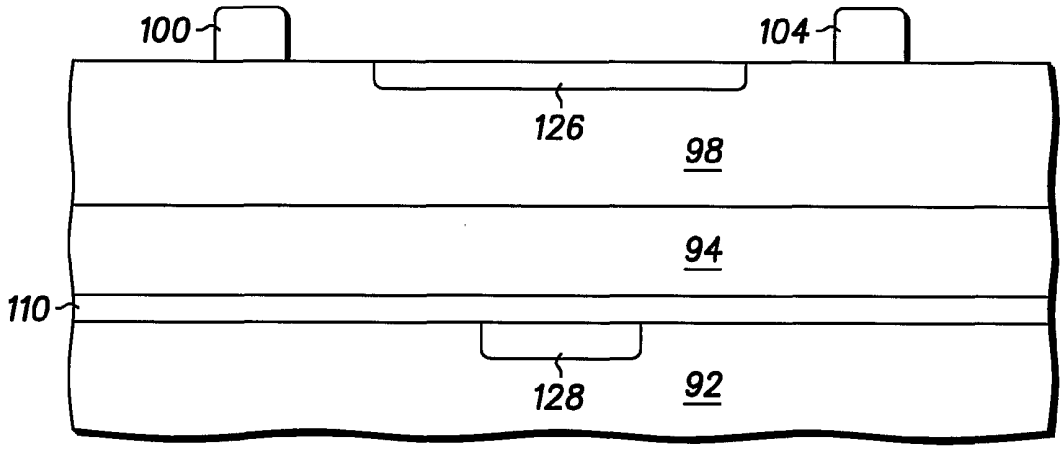

FIG. 14

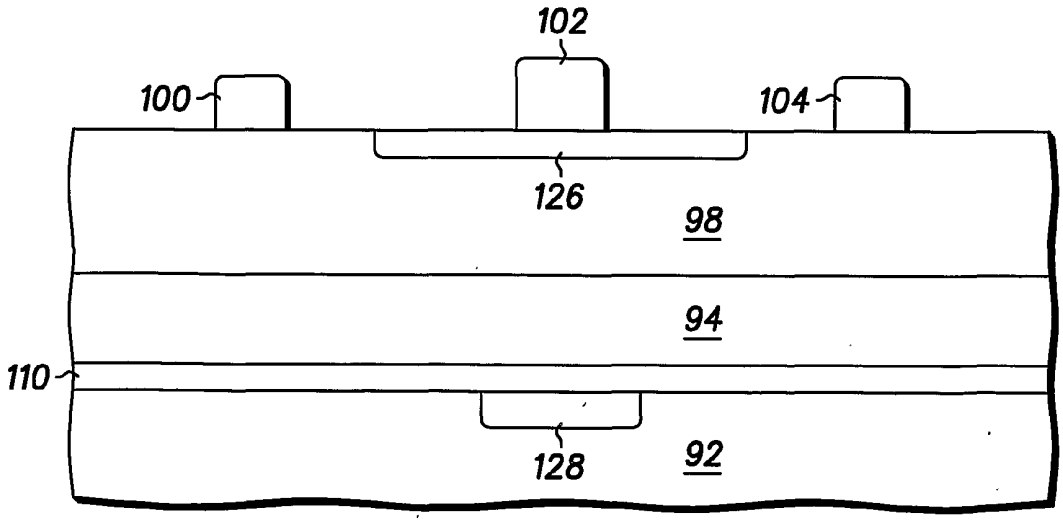

FIG. 15

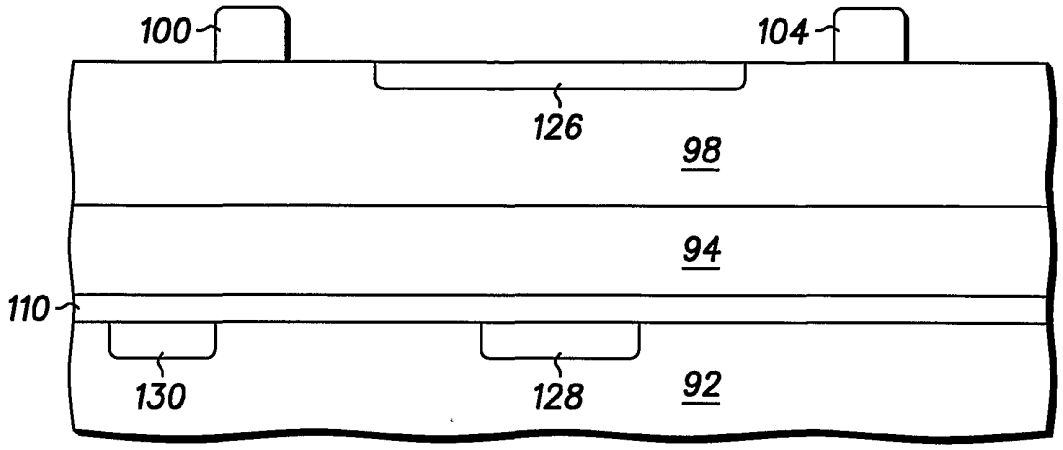

FIG. 16 134

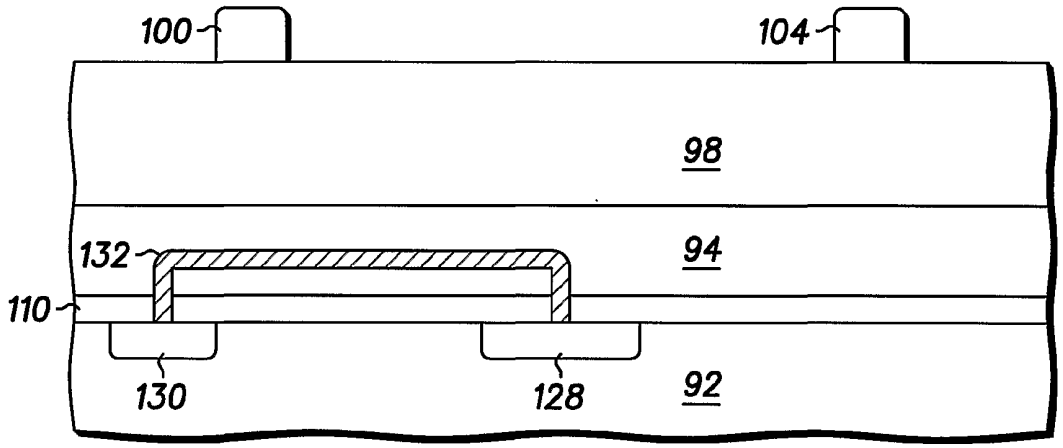

FIG. 17 136

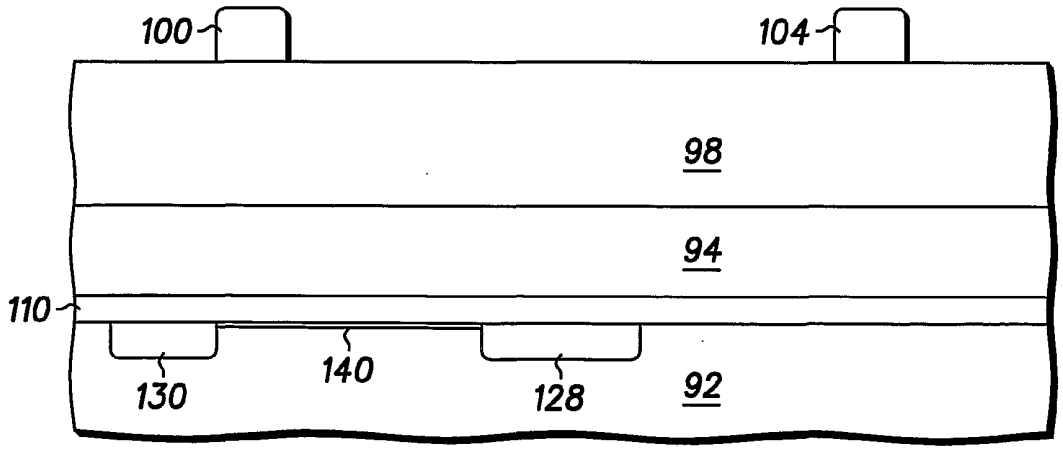

FIG. 18 138