Title: IQ PHASE IMBALANCE CORRECTION METHOD IN CARTESIAN LINEARIZATION FEEDBACK PATH WITH DUAL PHASE SHIFTERS

Abstract: A communication device, transmitter, and system containing dual quadrature phase shifters and method of training the transmitter are provided. During training, a phase training module determines the phase imbalance in each of in-phase and quadrature Cartesian feedback paths. The phase training module provides control signals to each of in-phase and quadrature dual phase shifters to provide separate and independent phase corrections for the paths. During one training cycle, individual sessions are used to train the in-phase and quadrature dual phase shifters. The latter session uses the results of the former session to provide an initial value for the phase shift to be provided as a result of the latter session, thereby reducing the overall time used to train both the in-phase and quadrature dual phase shifters.
Technical Field

[0001] This application is related to radio transmitters and, in particular, radio transmitters that employ linearization feedback paths with dual phase shifters to correct for IQ phase imbalance.

Background of the Invention

[0002] Wireless communication systems, for example cellular telephony or private mobile radio communication systems, typically provide for radio telecommunication links to be arranged between a plurality of subscriber units (or mobile stations (MSs)) via a system infrastructure having fixed installations including one or more base transceiver stations (BTSs). Radio frequency (RF) transmitters are located in both BTSs and MSs in order to facilitate wireless communication between the communication units.

[0003] Mobile communication systems typically operate according to a set of industry standards or protocols. An example of such standards is the TErrestrial Trunked Radio (TETRA) standards, which have been defined by the European Telecommunications Standards Institute (ETSI). A system that operates according to TETRA standards is known as a TETRA system. TETRA systems are primarily designed for use by professional radio users, such as the emergency services.

[0004] There is continuing pressure on the limited radio spectrum available for radio communication systems. To provide improved usage of this spectrum, one aspect of the system has focused on the development of spectrally efficient linear modulation schemes. By using spectrally efficient linear modulation schemes, more communication devices are able to share the allocated spectrum within a defined geographical coverage area (cell).

[0005] Since the envelopes of these linear modulation schemes fluctuate, intermodulation products can be generated in the non-linear radio frequency (RF) power amplifier(s). Specifically in the digital private mobile radio (PMR) market, restrictions on out-of-band emissions are severe (to the order of -60dBc to -70dBc)
relative to the power in adjacent frequency channels). Hence, linear modulation schemes used in this scenario require highly linear transmitters.

[0006] The actual level of linearity needed to meet particular out-of-band emission limits, is a function of many parameters, of which the most critical parameters are modulation type and bit rate. Quantum processes within a typical radio frequency (RF) amplifying device are non-linear by nature. Only a straight line may approximate the transfer function of the amplifying device when a small portion of the consumed direct current (DC) power is transformed into radio frequency (RF) power, i.e. as in an ideal linear amplifier case. This mode of operation provides a low efficiency of DC to RF power conversion, which is unacceptable for portable units.

[0007] One emphasis in portable PMR equipment is to increase battery life. Hence, it is desirable to maximize the operating efficiencies of the amplifiers used, e.g., improving transmitted signal ACCPR (Adjacent Channel Coupled Power Ratio) while keeping high RFPA (Radio Frequency Power Amplifier) efficiency. To achieve both linearity and efficiency, linearization techniques are used to improve the linearity performance of the more efficient classes of amplifier, for example class AB, B or C amplifiers. One such linearization technique, often used in designing linear transmitters, is Cartesian feedback. Cartesian feedback loop based linearizers are commonly used in linear digital cellular portable transmitters (TETRA, iDEN, etc.) Cartesian feedback linearizer allows an improvement in adjacent and alternative channels ACP (Adjacent Channel Power) while still allowing RFPA to work close to its saturation point thus maintaining good efficiency. Cartesian feedback is a ‘closed loop’ negative feedback technique having a forward path and a feedback path, in which the baseband feedback signal in the feedback path is summed in its digital in-phase (I channel) and quadrature phase (Q channel) formats with the corresponding generated I and Q input signals in the forward path. The linearizing of the power amplifier output requires the accurate setting and on-going control of the phase and amplitude of a feedback signal.

[0008] The linearizer circuit optimizes the performance of the transmitter, for example to comply with linearity or output power specifications of the communication system, or to optimize the operating efficiency of the transmitter power amplifier. Operational parameters of the transmitter are adjusted to optimize
the transmitter performance and include as an example, one or more of the following: amplifier bias voltage level, input power level, phase shift of the signal around the feedback path. Such adjustments are performed by say, a microprocessor. Due to the sensitivity of such transmitter circuits, a range of control and adjustment circuits and/or components are needed so that a linear and stable output signal can be achieved under all operating circumstances.

[0009] All linearization techniques require a finite amount of time in which to linearize the performance of a given amplifier. The amplifier may be linearized by initially applying a training sequence to the linearizer circuit and the amplifier to determine the levels of phase and gain distortion introduced by the linearization loop and the amplifying device. Once the phase and gain distortion levels have been determined, they can be compensated for, generally by adjusting feedback components/parameters.

[0010] To accommodate for such linearization requirements, communication systems typically allocate specific training periods for individual users to train their transmitters. The TETRA standard includes a time frame, termed a Common Linearization Channel (CLCH) as is described in UK Patent Application No. 9222922.8, to provide a full-training period approximately once every second. The CLCH frame allows a radio to train prior to gaining access to the system. However, a radio having to wait up to one second before training and then accessing the system is undesirable. To minimize the effect of this significant delay in call set-up times, and also provide an additional period for fine tuning a radio's output characteristics, due to changes in temperature, supply voltage or frequency of operation, a reduced training sequence has been inserted at the beginning of each TETRA traffic time slot for the radio allocated that slot to perform a minimal amount of training or fine tuning. This period may be used for phase training.

[0011] Examples of training are described in US Patent No. 5,066,923 of Motorola Inc., which describes a training scheme where the phase of the amplifier is adjusted in an 'open-loop' mode and the gain of the amplifier is adjusted when the loop is closed, and U.S. Patent Application 10/991,735 entitled "Wireless Communication Unit, Linearised Transmitter Circuit And Method of Linearising Therein," which describes a training scheme in which e.g. phase corrections are provided for the I and Q signals
to correct for the imperfections in the phase shifter intended to provide a 90° phase shift for signals to each of the I and Q signals, both of which are herein incorporated by reference in their entireties.

[0012] Phase training is used in Cartesian feedback loop to correctly adjust the loop phase to ensure stability using negative feedback. During phase training, the Cartesian feedback loop is configured to be 'open loop', i.e. a switch is used to prevent the feedback signal from being combined with the signal routed through the transmitter circuit. In a phase training mode of operation, a positive signal is applied to the I-channel input. The phase shift of the feedback path is measured and, in response to the measured I-channel phase shift, the phase around the loop on both the I-channel and the Q-channel is adjusted by a phase shifter.

[0013] Figure 1 illustrates a block diagram of a transmitter 100 containing a typical set of Cartesian feedback loops 100. The transmitter 100 is in phase training mode, as the switches 132, 134 for the I and Q channels are open. Each of the analog baseband I and Q signals are respectively supplied to a summer 102, 112. The signals from the summers 102, 112 are amplified by an amplifier 104, 114 of predetermined gain and then passed through a low-pass filter 106, 116. The resulting low-pass filtered signals are then upconverted by a mixer 108, 118 supplied with signal at the desired frequency by a local oscillator (LO) 140 and phase shifted by a 90° phase shifter 110. The upconverted signals are then combined at a summer 122, amplified by a power amplifier 124 of predetermined gain and supplied to an antenna 136. A coupler 138 samples the transmitted signal and feeds it to down-converting mixers 124, 126 again supplied with a signal that is phase shifted by a 90° phase shifter 128. The signals from the mixers 124, 126 are fed to phase training control 130, which using a successive approximation register (SAR) algorithm adjusts the phase of the phase shifter 150. Phase training is described below. The Cartesian loop is open (switches 132 and 134 open) and a positive baseband signal applied to the input of the I-channel. Phase training control circuitry 130 monitors the signal before switch on the Q-channel - indicated as Vfq 140. A SAR phase training algorithm controls the phase shifter 150 and minimizes the Vfq voltage. A voltage value measured on the Q-channel prior to the switch 134 is then reduced to a level close to zero. The same process is repeated for a negative baseband signal input to the I-channel. The
calculated results from both the positive and negative training applied to the I-channel are then further processed by averaging the results and using the averages to adjust the phase around both the I-channel loop and the Q-channel loop.

[0014] While the above architecture illustrated in Fig. 1 is currently favoured, it is possible to improve the IQ characteristics for current generation of transmitters.

**Brief Description of the Drawings**

[0015] The accompanying figures, where like reference numerals refer to identical or functionally similar elements throughout the separate views and which together with the detailed description below are incorporated in and form part of the specification, serve to further illustrate various embodiments and to explain various principles and advantages all in accordance with the present application.

[0016] Figure 1 illustrates a block diagram of a known transmitter.

[0017] Figure 2 illustrates a block diagram of one embodiment of a wireless communication device.

[0018] Figure 3 illustrates a communication system incorporating the device of Fig. 2.

[0019] Figure 4 illustrates a block diagram of one embodiment of phase shifter architecture in a transmitter.

[0020] Figure 5 illustrates a block diagram of one embodiment of a transmitter.

[0021] Figure 6 is a flowchart of one embodiment of a linearization training process.

[0022] Figure 7 is a flowchart of another embodiment of a linearization training process.

[0023] Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

**Description of Preferred Embodiments**

[0024] The following detailed description is merely exemplary in nature and is not intended to limit the invention defined by the claims or the application and uses of such invention. Furthermore, there is no intention to be bound by any expressed or
implied theory presented in the preceding technical field, background, brief summary or the following detailed description. As used herein, the word "exemplary" means "serving as an example, instance, or illustration." Any embodiment described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments. All of the embodiments described in this Detailed Description are exemplary embodiments provided to enable persons skilled in the art to make or use the invention and not to limit the scope of the invention, again which is defined by the claims.

[0025] Before describing in detail the embodiments, it should be observed that the embodiments reside primarily in combinations of method steps and apparatus components related to a transmitter containing a dual phase shifter. Accordingly, the apparatus components and method steps have been represented where appropriate by conventional symbols in the drawings, showing only those specific details that are pertinent to understanding the embodiments so as not to obscure the disclosure with details that will be readily apparent to those of ordinary skill in the art having the benefit of the description herein.

[0026] In various embodiments, a communication system contains a communication device, itself having a transmitter using in-phase and quadrature signals. The transmitter has a Cartesian feedback loop containing a forward path and, for each of the in-phase and quadrature signals, a feedback path. Each feedback path contains a phase shifter supplied with a different output from a phase training module such that in-phase and quadrature phase rotations provided by the phase shifters are separate and independent of each other. Each phase shifter is supplied with a local oscillator signal and a phase shifted local oscillator signal as well as a control signal from the phase training module. A first or second phase training signal is applied to the phase shifters respectively during a first or second training session. The second training session is shorter than the first training session. The phase shift at the output of each respective feedback path is repeatedly compared (during the appropriate phase training session) to the midpoint phase shift in a range of phase shifts, with the range being halved in each successive repetition. The initial range at the start of the second training session is smaller than that at the start of the first training session as the phase
rotation applied at the end of the first training session is used as the initial phase rotation applied at the start of the second training session.

[0027] Figure 2 illustrates a block diagram of an exemplary communication device 200. As shown, the communication device 200 is a handheld mobile device such as a Professional Mobile radio (PMR), cellular telephone, personal digital assistant (PDA), push-to-talk (PTT) radio, or wireless laptop computer, however, in other embodiments the communication device can be vehicle mounted or fixed to a particular geographic location, such as a base station.

[0028] The device 200 contains, among other components, a processor 202, a transceiver 204 including transmitter circuitry 206 and receiver circuitry 208, an antenna 222, a display 210, an input device(s) 212, a program memory 214 for storing operating instructions that are executed by the processor 202, a buffer memory 216, one or more communication interfaces 218, and a removable storage 220, all connected by a bus 230. Although not shown, the device 200 also preferably includes an antenna switch, duplexer, circulator, or other highly isolative means for intermittently providing information packets from the transmitter circuitry 206 to the antenna 222 and from the antenna 222 to the receiver circuitry 208. The device 200 is preferably an integrated unit containing at least all the elements depicted in Fig. 2, as well as any other elements necessary for the device 200 to perform its particular electronic function. Alternatively, the device 200 may comprise a collection of appropriately interconnected units or devices, wherein such units or devices perform functions that are equivalent to the functions performed by the elements of the device 200. For example, the device 200 may comprise a laptop computer and a Wireless Local Area Network (WLAN) card.

[0029] The processor 202 preferably includes one or more microprocessors, microcontrollers, DSPs, state machines, logic circuitry, or any other device or devices that process information based on operational or programming instructions. Such operational or programming instructions are preferably stored in the program memory 214. The program memory 214 may be an IC memory chip containing any form of random access memory (RAM) or read only memory (ROM), a floppy disk, a compact disk (CD) ROM, a hard disk drive, a digital video disk (DVD), a flash memory card or any other medium for storing digital information. One of ordinary
skill in the art will recognize that when the processor 202 has one or more of its functions performed by a state machine or logic circuitry, the memory 214 containing the corresponding operational instructions may be embedded within the state machine or logic circuitry. The operations performed by the processor 202 and the rest of the device 200 are described in detail below.

[0030] The transmitter circuitry 206 and the receiver circuitry 208 enable the device 200 to communicate information packets to and acquire information packets from the other nodes. In this regard, the transmitter circuitry 206 and the receiver circuitry 208 include appropriate, conventional circuitry to enable digital or analog transmissions over a wireless communication channel. The transmitter circuitry 206 and the receiver circuitry 208 are designed to operate over an ad hoc networking air interface (e.g., BLUETOOTH, 802.11 WLAN, Wi-Fi, WiMAX, . . . , etc.).

[0031] The implementations of the transmitter circuitry 206 and the receiver circuitry 208 depend on the implementation of the device 200. For example, the transmitter circuitry 206 and the receiver circuitry 208 may be implemented as an appropriate wireless modem, or as conventional transmitting and receiving components of two-way wireless communication devices. In the event that the transmitter circuitry 206 and the receiver circuitry 208 are implemented as a wireless modem, the modem can be internal to the device 200 or insertable into the device 200 (e.g., embodied in a wireless RF modem implemented on a Personal Computer Memory Card International Association (PCMCIA) card). For a wireless communication device, the transmitter circuitry 206 and the receiver circuitry 208 are preferably implemented as part of the wireless device hardware and software architecture in accordance with known techniques. One of ordinary skill in the art will recognize that most, if not all, of the functions of the transmitter circuitry 206 and/or the receiver circuitry 208 may be implemented in a processor, such as the processor 202. However, the processor 202, the transmitter circuitry 206, and the receiver circuitry 208 have been artificially partitioned herein to facilitate a better understanding.

[0032] The receiver circuitry 208 is capable of receiving RF signals from at least one band and optionally more bands, if the communications with the proximate device are in a frequency band other than that of the network communications. The receiver circuitry 208 may optionally comprise a first receiver and a second receiver, or one
receiver capable of receiving in two or more bandwidths. The receiver 208, depending on the mode of operation, may be attuned to receive, for example, Bluetooth or WLAN, such as 102.11, communication signals. The transceiver 204 includes at least one set of transmitter circuitry 206. The transmitter circuitry 206 may be capable of transmitting to multiple devices potentially in multiple frequency bands. The receiver circuitry 208 includes, for example, receiver front-end circuitry (effectively providing reception, filtering and intermediate or base-band frequency conversion), a signal processor (generally realized by at least one digital signal processor (DSP)) serially coupled to the front-end circuitry, a controller to calculate receive bit-error-rate (BER) or frame-error-rate (FER) or similar link-quality measurement data from recovered information via a received signal strength indication (RSSI) function, a memory to store data such as decoding/encoding functions, amplitude and phase settings to ensure a linear and stable output, and a timer to control the timing of operations, namely the transmission or reception of time-dependent signals. As shown in Fig. 2, the signal processor and controller may be provided by the processor 202 and the receiver memory may be provided in the program memory 214.

[0033] The antenna 222 comprises any known or developed structure for radiating and receiving electromagnetic energy in the frequency range containing the wireless carrier frequencies. Although not shown, the antenna 222 may be coupled to a switch that provides signal routing control of radio frequency (RF) signals in the device 200, as well as isolation between the transmitter circuitry 206 and the receiver circuitry 208. Alternatively, the switch could be replaced with a duplex filter, for frequency duplex devices as known to those skilled in the art. The buffer memory 216 may be any form of volatile memory, such as RAM, and is used for temporarily storing received information packets. The display 210 may be an LCD, OLED, or any other known display. The Input Device 212 may be one or more of: an alpha-numeric keyboard, isolated buttons, soft and/or hard keys, touch screen, jog wheel, or any other known input device.

[0034] A block diagram of a system using the device of Fig. 2 is shown in Fig. 3. As shown, the system 300 contains multiple communication devices 302, 304, 306, 308, 310. One of the devices 302 transmits to at least one of the other devices 302, 304,
This communication may be direct, i.e., device-to-device, or indirect, employing base stations 320 and other infrastructure 330. The devices 302, 304, 306, 308, 310 may be the same type of device (as shown, e.g., 302, 304, 306, 310) or different (as shown, e.g., 304 and 308). As shown, when communicating in direct mode (without using the infrastructure 320, 330), the receiving devices 304, 306, 308 receive the communication either directly (204, 308) or using one of the receiving devices 304 as an intermediary to forward the data to other of the receiving devices 306.

[0035] As above, prior to transmitting real data, the transmitter 206 of the device 200 employs a training algorithm to determine appropriate gain and phase adjustment parameters to ensure a stable, linear output from the transmitter during transmission of the real data. To this end, the transmitter employs a phase shifter architecture that is based on separate and independent in-phase (I channel) and quadrature (Q channel) phase rotation. One example of such phase shifter architecture is illustrated in Fig. 4. In this structure 400, the VCO (voltage controlled oscillator) 402 generates an RF carrier at twice the transmit carrier frequency (2/0 or 2ω0), which is then provided to a divide-by-2 (÷2) quadrature generator 404 that generates I and Q quadrature signals (I = cos(ωt), Q = sin(ωt)). Each of the I and Q signals are provided to a low pass filter 406, 408 and the low pass filtered I and Q signals are supplied to pairs of I and Q mixers 410, 412 and 414, 416 and to an up mixer 422 that converts the I and Q signals to transmission signals. The I and Q mixers 410, 412 and 414, 416 are also supplied with phase shift signals sin(γ), cos(γ) that are 90° out of phase. The mixed signals from each pair of mixers 410, 412 and 414, 416 are then combined at a respective I and Q summers 418, 420. The I summer 418 subtracts the sin(γ) mixed I component from the cos(γ) mixed I component to form F. The Q summer 420 adds the sin(γ) mixed Q component to the cos(γ) mixed Q component to form Q. The F and Q’ signals are provided to a down mixer 424. As illustrated, F and Q’ are:

\[
\begin{align*}
&W\cos\omega_0 - Q\sin\omega_0 \quad (1) \\
Q' &= Q\cos(\gamma) + Ism(\gamma) \quad (2)
\end{align*}
\]

Thus, as I = cos(ωt) and Q = sin(ωt):
\[ I' = \cos(\omega t)\cos(f) - \sin(\omega t)\sin(f) = \cos(\omega t + \gamma) \quad (3) \]

\[ Q = \sin(\omega t)\cos(f) + \cos(\omega t)\sin(f) = \sin(\omega t + \gamma) \quad (4) \]

[0036] The dual phase shifter architecture 400 of Fig. 4 has a number of benefits: it is wideband, reduces the number of frequency doublers (which are inherently relatively noisy) that are used in other architectures without dual phase shifting, and solves problems of other architectures related to IQ ambiguity during phase training because there is only one divide-by-2 quadrature generator and it is driven by a constant \( \omega \) VCO signal. However, the dual phase shifter architecture of Fig. 4, while having significant advantages over other architectures, also engenders a new problem: a not-insubstantial amount of IQ imbalance is introduced due to the fact that the I and Q quadrature signals are shifted by separate mixers. Furthermore, unlike other architectures, in which the phase shifts of both the I and Q channels are measured, a calculation is performed to determine the proper amount of adjustment, and then the adjustment applied, in the present architecture such a calculation is avoided (one phase shift is measured and the adjustment applied before the other measurement and adjustment - calculation to determine the proper amount of adjustment for both channels after both measurements are taken is avoided).

[0037] To solve this new problem, Fig. 5 illustrates a block diagram of a dual phase shifter architecture of a transmitter 500. The transmitter 500 is supplied with analog baseband signals (I and Q signals). Each of the I and Q signals are respectively supplied to a summer 502, 512. The signal from each of the summers 502, 512 is amplified by a corresponding amplifier 504, 514 of predetermined or variable gain and then respectively passed through a low-pass filter 506, 516. Note that although the term amplifier is used through these embodiments, the amplifier can act as, or in conjunction with, an attenuator.

[0038] The resulting low-pass filtered signals are then up-converted by a mixer 508, 518 supplied with signals at the desired frequency (\( \omega \)) from a local oscillator (LO) 560 and phase shifted by a 90° phase shifter 510 (i.e., either \( \sin(\omega t) \) or \( \cos(\omega t) \)). The upconverted signals are then combined at a summer 520, amplified by a power amplifier 522 of predetermined (or variable) gain and supplied to an antenna 540. A directional coupler 538 feeds a portion of the transmitted signal back to down-converting mixers 524, 526 where the fed-back signal is mixed with a phase-shifted
version of the signal from the LO 560, which includes using a 90° phase shifter 542 to phase shift the local oscillator signal. The shifted signal from the phase shifter 542 and the signal fed to the phase shifter 542 are provided to individual I and Q channel phase shifters \( \phi_i, \phi_q \) 544, 546. The signals supplied from the \( \phi_i, \phi_q \) phase shifters 544, 546 have a respective phase imbalance \( \alpha_i, \alpha_q \) 548, 550 and are respectively supplied to the mixer 524, 526. The output of each mixer 524, 526 is low-pass filtered by a low pass filter 528, 532 and then this feedback signal \( Q_{ib}, I_{ib} \) respectively fed to a summer 502, 512 through a switch 534, 536. As above, the switches 534, 536 are open in training mode and closed during normal operation. The feedback signals \( Q_a, I_b \) are also supplied to phase training module 530, which is used for SAR phase training and IQ imbalance correction and correspondingly controls the phase shift provided by the \( \phi_i, \phi_q \) phase shifters 544, 546 using control signals supplied to the \( \phi_i, \phi_q \) phase shifters 544, 546. The phase correction is made in real-time.

[0039] Referring to Fig. 6, a method of correcting IQ phase imbalance in the transmitter of Fig. 5 containing dual phase shifters is shown. As is apparent, multiple (as shown, two) phase trainings are performed to correct the IQ phase imbalance. When IQ phase correction is to occur (i.e., before or between when signals are to be transmitted by the open loop transmitter 500), the switches 534, 536 are open so that Cartesian feedback loop is open. With the Cartesian feedback loop open, a first training signal is supplied to the I and Q channel summers 502, 512 during a first phase training session at step 602. A training signal, as used herein, is defined by both in-phase and quadrature inputs. Specifically, the analog inputs of the first training signal are, \( I_u = 1 \) Volt (or some other positive voltage depending on implementation) and \( Q_m = 0 \) Volt. During the first phase training session, the SAR algorithm changes the phase shift \( \phi_q \) of the Q-channel phase shifter until \( Q_a = 0 \).

[0040] The SAR algorithm operates using a successive halving method in which a value representing the unknown phase shift is compared to a series of values representing predetermined phase shifts in a range of phase shifts. The range is divided into halves and the midpoint used to determine whether the unknown (in this case, \( \phi_q \)) phase shift is larger or smaller than the midpoint. The midpoint of the half of the phase shift range in which the unknown phase shift lies is selected and the unknown phase shift compared against this new midpoint. This continues until the
unknown phase shift is determined. Thus, generally, the unknown phase shift is repeatedly compared with a phase shift in a particular range of phase shifts, each range of phase shifts being a member of a predetermined set of phase shifts and being reduced with each successive repetition. In a typical embodiment, an eleven digit binary number is selected and then converted into an analog signal by a digital-to-analog converter (DAC). The analog output is then compared to a value corresponding to the unknown phase shift. As an eleven digit binary number is used, the SAR algorithm operates has ten steps, with the initial midpoint being 0111111111 and the next step being x0111111111 (where x can be 0 or 1 depending on whether the value representing the unknown phase shift is respectively smaller than or larger than the midpoint).

Mathematically, the $Q_{fb}$ signal during first phase training 602 can be described as:

$$Q_{fb} = LPF\{ \hat{u}(n(\omega t - \theta) \cos(\omega t - \hat{\phi}_Q - a_Q)) \} \quad (S)$$

where $\theta$ is the Cartesian loop phase shift and the other symbols have the meanings provided above. Using the standard trigonometric relationships, this can be rewritten as:

$$Q_{fb} = LPF\{ \sin(2\omega t - \theta - \hat{\phi}_Q - a_Q) + \sin(-0 + \hat{\phi}_Q + a_Q) \} \quad (6)$$

which, when low-pass filtered, removes the $\sin(2\omega t)$ portion. This leaves the $Q$-channel phase shift as:

$$Q_f = \sin(-\theta + \hat{\phi}_Q + a_Q) \quad (7)$$

Thus, if it is desirable for $Q_a=0$, then the phase shifter $\Phi_Q$ is programmed such that $\Phi_Q = \theta - iX_Q$ during the first phase training session in step 606. $Q_{fb}$ will be close to zero at the end of SAR algorithm execution.

Next, a second phase training session is performed using $I_n=0$ Volt and $Q_m=1$ Volt at step 608. During the second phase training session, the SAR algorithm is used to change the I-channel phase shifter $\Phi$ until $I_a=0$ in step 610 in a manner similar to the above. Mathematically, this is represented in equations (8)-(10) below in a similar fashion as equations (5)-(7):
\[ I_\beta = \text{LPF}\{\cos(\omega t - \theta)\sin(\omega t - \phi_f - \Delta \chi_f)\} \] (8)

where again, using the standard trigonometric relationships, this can be rewritten as:

\[ I_\beta = \text{LPF}\{\sin(2\omega t - \theta - \phi_f - C \chi_f) - \sin(\# + \phi_f + \alpha_f)\} \] (9)

which, when low-pass filtered, removes the \(\sin(2\omega t)\) portion. This leaves the I-channel phase shift as:

\[ I_{\text{fb}} = \text{sm}(-\theta + \phi_f + a_f) \] (10)

[0044] Thus, if it is desirable for \(I_a = 0\), then the I channel phase shifter \(\phi_i\) 544 is programmed such that \(\phi_i = \theta - \alpha_i\) during the second phase training in step 612. After programming both the I channel phase shifter \(\phi_i\) 544 and the Q channel phase shifter \(\phi_i\) 546, the IQ phase imbalance is now compensated at step 614 before the end of the allocated phase training period (predefined by the communication system used). Thus, the first and second phase training sessions are completed within the allocated phase training period. The compensation data can be stored in a memory 214 of the transmitter 500 and updated as desired. Previous compensation data can also be used as an initial starting point for each of the I and Q channels in later phase training sessions. Training can be performed at a convenient time period after specific event such as after a programmed amount of operation time of the transmitter or absolute (wall clock) time. After the IQ phase imbalance is compensated, the switches 534, 536 are closed so that Cartesian feedback loops are closed for both the I and Q channels and the transmitter 500 now transmits data to other devices at step 616.

[0045] However, in many systems (such as TETRA-based systems) the time allowed for phase training is limited. This becomes increasingly problematic if multiple phase trainings are to occur in this limited amount of time. To overcome this problem, it is recognized that in general the phase shift of the I channel will be fairly close to that of the Q channel. Thus, to reduce the training time to an acceptable amount, the final result of the first phase training \(\phi_q\) can be used as an initial condition for the second phase training. This permits the second phase training to perform only last few steps of the SAR algorithm, thus reducing total training time.
To this end, the modified method of correcting IQ phase imbalance in the transmitter of Fig. 5 containing dual phase shifters is illustrated in Fig. 7. The switches 534, 536 are opened and a first input is supplied to the I and Q channel summers 502, 512 at step 702. Specifically, the inputs of the second training signal are, digitally, $I_n = 1$ V and $Q_n = 0$ V. During the first phase training, the SAR algorithm changes the phase shift $\Phi_q$ of the Q-channel phase shifter until $Q_a = 0$ at step 704. When $Q_n = 0$, the Q channel phase shifter $\Phi_q$ 546 is programmed such that $\Phi_q = \Theta - \alpha_{Q}$ at step 706. The I channel phase shifter $\Phi_i$ 544 is also programmed such that $\Phi_i = \Phi_q$ at step 708.

The second phase training then begins in which $I_n = 0$ V and $Q_n = 1$ V at step 710. During the second phase training, the SAR algorithm changes the phase shift $\Phi_i$ of the I-channel phase shifter 544 until $I_a = 0$ at step 712. As the phase of the I channel $\Phi_i$ is already somewhat close, only the last five steps of the SAR algorithm are used. Using the above example provided in Fig. 6, the first six known digits of the eleven digit binary number determined during phase training of the Q channel are known and used, leaving the last five digits to be determined when training the I channel (e.g., taking about half the time as for the first training session for the second training session). This reduces the phase training time so that phase training is able to be accomplished in, for example, the amount of time allotted by the TETRA standard. If further reduction is desired, fewer digits can be used during the second phase training, although this also limits the range of phase correction values able to be provided. In any case, in the above embodiments, the second phase training session is shorter than the first phase training session. Thus, the initial range of phase shifts at the start of the first training session is smaller than the initial range of phase shifts at the start of the second training session.

When $I_a = 0$, the I channel phase shifter $\Phi_i$ 544 is programmed such that $\Phi_i = \Theta - \alpha_i$ at step 714. After programming both the I channel phase shifter $\Phi_i$ 544 and the Q channel phase shifter $\Phi_i$ 546, the IQ phase imbalance is now compensated at step 716. This data can be stored in a memory 214 of the transmitter 500 and updated. After the IQ phase imbalance is compensated, the switches 534, 536 are closed so that Cartesian feedback loops are closed for both the I and Q channels and the transmitter 500 now transmits data to other devices at step 718.
[0049] Note that in either transmitter 500, 600 shown in Figs. 5 and 6, although quadrature phase imbalance compensation has been applied in the down-mixed feedback path, in other embodiments the compensation may be applied to in the up-mixed direct path as the phase imbalance is actually the sum of the up and down-mix I-Q generator imbalance. In addition, once phase training has been performed, resulting in a quadrature phase balance between the I- and Q-channel, quadrature amplitude imbalance between the I-channel and Q-channels may be performed to ensure that there is minimal I-Q leakage.

[0050] It will be understood that the terms and expressions used herein have the ordinary meaning as is accorded to such terms and expressions with respect to their corresponding respective areas of inquiry and study except where specific meanings otherwise have been set forth herein. Relational terms such as first and second and the like may be used solely to distinguish one entity or action from another entity or action without necessarily requiring or implying any actual such relationship or order between such entities or actions. The terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus. An element proceeded by "comprises …a" does not, without more constraints, preclude the existence of additional identical elements in the process, method, article, or apparatus that comprises the element.

[0051] It will be appreciated that some or all functions could be implemented by a state machine that has no stored program instructions, or in one or more application specific integrated circuits (ASICs), in which each function or some combinations of certain of the functions are implemented as custom logic. Of course, a combination of the two approaches could be used. Thus, methods and means for these functions have been described herein.

[0052] In various embodiments, the disclosed methods may be implemented as a computer program product for use with a computer system. Such implementations may include a series of computer instructions fixed either on a tangible medium, such as a computer readable medium (e.g., a diskette, CD-ROM, ROM, or fixed disk) or transmittable to a computer system, via a modem or other interface device, such as a
communications adapter connected to a network over a medium. The medium may be either a tangible medium (e.g., optical or analog communications lines) or a medium implemented with wireless techniques (e.g., microwave, infrared or other transmission techniques). The series of computer instructions embodies all or part of the functionality previously described herein with respect to the system. Those skilled in the art should appreciate that such computer instructions can be written in a number of programming languages for use with many computer architectures or operating systems. Furthermore, such instructions may be stored in any memory device, such as semiconductor, magnetic, optical or other memory devices, and may be transmitted using any communications technology, such as optical, infrared, microwave, or other transmission technologies. It is expected that such a computer program product may be distributed as a removable medium with accompanying printed or electronic documentation (e.g., shrink wrapped software), preloaded with a computer system (e.g., on system ROM or fixed disk), or distributed from a server or electronic bulletin board over the network (e.g., the Internet or World Wide Web). Of course, some embodiments of the invention may be implemented as a combination of both software (e.g., a computer program product) and hardware. Still other embodiments are implemented as entirely hardware, or entirely software (e.g., a computer program product).

[0053] The Abstract of the Disclosure is provided to allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, it can be seen that various features are grouped together in various embodiments for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separately claimed subject matter.

[0054] Those skilled in the art will recognize that a wide variety of modifications, alterations, and combinations can be made with respect to the above described
embodiments without departing from the spirit and scope of the invention defined by any claims issuing herefrom, and that such modifications, alterations, and combinations are to be viewed as being within the inventive concept. Thus, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention. The benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the issuing claims. The invention is defined solely by the issuing claims including any amendments made and all equivalents of those claims.
Claims

1. A wireless communication device comprising a transmitter using in-phase and quadrature signals, the transmitter comprising a Cartesian feedback loop having a forward path and a feedback path for each of the in-phase and quadrature signals, each feedback path containing a phase shifter supplied with a different output from a phase training module such that in-phase and quadrature phase rotations provided by the phase shifters are separate and independent of each other.

2. The device of claim 1, further comprising a local oscillator that produces a local oscillator signal and a 90° phase shifter supplied with the local oscillator signal and that provides a phase shifted local oscillator signal, wherein each feedback path further comprises a down-converting mixer, one of the down-converting mixers mixing a feedback signal with a first phase rotated signal from one of the phase shifters and the other of the down-converting mixers mixing the phase shifted local oscillator signal with a second phase rotated signal from the other of the phase shifters.

3. The device of claim 2, wherein each phase shifter is supplied with the local oscillator signal and the phase shifted local oscillator signal as well as a control signal from the phase training module.

4. The device of claim 3, wherein each feedback path further comprises a low pass filter to which a mixer output from the corresponding mixer is supplied, the low pass filters providing low pass filtered in-phase and quadrature feedback signals to the phase training module, and to the forward path as well only when the transmitter is not in a phase training mode.

5. The device of claim 4, wherein the transmitter is operable to apply a first phase training signal to the phase shifters during a first training session and a second phase training signal that is different from the first training signal to the phase shifters during a second training session, the second training session being shorter than the first training session.
6. The device of claim 1, wherein the in-phase phase rotation is $\phi_i = \theta - \alpha_i$ and the quadrature phase rotation is $\Phi_Q = \theta - \alpha_Q$, where $\theta$ is a loop phase shift and $\alpha_i$ and $\alpha_Q$ are in-phase and quadrature phase imbalances, respectively.

7. A method of linearizing a transmitter, the method comprising:
   - applying a first training signal to the transmitter;
   - determining a first quadrature imbalance of one of in-phase or quadrature feedback signal, the in-phase and quadrature feedback signals being supplied respectively in in-phase and quadrature feedback paths of the transmitter and being provided to a forward path of the transmitter only when the first training signal is not applied;
   - providing one of an in-phase or quadrature phase rotation in the in-phase and quadrature feedback path, respectively, based on the determination of the first quadrature imbalance, the in-phase or quadrature phase rotation corresponding to which of the in-phase and quadrature feedback signals is measured for the determination of the first quadrature imbalance;
   - applying a second training signal to the transmitter, the first and second training signals being different and being applied at different times within an allotted training period;
   - determining a second quadrature imbalance of the other of the in-phase or quadrature feedback signals when the second training signal is applied; and
   - providing the other of the in-phase or quadrature phase rotation based on the determination of the second quadrature imbalance, the in-phase and quadrature phase rotations being separate and independent of each other.

8. The method of claim 7, further comprising:
   - providing a local oscillator signal at a frequency employed for up-conversion and down-conversion in the transmitter;
   - providing $90^\circ$ phase shift for the local oscillator signal to produce a phase shifted local oscillator signal; and
down-converting the feedback signal using a first phase rotated signal produced by the one of the in-phase or quadrature phase rotation and a second phase rotated signal produced by the other of the in-phase or quadrature phase rotation.

9. The method of claim 8, further comprising producing each of the first and second phase rotated signals using the local oscillator signal, the phase shifted local oscillator signal, and a control signal to adjust the first or second phase rotated signal being produced.

10. The method of claim 9, further comprising controlling the production of each of the first and second phase rotated signals using a low-pass filtered, down-converted version of the first or second phase rotated signal being produced, the low-pass filtered, down-converted versions of the first and second phase rotated signals being supplied to the forward path.

11. The method of claim 10, wherein each of the first and second phase training signals is respectively applied during a first and second phase training session, the method comprising limiting the duration of the second training session to be shorter than the duration of the first training session.

12. The method of claim 11, wherein limiting the duration of the second training session comprises decreasing the number of steps performed by a SAR (Successive Approximation Register) algorithm used by a phase training module that provides the control signals.

13. The method of claim 12, wherein decreasing the number of steps comprises using the one of the in-phase or quadrature phase rotation provided after the first training session as an initial phase rotation to be applied as the other first and second quadrature phase rotated signals at the start of the second training session.

14. The method of claim 12, wherein the phase training module repeatedly compares the low-pass filtered, down-converted version of the first or second
quadrature phase rotated signal to a midpoint phase shift in a range of phase shifts, the
range of phase shifts being provided from a predetermined set of ranges and being
reduced with each successive repetition, an initial range at the start of the second
training session being smaller than an initial range at the start of the first training
session.

15. The method of claim 8, wherein the in-phase phase rotation is \( \phi_i = \theta - \alpha_i \) and
the quadrature phase rotation is \( \Phi_Q = \theta - \alpha_Q \), where \( \theta \) is a loop phase shift and \( \alpha_i \) and
\( \alpha_Q \) are in-phase and quadrature phase imbalances, respectively.
START 1\textsuperscript{st} PHASE TRAINING $I_{in} = 1; Q_{in} = 0$

PHASE TRAINING SAR ALGORITHM ON Q-CHANNEL PHASE SHIFTER $\Phi_Q$

PROGRAM SAR RESULT INTO Q-CHANNEL PHASE SHIFTER $\Phi_Q$

START 2\textsuperscript{nd} PHASE TRAINING $I_{in} = 0; Q_{in} = 1$

PHASE TRAINING SAR ALGORITHM ON I-CHANNEL PHASE SHIFTER $\Phi_I$

PROGRAM SAR RESULT INTO I-CHANNEL PHASE SHIFTER $\Phi_I$

IQ PHASE IMBALANCE COMPENSATED

TRANSMIT DATA

FIG. 6
START 1\textsuperscript{st} PHASE TRAINING $I_{in} = 1; Q_{in} = 0$

PHASE TRAINING SAR ALGORITHM ON Q-CHANNEL PHASE SHIFTER $\phi_Q$

PROGRAM SAR RESULT INTO Q-CHANNEL PHASE SHIFTER $\phi_Q$

PROGRAM SAR RESULT INTO I-CHANNEL PHASE SHIFTER $\phi_I$

START 2\textsuperscript{nd} PHASE TRAINING $I_{in} = 0; Q_{in} = 1$

PHASE TRAINING SAR ALGORITHM ON I-CHANNEL PHASE SHIFTER $\phi_I$ [ONLY LAST 5 STEPS]

PROGRAM SAR RESULT INTO I-CHANNEL PHASE SHIFTER $\phi_I$

IQ PHASE IMBALANCE COMPENSATED

TRANSMIT DATA

FIG. 7