United States Patent [19]

Berg

[11] **3,728,710**

[45] **Apr. 17, 1973**

[54] CHARACTER DISPLAY TERMINAL

[75] Inventor: **Nephi Edward Berg**, Bedford, N.H.

[73] Assignee: **Hendrix Wire & Cable Corp.**, Milford, N.H.

[22] Filed: **Dec. 1, 1969**

[21] Appl. No.: **881,105**

Related U.S. Application Data

[63] Continuation-in-part of Ser. Nos. 587,583, Oct. 18, 1966, and Ser. No. 835,591, June 23, 1969.

[52] **U.S. Cl.**.....**340/324 A**, 340/152, 340/172.5

[51] **Int. Cl.**.....**G06f 3/14**

[58] **Field of Search**.....340/324, 152–154, 340/172.5

[56] **References Cited**

UNITED STATES PATENTS

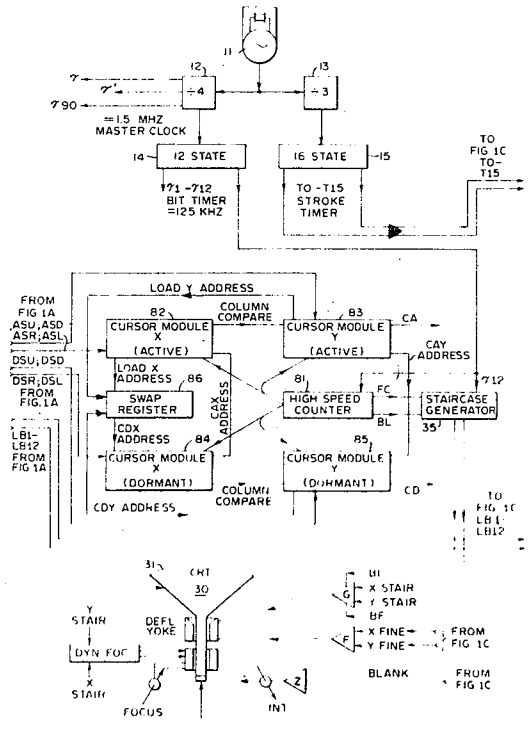
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Primary Examiner—John W. Caldwell
Assistant Examiner—Marshall M. Curtis
Attorney—Frederick D. Goode

[57] **ABSTRACT**

A synchronous refresh memory CRT Display Terminal continuously generates the individual deflection waveforms for the complete repetoire of characters and symbols which it is desired to display. The recirculating memory provides storage for the identity code and editing tags for each character position on the CRT display and recirculation in the memory loop is synchronized with a character by character beam deflection of the CRT to provide a page format indication. Provision is made for reading into the memory loop the character identity code at a preselected position corresponding to the screen character location at which the character is to be displayed and once in memory the refresh rate will continually display the character sequence in the memory loop in the corresponding sequence of character positions on the screen format with only the code address for each character being read from memory and upon decoding selecting from the repetoire character generator each so identified character for display by the continuously generated fine waveform deflection signals. An active and dormant cursor are presented on the screen generated in the same manner as any character or symbol but controllable as to position at will to identify the screen location for insertion and deletions. Editing controls for the cursors and the insertion and deletion operations independent of memory permit a full range of editing functions to be performed on the character content of the memory and display screen.

22 Claims, 31 Drawing Figures



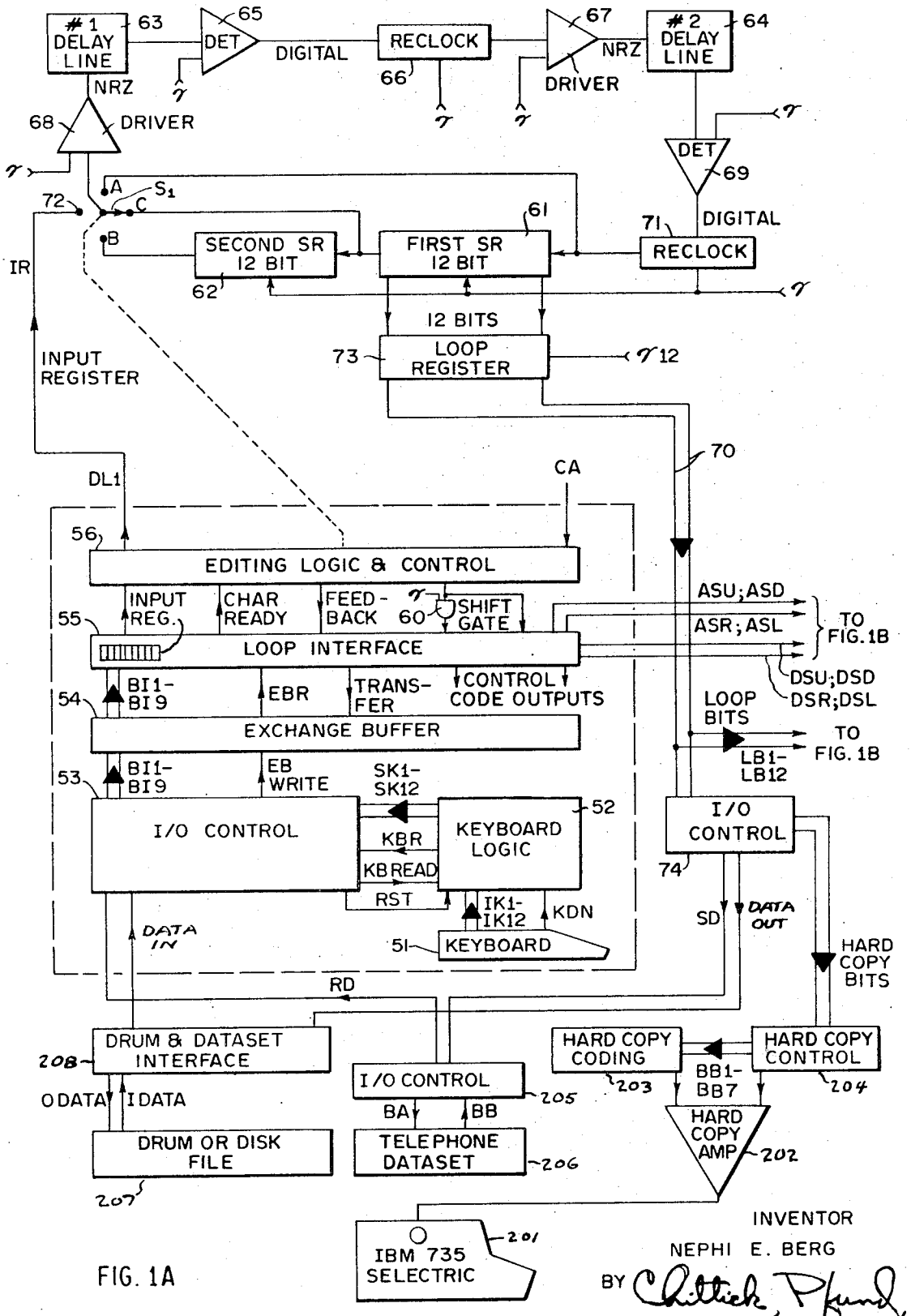


FIG. 1A

INVENTOR
NEPHI E. BERG
BY Chittick, Pfund, Birch, Samuels & Gauthier
ATTORNEYS

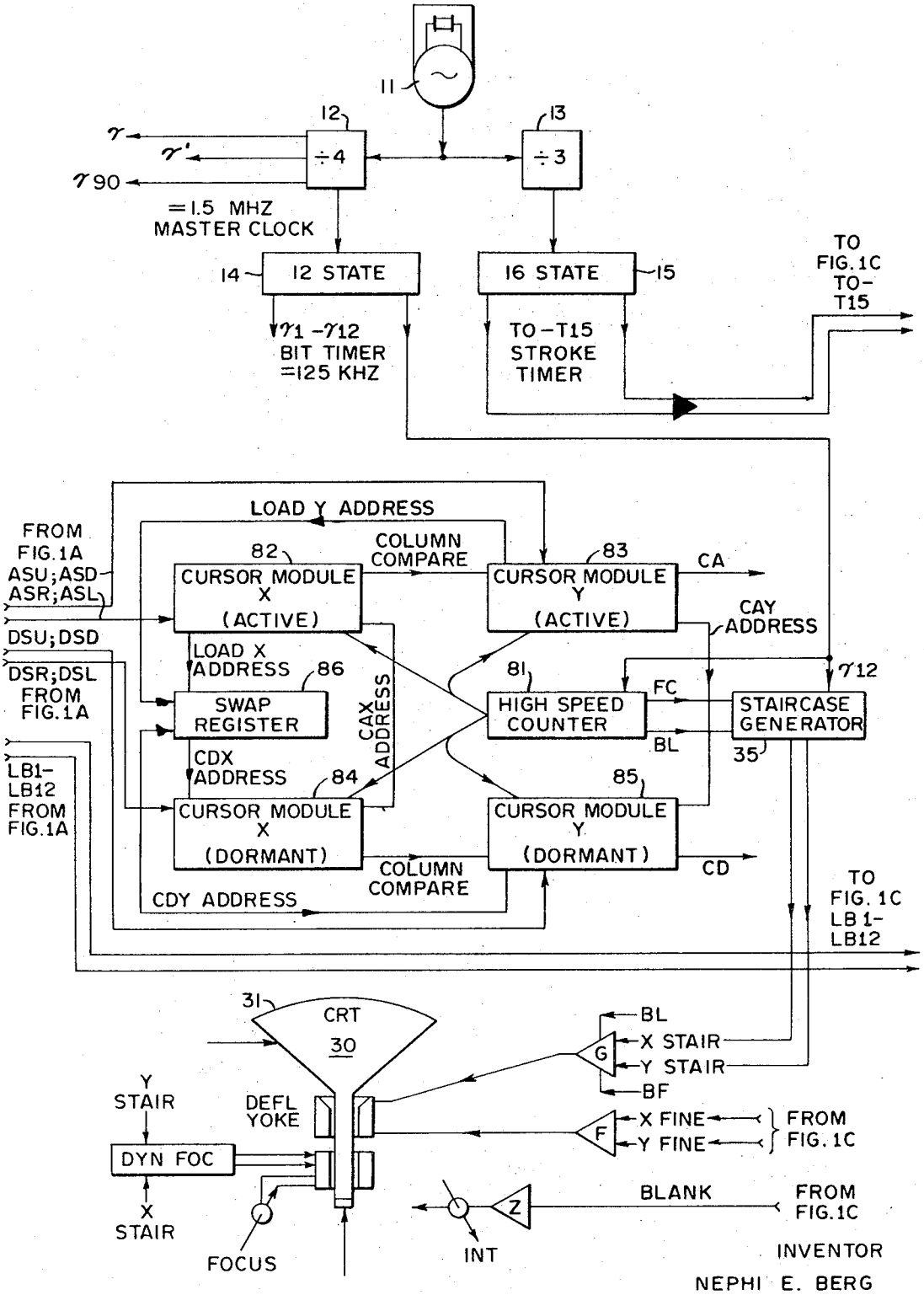


FIG. 1B

INVENTOR
NEPHI E. BERG

BY Chittick, Pfund, Birch, Samuels & Gauthier
ATTORNEYS

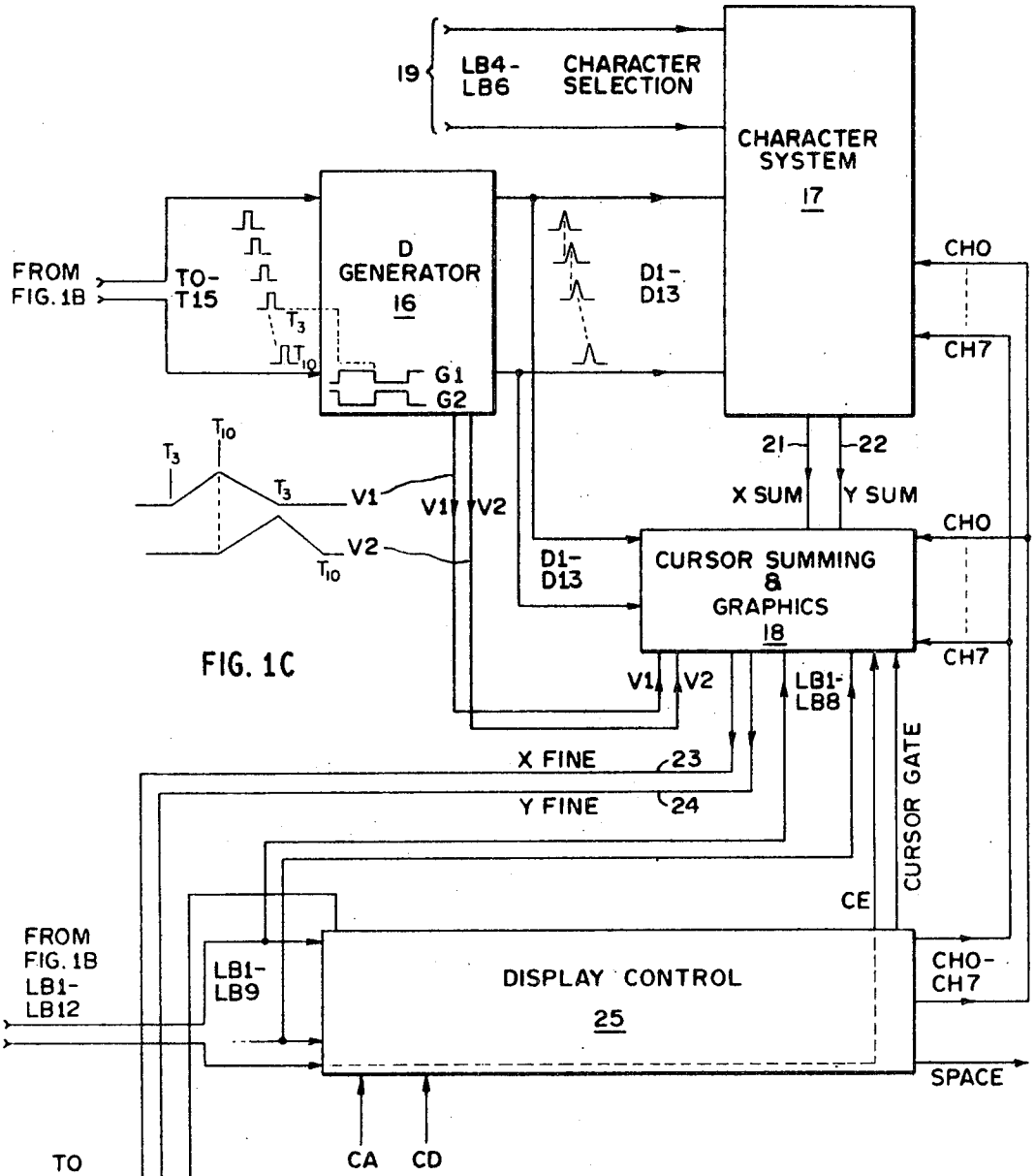


FIG. 1C

FIG. 1D

INVENTOR
NEPHI E. BERG
BY Chittick, Pfund, Birch, Samuels & Gauthier
ATTORNEYS

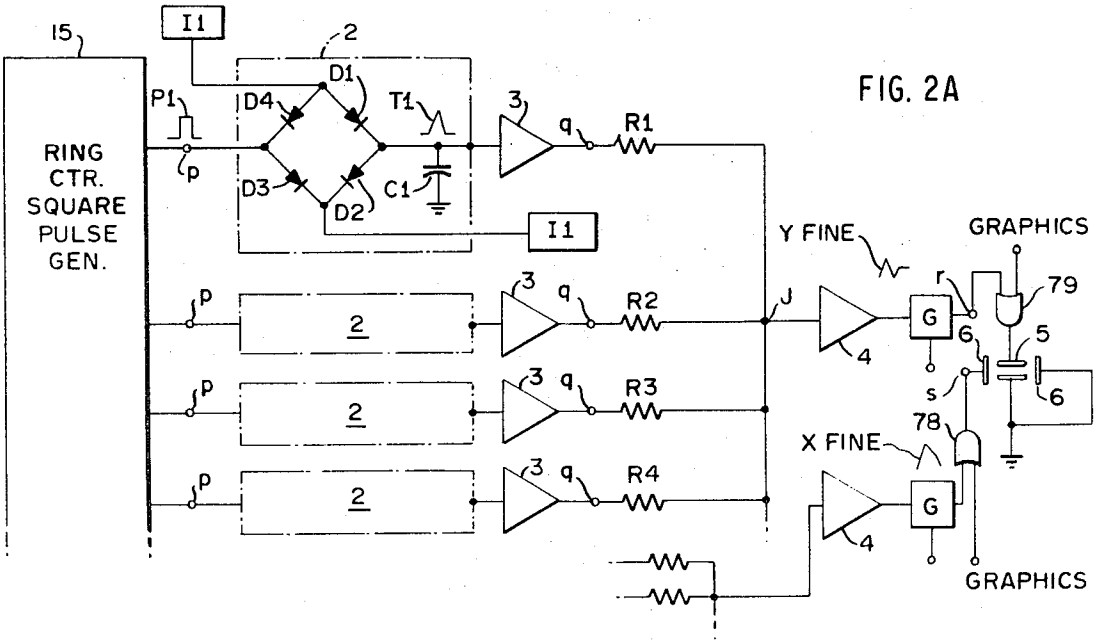


FIG. 2A

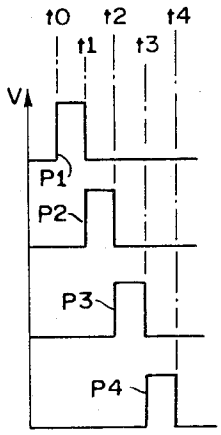


FIG. 2B

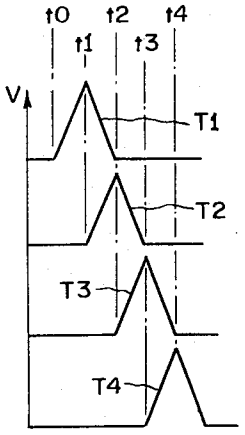


FIG. 2C

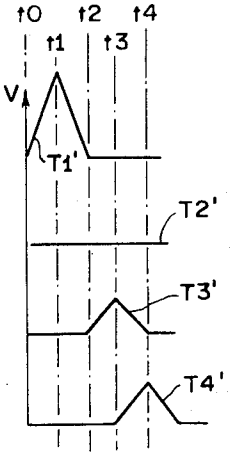


FIG. 2D

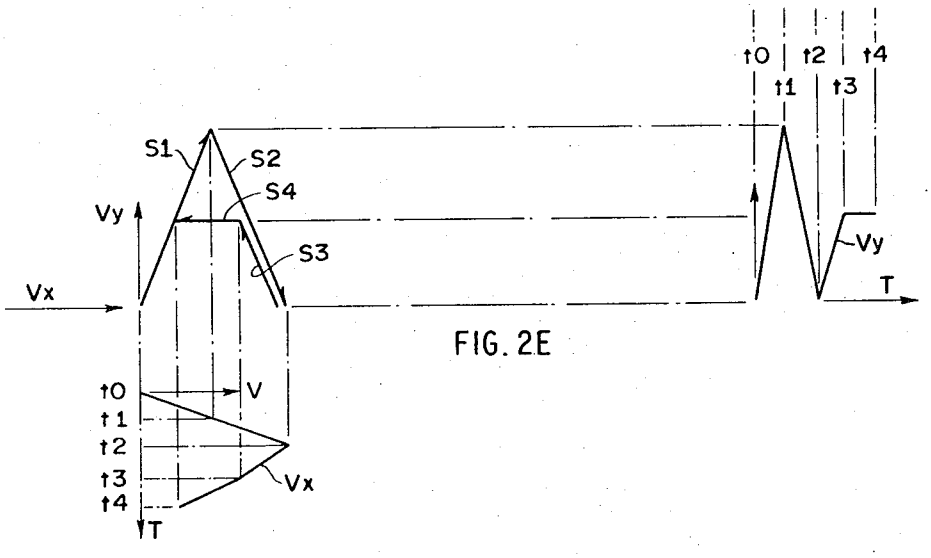
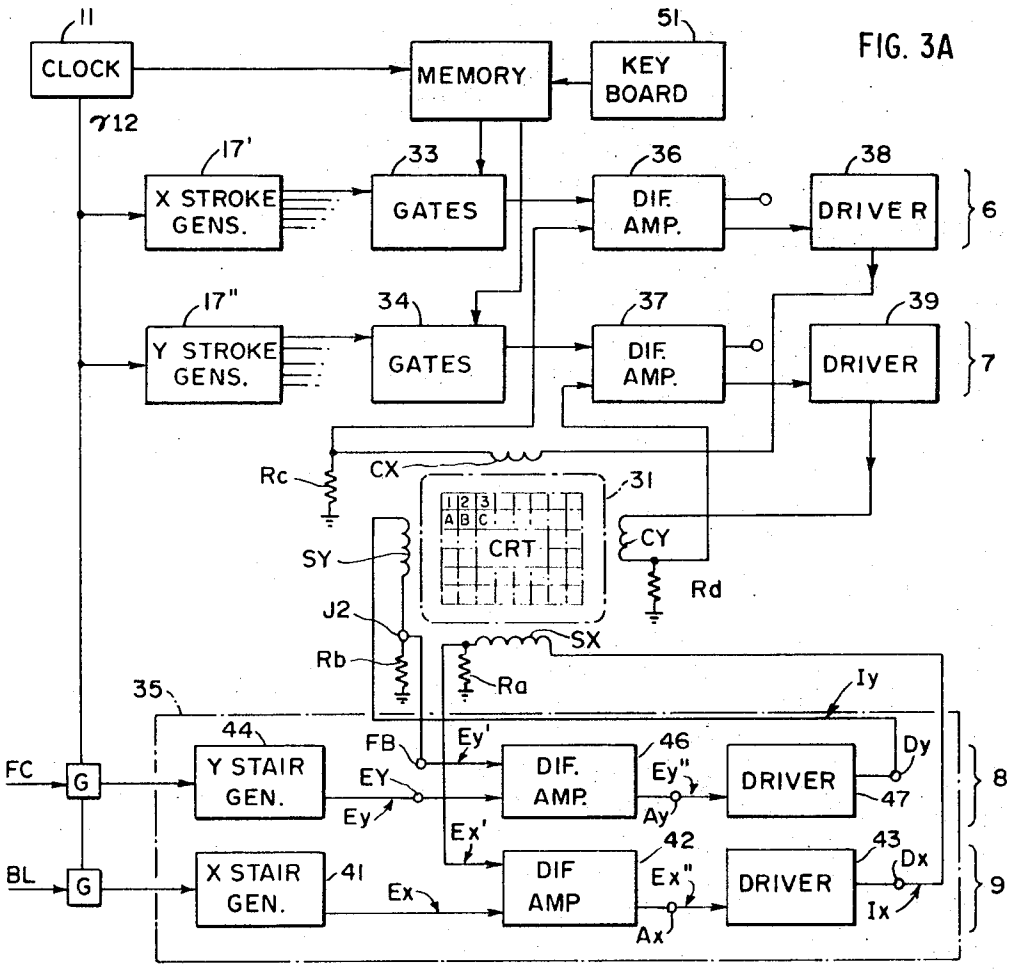


FIG. 2E


11
CLOCK
712
MEMORY
51
KEY BOARD
17'
X STROKE GENS.
33
GATES
36
DIF. AMP.
38
DRIVER
6
17"
Y STROKE GENS.
34
GATES
37
DIF. AMP.
39
DRIVER
7
Rc
CX
31
CRT
CY
Rd
SY
J2
Rb
SX
Ra
Iy
35
44
Y STAIR GEN.
FB
Ey'
EY
Ey
46
Ey"
Ay
DIF. AMP.
DRIVER
Dy
47
8
FC
G
BL
G
X STAIR GEN.
41
Ex
Ex'
DIF AMP
42
Ex"
Ax
DRIVER
43
Dx
Ix
9

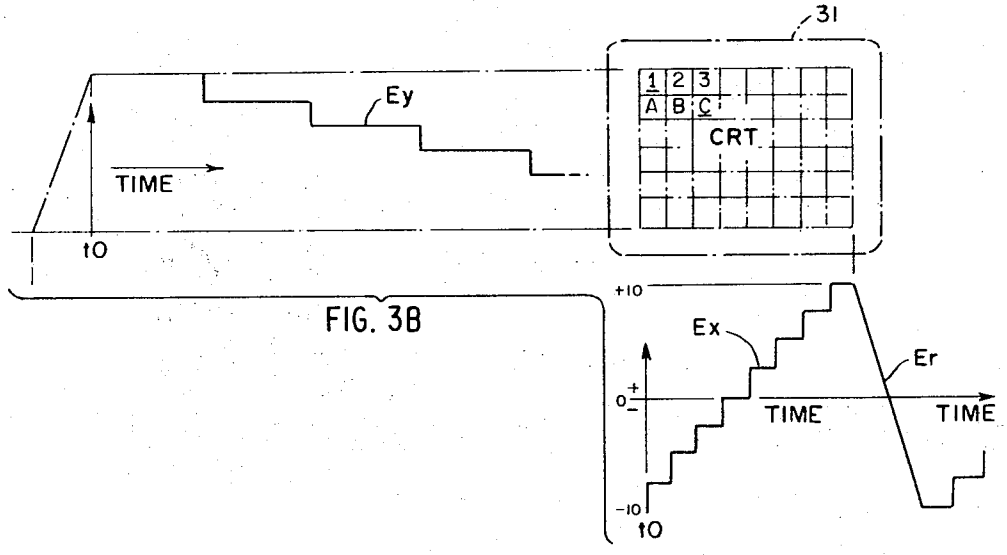

31
Ey
TIME
t0
1 2 3
A B C
CRT
+10
Ex
Er
0
TIME
TIME
-10
t0

FIG. 3B

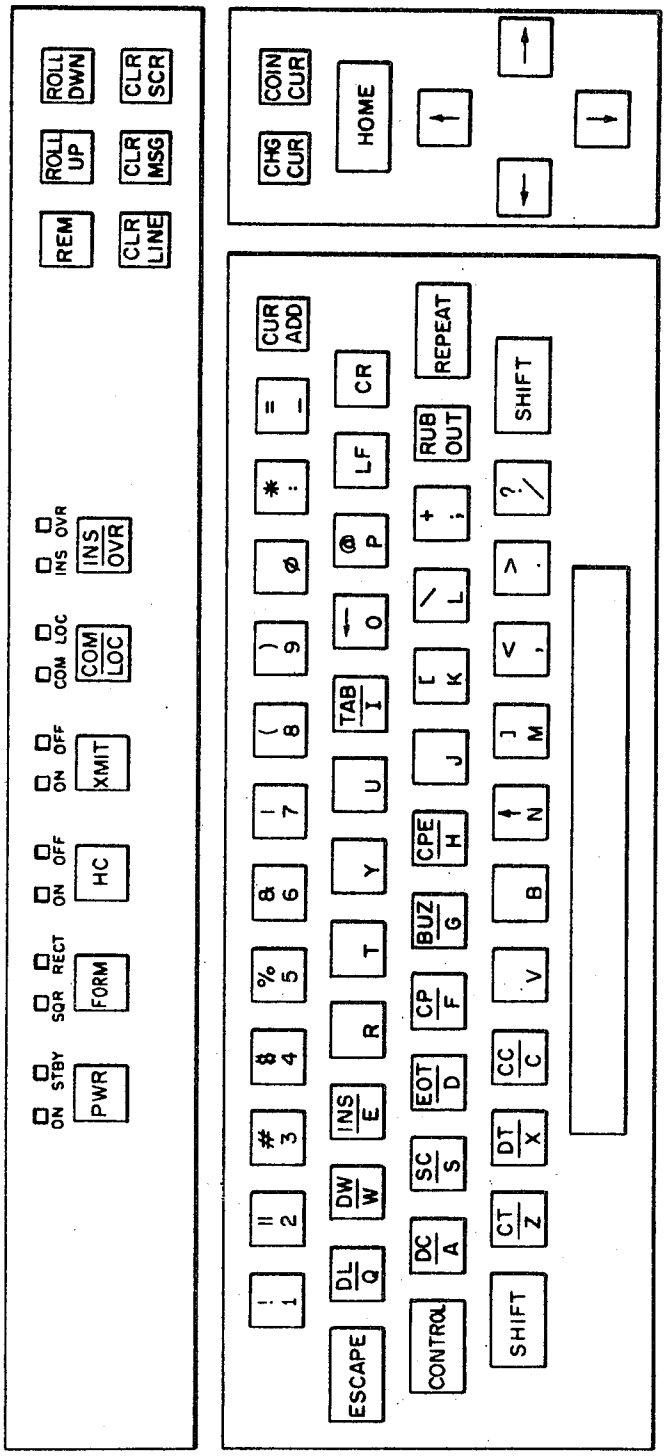

ON STBY
PWR
SQR RECT
FORM
ON OFF
HC
ON OFF
XMIT
COM LOC
COM LOC
INS OVR
INS OVR
REM
CLR LINE
ROLL UP
CLR MSG
ROLL DWN
CLR SCR
CHG CUR
COIN CUR
HOME
ESCAPE
CONTROL
SHIFT
SHIFT
REPEAT
RUB OUT
CR
LF
CUR ADD

FIG. 4

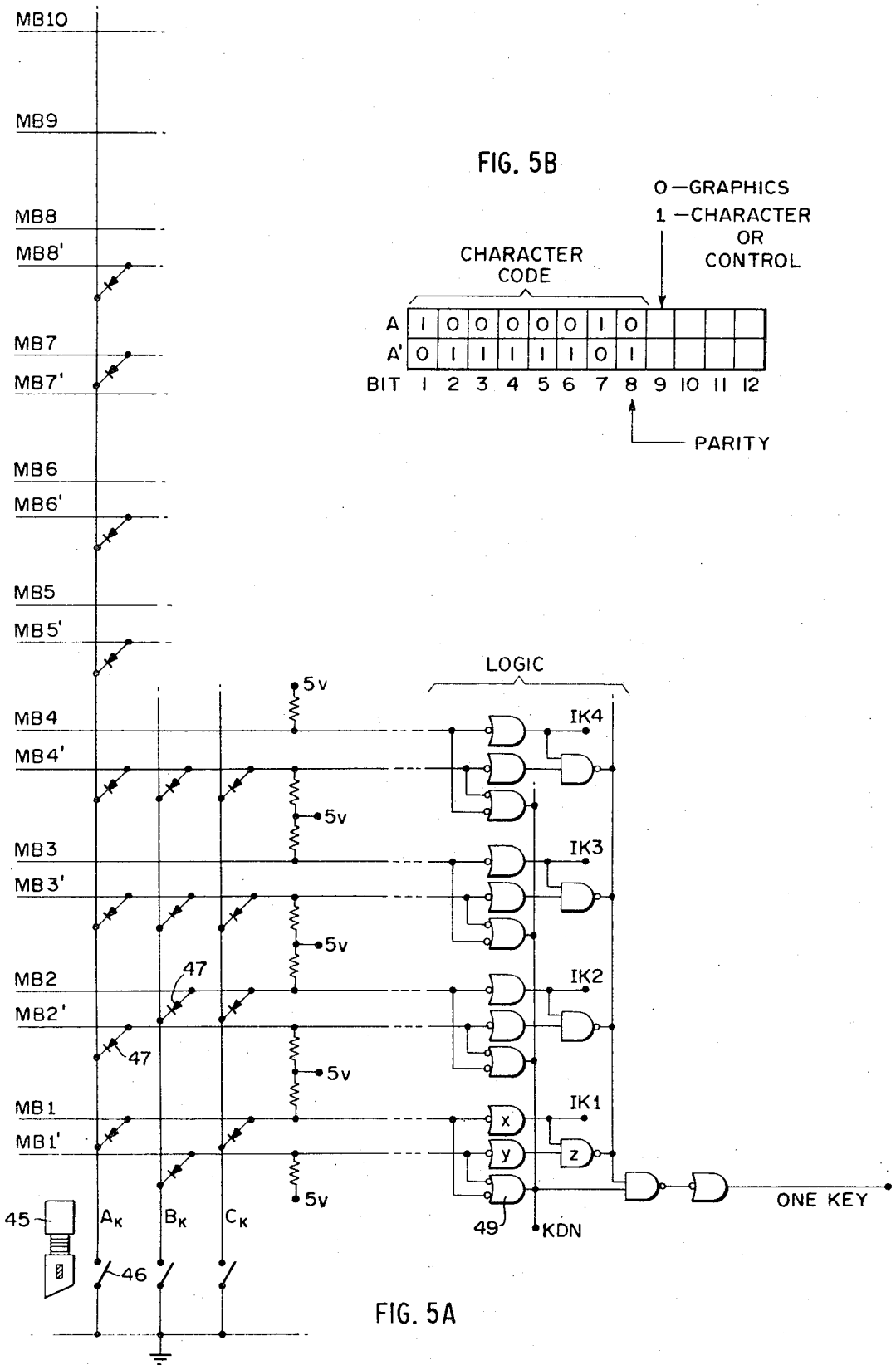

MB10
MB9
MB8
MB8'
MB7
MB7'
MB6
MB6'
MB5
MB5'
MB4
MB4'
MB3
MB3'
MB2
MB2'
MB1
MB1'
5v
47
45
A_K
B_K
C_K
46
LOGIC
IK4
IK3
IK2
IK1
x
y
z
49
KDN
ONE KEY

FIG. 5A

FIG. 5B

0—GRAPHICS
1—CHARACTER OR CONTROL
CHARACTER CODE
A 1 0 0 0 0 0 1 0
A' 0 1 1 1 1 1 0 1
BIT 1 2 3 4 5 6 7 8 9 10 11 12
PARITY

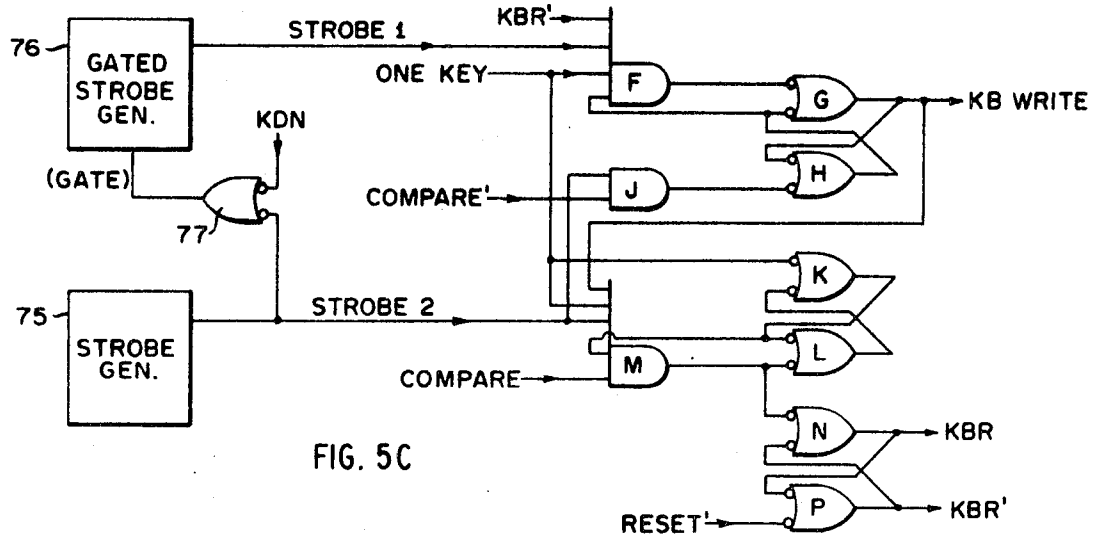


FIG. 5C

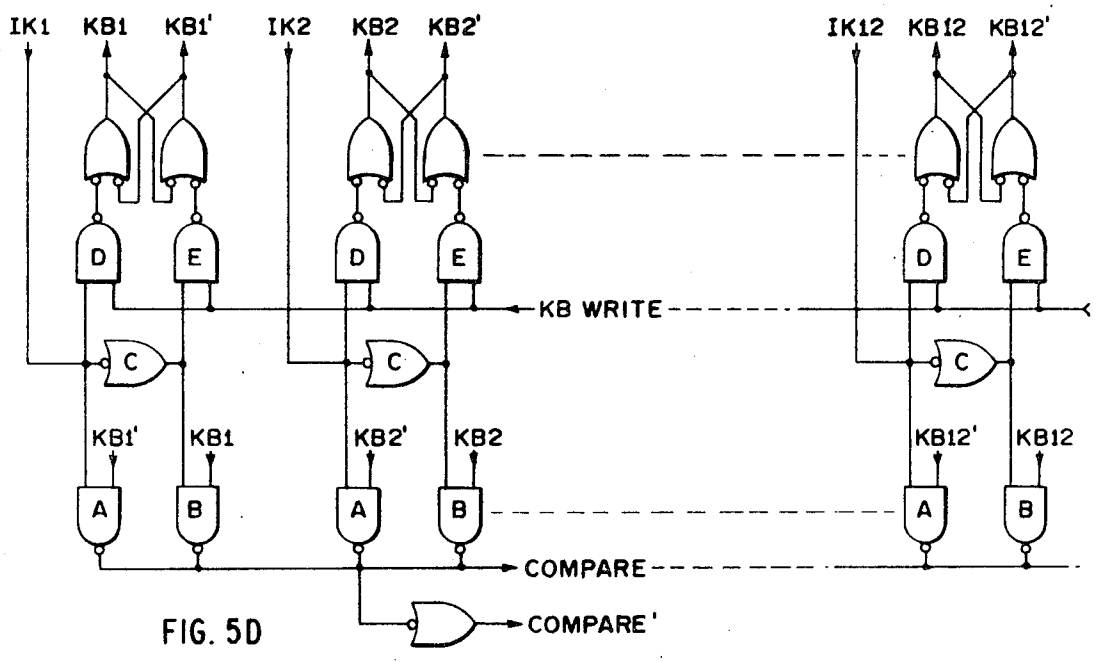


FIG. 5D

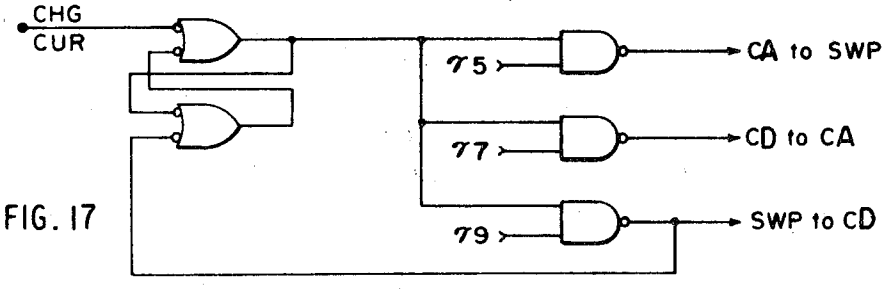


FIG. 17

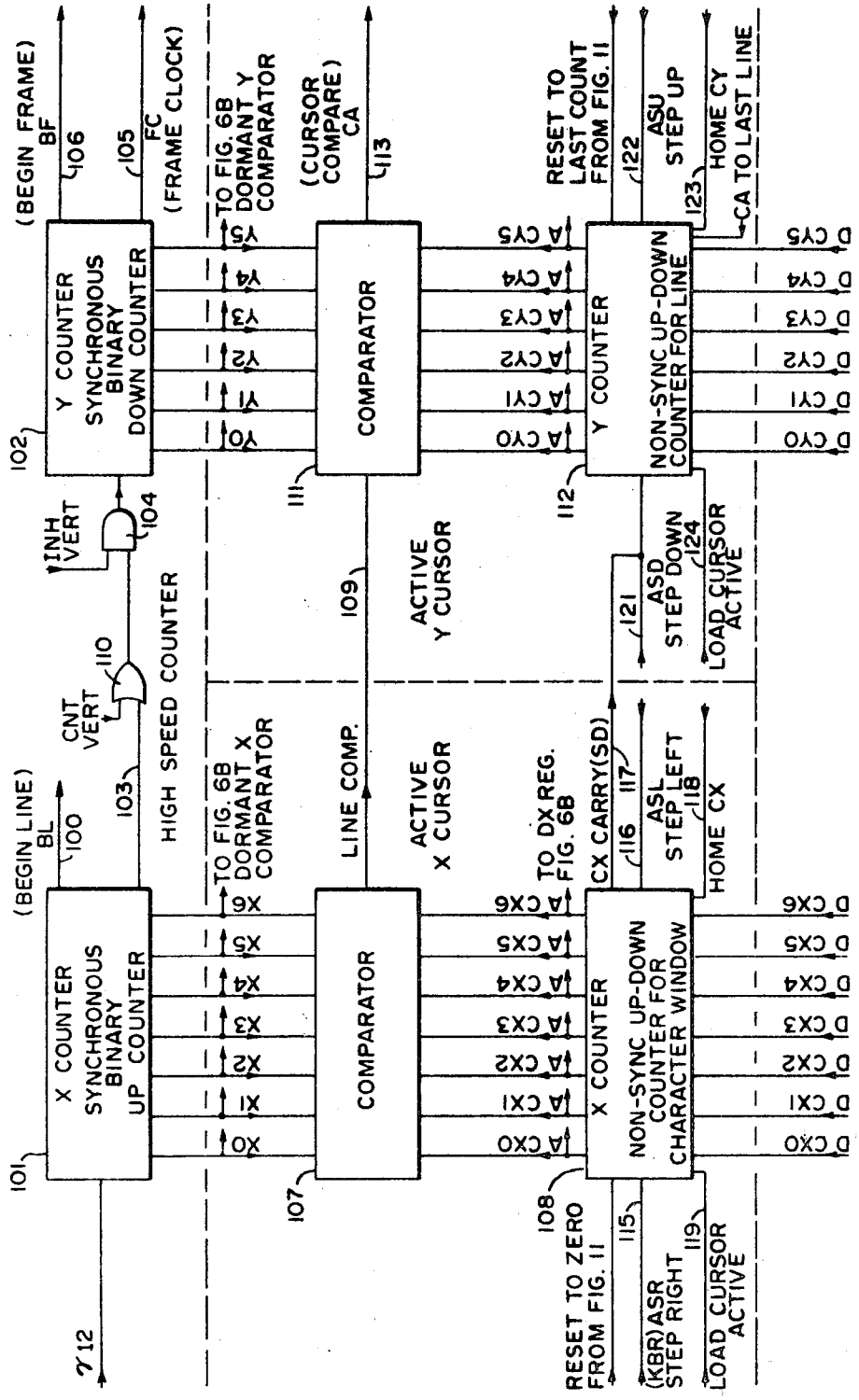

(BEGIN FRAME)
BF
106
105
FC
(FRAME CLOCK)
TO FIG. 6B
DORMANT Y
COMPARATOR
(CURSOR
COMPARE)
CA
113
RESET TO
LAST COUNT
FROM FIG. 11
122
ASU
STEP UP
123
HOME CY
CA TO LAST LINE
Y COUNTER
SYNCHRONOUS
BINARY
DOWN COUNTER
102
Y5
Y4
Y3
Y2
Y1
Y0
COMPARATOR
111
A CY5
A CY4
A CY3
A CY2
A CY1
A CY0
Y COUNTER
NON-SYNC UP-DOWN
COUNTER FOR LINE
112
D CY5
D CY4
D CY3
D CY2
D CY1
D CY0
INH
VERT
104
ACTIVE
Y CURSOR
109
121
ASD
STEP DOWN
124
LOAD CURSOR
ACTIVE
CNT
VERT
110
HIGH SPEED COUNTER
(BEGIN LINE)
BL
100
103
TO FIG. 6B
DORMANT X
COMPARATOR
LINE COMP.
ACTIVE
X CURSOR
TO DX REG.
FIG. 6B
CX CARRY(SD)
116
117
ASL
STEP LEFT
118
HOME CX
X COUNTER
SYNCHRONOUS
BINARY
UP COUNTER
101
X6
X5
X4
X3
X2
X1
X0
COMPARATOR
107
A CX6
A CX5
A CX4
A CX3
A CX2
A CX1
A CX0
X COUNTER
NON-SYNC UP-DOWN
COUNTER FOR
CHARACTER WINDOW
108
D CX6
D CX5
D CX4
D CX3
D CX2
D CX1
D CX0
7'12
RESET TO ZERO
FROM FIG. 11
115
(KBR) ASR
STEP RIGHT
119
LOAD CURSOR
ACTIVE

FIG. 6A

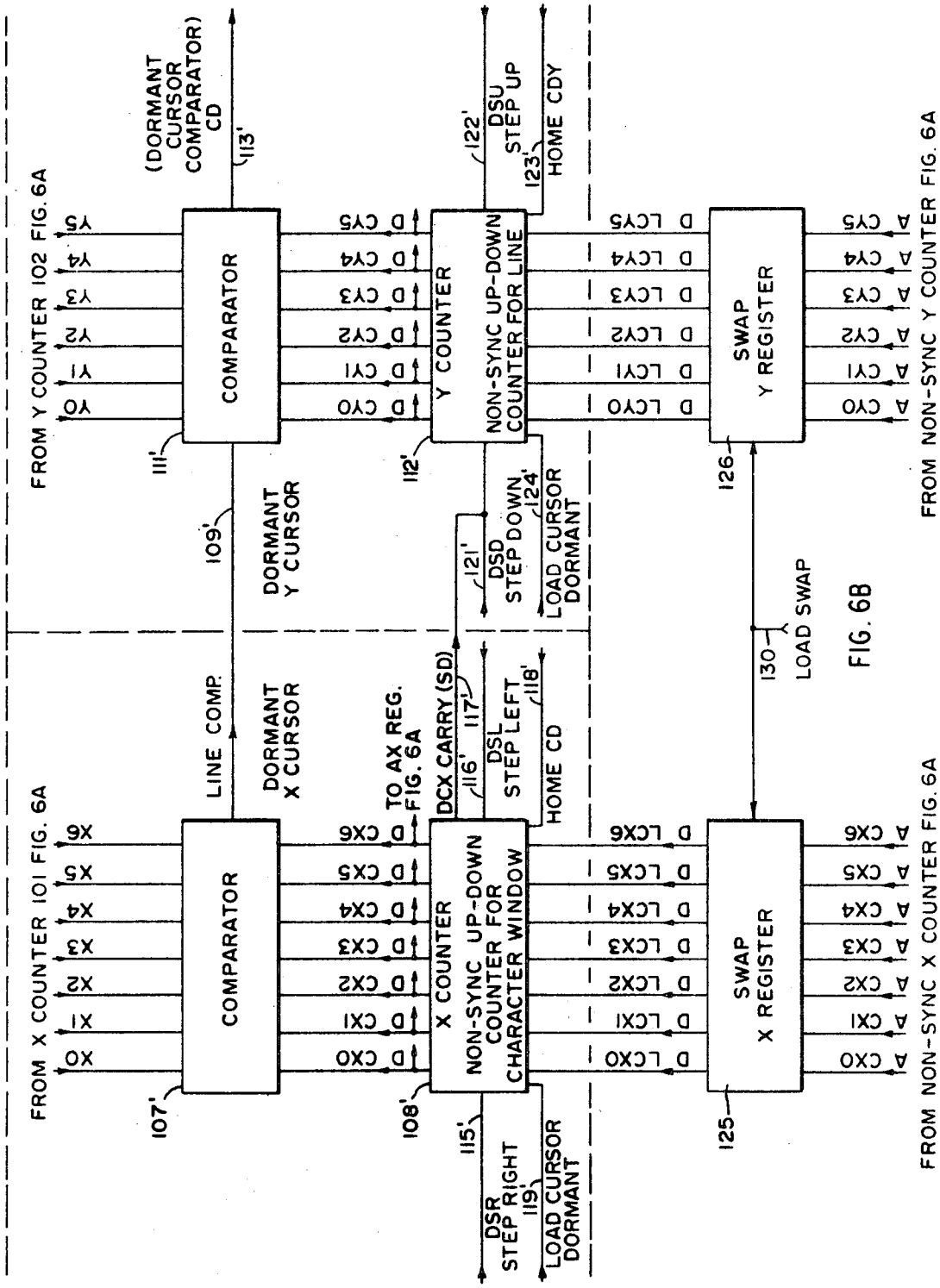

FROM Y COUNTER 102 FIG. 6A
(DORMANT CURSOR COMPARATOR) CD
113'
Y5
Y4
Y3
Y2
Y1
Y0
COMPARATOR
111'
D CY5
D CY4
D CY3
D CY2
D CY1
D CY0
Y COUNTER
112'
122'
DSU STEP UP
123'
HOME CDY
NON-SYNC UP-DOWN COUNTER FOR LINE
D LCY5
D LCY4
D LCY3
D LCY2
D LCY1
D LCY0
SWAP Y REGISTER
126
A CY5
A CY4
A CY3
A CY2
A CY1
A CY0
FROM NON-SYNC Y COUNTER FIG. 6A
109'
DORMANT Y CURSOR
121'
DSD STEP DOWN
124'
LOAD CURSOR DORMANT
LINE COMP.
DORMANT X CURSOR
TO AX REG. FIG. 6A
DCX CARRY (SD)
116'
117'
DSL STEP LEFT
118'
HOME CD
130
LOAD SWAP
FIG. 6B
FROM X COUNTER 101 FIG. 6A
X6
X5
X4
X3
X2
X1
X0
COMPARATOR
107'
D CX6
D CX5
D CX4
D CX3
D CX2
D CX1
D CX0
X COUNTER
NON-SYNC UP-DOWN COUNTER FOR CHARACTER WINDOW
108'
D LCX6
D LCX5
D LCX4
D LCX3
D LCX2
D LCX1
D LCX0
SWAP X REGISTER
125
A CX6
A CX5
A CX4
A CX3
A CX2
A CX1
A CX0
FROM NON-SYNC X COUNTER FIG. 6A
115'
DSR STEP RIGHT
119'
LOAD CURSOR DORMANT

FIG. 7

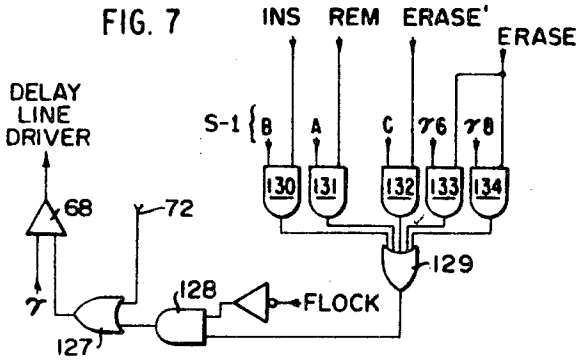


FIG. 9

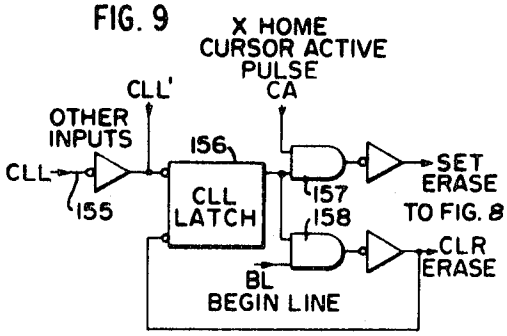


FIG. 8

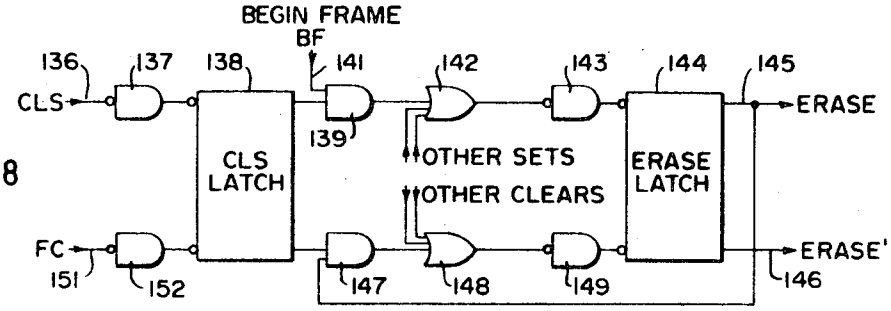


FIG. 10

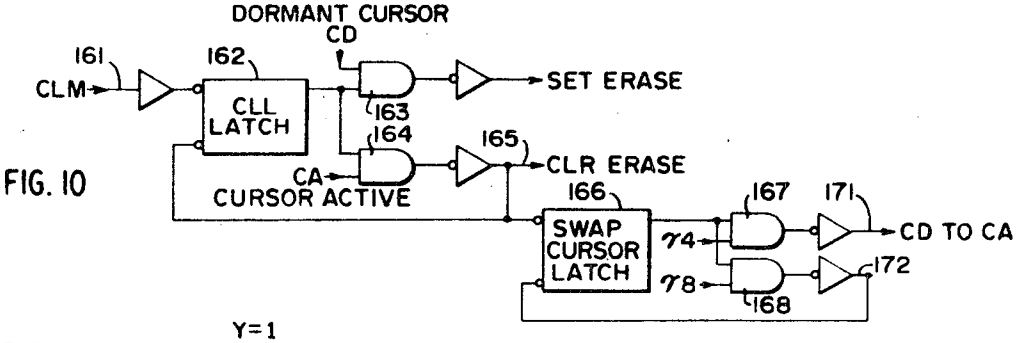
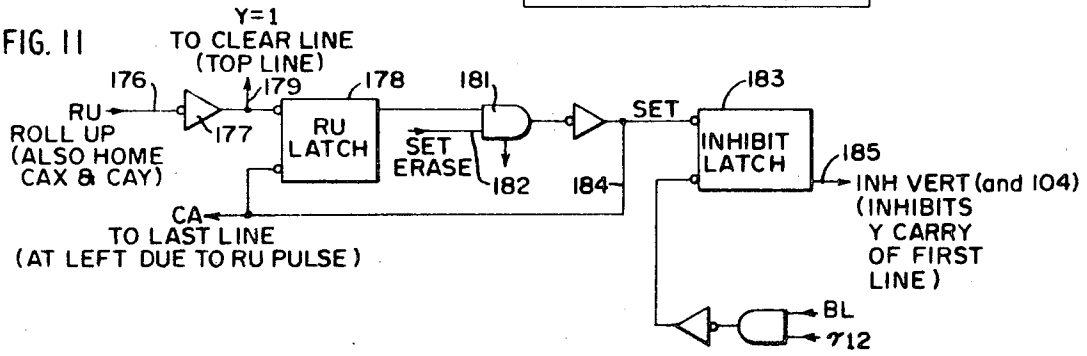


FIG. 11



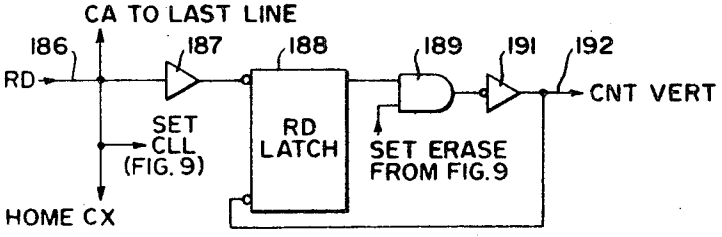


FIG. 12

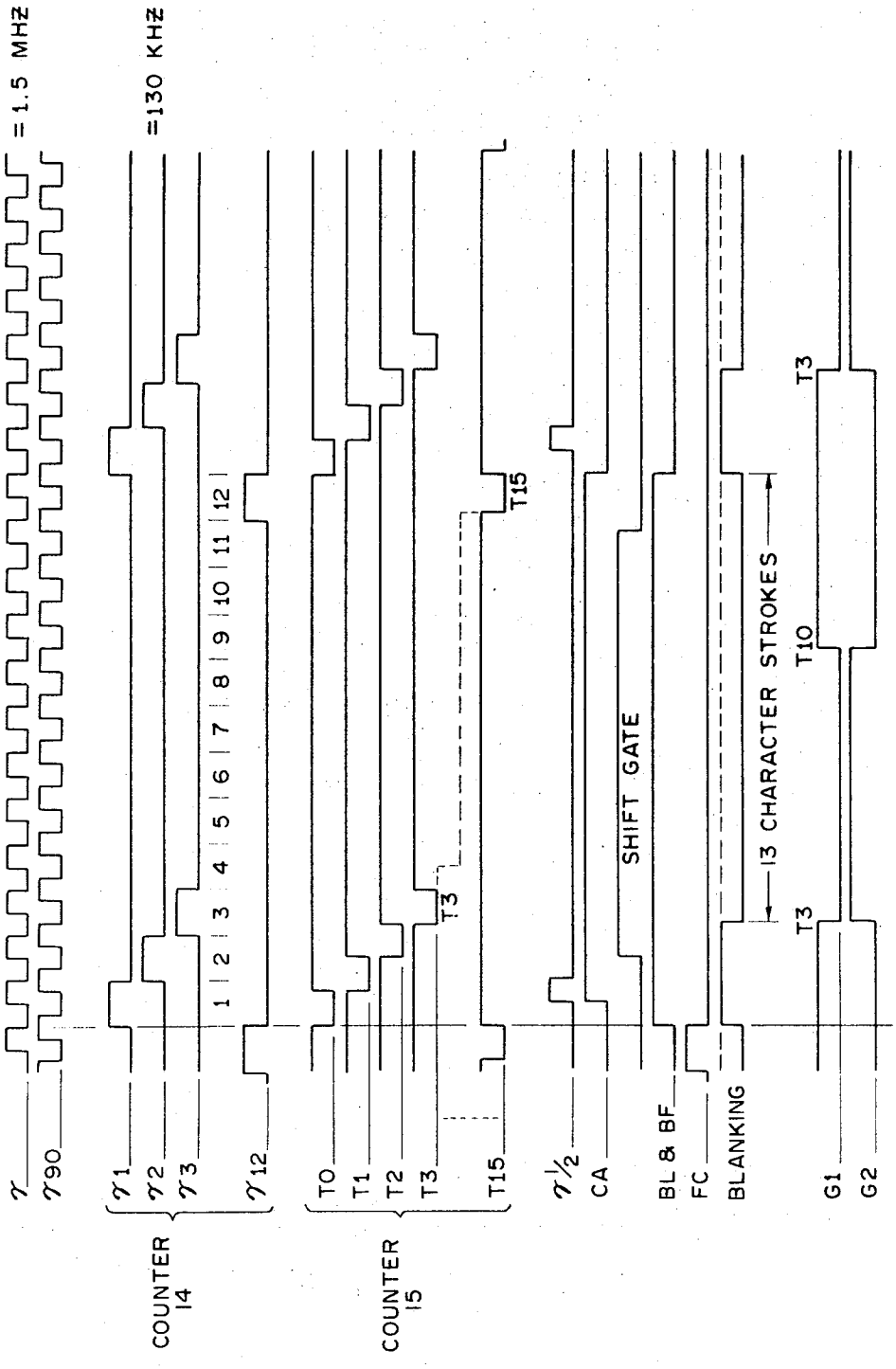

= 1.5 MHz
=130 KHz
γ
γ90
γ1
γ2
γ3
γ12
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
COUNTER 14
T0
T1
T2
T3
T15
COUNTER 15
γ½
CA
SHIFT GATE
BL & BF
FC
BLANKING
13 CHARACTER STROKES
T3
T10
T3
G1
G2

FIG. 13

FIG. 14

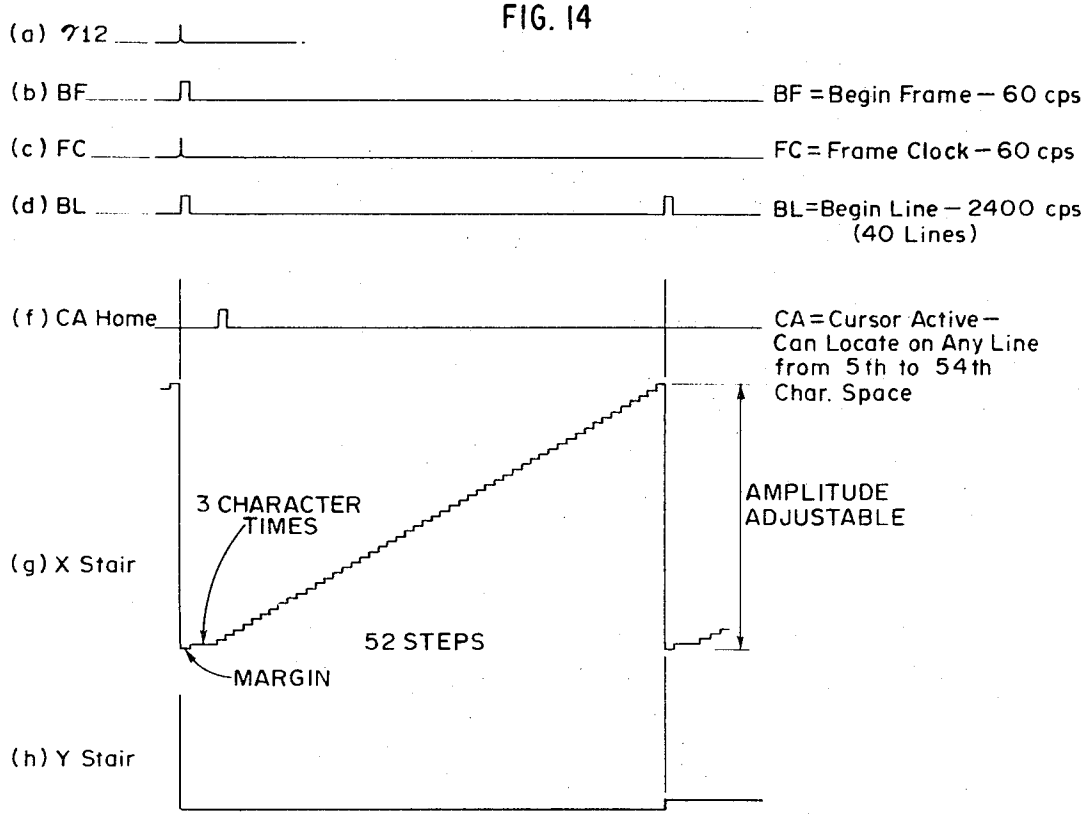
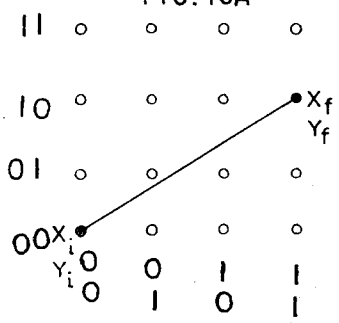


FIG. 16A



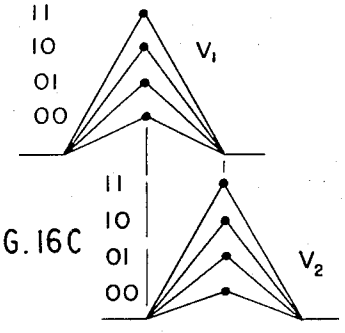


FIG. 16C

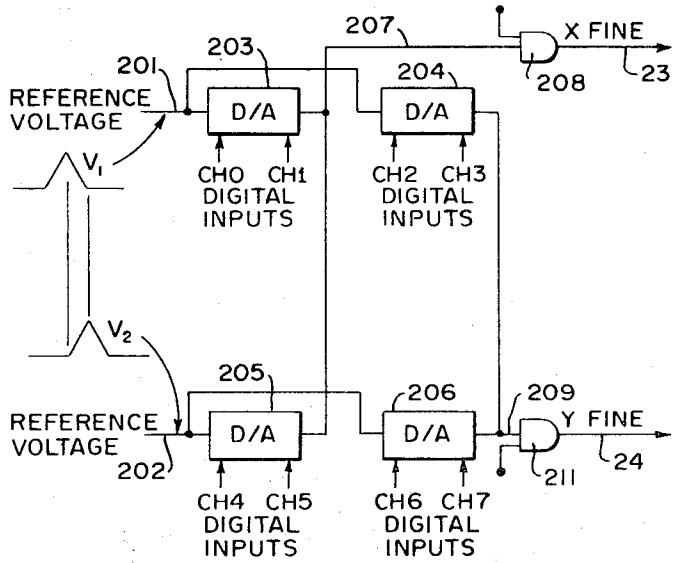
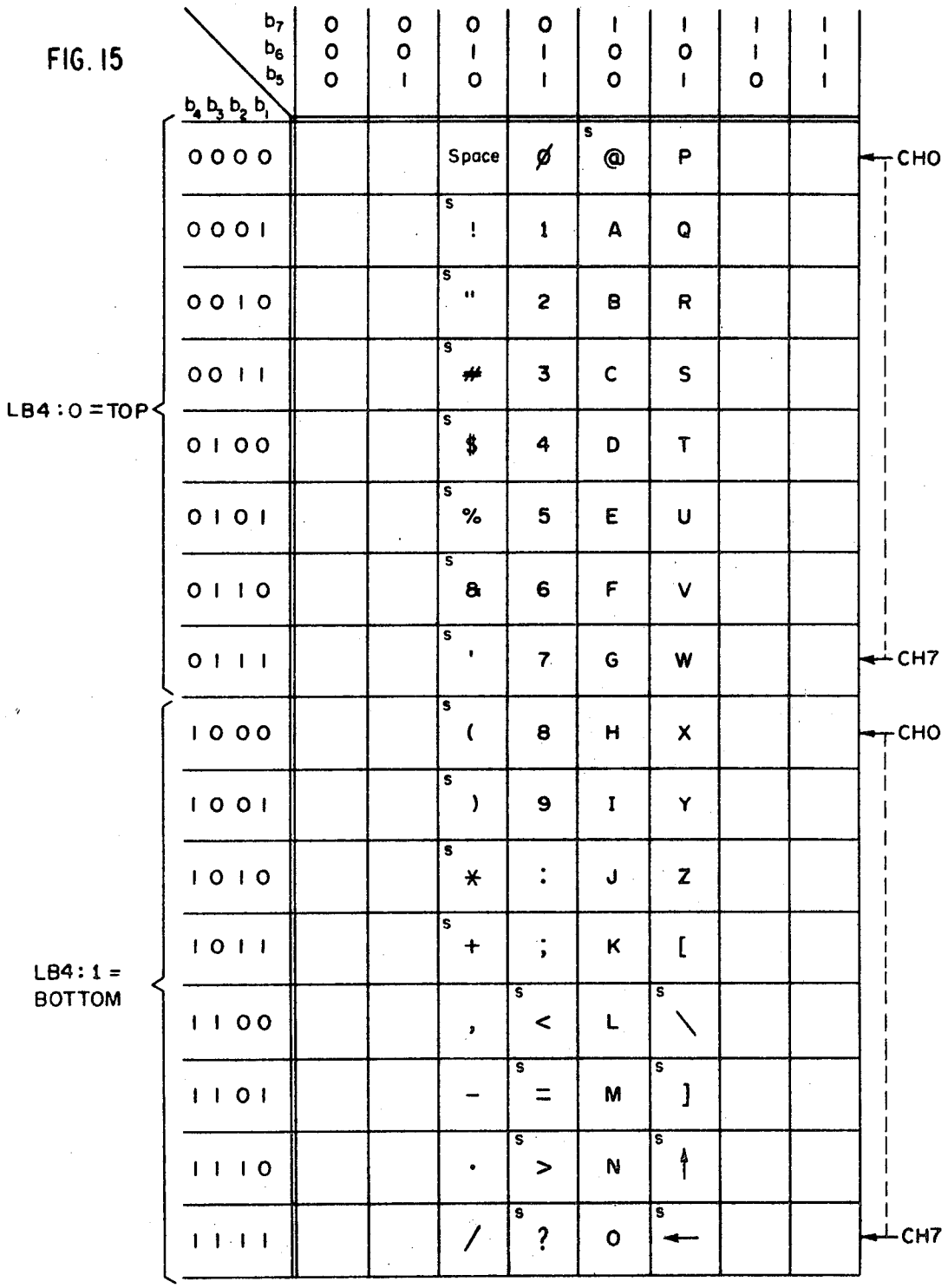


FIG. 16B

FIG. 15


b7 b6 b5 / b4 b3 b2 b1
000 001 010 011 100 101 110 111
0000 Space ø @ P
0001 ! 1 A Q
0010 " 2 B R
0011 # 3 C S
0100 $ 4 D T
0101 % 5 E U
0110 & 6 F V
0111 ' 7 G W
1000 (8 H X
1001) 9 I Y
1010 * : J Z
1011 + ; K [
1100 , < L \
1101 - = M]
1110 . > N ↑
1111 / ? O ←
S
LB4 : 0 = TOP
LB4 : 1 = BOTTOM
CH0
CH7
CH0
CH7

CHARACTER DISPLAY TERMINAL

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of my copending applications U. S. Ser. No. 587,583, filed Oct. 18, 1966, entitled ELECTRICAL SIGNAL GENERATOR, and U. S. Ser. No. 835,591, filed June 23, 1969, entitled CHARACTER DISPLAY SYSTEM.

BACKGROUND OF THE INVENTION

This invention relates to cathode ray tubes display terminals for communication and computer control systems wherein provision is made for keyboard entry of alphanumeric and graphic character symbols with the display of characters in a page format or other form and graphic display of any desired configuration.

Prior art display terminals are known, for example, as disclosed in the U.S. Pat. to Durr, No. 3,307,156 wherein a system is disclosed which employs a central symbol generator to which each display console has access on a time shared basis and from which it receives binary information in the form of a character identification code followed by the video information required for printing the selected character in a dot raster display. In each display console local recirculating storage is provided for the information currently displayed thereby to provide a refresh rate which maintains the alphnumeric display visible on the screen of a cathode ray tube. Systems of this type have inherent limitations due to the stylized display which is required as a result of a dot raster type video data storage and display system. For example, each character position on the screen is subdivided into a dot format and only the predetermined array of dots is capable of being displayed. Any alphanumeric or other characters which are desired to be presented must be synthesized by selecting predetermined groups of the dots in the raster. This requirement for a restricted range of visual presentation is related to the requirement of such systems to store video information in the recirculating memory. Conversely, attempts to provide a full degree of freedom in forming the visual image entails concomitant video requirements which greatly limit the capacity for any given system size.

This latter limitation (the uneconomical use of storage capacity for storing video information) is recognized in the patent to Durr where the suggestion is made that each console may contain its own symbol generator and therefore the memory contents can be confined to character identification codes only. Even though this suggestion increases the character capacity of a given delay line storage unit it cannot in and of itself provide the full capacity required for efficient communication display consoles since the video generation of a character must be accommodated between the time occurrence of successive character codes. To overcome this difficulty the Durr patent suggests an interlace pattern in the memory for the character codes which permits reading each character followed by a video display interval before the next character is read with the total length of the line such that on successive revolutions of data through the delay line an adjacent character code will be read on each subsequent revoltuion thereby requiring a number of revolutions of the delay line corresponding to the subdivision of the interlace pattern. Under such circumstances the refresh rate for the cathode ray tube screen imposes a limiting factor in relation to the number of characters which can be maintained in storage since the recirculation rate of the delay line cannot drop below that which will read all the characters from the total capacity of the delay line at a rate which will assure the presentation of a visually continuous image on the screen.

It is accordingly one of the principle objects of the present invention to provide a recirculating memory refresh display system in which character identity codes only are stored in the local memory and the characters so stored are contiguous in relation to the read and write access to the storage device and the display screen. Thus in the simplest case where the character identity codes are physically contiguous in the delay line and propagate continuously around the delay loop the identity codes can be read continuously as they pass the readout station on the recirculating loop to be simultaneously displayed on the cathode ray tube screen. This is achieved by virtue of the synchronous character video generator which supplies synchronously with character time each and every character which is in the repetoire of the system for display on the cathode ray screen and without limitation as to format or raster thereby permitting substantially any character shape to be displayed. This display is accomplished in character read time so that as character identity codes are successively read from the delay loop, the corresponding selected characters are processed from the character generators to the cathode ray tube for simultaneous display with a full screen format corresponding to the capacity of the recirculating delay and the full screen display being reproduced for each recirculation of the character codes through the delay loop. The system of the present invention therefore provides a vastly increased character capacity in the screen format together with unlimited flexibility in the actual characters displayed (e. g., upper and lower case letters) and a read in and read out capability which corresponds to the unit capacity for characters and the recirculation time of the delay loop.

Various other forms of the display systems have been suggested in the prior art in which a wide range of symbols with improved definition could be presented on the screen of the cathode ray tube. The U.S. Pat. to Halsted No. 3,329,948 shows a form of symbol generator in which a plurality of positive and negative angles and a selected group of line lengths can be combined to produce any desired symbol representation on the cathode ray tube screen. These systems have generally been non-synchronous however in the sense that the time for symbol formation and presentation varies for different symbols and the selection and generation of any symbol is in response to predetermined program controls which advance character by character only as the currently written character is completed and the program is advanced as a result of the end of character signal. Systems employing this kind of character generation operate with complicated programming for the presentation of the desired information on the screen and thus are not readily adapted to the simplified display and control aspects of a synchronous display system. In addition, wide band channels are required for all character video circuits since the pulse

signals are first synthesized and subsequently integrated.

An additional object of the present invention is, accordingly, the provision of a synchronous display system having a full range of controls which are readily incorporated and compatible with the video symbol generator system while at the same time providing a maximum degree of flexibility and clarity in the symbol generation and display. For this purpose applicant's novel signal generator provides a full range of alphanumeric and graphic character generation in a display operating synchronously with the aforementioned contiguous character code recirculating storage feature to provide maximum character capacity with a stable display of highly accurate and versatile configuration characters. These characters are generated and displayed with minimum bandwidth circuits since the stroke pulse generator outputs are first integrated individually and the resulting linear slope waveforms are synthesized into the desired character waveform.

The usefulness of character display systems in the prior art has been extended by the provision of certain editing functions which provide for modification or correction of the text present in memory and currently displayed. For example, the patent to Dammann et al. U.S. Pat. No. 3,248,705 discloses a display system in which the character codes can be tagged with an additional information bit to identify that character and its position on the screen relative to certain editing operations. With adequate programming and a forward-backward memory access sequence, this editing operation greatly increases the utility of systems of this type inasmuch as in composing any text for the first time certain errors will appear as well as omissions and for the purpose of rewriting various insertions, deletions and recomposition may be desired. If these functions can be accomplished on the display screen which is currently presenting the memory contents the final form of the text can be achieved prior to its transmission to remote points or other utilization. On the other hand, by the very nature of the editing functions which it is desired to perform the danger exists of inadvertent deletions and the consequent loss of information which, if available only in the memory of the device, may be totally lost if a deletion operation is performed relative to text which it is not desired to discard. Accordingly, the association of editing functions with the information which is circulating in memory, especially where it is accomplished by means of a relatively unsophisticated code such as a single bit, presents the possibility that a noise bit or other malfunction can be effective to lose or disarrange valuable information for which no other source exists.

It is, accordingly, an important object of the present invention to provide in a synchronous refresh character display system a full range of editing functions which are accomplished independently of the information content of the memory store and under the control of the operator by means of independent and reliable hardwire circuit elements thereby assuring that all editing functions will be accomplished as selected under the control of the operator or other control source independently of the information recirculation through memory.

The foregoing objects of the invention are achieved in a synchronous character display system which employs versatile and extremely high speed character generators for each character to be displayed, which generators are operated synchronously with the character position determining sequence of the cathode ray tube display thereby making possible the display of any character at any character position on the display. This display system is controlled by a recirculating memory which in the preferred form stores a character identity code sequence which is contiguous relative to the characters displayed and from which information can be read continuously and without time gaps for simultaneous display. Thus maximum character storage with minimum access time and optimum visual display characteristics are all combined in a symtem which by virtue of its independent editing system can be controlled without loss of data or further complications due to requirements for complicated programming or storage of control and editing functions in the memory. The invention therefore achieves improved operation with respect to the foregoing shortcomings of the prior art all as described herein and as will be apparent from the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A, B and C when assembled as indicated show an overall system block diagram of the invention.

FIG. 1D shows the editing control signals derived from keyboard operation in response to control code outputs.

FIGS. 2A–E show a circuit and descriptive diagrams for the character generator employed in the invention.

FIG. 3A is a simplified block diagram of the system of the invention showing the arrangement for gross deflection signal generation for the cathode ray tube.

FIG. 3B is a waveform diagram describing gross deflection signals for positioning the cathode ray beam in character positions corresponding to a page format.

FIG. 5 is a representation of a keyboard layout for use as a terminal input for the invention.

FIG. 5A is a partial schematic diagram of the key encoding matrix used with the keyboard keys of FIG. 4 and associated logic circuits for producing the selected key code signal as well as KEY DOWN and ONE KEY signals.

FIG. 5B is a diagram representing the code for the letter A and its complment as used in the machine.

FIG. 5C shows the logic for keyboard gating used in conjunction with the logic of FIG. 5D which shows the keyboard buffer and comparator for contact bounce error elimination.

FIG. 6A and 6B are block diagrams showing the cursor counters and comparators.

FIG. 7 is a logic diagram showing the input gating.

FIG. 8 is a logic diagram for the CLEAR SCREEN operation.

FIG. 9 is a logic diagram for the CLEAR LINE operation.

FIG. 10 is a logic diagram for the CLEAR MESSAGE operation.

FIGS. 11 and 12 are logic diagrams for the operations ROLL UP and ROLL DOWN respectively.

FIG. 13 is a waveform diagram of the synchronous pulses employed in the system.

FIG. 14 is a waveform diagram of the gross deflection signals generated in the system.

FIG. 15 is an ASCII code table showing its relation to the access codes used in the system.

FIG. 16A is a representation of the subdivision of a character window for graphic stroke generation.

FIG. 16B is a block diagram of a graphic stroke generator.

FIG. 16C is a diagram useful in explaining the generation of graphic strokes.

FIG. 17 is a logic diagram for the CHANGE CURSORS operation.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIGS. 1A, 1B and 1C assembled as indicated to show an overall block diagram of the system, the general system will first be described. Further details of the operating elements of the system will subsequently be described with respect to more detailed showings of the representations given in FIGS. 1A, 1B and 1C, the timing waveforms of FIG. 13 and the step waveforms of FIG. 14.

The system of the present invention is synchronous in memory and display operations and for this purpose these operations are controlled by pulses derived from a stable crystal oscillator **11** operating, for example, at approximately 6mHz. The frequency of oscillator **11** is subdivided by a first division by four in a divider **12** and a division by three in a divider **13**. The output of the divider **12** provides as shown in FIG. **13** a series of timing pules identified as γ, γ' and $\gamma 90$ at approximately 1.5mHz to provide the master clock signals for the device. The 1.5 mHz master clock signal is applied to a 12-state ring counter **14** which supplies from its various stages $\gamma 1$ to $\gamma 12$ bit timer pulses at approximately 125 kHz. The divider **13** applies an approximately 2 mHz signal to a 16-state ring counter **15**, the output of which provides a contiguous set of square pulses **T0** to **T15** which pulses are identified as the stroke timer pulses.

The output of the ring counter **15** applies the contiguous pulses to **T0** and **T15** to a triangular or delta D waveform generator **16** which produces as its output a series of overlapped equilaterial triangle waveforms designated **D1** to **D13** which are applied to a character generating system **17** and to a cursor summing and graphics unit **18**. The D generator **16** produces gate signals **G1** and **G2** synchronized to begin with **T3** and end with **T10** and integrates them to produce the graphic stroke outputs **V1** and **V2**.

The character system **17** contains circuits which continuously and synchronously generate the stroke waveforms for writing each character in the repetoire which the machine is designed to display. For this purpose it combines the overlapping positive and negative slope portions of the input triangle waveforms **D1** to **D13** to generate each character as a series of connected strokes having the desired slope as determined by the relative magnitudes with which the positive and negative overlapping slope portions of the waves **D1** to **D13** are combined. The particular character which is to be displayed in any given position on the screen of the cathode ray tube is determined by character board selection code bits **LB4, 5** and **6** and character selection code bits **1, 2** and **3** which determined **CH0–CH7** applied to the character system **17**. As shown in the code table while bits **b5** and **b6** select the column, the bits **1, 2** and **3** determine **CH0–CH7** which operate to select one of the seven rows in the top or bottom half of the code table which thus uniquely defines the character selected. As a result of this action there appears on output lines **21** and **22** of the character system **17** the summation voltages for X deflection and Y deflection to generate the particular character desired. The details of the circuit for producing the X sum and Y sum voltages on lines **21** and **22** are explained briefly with reference to FIG. **2A, B, C, D** and **E** hereinafter and in greater detail in applicant's copending application Ser. No. 587,583, filed Oct. 18,1966, entitled ELECTRICAL SIGNAL GENERATOR.

The X sum and Y sum voltages on lines **21** and **22** are processed in the cursor summing and graphics unit **18** to produce on output lines **23** and **24** the deflection quantities (either voltage or current) for deflecting an electron beam in the cathode ray indicator tube in accordance with the selected character. For this purpose the unit **18** is under the control of a display control unit **25**, which unit operates in response to loop bit inputs **LB1** to **LB9** obtained from the refresh storage system hereinafter described. As a result of processing the loop bits the display control unit **25** calls up the desired character or graphic strokes for each character position on the display screen of the cathode ray tube sequentially as the information in storage recirculates including the entry of new data and the discarding of old data all as hereinafter more completely described. To perform this function the display control **25** supplies to the summing and graphics unit **18** signals **CE, LB1** to **LB8, CH0** to **CH7**, and **CURSOR GATE**. The signal **CE** provides for character enable control in response to bit **9** of the loop bit code being a zero and when enabled writes a character corresponding to the loop bit code as previously described with reference to FIG. **15**. When bit **9** is a one the signal **CE** is negated and calls for a graphic stroke generation from the cursor summing and graphic generator **18** thereby writing the corresponding graphic's stroke designated by the loop bit code. Loop bit signals **LB1, LB8** define the beginning and end of the graphic stroke generation while **CH0–CH7** as applied to graphics unit **18** to select predetermined graphic strokes defined by the 16 geometric points obtained by subdividing the character window into nine equal squares as shown in FIG. **16A**. The approximate X and Y fine deflection signals are gated out on lines **23** and **24** for the graphic stroke selected.

The **CURSOR GATE** is generated at a random rate timed in response to cursor active compare (CA; FIG. **6A**) to write the cursor in predetermined alternation with the character at the active cursor location on the screen. Thus the active cursor location is identified visually by a blinking appearance of the cursor (for example underlining) displayed with any character which may be displayed. In addition the display control **25** supplies a blanking signal during **T0–T2** to the cathode ray tube so that only the desired portions of the deflection of the electron beam produce a visible trace on the screen. Times **T1** and **T2** are used to position the beam at a suitable starting point within the character window before writing begins at **T3**.

In addition to supplying characters selected from the character system **17**, the unit **18** supplies graphic increment strokes available upon command. For this purpose a full character interval is converted into a single pair of opposite slope triangular waveforms in generator **16** as indicated in FIG. **1C** and these waves can be combined in any proportion in unit **18** to produce a stroke of any desired slope, positive, negative or zero over the character interval **T3–T10**. By calling forth a succession of graphics strokes defined by subdividing the character window into a 4 × 4 matrix any desired waveform or curve can be drawn with sufficient accuracy on the face of the cathode ray tube. These graphics strokes are selected by an identifying code obtained from LB1–LB8 and the CH0 to CH7 line from the display control **25** to the summing and graphics unit **18** as descirbed in detail in connection with FIGS. **16A–16C**.

THE DISPLAY SYSTEM

The display system shown in FIG. **1B** used by the present invention is a cathode ray tube indicator generally designated **30** which is provided with two sets of deflection coils for the X and Y fine signals applied from the unit **18** and X and Y staircase signals applied from staircase generator **35**. The staircase generator **35** is synchronized with the system clock by means of the γ12 derived signals and operates to subdivide the viewing screen into a regular raster of character windows or positions in line and column letter positions for a page format under the control of a frame clock (FC) signal and a begin line (BL) signal timed as shown in FIG. **13**. A description of the X and Y staircase generator and deflection system as it is incorporated with the X and Y fine deflection system is given in connection with FIGS. **3A** and **3B** hereinafter. FIG. **14** further shows the relation of the timing waveforms FC and BL to the stair waves for the X and Y deflections.

THE KEYBOARD INPUT AND RECIRCULATING DELAY SYSTEM

Referring now to FIG. **1A**, a keyboard input device **51** is provided with a standard typewriter keyboard layout which has in addition keys for the various control functions all as shown on FIG. **4**. The operation of an individual key on the keyboard generates a fixed code representing the character of the individual key as described in connection with FIG. **5**. The output provided by the keyboard diode coding matrix of FIG. **5** is the ASCII code and its complement in which **8** bits are used to uniquely identify the character and its parity, with the remaining four bits reserved for tag information. Single key operation is assured and bounce elimination is provided by reading the key code into a register in keyboard logic **52** and subsequently comparing the register word with the keyboard word in the keyboard logic unit **52**.

If a comparison exists the keyboard ready signal KBR reads the keyboard and writes the word into an exchange buffer **54**. This is a parallel transfer on BI1–BI9 with the writing control signal for the exchange buffer **54** appearing on line EBWRITE. Once a word is written in the exchange buffer **54** the internal state counters differ and exchange buffer ready (EBR) signals the loop interface **55** to produce a TRANSFER pulse to the exchange buffer **54** at the next character time γ1. This produces a parallel transfer of the character code to the input register of the loop interface **55**. Character codes are shifted out of the input register into the delay loop as subsequently described herein. If a control code is detected it is routed to perform the appropriate control function such as SHIFT UP, SHIFT DOWN, etc. for the active or dormant cursors, or editing control.

The recirculating storage loop is adapted to provide storage of the identity codes for the full capacity of the display screen of cathode ray tube **30**. Using a refresh rate of 60 Hz approximately 16 milliseconds of delay is required which is subdivided as follows. The bit rate is approximately 1.5 mHz and the total storage is 2,080 characters with 12 bits per character giving it a total of 24,960 bits in storage when the storage loop is full, i.e., when the screen of the cathode ray tube **30** is written in full-page format (50 chracters by 40 lines plus margin).

Since all operations are performed character by character, entry into and out of the memory loop with or without deletion of existing characters can be accomplished by providing additional storage for two characters in succession. This is achieved by means of first and second shift registers **61** and **62** and appropriate switching represented schematically by switch S1. The actual delay and storage achieved in the memory loop is provided by magnetostrictive delay lines **63** and **64** which are serially connected through a detector **65**, a reclock unit **66** and a driver **67**. Since magnetostrictive delay lines tend to become inaccurate with greater delay periods the 16 millisecond delay interval is divided equally between the two delay lines **63** and **64** and the information is reclocked in the unit **66** so that time errors introduced by the parameters of the delay lines are held to a minimum. Delay line **63** is driven by a driver **68** and the output of delay line **64** is detected by detector **69**. The output of detector **69** is a digital signal which is reclocked by unit **71** to supply the serial bit input to the first shift register **61** and is available on terminal A of switch S1 as a direct input to the driver **68**. The output of the first shift register **61** supplies the serial bit input of the second shift register **62** and terminal C of switch S1, while the output of the second shift register **62** supplies terminal B of switch S1. The shift registers **61** and **62** and the reclocking devices **66** and **71** are all synchronized to the clock pulse γ thereby providing a synchronous closed loop refresh memory with entry and editing of the memory store available through the switch S1 as it is switched to terminals A, B or C. Original input codes to the memory are derived from an additional terminal **72** which supplies serial bit signals from the input register of editing logic unit **56**.

The contents of the recirculating memory loop are utilized one character interval at a time by means of a loop register **73** which has a 12-bit parallel input from the first shift register **61** and for each character time has a character code registered corresponding to that in the first shift register **61**. This code is shifted from register **61** to register **73** in parallel at time γ12. The code is shifted serially out of register **73** over lines **70** to supply the loop bits LB1–LB12 to display control **25** and other parts of the system such as I/O control **74** for hard copy, dataset or drum storage options.

The operation of the refresh memory loop will be briefly described. The delay lines **63** and **64** are the ultrasonic spirally coiled wire type, for example, MSD type 505—2087 (8328μs delay) manufactured by Digital Devices, Syosset, N.Y. The lines are energized with non-return to zero (NRZ) signals supplied by the respective driver circuits **67** and **68**. With approximately 8 MS delay in each line, the respective detectors **65** and **69** convert the output signals thereof into digital pulse code signals which are reclocked by the respective devices **66** and **71**. Thus a serial pulse stream representing a keyboard code from the input register of the editing logic **56** appears on terminal **72** and with switch S1 connected thereto enters storage in the delay line loop. This process is repeated with the appropriate switching of switch S1 to maintain characters that have been entered circulating in the delay loop and entering keyboard codes as they appear up to the full capacity of the loop for 2,080 characters of 12 bits each. With switch S1 changed to terminal C the information in the loop will recirculate indefinitely without change. The information that is recirculating in the loop passes through the shift register **61** in the succession in which it recirculates through the loop. Each full 12 bit code can be read from the register **61** by parallel transfer at $\gamma 12$ to the loop register **73** and serially transferred out of loop register **73** by the γ pulse for display purposes on the lines **70** as loop bits LB1 to LB12.

The provision of a character code at terminal **72** of switch **1** from the input register of the loop interface **55** as controlled by the editing logic **56** will now be described with reference to FIG. 5A. When a key **45** on the keyboard unit is pressed, a magnet attached to a plunger causes a reed switch **46** to close, thus grounding a string of diodes **47** used to generate the code for that particular key. The fact that some of the signal lines have zero (GND level) on them indicates that a key is down. The keyboard diode matrix generates each bit and its complement (e. g., MB1–MB1'). Using ASCII code, eight bits (MB1–MB8 uniquely identify the character selected and its parity, with two bits MB9, MB10 being reserved for tag information.

More than oNE KEY and contact bounce errors are eliminated as described with reference to FIGS. 5C and 5D by successively reading the keyboard bits, and then several milliseconds later comparing the present bit values to the past stored values. If they compare, the keyboard ready (KBR) signal is generated.

In local mode, keyboard ready (KBR) signals the I/O control **53** circuitry to simultaneously read the keyboard and write on the exchange buffer **54** in the following manner. A keyboard read pulse (KBREAD) causes the contents of the latches in the keyboard logic board to be strobed (SK1 to SK9 are used) and a simultaneous EBWRITE pulse causes the bits strobed out of the keyboard logic to be written into the exchange buffer **54**.

Once a character is loaded into the exchange buffer **54**, its internal state counters differ, producing the exchange buffer ready (EBR) signal. EBR signals the loop interface **55** which gives a transfer pulse at the next character time ($\gamma 1$). The transfer pulse causes the contents of the exchange buffer **54** to be loaded into the input serial shift register of loop interface **55** in parallel.

With a word in the input serial shift register, bits **6**, **7** and **9** are examined. If bits **6** and **7** are different and bit **9** is zero, the word is a character and the logic in loop interface **55** tells the editing logic **56** that a chracter is ready (CHAR READY). If bits **6** and **7** are not different and bit **9** is a zero, the word is a control code. That code is examined and the appropriate output is pulsed and the input register is cleared. These outputs shown in FIG. 1D, are used by the logic described in FIGS. **7–12** and **17** for editing in conjunction with the cursor controls of FIGS. 6A and 6B or to generate cursor shift signals, etc. If bit **9** is a one, however, the word entered is a graphic character, and it is entered into the loop in the same fashion as a character, i. e., the loop interface **55** tells the editing logic **56** that a character is ready.

Character ready (CHAR READY) signals the editing logic **56** that the input register is to be read. When the cursor compare (CA) occurs, the editing logic opens a shift gate at T2 which closes after none γ periods causing the input register to shift its contents serially in response to γ pulses from AND **60** into the loop via switch terminal **72**. At the end of the nine γ intervals the cursor CA is stepped to the right one position by the loop interface. Feedback generated by the editing logic causes the loop interface to drop character ready and the cycle can then repeat. Bit by bit the contents of the input register are presented to the delay line driver **68** input which is connected by switch S1 to terminal **72**. At the completion of the shift gate, the editing logic again recloses the loop (S1=C), dropping the character that would have gone into the loop had not the character entry been made (override mode). In insert mode, the editing logic switches to the output of the second shift register (S1=B) rather than the first, thus inserting the character from terminal **72** without deletion. In insert mode, the editing logic switches back to S1=C, the output of the first shift register, when the display reaches the margin spaces at the beginning of the next line.

The loop memory and keyboard entry systems described with reference to FIG. 1A are able to control the character generation and display elements of FIG. 1C by the operation of the cursor counter and control system shown primarily in connection with FIG. 1B. During the steady state display of a page format on the screen of the cathode ray tube **30** the contents of the memory loop are read character by character from the first shift register **61** into the loop register **73** upon the occurrence of $\gamma 12$ and this same γ pulse is used to step the staircase generator **35** character by character and line by line through the page format subdivisions of the cathode ray tube screen. The character identity word read from the loop register **73** is applied to the display control **25** which selects the identified character either as a character, cursor or graphic to determine the X and Y fine deflection control signals which will be applied during that particular character window.

The components shown in FIG. 1B provide the timing controls for the editing logic which controls location and movement of the active and dormant cursors. The units shown in FIG. 1B comprise a high speed counter **81** which has both an X and Y counter running in response to $\gamma 12$ in synchronism with the staircase generator **35** thereby providing a unique count for each

character position in each line on the display screen. The high speed counter **81** is coupled to an active cursor X module **82** and an active cursor Y module **83** which operate in conjunction with signals from the loop interface **55** to define the X and Y position of the active cursor. The high speed counter **81** is also coupled to a dormant cursor X module **84** and a dormant cursor Y module **85** which similarly define the X and Y position of the dormant cursor in accordance with control signals received from the loop interface **55**. The dormant and active cursor modules **82** and **84** are interconnected by a swap register **86** as are the dormant and active Y cursor modules **83** and **85**. The units **81–86** provide cursor signals for the editing functions CLEAR SCREEN, CLEAR MESSAGE, CLEAR LINE, ROLL UP, ROLL DOWN and CHARACTER REMOVE, all as hereinafter described.

When the count set in the X and Y modules for either the active or dormant cursors corresponds to the count of the high speed counter **81** the respective cursor signals CA or CD are generated. These cursor signals are used to alter the synchronous relation between the display and the recirculating delay to modify the visual display on screen **31**. The underlining of a character position (numeral "1" and letter "C" in FIG. 3B) by a cursor graphic stroke serves to visually identify the location of the active and dormant cursors.

DESCRIPTION OF THE KEYBOARD

The keyboard unit of FIG. **5**A by means of magnets attached to the key plunger **45** closes reed switches **46** for each key depressed. The reed switch closure grounds a single input to a diode coding matrix which has diodes **47** connected according to the code to the matrix output lines. When a switch **46** closes the diode connected outputs go to zero and the remainder stay at logical **1**. The diode matrix is arranged so that both the bit and its complement are generated. For an eight bit code, therefore, eight diodes are used for each code regardless of the actual code. In FIG. **5**A, the full diode array for code character "A" is shown with a portion (four bits) of other codes generated. When any one key is depressed, closing one of the switches **46**, the appropriate key line is grounded. This ground is fed to the horizontal MB*i* and MB*i*′ lines through the diodes **47**. If, for example, B_k is at ground, the diodes to MB1′, MB2, MB3′ and MB4′ force those lines to "zero" while MB1, MB2′ MB3 and MB4 remain at "logic one." These lines are fed to NOR gates *x* and *y*. MB1′ is low, thus IK1 is also low. Likewise for B_k at ground, IK3 and IK4 are zero and IK2 is one.

As long as any keys are depressed, either (or both) of the MB1 or MB1′ lines are low, thus KDN (key down) is high at the output of the NOR gates **49**. If more than one key is depressed, at least one set of the MB*i* and MB*i*′ lines will both be zero, thus forcing ONE KEY to remain zero by the circuit described as follows. A comparator is formed by three gates *x*, *y* and *z* for each of the MB*i* and MB*i*′ lines. The outputs of the *z* gates are WIRE-OR connected together. Under normal single key down operation MB*i* and MB*i*′ are different, and gate *z* has one zero at its input, thus its output is high, and ONE KEY is high.

If two keys are depressed, for example B_k and C_k, one line pair (in this case MB1 and MB1′) are both zero, and the WIRE-OR bus is pulled to zero by gate *z* thereby making ONE KEY zero. In similar fashion if any two keys are depressed a set of MB*i* and MB*i*′ lines would be grounded. Thus, had A_k and B_k been depressed double, both MB1 and MB2 lines are the same; with A_k and C_k selected double, only MB2 and MB2′ are both zero.

Bounce error elimination in the keyboard system is performed in the circuits of FIG. **5**C and **5**D. FIG. **5**D is the buffer and comparator portion of the keyboard logic showing the array of 12 stages forming a KB*i* flip flop register as the keyboard buffer. When the IK*i* lines from the keyboard unit differ from the KB*i* data in the buffer, the COMPARE line is low due to the logic provided by ANDS A and B and inverter C. Thus if IK1 is zero, gate A wants to have a high output, but if gate B has two ones at its input, COMPARE will be zero. The output of gate C is the inverse of IK1, or one, so that if KB1 is one, the no compare condition is met for this bit. All 12 bits must have IK and KB lines which are the same respectively for COMPARE to be high.

The KBWRITE signal loads the KB*i* buffer of FIG. **5**D with the value of IK*i* at the time KBWRITE pulse occurs. With IK*i* at zero, gates D have a high at their output, and gates E will pulse low when KBWRITE occurs. When gate E pulses low, KB*i*′ goes high and KB*i* goes to zero, holding in this state until such time as gates D pulse low.

The gating of KBWRITE for FIG. **5**D is illustrated in FIG. **5**C. There are two STROBE generators **75** and **76**. The generator **75** is a free running pulse generator, delivering a 1 μs pulse with about 6 ms period called STROBE **2**. The generator **76** when it is gated on by OR **77** pulses about 3 ms after STROBE **2** and produces the same pulse width output which is called STROBE **1**.

The STROBES 1 and 2 drive logic which comprises flip flop G, H driven by AND's F and J; flip flop K, L driven by ONE KEY and AND M; and KBR and KBR′ flip flop N, P.

When KDN is high, STROBE **1** is gated on. If ONE KEY is also high, but KBR′ is low, STROBE **1** will cause gate F to pulse to zero latching gate G to high. If COMPARE is high at the next STROBE **2**, gate M will pulse down and latch gate L and KBR high. If COMPARE is low, gate J will pulse low at STROBE **2** (instead of gate M) latching gate G low, thus inhibiting KBR until COMPARE at STROBE **2** occurs. At the next STROBE **1** if KBR is still low gate F pulses again, and the buffers are again loaded by KBWRITE and gate G latches high.

When KDN and ONE KEY fall the only change that occurs is that STROBE **1** is inhibited. The keyboard logic buffer is now loaded with valid data. After this data has been utilized, a RESET′ pulse from the I/O control **53** causes KBR to drop back to zero, releasing the keyboard for the next operation.

THE CHARACTER GENERATORS

A detailed description of the character generation will now be given with reference to FIGS. **2**A–**2**E, where for the purpose of simplicity the generation of a four-stroke character is described. It will be readily understood that the extension of the technique described with reference to these figures to generate a 13-stroke

character as described in connection with FIG. 1A–C can be achieved by those skilled in the art.

The circuit shown in FIG. 2A comprises a ring counter corresponding to ring counter 15 having a plurality of outputs p, at each of which appears a positive square wave pulse P1, P2, etc. typically of +8 volts, and of form shown in FIG. 2B (similar to pulses T0–T15 shown in FIG. 1C). Thus the interval from time *t*0 to time *t*1 of the first pulse P1 is the same as the interval *t*1 to *t*2 of the second pulse P2, and so on. Connected to each output *p* is a converter 2 comprising a dide bridge 3 having a positive constant current supply I1, e. g., 2 milliamperes at +6 volts, and a negative constant current supply, e.g., 2 milliamperes at −10 volts. The converters 2 produce as output signals the overlapping triangular waveforms T1, T2 . . . as shown in FIG. 2C. These waves may be amplified by amplifiers 3 which have output terminals *q*.

The several terminals *q* are connected through resistances R1, R2, R3, R4, etc. to a summing junction J. These resistances have ohmic values selected to reduce the amplitude of the triangular voltages T1, etc. by different amounts so as to produce attenuated triangular voltages T'1, etc. as shown in FIG. 2D. From FIG. 2D it can be seen that resistor R1 has a very low or nearly zero value and voltage T'1 is not attenuated with respect to voltage T. Resistance R2 has an extremely high or open circuit value so that voltage T'2 is attenuated to zero level. Resistances R3 and R4 have intermediate values and produce voltages T'3 and T'4 attenuated about one-half. The attenuated voltages retain their equal frequency, duration and overlap, but are added together during transmission through the resistors to the summing junction J. This addition is shown graphically by projection of FIG. 2D to FIG. 2E.

As shown in FIGS. 2D and 2E from time *t*0 to time *t*1 attenuated triangular pulse T1' appears as an upward excursion from zero of voltage *Vy* appearing at the junction J. From time *t*1 to time *t*2 the downward excursion of pulse T1' is added to pulse T2' Pulse T2' remaining at zero level, however, the junction voltage *Vy* follows pulse T1' to zero. From time *t*2 to time *t*3 the junction voltage follows the upward excursion of pulse T3' to an intermediate amplitude unaffected by the overlap with zero level pulse T2'. From time *t*3 to time *t*4 the upward excursion of pulse T4' is compensated by the equal and opposite excursion of pulse T3' thereby holding voltage *Vy* at the intermediate level. By suitable blanking techniques the subsequent excursion of pulse T4' is blocked from entering into the generation of waveform *Vy*.

Waveform *Vy* of FIG. 2E respesents the time versus vertical amplitude of a cathode ray tube deflecton voltage. Waveform *Vx* represents the horizontal deflection voltage and is generated by a circuit generally identical with that of FIG. 2A but with attenuator resistor selected to produce suitable excursions of waveform *Vx* during the same time intervals *t*0 to *t*1, etc. Projected from waveforms *Vx* and *Vy* is the character "A" which the beam of the cathode ray tube traces when the signals *Vx* and *Vy* are applied respectively to its horizontal and vertical deflection circuits. During time *t*0 to time *t*1 the excursions of voltages *Vx* and *Vy* produce a traverse or stroke S1 along one leg of the character A. During the subsequent time intervals strokes S2, S3 and S4 complete the tracing of the character.

The vertical deflection signal at the junction J is amplified in a typical amplifier stage 4 and the amplified signal *Vy* is applied through a gate G to the cathode ray input *r* of deflection circuits indicated as deflection plates 5 for the vertical signal component *Vy*. The gate is opened from time *t*0 to time *t*4 and blanks out excursions of voltages *Vy* occurring outside this interval. Simultaneously the corresponding horizontal deflection voltage *Vx* is gated through a terminal *s* to the horizontal deflection system shown as plates 6. In similar manner the graphic strokes obtained using V1 and V2 waveforms in FIG. 1C can be gated to the deflection means 5, 6 of the CRT through ORS 78,79.

While a four stroke character requiring only four resistors is shown and has been given as an example, other more elaborate characters can obviously be synthesized in the same manner by an extension of these techniques. In the preferred embodiment of FIG. 1 the characters are generated with 13 strokes between times T3 and T10.

THE DEFLECTION CONTROL SYSTEM

The description of the gross deflection controls and the application of the fine deflection control signals to control the position of the cathode ray beam in the indicator tube 30 will now be described with reference to FIGS. 3A and 3B. While the system described with reference to these figures subdivides the screen of the cathode ray tube into a page format having a plurality of horizontal lines each of which is subdivided into a plurality of character positions and for the purpose of illustration a particular subdivision is shown, it will be understood that the disclosure can be extended to subdivide the screen 31 of the cathode ray tube 30 into many more character positions and in particular for the system shown in FIGS. 1A–C, a subdivision into 2,000 character positions is described. The cathode ray tube character display system shown in FIG. 3A provides for tracing alphanumeric characters, symbols, graph elements and like information units in predetermined selected spaces on the screen 31 of the tube. At the center of FIG. 3A is the screen 31 of a CRT imaginarily divided into rows and columns of adjacent small rectangular areas or elemental spaces. On a 17 in. CRT screen there may be, for example, 40 lines of 50 character keyboard spaces for a 2,000 character display. A typewriter keyboard 51 is used as herein described to manually select one of the spaces and the character to be displayed in the selected space. The character identity code is stored as a digitally coded electrical signal in the loop delay memory system 33 as shown in FIG. 1A capable of storing 2,000 character codes plus margin codes in a timed relationship to the location of the electron beam in a selected space on the CRT screen. Circulation of the codes in the memory system 33 is timed from the master clock 11 which also times four CRT deflection channels 6, 7, 8 and 9. The first two channels 6 and 7 respectively generate the X and Y components of analog electrical signals, as described with reference to FIG. 1C, representing each of the characters on the keyboard, typically 50 to 100 characters. Each X, Y pair of analog character signals, when selected, is applied to the fine X and Y deflection

coils CX and CY of the cathode ray tube to cause the cathode ray to trace the character within the selected space of the screen **31**.

Concomitantly gross deflection channels **8** and **9** generate and apply X and Y step deflection currents to the gross X and Y deflection coils SX and SY of the cathode ray tube. These gross deflection currents cause the electron beam to scan the CRT screen horizontally line by line, the ray pausing at each space where it is finely deflected within the space by the character channels to trace any character selected for the space. The gross deflection channels **8** and **9** will be described in detail after a brief consideration of the fine deflection channels **6** and **7**.

Each fine or character channel comprises a plurality of character generators **17'** or **17''** which as previously stated may be of the type described in my copending application Ser. No. 587,583, filed Oct. 18, 1966 and entitled ELECTRIC SIGNAL GENERATOR. The respective X Character Generators **17'** and Y Character Generators **17''** continuously generate analog deflection voltage signals which, when applied to the fine deflection coils CX and CY cause the strokes of alphanumeric characters to be reproduced as the characters within each elemental space in visibly readable form as shown in FIG. **3B**. For this purpose each character generators **17'** and **17''** deliver the total repetoire of analog signal voltages respectively to an equal number of gates represented by the stages **33** and **34**. At an appropriate time depending on the position of a character identity code in the memory cycle the selected character identity code will open one of the X gates **33** and a corresponding Y gate **34** thereby gating one each of the X and Y analog current signals to the respective differential amplifier stages **36** and **37** and in coil driver stages **38** and **39**, and thence to the X and Y fine deflection coils CX and CY. The selected character is then traced in the selected space on the CRT screen in the very brief interval, for example, 8 microseconds, during which the gross deflection current holds the cathode ray at the particular space.

The gross deflection channels **8** and **9** step the cathode ray over the screen area in about one-sixtieth of a second by applying to the gross deflection coils SX and SY currents which produce deflections according to the step waveforms shown in FIG. **3B** where for illustration the cathode ray tube screen shows only six lines of eight squares as representative of a 40 by 50 square display. In FIG. **3B** the waveform *Ex* is produced by a step or staircase generator **41**. This step waveform undergoes amplifications in a differential amplifier **42** and power amplification in a driver **43** which applies a corresponding current waveform IX to the deflection yoke SX. As the current waveform steps from a negative value, through zero to a positive value, the cathode ray is stepped horizontally at 8 microsecond intervals from one space to the next as shown in waveform *Ex* in FIG. **3B** and in more detail in FIG. **14***g*.

After each stepwise horizontal line scan, a vertical deflection signal *Ey* produces a downward deflection of one line at intervals of time so that the cathode ray stops for an 8 microsecond interval each space in progression proceeding from the upper left-hand space and each downwardly succeeding left-hand space to the lower right-hand space. Thus a *y* stair generator **44** produces a waveform *Ey* for every predetermined multiple of the steps of *Ex* thereby advancing the scan line by line. The staircase wave *Ey* is amplified in differential amplifier **46** and driver **47** to supply the current *Iy* to the deflection yoke SY. Feedback resistors *Ra* and R_b supply error signals to the amplifiers **42** and **46** respectively to linearize the sweeps. Similar feedback may be employed from resistors *Rc* and *Rd* in the fine deflection system.

The progressive scan of the cathode ray over the screen **31** continues repeatedly under the control of the clock **11**. And at times in the progression selected by the keyboard **51**, or other data source characters or other information units whose identity codes are in memory are written in selected spaces by currents applied to the fine deflection yokes CX and CY.

CURSOR COUNTERS AND CONTROLS

FIGS. **6A** and **6B** show details of the active and dormant cursor counters, the high speed counter and the swap register as previously described with reference to FIG. **1B**. Referring now to FIG. **6A**, the description and operation of the high speed counter **81** and the active cursor modules **82** and **83** of FIG. **1B** will be further described. The high speed counter comprises a 7-stage X counter **101** and a 6-stage Y counter **102**. The 7-stage counter **101** counts the $\gamma 12$ input pulses and resets itself after a full line count of 52 characters while counter **102** resets itself after a full page count of 40 lines. The counters **101** and **102** thus have a count registered therein which is uniquely identified with a single character position on the lines of the display screen **31**. When the count reaches the end of the line the next $\gamma 12$ pulse resets the counter **101** and produces a begin line (BL) pulse on line **100** and a line clock signal on line **103**. The line clock signal on line **103** passes through an enabled AND **104** to provide the count input signal to counter **102**. At the end of a count in the Y counter **102** corresponding to the number of lines on the screen format frame clock (FC) and begin frame (BF) output signals on lines **105** and **106** are produced.

The count in the X counter **101** is applied in parallel to a comparator **107** for comparison with the count in a non-synchronous up-down X counter **108**. The comparator **107** thus will produce an output (LINE COMP) on line **109** whenever the synchronous X counter **101** registers a count corresponding to the count standing in the non-synchronous X counter **108**. Similarly the stages of the synchronous Y counter **102** are read in parallel to a comparator **111**, the other input of which is derived from a non-synchronous up-down Y counter **112** so that the comparator **111** is conditioned for an output (CA) on line **113** whenever the count in the synchronous Y counter **102** reaches the count standing in the non-synchronous Y counter **112**. The output of the comparator **111** only occurs when the parallel inputs from the counters **102** and **112** compare and a LINE COMP signal on line **109** is applied at the input. This output called cursor compare (CA) appears on line **113** and thus defines in time identity a particular character window by line and column on the full page format of the cathode ray screen **31**. The CA pulse is applied to the display control **25** (FIG. **1C**) to produce a code selection signal for producing a visible cursor marker on the screen **31** such as an underlining of the particular character location, as previously described.

The count in the non-synchronous X counter **108** can be set in a number of ways. Depressing any character key will produce a SHIFT GATE signal to the loop interface **55** (FIG. 1A) which permits the character code to be read by γ pulses through AND **60** and also produces on line ASR:ASL a shift right signal to input **115** which advances counter **108** to keep the active cursor located at the position for next keyboard entry of a character on the screen **31**. By depressing the STEP RIGHT key on the keyboard a signal appears on line **115** which steps the X counter **108** to the right one character position. Holding the STEP RIGHT key down after a short delay produces a repetitive pulse signal which steps the cursor automatically as many spaces as desired. Similarly the step left key will produce on line **116** a signal to reverse the counter **108** one character position.

By means of signals on the lines **115** and **116** therefor, the count in the non-synchronous X counter **108** can be stepped position by position right or left on a line and if stepped successively to the right to the end of the line produces an X carry signal on line **117**. The counter **108** can be reset by a pulse on line **118** which establishes the home position (HOME CX) for the X counter and moves the cursor to the extreme left character position on a line. A load active cursor pulse on line **119** operates to load the address appearing on lines DCX0–DCX6 into the X counter **108**. This feature is used for positioning and interchange of the active and dormant cursors as hereinafter described.

In similar manner the non-synchronous Y counter **112** can be stepped up or down by a step down signal **121** or a step up signal **122** thus selecting the line on which comparison will occur. A home CY pulse on line **123** resets the counter **112** to provide the comparison on the top line of page format. If both home CY and home CX pulses occur on lines **123** and **118** respectively the HOME position for the cursor in the upper left hand corner of the page format is established. The dormant cursor address on lines DCY0–DCY5 can be loaded into the Y counter **112** by a load cursor active pulse on line **124**.

Referrng now to FIG. **6B** comparators and counters are shown for performing the same function for the dormant cursor as has been described in connection with FIG. **6A** for the active cursor. For this purpose corresponding parts are numbered with the primed numbers relating them to their counterparts in FIG. **6A** and the description of FIG. **6A** applies as well to the primed number components of FIG. **6B**. The principle difference between the dormant cursor and the active cursor resides in the fact that the dormant cursor remains at a fixed position established by the non-synchronous dormant X counter **108'** and the Y counter **112'** without a keyboard signal on line **115'**. Thus the comparison in comparator **111'** does not advance character by character as input data is obtained from the keyboard. Conversely, when data is to be transmitted (XMIT) or printed (HARD COPY) either mode produces a readout starting at the dormant cursor and SHIFT GATE for these modes produces a STEP RIGHT signal on line DSR:DSL to input **115'** of register **108'**. Thus the dormant cursor follows the removal of characters as they are read off the screen.

Referring now again to FIG. **6B**, an X swap register **125** is provided for interim storage of the word read from the non-synchronous active X counter **108** of the cursor system as applied on input lines ACX0–ACX6. Similarly Y swap register **126** is provided for interim storage of the word read from the non-synchronous active Y counter **112** in the cursor system of FIG. **6A** as applied on lines ACY0–ACY5. The word stored in the X swap register **125** can be transferred to the non-synchronous X counter **108'** in response to load dormant cursor X signal on line **119'** resulting from keyboard operation. Similarly the Y swap register **126** supplies the word determined by the X and y active inputs thereto to the non-synchronous X and Y counters **108'** and **112'**, the outputs of which will transfer the position of the dormant cursor to that of the active address so obtained.

This provision of the swap registers **125** and **126** permits interchange of the active and dormant cursor locations performed as follows. A change cursors (CHG CUR) signal from the keyboard produces a load swap signal on line **130** and loads the swap registers **125** and **126** with the respective X and Y address of the active cursor obtained on lines ACX0–ACX6 and ACY0–ACY5. Subsequently in response to load cursor active signals on lines **119** and **124** the dormant cursor address on lines DCX0–DCX5 sets the respective X and Y non-synchronous active cursor counters **108** and **112** thereby causing the active cursor compare signal CA to occur at the dormant cursor location. Thereafter, in response to load cursor dormant signals on lines **119'** and **124'** the contents of the swap registers **125** and **126** are transferred to the respecive non-synchronous dormant cursor counters **108'** and **112'** where it is available for the next cycle comparison in comparators **107'** and **111'** to produce dormant cursor compare CD. Thus the dormant cursor appears at the former active cursor address location. This sequence is controlled at γ5, γ7 and γ9 by the logic shown in FIG. **17**.

Referring again to FIGS. **6A** and **6B** the description for changing the location of the active cursor to the position of the dormant cursor or the position of the dormant cursor to the position of the dormant cursor to the position of the active cursor will be given.

To change the location of the active cursor to that occupied by the dormant cursor the load cursor active signals on lines **119** and **124** are produced in response to the coincedent cursors key (COIN CUR) thereby loading the counters **108** and **112** with the address of the dormant cursor obtained from counters **108'** and **112'**. The next comparison in comparators **107** and **111** will, therefore, produce CA on line **113** at this address.

To change the location of the dormant cursor to that occupied by the active cursor, the control key and COIN CUR are depressed to produce the load swap signal on line **130** which loads the swap registers **125** and **126** with the address of the active cursor obtained from counters **108** and **112**. Thereafter the load cursor dormant signals on lines **119'** and **124'** load the active cursor address present in the swap registers into the registers **108'** and **112'** so the following comparison in comparators **107'** and **111'** produce CD on line **113'** at this address. This sequence occurs at γ4 and γ8 as indicated in FIG. **1D**.

LOOP GATING AND EDITING LOGIC

The editing control **56'** of FIG. 1D receives the control code outputs from the loop interface **55** which are produced by decoding keyboard control codes. These inputs to the editing control **56'** produce outputs as shown in FIGS. **8–12** and **17** to control the loop gating logic of FIG. **7** and the various counters to achieve the desired functions of clear screen (CLS), clear message (CLM), clear line (CLL), roll up (RU), roll down (RD), insert (INS), overwrite (OVR), remove (REM) and change cursors (CHG CUR).

Referring now to FIG. **7** loop gating logic for control of the switch S1 described in FIG. 1A will be described. The delay line driver **68** receives the data word output of the input register of the loop interface **55** which appears at terminal **72** through OR **127** and the bits are clocked by the γ input to driver **68** for insertion into the delay line **63**. The OR **127** also receives the output of AND **128** which is enabled by FLOCK whenever keyboard data is to be received and when enabled passes the output of OR **129**.

For overwrite (OVR) which is the normal data entry mode, the characters from terminal **72** are entered into the loop and the previously existing loop character for that point is lost. The OR **129** has a plurality of inputs from ANDs **130, 131, 132, 133** and **134**. The AND **130** is enabled by the keyboard insert INS assertion and when enabled passes data from terminal B, the serial output of the second shift register **62**. The AND **131** is enabled by the keyboard remove REM assertion and when enabled passes the data from terminal A, the serial input to the first shift register **61**. The AND **132** is enabled by the ERASE' (NOT ERASE) assertion and when enabled passes the data on terminal C, the serial output of the first shift register **61**. The ANDs **133** and **134** are both enabled by the ERASE assertion and when enabled pass the space code which is a one bit at $\gamma 6$ and $\gamma 8$.

Referring now to FIG. **8** the clear screen logic will be described. A keyboard clear screen signal CLS on line **136** is applied through an inverter **137** to set a clear screen latch **138**. The latch **138** is a circuit which provides the logic function of a bistable flip flop having set and reset inputs and complementary outputs which reverse whenever the latch is set or reset. The set output of the latch **138** is applied to an AND **139** which has a begin frame (BF) input on line **141** thereby providing an output to OR **142** whenever the latch **138** is set and the begin frame pulse appears on line **141**. The output of OR **142** is inverted in inverter **143** to set an erase latch **144**. The erase latch provides an assertion on line **145** of the ERASE signal and the ERASE' (NOT ERASE) on line **146**. The output of line **145** is used as an input for an AND **147** which has as its other input the negation output of the clear screen latch **138**. Thus after the erase latch **144** has been set the AND **147** will produce an output when the clear screen latch **138** is reset which signal passes through OR **148** and inverter **149** to reset the erase latch **144**. The reset of the clear screen latch **138** is provided by the frame clock pulse (FC) on line **151** after inversion in inverter **152**. The assertion and negation of the erase signal appearing on lines **145** and **146** respectively are applied to the loop gating logic in FIG. **7**. The circuit operates in response to a keyboard clear screen (CLS) signal to set the erase latch **144** at begin frame (BF) and reset the erase latch **144** at frame clock (FC). The erase latch assertion and negation signals between BF and FC applied to the ORs **132, 133** and **134** of FIG. **7** clear the entire screen by disabling data input to the memory loop from terminal B and substituting the blank or space code bits at $\gamma 6$ and $\gamma 8$ from ANDs **133** and **134**.

Referring now to FIG. **9** the logic for clear line CLL function will be described. The clear line function is defined as erasing from the screen and loop memory characters located from the selected position of the active cursor to the end of that particular line. Clear line (CLL) input signals from the keyboard are applied on line **155** to set a clear line latch **156** which has its set output applied to two ANDs **157** and **158**. The AND **157** produces an output when the active cursor pulse (CA) occurs which output is applied to set the erase latch **144** by application through one of the alternate inputs to the OR **142** in FIG. **8**. The AND **158** when enabled by the set output of the latch **156** produces at occurrence of the begin line pulse (BL) an output which clears the erase latch **144** by applying one of the alternate signal inputs to the OR circuit **148** in FIG. **8**. The occurrence of this signal from the AND **158** is also applied to reset the clear line latch **156**. Thus the circuit of FIG. **9** provides for erasing information from memory from the active cursor (CA) position until the next begin line (BL) signal which eliminates that portion of the particular line in question as determined by the location on the screen of the active cursor.

Referring now to FIG. **10** the logic for performing the clear message CLM function will be described. Clear message is defined as the removal of the portion of the message on the screen **31** which appears between the dormant and active cursors. A clear message signal (CLM) from the keyboard on line **161** is applied to set a clear message latch **162** the set output of which is applied to an AND **163**. The dormant cursor compare pulse (CD) is applied as the second input to the AND **163** and when CD occurs an output is produced from AND **163** if the latch **162** is set. The output of the AND **163** is applied to set the erase latch **144** through OR **142**. The set output of clear message latch **162** is applied to a second AND **164** which has the active cursor compare pulse (CA) applied as a second input and when both inputs are present the AND **164** produces an output which resets the erase latch **144** through OR **148**. This same output on line **165** is applied to reset the clear message latch **162** and to set a swap cursor latch **166**.

The output of the swap cursor latch **166** is applied to two ANDs **167** and **168** which have respective inputs $\gamma 4$ and $\gamma 8$ to produce output pulses at the respective times of these pulses on lines **171** and **172**. The output on line **171** is applied to lines **119** and **124** in FIG. **6A** and operates to load the active cursor counters **108** and **112** with the address for the dormant cursor. The output on line **172** operates at $\gamma 8$ to reset the swap cursor latch **166**. Thus this operates to place the active cursor on the location of the dormant cursor thereby making the unit ready to write at the starting point of the message which has been cleared.

Referring now to FIG. **11** the logic for performing the ROLL UP function will be described. The ROLL UP function is defined as the continual elimination of

the top line on the screen with the corresponding moving of all lower lines up one line and the corresponding changes of the information in the memory loop. The ROLL UP function can be modified to include the continual adding of a bottom line from an external memory into the active loop memory thereby giving the impression of a continual presentation in a normal reading sequence of the full screen format to eventually present the entire contents of the external memory store. A ROLL UP signal (RU) appears from the keyboard on line **176** and this same signal is applied to home the active cursor (CA) by energizing the home CX and CY lines **118** and **123** in the counters **108** and **112** of FIG. **6A**. The ROLL UP pulse on line **176** after inversion in inverter **177** sets a ROLL UP latch **178** and the same signal on line **179** is applied to set the clear line latch **156** of FIG. **9**. Since the active cursor (CA) has been previously homed in both X and Y by the ROLL UP signal on line **176**, the line which is cleared by setting the clear line latch with the signal on line **179** is the top line of the screen format. The set output of the latch **178** is applied to enable an AND **181** which during the set erase signal obtained from the output of FIG. **9** and applied on line **182** produces an output which sets an inhibit latch **183**. This same signal which sets the latch **183** is also applied on line **184** to the CA to last line input on the counter **112** of FIG. **6A**. The same signal is used to reset the ROLL UP latch **178**. The reset output of the inhibit latch **183** is connected by line **185** to input INH VERT of AND **104** which supplies the carry count to the Y counter **102** of FIG. **6A**. Thus while the inhibit latch of **183** is set the AND **104** is disabled and the first line carry pulse from counter **101** to **102** in FIG. **6A** is inhibited. The inhibit latch **183** is reset by a begin line signal passing through AND **186** at $\gamma 12$ thereby permitting the carry count from X counter **101** to Y counter **102** to occur for all lines subsequent to the first line which has the effect of writing the second line in the position of the erased first line and all subsequent lines on the screen are moved up one line.

Referring to FIG. **12** the logic for performing the ROLL DOWN function will be described. ROLL DOWN is defined as generally the converse of ROLL UP in which the bottom line on the screen is removed and each higher line is moved down one line position to give the screen the appearance of rolling down the information displayed with all lines moving down together. A ROLL DOWN (RD) signal from the keyboard is applied on line **186** where it is coupled to set CA to last line in FIG. **6A**, to set the clear line latch **156** of FIG. **9** and through inverter **187** to set the ROLL DOWN latch **188**. The set output of the ROLL DOWN latch **188** enables an AND **189** which upon the occurrence of the set erase signal from FIG. **9** produces an output through inverter **191** on line **192**. The signal on line **192** is applied to OR **110** to step the vertical counter **102** thereby causing character information from memory which previously was written on the first line of the display screen to be written on the second line and due to the regular generation of the Y stair waveform each subsequent line of characters will be written one line lower than it previously appeared. The output on line **192** is also applied to reset the ROLL DOWN latch **188**.

Referring now to FIG. **16A, B** and **C**, a description of the generation of graphic strokes will be given. Graphic codes may be derived from any external source or as shift or control keyboard codes for selecting the sequence of graphic strokes desired. FIG. **16A** shows the imaginary subdivision of a character window on the cathode ray screen **31** into a plurality of points which can be used as the locus of the beam at the start of the stroke $X_i\ Y_i$ and the locus of the beam at the end of the stroke $Y_f\ Y_f$. The subdivision of the character interval is provided by four equally spaced imaginary dots in both the horizontal and vertical direction and these rows and columns can be selected by a two bit binary word as indicated. The generation of the stroke between any two points in FIG. **16A** is accomplished by selecting the appropriate analog quantities for the X and Y deflection in accordance with the digital identification of the starting point $X_i\ Y_i$ and the finishing point $X_f\ Y_f$. For this purpose in FIG. **16B** the overlapping slope waveforms V_1 and V_2 of FIG. **1C** are shown applied to input lines **201** and **202** respectively. The V_1 waveform is applied to a D/A converter **203** and another D/A converter **204**. Similarly the waveform V_2 on line **202** is supplied to a D/A converter **205** and another D/A converter **206**. The outputs of the D/A converters **203** and **205** are summed for application on line **207** to a gate **208** which when enabled supplies the X fine signal output on line **23**. Similarly the D/A converters **204** and **206** have their outputs added and applied on line **209** to a gate **211** which when enabled supplies the Y fine output signal of line **24**.

The D/A converters **203, 204, 205** and **206** are all controlled by two bit digital words which are the CH0–CH7 selection pulses. These pulses taken two at a time permit the D/A converters to select the analog amplitude to which the input voltage V_1 or V_2 will be modified to as it passes through the D/A converter. This amplitude selection is indicated in FIG. **16C** and the selected portion amplitude versions of V_1 and V_2 are combined in the same manner as described for the triangular waveforms in FIG. **2** to provide the desired X fine or Y fine deflection signal on lines **23** and **24**.

For example, to produce the X– deflection shown in FIG. **16A** V_1 would be selected by D/A **203** at the binary zero—zero amplitude level while V_2 would be selected by the D/A **205** at the one—one level. The Y deflection on line **24** on the other hand would be obtained by a binary zero—zero amplitude contribution from V_1 and a full amplitude contribution from D/A **206** corresponding to the bits one–zero. In this fashion any starting point $X_i\ Y_i$ and any finishing point $X_f\ Y_f$ on the array of points shown in FIG. **16A** can be obtained at any character interval. Since this interval on the face of the screen is approximately one-eighth of an inch long is obvious that any desired curve can be traced by a succession of such strokes either smoothly connected or discontinuous.

The character display terminal of the present invention has been described in terms of the basic elements for data input, display and editing at a local terminal to provide flexibility, speed, capacity and editing features not heretofore available using relatively simple and reliable components. The usefulness of such local terminals is readily extended to applications for computer input-output and communications applications by in-

terfacing with an output printer or communications line. As previously stated I/O control **74** permits loop bits to be transferred to hard copy or dataset units as shown in FIG. **1A**. An electric code responsive typewriter **201** is supplied print signals from an amplifier **202** which receives typewriter code signals from the hard copy coding and control units **203, 204**. Similarly the I/O control **74** can supply serial data bits on line SD to I/O control **205** for a telephone dataset **206**. Data signals received from the dataset **206** are applied on line RD to I/O control **53** for processing in the same manner as described for data originating from keyboard **51**.

The capacity of the present system can be greatly increased by the addition of a drum storage unit **207**. The drum **207** is interfaced through an interface unit **208** which provides buffer storage. Data received on the DATA OUT line from I/O control **74** is stored in the buffer and written on the drum **207**. Data read from the drum is stored in buffer **208** and supplied on line DATA IN to the I/O control **53** for similar processing in the loop storage or editing control systems. As previously mentioned the presence of external storage such as drum **207** permits comprehensive editing of extensive text materials when used with roll up and roll down controls to review on the screen the entire contents of the external storage unit. For this purpose the drum data is entered into recirculating storage loop via I/O control **53** and returned to the drum **207** via I/O control **74**.

Many variations and modifications both as to structure and utilization of the disclosed embodiment will now be apparent to those skilled in the art. The invention, accordingly, should not be considered as limited to the specific structure shown but only as defined by the scope of the appended claims.

I claim:

1. A refresh display terminal comprising:

a. display means operative to produce a visual display in direct response to externally supplied character defining digital signals applied thereto;

b. recirculating storage means operative to sequentially store a plurality of character defining codes corresponding to an array of characters to be displayed on said display means;

c. means responsive to said codes for generating character forming signals to control generation of characters on said display means;

d. means for synchronously operating said display means and said storage means whereby the location of said character defining code in said storage means corresponds to a display position on said display means thus providing a cyclic refresh of the characters visible on said display means from the character defining codes carried in said recirculating storage means;

e. synchronous register means operating synchronously with said display and storage means for providing a signal representing a relative time identification in each refresh cycle for each said character position;

f. non-synchronous register means selectively operable to be set corresponding to said character position for producing control function signals upon correspondence between said character positions selected and said time identification; and

g. means responsive to said control function signals for altering the sequence of character defining codes whereby the array of characters appearing on said visual display are selectively modified.

2. Apparatus according to claim **1** in which said control function signals modify the sequential code store in said recirculating storage means for modifying said visual display.

3. Apparatus according to claim **1** in which said visual display is a page format comprising a plurality of lines each of which is subdivided into a plurality of character positions, means for setting said non-synchronous register to select any line and any subdivision thereof and means for visually indicating on said display the character position selected.

4. Apparatus according to claim **3** and including means for entering codes in said storage means character by character and means for advancing said non-synchronous register one character position for each character code entered.

5. Apparatus according to claim **3** and including means for setting said non-synchronous register to correspond to a predetermined character at the left end of the top line of said page format.

6. Apparatus according to claim **3** and including a keyboard operated switch means within the refresh memory for opening the circuit therein to clear said storage means of selected character defining codes and sequentially permit the insertion of new character defining codes whereby to allow various editing operations on said page format.

7. Apparatus according to claim **5** and including means operable upon setting said non-synchronous register for clearing said storage means of all of said codes.

8. Apparatus according to claim **3** and including a second non-synchronous register, means for setting said second non-synchronous register to select any line and any subdivision thereof, and means for visually indicating on said display the character position selected by said second non-synchronous register.

9. Apparatus according to claim **8** and including a keyboard operated switch means within the refresh memory for opening the circuit therein to clear said storage means of selected character defining codes corresponding to characters displayed between the character positions selected by both of said non-synchronous registers.

10. Apparatus according to claim **9** and including a keyboard controlled multi-vibrator operatively connected to the second non-synchronous register for stepping said second non-synchronous register one character position at a time as said codes are cleared from said storage means.

11. Apparatus according to claim **10** and including a buffer means operably connecting the refresh memory directly to an output device for reading said codes transferred from said storage means as outputs to said buffer means.

12. Apparatus according to claim **8** and including logic gates operable for transferring the count in one of said non-synchronous counters to the other said non-synchronous counter.

13. Apparatus according to claim **5** and including a buffer register, means operable for transferring the count in one of said non-synchronous counters to said

buffer register, and means operable for transferring the count in said buffer register to the other of said non-synchronous counters.

14. Apparatus according to claim 13 and including a swap register operable in conjunction with said buffer register for transferring the count in said other counter to said one counter after the count in said one counter has been transferred to said buffer register but before the count in said buffer register has been transferred to said other counter.

15. A cathode ray tube display terminal comprising:

a. a cathode ray tube having orthogonal deflection means for positioning the electron beam to produce a visible trace on the screen of said tube;

b. first deflection signal means comprising means coupled to said deflection means for regularly positioning said beam at a plurality of ordered positions on said screen with a predetermined dwell time at each said position to subdivide said screen into a character page format;

c. recirculating storage means operative synchronously with said first deflection signal means for providing sequential storage of a plurality of character defining codes corresponding to an array of characters for each of said ordered positions whereby to read in or out of storage each of the character defining codes in timed relation of each said dwell time;

d. character waveform generator means operative synchronously with said first deflection signal means for generating character waveforms during each of said dwell times corresponding to each stored character defining code to be displayed;

e. second deflection signal means coupled to said deflection means and operative in response to said character waveform generator means for tracing selected character waveforms on said screen during said dwell times;

f. refresh signal means for synchronously decoding from said storage means the character defining code for each of said ordered positions and applying the character waveform identified by said code to said second deflection signal means for displaying an image thereof on said screen;

g. non-synchronous means selectively operable for identifying any of said ordered positions on said screen;

h. means for comparing the position identified by said non-synchronous means with that determined by said first deflection signal means and producing a control function signal when said positions compare; and

i. means responsive to said control function signal for altering the sequence of character defining codes whereby the array of characters appearing on said visual display are selectively modified.

16. Apparatus according to claim 15 and including graphic stroke selection means operative to enter graphics codes into said storage means; and graphic waveform generator means operative synchronously with said first deflection signal means comprising:

means operating synchronously with said first deflection signal means for generating a set of time overlap opposite slope waveforms during each of said dwell times;

means responsive to detection of a graphics code stored in said storage means for selectively combining said time overlap waveforms in predetermined proportion to produce resultant graphics deflection waveforms as determined by the information content of said graphics code; and

means responsive to said detection of a graphics code for disabling the application of character waveforms to said second deflection signal means by said refresh signal means and applying instead said resultant graphics deflection waveforms.

17. Apparatus according to claim 15 and including means for visually indicating on said screen the position identified by said non-synchronous means.

18. Apparatus according to claim 17 and including switch means within the refresh memory for opening the circuit therein and operatively connected to the keyboard and selectively operable therefrom for clearing said storage means of character defining codes corresponding to characters displayed on said page format subsequent to said position identified.

19. Apparatus according to claim 18 and including means for altering the relation between the remaining stored character identity codes and said ordered positions in accordance with said predetermined portion of said page format.

20. Apparatus according to claim 17 and including:

a. a second non-synchronous means selectively operable for identifying any of said ordered positions on said screen;

b. means for comparing the position identified by said second non-synchronous means with that determined by the said first deflection signal means and producing a second control function signal when said positions compare; and

c. means responsive to said second control function signal for altering the sequence of character defining codes whereby the array of characters appearing on said visual display are selectively modified.

21. Apparatus according to claim 20 and including means selectively operable for transferring one of said visual indications to the position occupied by the other said visual indication.

22. Apparatus according to claim 20 and including means selectively operable for interchanging the positions occupied by said visual indication.

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