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(54) Title: DELAY TRACKING METHOD AND MEMORY SYSTEM

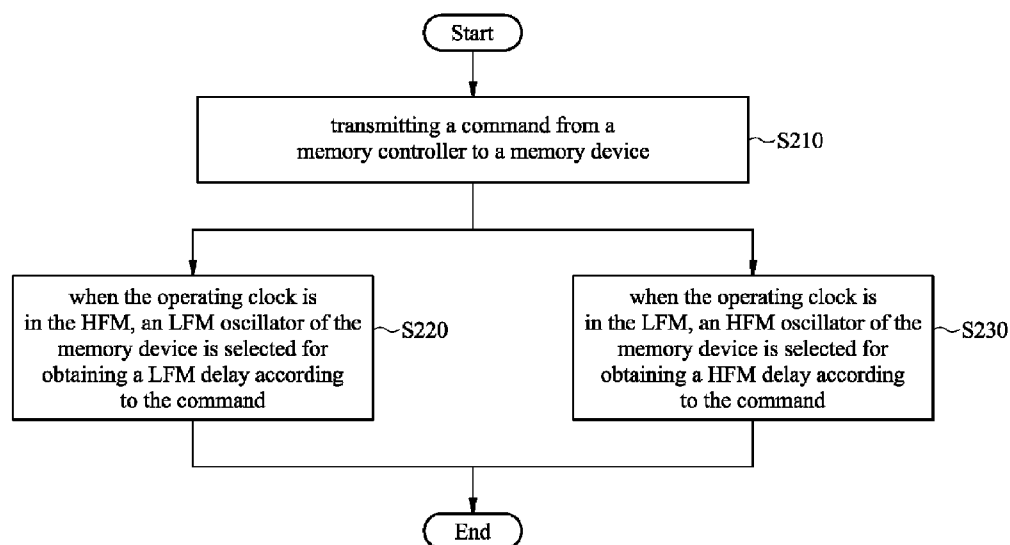


FIG. 2

(57) Abstract: A delay tracking method and a memory system are provided. The delay tracking method is applied to a memory system supporting a low-frequency-mode (LFM) and a high-frequency-mode (HFM) of an operating clock. The delay tracking method includes the steps of selecting a LFM oscillator for obtaining a LFM delay value when the operating clock is in the HFM; and selecting a HFM oscillator for obtaining a HFM delay value when the operating clock is in the LFM.

TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

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DELAY TRACKING METHOD AND MEMORY SYSTEM

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This Application claims priority of U.S. Provisional Patent Application No. 62/718,535, filed on August 14, 2018, the entirety of which is incorporated by reference herein.

FIELD OF THE INVENTION

[0002] The invention generally relates to a wireless communication technology, and more particularly, to the delay tracking for fifth-generation low-power DDR (LPDDR5) technology.

DESCRIPTION OF THE RELATED ART

[0003] In the current fifth-generation low-power DDR (LPDDR5) standard, a WCK2DQI oscillator (i.e. writing oscillator) is introduced for delay tracking in writing operations, and a WCK2DQO oscillator (i.e. reading oscillator) is introduced for delay tracking in reading operations. In addition, in the current LPDDR5 standard, a multipurpose command (MPC) is used to enable or disable the WCK2DQI oscillator or the WCK2DQO oscillator. Furthermore, in the current LPDDR5 standard, different frequency modes are introduced to save power.

[0004] However, in the current LPDDR5 standard, how to efficiently use the WCK2DQI oscillator or WCK2DQO oscillator for delay tracking in different frequency modes is not specified.

BRIEF SUMMARY OF THE INVENTION

[0005] A delay tracking method and a memory system are provided to overcome the problems mentioned above.

[0006] An embodiment of the invention provides a delay tracking method. The delay tracking method is applied to a memory system supporting a low-frequency-mode (LFM) and a high-frequency-mode (HFM) of an operating clock. The delay tracking method includes the steps of selecting a LFM oscillator for obtaining a LFM delay value when the operating clock is in the HFM; and selecting a HFM oscillator for obtaining a HFM delay value when the operating clock is in the LFM.

[0007] In some embodiments, the LFM delay value is obtained before the operating clock is switched from the HFM to the LFM. In an embodiment, the LFM delay value is obtained by periodically enabling the LFM oscillator. In another embodiment, the LFM delay value is obtained by aperiodically enabling the LFM oscillator. The LFM delay value is applied for a LFM delay tracking when the operating clock is in the LFM.

[0008] In some embodiments, the HFM delay value is obtained before the operating clock is switched from the LFM to the HFM. In an embodiment, the HFM delay value is obtained by periodically enabling the HFM oscillator. In another embodiment, the HFM delay value is obtained by aperiodically enabling the HFM oscillator. The HFM delay value is applied for a HFM delay tracking when the operating clock is in the HFM.

[0009] In some embodiments, the LFM oscillator and the HFM oscillator are selected via Multipurpose Command (MPC) command or Mode Register Operand (MR OP).

[0010] An embodiment of the invention provides a memory system. The memory system comprises a memory controller and a memory device. The memory controller generates a command. The memory device

comprises a low-frequency-mode (LFM) oscillator, and a high-frequency-mode (HFM) oscillator. The memory device receives the command from the memory controller to select the LFM oscillator or the HFM oscillator. The LFM oscillator is selected for obtaining a LFM delay value, when the operating clock is in the HFM. The HFM oscillator is selected for obtaining a HFM delay value, when the operating clock is in the LFM.

5 [0011] Other aspects and features of the invention will become apparent to those with ordinary skill in the art upon review of the following descriptions of specific embodiments of delay tracking method and the memory system.

BRIEF DESCRIPTION OF THE DRAWINGS

10 [0012] The invention will become more fully understood by referring to the following detailed description with reference to the accompanying drawings, wherein:

[0013] FIG. 1 is a block diagram of a memory system 100 according to an embodiment of the invention.

[0014] FIG. 2 is a flow chart 200 illustrating a delay tracking method according to an embodiment of the invention.

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DETAILED DESCRIPTION OF THE INVENTION

[0015] The following description is of the best-contemplated mode of carrying out the invention. This description is made for the purpose of illustrating the general principles of the invention and should not be taken in a limiting sense. The scope of the invention is best determined by reference to the appended claims.

20 [0016] FIG. 1 is a block diagram of a memory system 100 according to an embodiment of the invention. The memory system 100 may support a low-frequency-mode (LFM) and a high-frequency-mode (HFM), i.e. an operating clock of the memory system 100 may be in the LFM or HFM. The memory system 100 may comprise a memory controller 110 and a memory device 120. In the embodiments of the invention, the memory system 100 can be applied to the fifth-generation low-power DDR (LPDDR5) technology. It should
25 be noted that, in order to clarify the concept of the invention, FIG. 1 is a simplified block diagram in which only the elements relevant to the invention are shown. However, the invention should not be limited to what is shown in FIG. 1.

[0017] In an embodiment of the invention, the memory device 120 may be a dynamic random access memory (DRAM) device. As shown in FIG. 1, the memory device 120 may comprise a decoder 121, a register
30 122, a low-frequency-mode (LFM) oscillator 123, and a high-frequency-mode (HFM) oscillator 124. It should be noted that, in order to clarify the concept of the invention, the memory device 120 of FIG. 1 is a simplified block diagram in which only the elements relevant to the invention are shown. However, the invention should not be limited to what is shown in FIG. 1. The memory device 120 may also comprise other elements.

[0018] In an embodiment of the invention, the memory controller 110 may transmit a clock signal (e.g. a
35 WCK clock in LPDDR5 technology) to the memory device 120 to sample the timing signal for writing operation or reading operation to track the delay in the writing operation or reading operation. The timing signal for writing operation or reading operation may have different frequencies for the low-frequency-mode (LFM) and high-frequency-mode (HFM). The LFM oscillator 123 and the HFM oscillator 124 can be applied for delay tracking in the writing operation or the reading operation. The delay value (or delay parameters)
40 obtained in different frequency modes (i.e. LFM and HFM) are different.

[0019]When the LFM oscillator 123 and the HFM oscillator 124 are applied to a writing operation, the LFM oscillator 123 and the HFM oscillator 124 may be regarded as writing oscillators (e.g. WCK2DQI oscillator in LPDDR5 technology), and when the LFM oscillator 123 and the HFM oscillator 124 are applied to a reading operation, the LFM oscillator 123 and the HFM oscillator 124 may be regarded as reading oscillators (e.g. WCK2DQO oscillator in LPDDR5 technology), wherein the writing oscillators and the reading oscillators may not be operated simultaneously. That is to say, the memory device 120 may comprise writing oscillators and reading oscillators, and the writing oscillators may comprise LFM writing oscillator and the HFM writing oscillator and the reading oscillators may comprise LFM reading oscillator and the HFM reading oscillator. However, in order to illustrate simply, there are only one LFM oscillator and one HFM oscillator shown in FIG. 1, but the invention should not be limited to what is shown in FIG. 1. The writing oscillator and the oscillator are applied for delay tracking when the voltage and temperature change on the memory device 120. The memory controller 110 may read the value generated by the writing oscillator or the reading oscillator to determine the delay value.

[0020]In an embodiment of the invention, the LFM oscillator 123 and the HFM oscillator 124 may be integrated to an oscillator which can generate oscillation signals with different frequencies to be the LFM oscillator and the HFM oscillator. That is to say, in the embodiment, there are one writing oscillator and one reading oscillator in the memory device 120. The writing oscillator can generate oscillation signals with different frequencies to be the LFM oscillator and the HFM oscillator, and the reading oscillator can also generate oscillation signals with different frequencies to be the LFM oscillator and the HFM oscillator.

[0021]In an embodiment of the invention, the memory controller 110 may transmit a command to the memory device 120 to select the LFM oscillator 123 for obtaining a LFM delay value or the HFM oscillator 124 for obtaining a HFM delay value. When the decoder 121 of the memory device 120 receives the command from the memory controller 110, the decoder 121 may decode the command to generate a decode result. The LFM oscillator 123 or the HFM oscillator 124 are selected according to the decode result. According to an embodiment of the invention, the decode result may be a Multipurpose Command (MPC) command or a Mode Register Operand (MR OP). The LFM oscillator 123 or the HFM oscillator 124 may be enabled according to the MPC command or the MR OP in the memory device 120. In addition, according to the decode result, the MPC command or MR OP is further used to drive the LFM oscillator 123 for obtaining a LFM delay value or drive the HFM oscillator 124 for obtaining a HFM delay value. In an embodiment of the invention, the obtained LFM delay value and the HFM delay value may be stored in the register 122. The memory controller 110 may perform a LFM delay tracking or a HFM delay tracking according to the LFM delay value or the HFM delay value stored in the register 122 of the memory device 120.

[0022]In an embodiment of the invention, when the LFM oscillator 123 is selected for obtaining the LFM delay value (i.e. the memory device 120 is in the LFM currently or the operating clock is in LFM currently), the HFM oscillator 124 is enabled at the same time to obtain an HFM delay value in advance. That is to say, in the embodiment, although the operating clock is in LFM, the memory controller 110 may also transmit another command to enable the HFM oscillator 124 to obtain an HFM delay value in advance. The HFM delay value may be stored in the register 122. In the embodiment of the invention, the HFM oscillator 124 may be enabled periodically according to the command from the memory controller 110, or the HFM oscillator 124 may be enabled aperiodically according to the command from the memory controller 110. When the memory device

120 is switched from the LFM to the HFM (i.e. the operating clock is switched from the LFM to the HFM), the memory controller 110 will be able to directly use the HFM delay value for HFM delay tracking.

[0023] In another embodiment of the invention, when the HFM oscillator 124 is selected for obtaining the HFM delay value (i.e. the memory device 120 is in the HFM currently or the operating clock is in HFM currently), the LFM oscillator 123 is enabled at the same time to obtain an LFM delay value in advance. That is to say, in the embodiment, although the operating clock is in HFM, the memory controller 110 may also transmit another command to enable the LFM oscillator 123 to obtain an LFM delay value in advance. The LFM delay value may be stored in the register 122. In the embodiment of the invention, the LFM oscillator 123 may be enabled periodically according to the command from the memory controller 110, or the LFM oscillator 123 may be enabled aperiodically according to the command from the memory controller 110. When the memory device 120 is switched from the HFM to the LFM (i.e. the operating clock is switched from the HFM to the LFM), the memory controller 110 will be able to directly use the LFM delay value for LFM delay tracking.

[0024] In another embodiment of the invention, only when the memory device 120 knows that it will be switched from the LFM to the HFM (i.e. the memory device 120 is in the LFM currently or the operating clock is in LFM currently), the HFM oscillator 124 is enabled to obtain an HFM delay value in advance. The HFM delay value may be stored in the register 122. In the embodiment of the invention, the HFM oscillator 124 may be enabled periodically according to a command from the memory controller 110, or the HFM oscillator 124 may be enabled aperiodically according to a command from the memory controller 110. When the memory device 120 has been switched from the LFM to the HFM (i.e. the operating clock is switched from the LFM to the HFM), the memory controller 110 will be able to directly use the HFM delay value for HFM delay tracking.

[0025] In another embodiment of the invention, only when the memory device 120 knows that it will be switched from the HFM to the LFM (i.e. the memory device 120 is in the HFM currently or the operating clock is in HFM currently), the LFM oscillator 123 is enabled to obtain LFM delay value in advance. The LFM delay value may be stored in the register 122. In the embodiment of the invention, the LFM oscillator 123 may be enabled periodically according to a command from the memory controller 110, or the LFM oscillator 123 may be enabled aperiodically according to a command from the memory controller 110. When the memory device 120 is switched from the HFM to the LFM (i.e. the operating clock is enabled from the HFM to the LFM), the memory controller 110 will be able to directly use the LFM delay value for LFM delay tracking.

[0026] FIG. 2 is a flow chart 200 illustrating a delay tracking method according to an embodiment of the invention. The delay tracking method can be applied to the memory system 100 which supports a low-frequency-mode (LFM) and a high-frequency-mode (HFM), i.e. an operating clock of the memory system 100 may be in the LFM or HFM. As shown in FIG. 2, in step S210, a command is transmitted from a memory controller of the memory system 100 to a memory device of the memory system 100. In step S220, when the operating clock is in the HFM, an LFM oscillator of the memory device of the memory system 100 is selected for obtaining a LFM delay according to the command. In step S230, when the operating clock is in the LFM, an HFM oscillator of the memory device of the memory system 100 is selected for obtaining a HFM delay according to the command.

[0027] In some embodiments, the LFM delay value is obtained before the operating clock is switched

from the HFM to the LFM. In an embodiment, the LFM delay value is obtained by periodically enabling the LFM oscillator. In another embodiment, the LFM delay value is obtained by aperiodically enabling the LFM oscillator. The LFM delay value is applied for a LFM delay tracking when the operating clock is in the LFM.

[0028] In some embodiments, the HFM delay value is obtained before the operating clock is switched from the LFM to the HFM. In an embodiment, the HFM delay value is obtained by periodically enabling the HFM oscillator. In another embodiment, the HFM delay value is obtained by aperiodically enabling the HFM oscillator. The HFM delay value is applied for a HFM delay tracking when the operating clock is in the HFM.

[0029] In some embodiments, the LFM oscillator and the HFM oscillator are selected via Multipurpose Command (MPC) command or Mode Register Operand (MR OP).

[0030] In the tracking method of the invention, the memory device can obtain the HFM delay value or LFM delay value in advance. Therefore, when the memory device is switched from the LFM to the HFM, or switch from the HFM to the LFM, the memory device may not need to enable the HFM oscillator or LFM oscillator to obtain the HFM delay value or LFM delay value. The memory device can directly use the memory device HFM delay value or LFM delay value obtained in advance for delay tracking. Accordingly, in tracking method of the invention, the memory device can be operated more efficiently when the memory device is switched from the LFM to the HFM, or switch from the HFM to the LFM.

[0031] The steps of the method described in connection with the aspects disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module (e.g., including executable instructions and related data) and other data may reside in a data memory such as RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer-readable storage medium known in the art. A sample storage medium may be coupled to a machine such as, for example, a computer/processor (which may be referred to herein, for convenience, as a "processor") such that the processor can read information (e.g., code) from and write information to the storage medium. A sample storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in user equipment. In the alternative, the processor and the storage medium may reside as discrete components in user equipment. Moreover, in some aspects, any suitable computer-program product may comprise a computer-readable medium comprising codes relating to one or more of the aspects of the disclosure. In some aspects, a computer software product may comprise packaging materials.

[0032] It should be noted that although not explicitly specified, one or more steps of the methods described herein can include a step for storing, displaying and/or outputting as required for a particular application. In other words, any data, records, fields, and/or intermediate results discussed in the methods can be stored, displayed, and/or output to another device as required for a particular application. While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention can be devised without departing from the basic scope thereof. Various embodiments presented herein, or portions thereof, can be combined to create further embodiments. The above description is of the best-contemplated mode of carrying out the invention. This description is made for the purpose of illustrating the general principles of the invention and should not be taken in a limiting sense. The scope of the invention is best determined by reference to the appended claims.

[0033] The above paragraphs describe many aspects. Obviously, the teaching of the invention can be

accomplished by many methods, and any specific configurations or functions in the disclosed embodiments only present a representative condition. Those who are skilled in this technology will understand that all of the disclosed aspects in the invention can be applied independently or be incorporated.

5 [0034] While the invention has been described by way of example and in terms of preferred embodiment, it should be understood that the invention is not limited thereto. Those who are skilled in this technology can still make various alterations and modifications without departing from the scope and spirit of this invention. Therefore, the scope of the present invention shall be defined and protected by the following claims and their equivalents.

CLAIMS

1. A delay tracking method, applied to a memory system supporting a low-frequency-mode (LFM) and a high-frequency-mode (HFM) of an operating clock, comprising:

selecting a LFM oscillator for obtaining a LFM delay value when the operating clock is in the HFM; and
selecting a HFM oscillator for obtaining a HFM delay value when the operating clock is in the LFM.

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2. The delay tracking method of claim 1, wherein the LFM delay value is obtained before the operating clock is switched from the HFM to the LFM.

3. The delay tracking method of claim 2, wherein the LFM delay value is obtained by periodically enabling the LFM oscillator.

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4. The delay tracking method of claim 2, wherein the LFM delay value is obtained by aperiodically enabling the LFM oscillator.

5. The delay tracking method of claim 2, wherein the LFM delay value is applied for a LFM delay tracking when the operating clock is in the LFM.

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6. The delay tracking method of claim 1, wherein the HFM delay value is obtained before the operating clock is switched from the LFM to the HFM.

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7. The delay tracking method of claim 6, wherein the HFM delay value is obtained by periodically enabling the HFM oscillator.

8. The delay tracking method of claim 6, wherein the HFM delay value is obtained by aperiodically enabling the HFM oscillator.

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9. The delay tracking method of claim 6, wherein the HFM delay value is applied for a HFM delay tracking when the operating clock is in the HFM.

10. The delay tracking method of claim 1, wherein the LFM oscillator and the HFM oscillator are selected via Multipurpose Command (MPC) command or Mode Register Operand (MR OP).

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11. A memory system supporting a low-frequency-mode (LFM) and a high-frequency-mode (HFM) of an operating clock, comprising:

a memory controller, generating a command; and

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a memory device, comprising:

a LFM oscillator; and

a HFM oscillator,

wherein the memory device receives the command from the memory controller to select the LFM

oscillator or the HFM oscillator,

wherein the LFM oscillator is selected for obtaining a LFM delay value, when the operating clock is in the HFM, and

5 wherein the HFM oscillator is selected for obtaining a HFM delay value, when the operating clock is in the LFM.

12. The memory system of claim 11, wherein the LFM delay value is obtained before the operating clock is switched from the HFM to the LFM.

10 13. The memory system of claim 12, wherein the LFM delay value is obtained by periodically enabling the LFM oscillator.

14. The memory system of claim 12, wherein the LFM delay value is obtained by aperiodically enabling the LFM oscillator.

15 15. The memory system of claim 12, wherein the LFM delay value is applied for a LFM delay tracking when the operating clock is in the LFM.

20 16. The memory system of claim 11, wherein the HFM delay value is obtained before the operating clock is switched from the LFM to the HFM.

17. The memory system of claim 16, wherein the HFM delay value is obtained by periodically enabling the HFM oscillator.

25 18. The memory system of claim 16, wherein the HFM delay value is obtained by aperiodically enabling the HFM oscillator.

19. The memory system of claim 16, wherein the HFM delay value is applied for a HFM delay tracking when the operating clock is in the HFM.

30 20. The memory system of claim 11, wherein the LFM oscillator and the HFM oscillator are selected via Multipurpose Command (MPC) command or Mode Register Operand (MR OP).

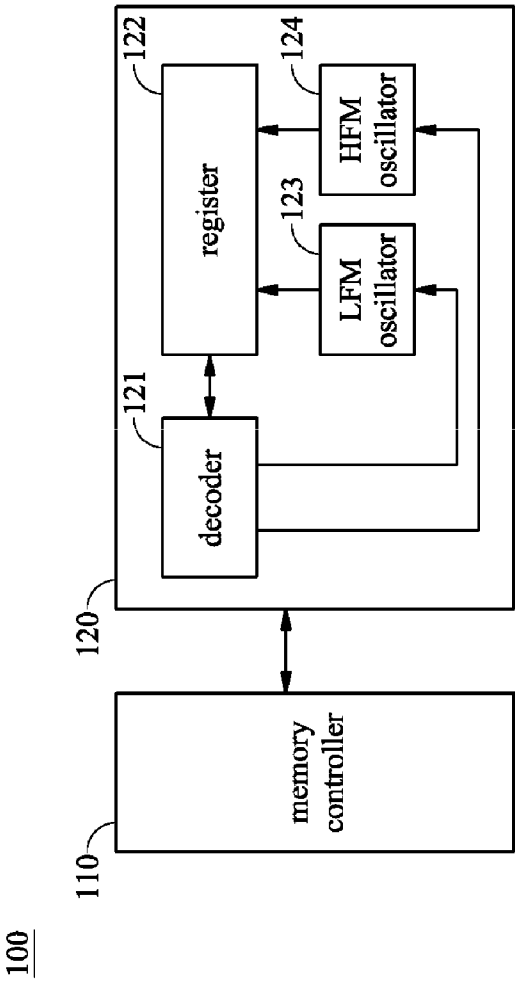


FIG. 1

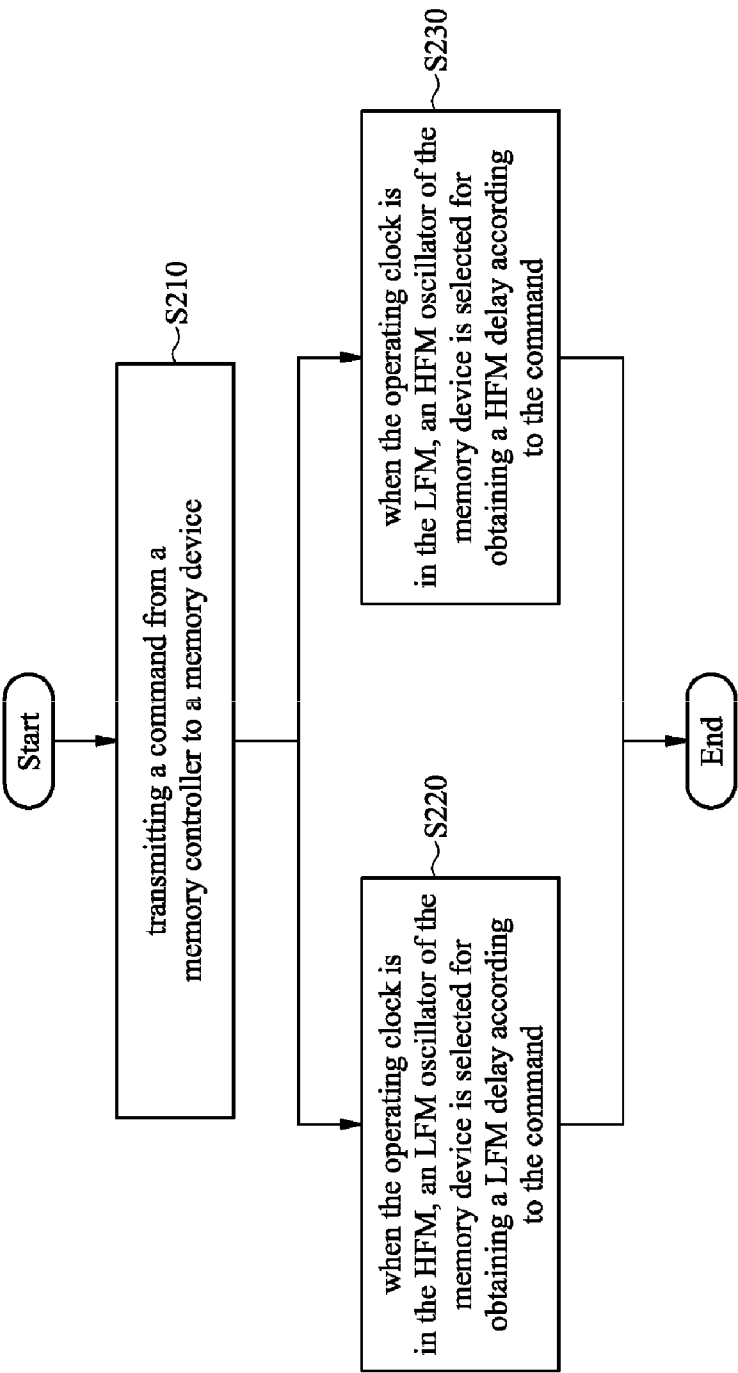


FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/100543

A. CLASSIFICATION OF SUBJECT MATTER

G11C 7/22(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C; G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT; CNKI; EPODOC; WPI; IEEE; DDR, LPDDR5, DRAM, SRAM, LFM, HFM, memory, low frequency, high frequency, mode, delay, latency, track, switch, oscillator, controller, command

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014013138 A1 (KABUSHIKI KAISHA TOSHIBA) 09 January 2014 (2014-01-09) description paragraphs [0029]-[0039], figure 3	1-20
A	US 9018980 B1 (XILINX INC.) 28 April 2015 (2015-04-28) the whole document	1-20
A	CN 107924693 A (INTEL CORPORATION) 17 April 2018 (2018-04-17) the whole document	1-20
A	US 9811273 B1 (CADENCE DESIGN SYSTEMS INC.) 07 November 2017 (2017-11-07) the whole document	1-20
A	US 2004022118 A1 (KIM ET AL.) 05 February 2004 (2004-02-05) the whole document	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

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“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

30 October 2019

Date of mailing of the international search report

12 November 2019

Name and mailing address of the ISA/CN

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Facsimile No. (86-10)62019451

Telephone No. 86-10-53961566

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/100543

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US	9018980	B1	28 April 2015	None			
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