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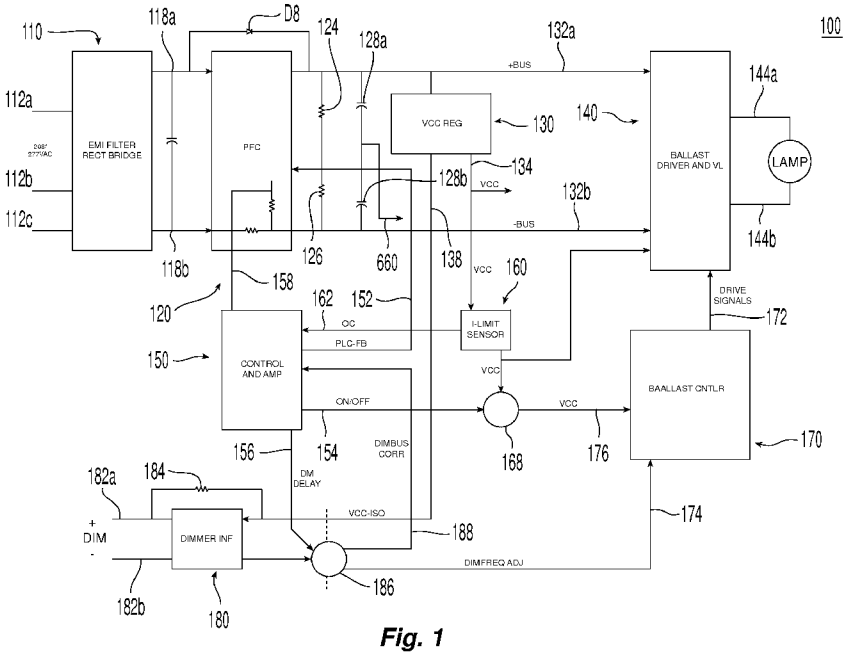

Fig. 1

(57) Abstract: An electronic ballast circuit includes a power factor correction circuit, a control and amplifier circuit, a ballast controller circuit and a ballast driver circuit. The ballast driver circuit includes a resonant circuit that connects to a lamp and a strike voltage limiter circuit that regulates the behavior of the resonant circuit. An overcurrent sensor circuit may be included to indirectly the control the ballast controller circuit via the control and amplifier circuit. The strike voltage limiter circuit uses varistors to change the resonant frequency of the resonant circuit to limit the voltage to the lamp.

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ELECTRONIC BALLAST CIRCUIT FOR LAMPS

RELATED APPLICATIONS

This application claims priority to U.S. Provisional Patent Application No. 61/257,194, filed November 2, 2009, the contents of which are incorporated by reference in their entirety.

BACKGROUND

This invention pertains to ballast circuits for lamps, such as high-intensity discharge lamps and fluorescent lamps. More particularly, this invention pertains to circuits for power limit characterization, current limiting, and voltage limiting for lamps driven by a ballast circuit.

SUMMARY OF THE INVENTION

In one aspect, the invention is directed to an electronic ballast circuit for limiting lamp strike voltage, comprising a ballast driver circuit which includes a resonant circuit having a first resonant frequency configured to drive a lamp, and a voltage limiter circuit connected to said resonant circuit.

The first resonant frequency may change to a second resonant frequency when a lamp voltage exceeds a threshold voltage, whereby said lamp voltage is clamped to said threshold voltage.

The resonant circuit may further comprise a first inductor connected in series with a run capacitor and a strike capacitor, with the lamp connected across the strike capacitor, and the voltage limiter circuit is connected across the run capacitor.

The voltage limiter circuit may comprise: a first varistor, a strike voltage charge high side capacitor and a first diode connected in series between a high side of the run capacitor and a common voltage; a second varistor, a strike voltage charge low side capacitor and a second diode connected in series between a low side of the run capacitor and said common voltage, wherein the first diode is arranged to conduct in a first direction and the second diode is arranged to conduct in a direction opposite to the first direction.

The voltage limiter circuit may further comprise a third varistor bridging a first point located between the strike voltage charge high side capacitor and the first diode and a second point located between the strike voltage charge low side capacitor and the second diode.

The common voltage may be derived from a voltage divider formed by first and second capacitors connected across a pair of bus lines.

The ballast driver circuit is devoid of a resistor configured for detecting current conditions therein to mitigate power consumption and generation of heat.

In another aspect, the invention is directed to an electronic ballast circuit comprising:

a ballast controller circuit configured to output at least one drive signal;

a power factor correction circuit outputting a current sense signal reflective of a voltage;

a control and amplifier circuit configured to receive said current sense signal, provide a power correction feedback signal to the power factor correction circuit, and provide one or more output signals to control the ballast controller circuit;

a ballast driver circuit configured to receive said at least one drive signal from the ballast controller circuit, the ballast driver circuit comprising:

a resonant circuit that connectable to a lamp; and

a voltage limiter circuit configured to regulate behavior of the resonant circuit; and

an overcurrent sensor circuit configured to output a signal to the control and amplifier circuit to thereby indirectly control the ballast controller circuit via the control and amplifier circuit.

In yet another aspect, the invention is directed to an electronic ballast circuit which includes a power factor correction circuit, a control and amplifier circuit, a ballast controller circuit and a ballast driver circuit. The ballast driver circuit includes a resonant circuit that connects to a lamp and a voltage limiter circuit that regulates the behavior of the resonant circuit. An overcurrent sensor circuit may be included to indirectly the control the ballast controller circuit via the control and amplifier circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned features of the invention will become more clearly understood from the following detailed description of the invention read together with the drawings in which:

Fig. 1 is a block diagram of an electronic ballast in accordance with one embodiment of the present invention.

Fig. 2 is a block diagram of one embodiment of power factor correction circuitry for use in the ballast of Fig. 1.

Fig. 3 is a block diagram of one embodiment of controller and amplifier circuitry for use in the ballast of Fig. 1.

Fig. 4 is a block diagram of one embodiment of dimmer interface and support circuitry for use in the embodiment of Fig. 1.

Fig. 5 is a block diagram of one embodiment of ballast controller and ballast driver circuitry in the embodiment of Fig. 1.

Fig. 6 is a block diagram of one embodiment of ballast driver and voltage limiter circuitry for use in the embodiment of Fig. 1.

Fig. 7 is one embodiment of a schematic for an electronic ballast of Fig. 1 showing EMI filtering and rectifier circuitry

Fig. 8 is one embodiment of a schematic for an electronic ballast of Fig. 1 showing power factor correction circuitry.

Fig. 9 is one embodiment of a schematic for an electronic ballast of Fig. 1 showing control and amplification circuitry.

Fig. 10 is one embodiment of a schematic for an electronic ballast of Fig. 1 showing voltage regulator circuitry.

Fig. 11 is one embodiment of a schematic for an electronic ballast of Fig. 1 showing ballast controller and ballast driver circuitry.

Fig. 12 is one embodiment of a schematic for an electronic ballast of Fig. 1 showing the dimmer circuit and current limiter circuitry.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 shows a block diagram of one embodiment of an electronic ballast 100 in

accordance with one embodiment of the present invention. The ballast 100 is configured to drive a lamp 602, for example, a high-intensity discharge (HID) lamp, such as the M132/M154, which has a rating of 320 watts with a voltage rating of 135 volts. Such a lamp 602 is suitable for lighting large areas, such as parking lots or warehouses. The ballast 100 for such a lamp 602 is connected to a power source of 208 Vac, 240 Vac, or 277Vac. The ballast 100 provides a strike voltage of 3 to 4KV peak and operates at a frequency of approximately 100KHz. Those skilled in the art will recognize that these values will vary with the lamp manufacturer's specifications and recommendations without departing from the spirit and scope of the present invention.

The ballast 100 includes an EMI filter and rectifier bridge ("power supply") circuit 110, a power factor controller circuit 120, a VCC regulator circuit 130, a ballast driver circuit 140, a control and amplifier circuit 150, an overcurrent sensor circuit 160, a ballast controller circuit 170 and a dimmer circuit 180. Additional components and functionalities are also present in the circuit 100.

The ballast 100 regulates the current flowing through a load, such as a lamp 120. The ballast 100 is an electronic ballast that, in one embodiment, simulates the voltage versus wattage curve of a reactor ballast. The ballast 100 has features that limit lamp strike current and voltage.

The EMI filter and rectifier bridge circuit 110 serves as a power supply 110 which provides power to the circuitry of the ballast 100 and the lamp 602. The power supply 110 accepts first and second power inlets 112a, 112b and also has a ground input 114. The power supply 110 outputs a filtered, rectified sinewave onto power lines 118a, 118b. The EMI filter and rectifier bridge circuit 110 connects downstream, via power lines 118a, 118b, to the power factor controller (PFC) circuit 120 via PFC input capacitor 116 connected across the power lines 118a, 118b.

The PFC circuit 120 receives a power correction feedback signal 152 from the control and amplifier circuit 150. The PFC circuit 120 adjusts the voltage of +Main bus 132a in response to the power correction feedback signal 152. The PFC circuit 120 outputs a current sense signal 158 which is used by other components in the ballast circuit 100. The generation and implementation of signals 152, 158 is described in detail further below. The PFC circuit 120 aims to keep the power factor as close to 100% as possible in order to

provide as high a real load to the power source 110 as possible, in order to satisfy IEC61000-3-2 requirements, and to improve efficiency. It is common for reactive ballasts to have a low power factor. The PFC circuit 120 is provided with a power limit characterization capability that allows the ballast 100 to approximate the voltage versus wattage characteristics of a reactive ballast. Downstream of the PFC circuit 120 is the ballast controller circuit 170, which is the circuit that provides the bias signal to the ballast driver circuit 140.

The ballast driver circuit 140 provides the power at an appropriate frequency to a resonant circuit 620, which drives the lamp 602. Associated with the ballast driver circuit 140 is a lamp strike voltage limiter (VL) circuit 610 that limits the strike voltage applied to the lamp 602 via lamp power leads 144a, 144b, thereby aiding to increase lamp longevity.

The VCC regulator circuitry 130 receives power from the +Main bus 132a and outputs a first voltage on the VCC bus 134 which is connected to various other components. The VCC regulator circuitry 130 also includes an isolation transformer T100 from which it outputs an isolated power signal VCC-ISO 138. The Vcc bus 134 is powered by the main bus 132a, 132b. The bus filter capacitors 128a, 128b are connected across the main bus. Therefore, the voltage of the main bus 132a, 132b corresponds to the voltage of the bus filter capacitors 128a, 128b. In this way the current to the lamp 602 is interrupted when the voltage of the bus filter capacitors 128a, 128b falls below a threshold value. In addition, there is a minimum drive voltage required to sustain the lamp 602 just by the nature of the lamp's physics. The voltage regulator circuit 130 is capable of producing Vcc voltage from the main bus 132a, 132b at below the lamp's sustain level. The voltage regulator circuit 130 can be thought of as the 'last-circuit-standing.' The lag in the Vcc shutdown is to accommodate power line interruptions, with an attempt to 'carry-thru' the temporary outage. In one embodiment, the voltage regulator circuit 130 carries the lamp 602 thru 8 cycles of 60Hz, but must retain the control status for recovery via the Vcc voltage that is applied to the control circuitry, if in the case the lamp 602 has not gone out. The voltage regulator circuit 130 has a different situation on power-up of the ballast. The voltage regulator circuit 130 has an MOV (not shown) in Fig. 1 that is connected its start-up bias pinto prevent the voltage regulator circuit 130 from starting at power line voltage levels less than a minimum value, for example, 190VAC, as a protection feature.

Associated with the ballast controller circuit 170 is a lamp strike overcurrent sensor circuit 160 that senses the back current and, as appropriate, resets the strike sequence to increase performance by providing more accurate control of current. The overcurrent sensor circuit 160 is connected to the voltage VCC bus 134 and also to the Voltage VCC-ballast driver which is supplied to the ballast driver circuit 140. If the overcurrent sensor circuit 160 senses that one or more voltages are outside of predetermined values, it output an overcurrent signal 162 to the control and amplifier circuit 150.

The control and amplifier circuit 150 receives the overcurrent signal 162 from the overcurrent sensor circuit 160, a dimmer bus correction signal 188 from a dimmer time delay switch 186, and PFC current sense signal 158 from the power factor controller circuit 120 and. In response, the control and amplifier circuit 150 outputs a power correction feedback signal 152 to the power factor controller circuit 120, a dimmer delay control signal back to the dimmer time delay switch 186, and a ballast controller on/off signal 154 to a ballast on-off switch 168 which controls voltage VCC-ballast controller 176 supplied to the ballast controller circuit 170.

The dimmer circuit 180 receives dimmer voltage signals 182a, 182b and outputs information which is used by circuitry, shown generally as a dimmer time delay switch 186, to produce a dimmer bus correction feedback signal 188 to the control and amplifier circuit 150 and a dimmer frequency adjustment signal 174 to the ballast controller circuit 170.

The ballast on/off switch 168 receives the ballast controller on/off signal 154 from the control and amplifier circuit 150. The ballast on/off switch 168 is configured to selectively connects voltage VCC bus 134 to the ballast controller circuit 170 depending on the ballast controller on/off signal 154, as discussed in detail below.

Fig. 2 shows one embodiment 200 of the PFC circuit 120. A PFC integrated circuit chip ("PFC IC") 210 such as the NCP1650, available from ON semiconductor, forms the nucleus of the PFC circuit 120. The peak power handling requirement of the power factor correction circuit 120 is reduced by the bypass rectifier D8 to provide power-up charging of the bus bulk capacitors 128a, 128b. With the bypass rectifier 420 providing a bypass during startup, the power factor correction circuit 120 does not have to provide the boosted voltage required by the ballast driver circuit 140. The power factor correction circuit 120 is able to operate efficiently over a load range from approximately 50%, e.g., when full dimmed, to

full power when it is not required to contend with the full initial startup current.

The high power line 118a connects, via a PFC bypass line 122 which includes an inductor L1 and a boost rectifier diode D2, to form the +Main Bus 132a for the circuit 100. The low power line 118b connects directly to the PFC IC current sense Is pin 226. Meanwhile, the –Main Bus 132b is connected to the ground pin GND of the PFC IC.

A PFC current sense resistor 206 is shunted between the Iavg pin and the ground pin GND of the PFC IC. The voltage across the PFC current sense resistor 206 is used by the PFC 210 and contributes to the value the latter's Iavg pin. The PFC current sense resistor 206 has a value selected to be the least resistance able to function in the circuit, allow the least efficiency loss from resistance heating, and be an economical implementation. At its Iavg pin, the PFC IC 210 outputs a PFC current sense signal 158 which is provided on other components, as discussed farther below. A PFC Iavg resistor 208 is connected on one side to the Iavg pin of the PFC IC and on the other side to ground (-Main bus 132b). The Iavg pin has a voltage level that varies with respect to an amplifier gain of the PFC IC 210.

Connected between the +Main bus 132a and –Main bus 132s are a high side first bus divider resistor 124 and a low side second bus divider resistor 126, which together form a voltage divider. A power correction feedback signal 152, whose generation is described further below, is input to a node between the two bus divider resistors 124, 126, which node is connected to the feedback/shutdown (FB_SD) pin 125 of the PFC IC 210.

Fig. 3 shows one embodiment 300 of the control and amplifier circuit 150. As seen in both Figs. 1 and 3, the control and amplifier circuit 150 receives the PFC current sense signal 158, a dimmer bus correction feedback signal 188, and an over-current feedback signal 162. The control and amplifier circuit 150 outputs the aforementioned power correction feedback signal 152 which is input to the PFC IC 210, a ballast controller on/off signal 154, and a dimmer delay control signal 156.

The control and amplifier circuit 150 includes a run comparator 310 implemented as an amplifier and configured to determine whether the lamp 602 has been struck and is in a sustained running condition. The run comparator 310 receives a first input from the PFC current sense signal 158 and a second input constituting a run comparator reference signal 314. The run comparator reference signal 314 is a threshold set at a level that is above the warm-up power level and below the run level for the lamp 602. In response to these two

inputs, the run comparator 310 outputs a run status signal 319.

The run status signal 319 is applied to dimmer delay timer circuitry 350 which outputs the dimmer delay control signal 156. The run status signal 319 is also applied to a strike oscillator 340 which is implemented using an amplifier and outputs a strike signal 342. The run status signal 319 and the strike signal 342, along with the over-current feedback signal 162, are all applied to ballast enable logic circuitry 360. In response, the ballast enable logic circuitry 360 outputs a ballast on/off signal 154 which is applied to the ballast on/off switch 168 to ultimately control the ballast controller circuitry 170.

The control and amplifier circuit 150 also includes power limit characterization (PLC) circuitry which ultimately outputs the power correction feedback signal 152. The PLC circuitry includes a PLC first amplifier 320, a PLC first amplifier integrator 322, a PLC second amplifier 330 and a PLC second amplifier limiter 332. The PLC first amplifier 320 receives a first input comprising the PFC current sense signal 158 and a second input comprising the dimmer bus correction feedback signal 188.

The output of the PLC first amplifier is then integrated by the PLC first amplifier integrator 322. The integrator circuit 322 has an integration time constant that accounts for the warm-up period of the lamp 602. During warm-up, the lamp 602 is less susceptible to bus voltage variations than during normal operation because of the various circuit impedances and the nature of the lamp 602. The output of the PLC first amplifier integrator 322 is then presented as a first input to the PLC second amplifier 330, while the dimmer bus correction feedback signal 188 is presented as the second input thereto. The output of the PLC second amplifier 330 is then thresholded by the PLC second amplifier limiter 332. The output of the PLC second amplifier limiter 332 then provided as the power correction feedback signal 152.

Fig. 4 shows one embodiment 400 of the combination of the dimmer interface and support circuit 180 in combination with the dimmer time delay switch 186. The combination 400 includes a dimmer converter voltage regulator 420, a voltage-to-duty-cycle converter 410, a pair of opto-isolators 440, 450 and an opto-isolator enable inverter circuit 460 comprising first and second enabling transistors Q105, Q106, respectively. The dimmer interface and support circuitry 180 also includes limit circuitry 470, 480 and integrator circuitry 472, 482, discussed below. Collectively, the first and second enabling transistors

Q105, Q106, the limit circuitry 470, 480 and the integrator circuitry 472, 482 functions as the item seen in Fig. 1 as the dimmer time delay switch 186.

The dimmer converter voltage regulator 420 receives the VCC-ISO power signal 138 and outputs high and low dimmer converter VCC signals 420a, 420b in response thereto. The voltage-to-duty-cycle converter 410 receives high and low (ground) dimmer input signals 182a, 182b respectively, which generally range from 0 - 10 volts. A dimmer shunt resistor 184 is coupled between the high dimmer input signal 182a and the high converter VCC signal 420a to pull up the high dimmer input, when no dimmer signal is present.

The voltage-to-duty-cycle converter 410 is implemented using a pair of Norton-type operational amplifiers provided in a single package, such as an LM2904. A first operational amplifier is operated in "free-run" mode to create a sawtooth waveform from 0 – 10 volts. The second operational amplifier is configured as a comparator. The output of the first operational amplifier is presented as a first input to the second operational amplifier. The second input to the second operational amplifier is the high input dimmer signal 182a. The second operational amplifier thus compares the instantaneous values of the sawtooth waveform output by the first comparator and the high input dimmer signal 182a, and outputs dimmer converter output signals 414a, 414b in response thereto.

The two opto-isolators 440, 450 may be implemented as a single package, such as a 4N35. The internal diodes of the two opto-isolators 440, 450 are connected in series, with the cathode of the first opto-isolator 440 connected to the anode of the second opto-isolator 450. This is done to make sure that the two opto-isolators 440, 450 are driven by the same signal. Thus, as seen in Fig. 4, the dimmer converter output signal 414a is presented to the anode of first the first opto-isolator 440 while dimmer converter output signal 414b is presented to the cathode of the second opto-isolator 450.

The enabling transistors Q105 and Q106 are both configured to be simultaneously activated by the dimmer delay control signal 156. When simultaneously activated by the dimmer delay control signal 156, the transistors Q105, Q106, via respective base enable leads 454, 444, enable the outputs of the opto-isolators 440, 450, respectively.

The output 442 of the first opto-isolator 440 is fed to a dimmer frequency adjust level limiter 470 whose output is supplied to a dimmer frequency adjust integrator 472. The dimmer frequency adjust integrator 472 integrates the output 442 of the first opto-isolator

440 to produce the dimmer frequency adjustment signal 174.

The output 452 of the second opto-isolator 440 is fed to a dimmer bus correction level limiter 480 whose output is supplied to a dimmer bus correction integrator 482. The dimmer bus correction integrator 482 integrates the output 452 of the second opto-isolator 450 to produce the dimmer bus correction signal 188.

An external circuit isolation barrier 490 is provided to enhance electrical isolation among some of the components of the embodiment 400 of the dimmer interface and support circuitry 18

Fig. 5 shows one embodiment 500 of the combined circuitry of the overcurrent sensor circuit 160, the ballast driver circuit 140, the ballast controller circuit 170 and a ballast on/off switch circuit 168.

The ballast controller circuit 170 comprises a ballast controller integrated circuit 520 (ballast controller IC 520), which may be implemented as the FAN7544, which is known to those skilled in the art.

One input to the ballast controller IC 520 is the dimmer frequency adjustment signal 174 created by the dimmer interface circuit. Dimmer frequency adjustment signal 174 is connected to the RT pin of the ballast controller IC 520. The parameter pins, shown generally as 511, are connected to set up the ballast IC 520. These parameter pins may be connected to a ballast controller setup sweep TC capacitor 512, a ballast controller setup sweep TC resistor 514 (pin RPH), a ballast controller setup run frequency capacitor 516, and a ballast controller setup run frequency resistor 518 (pin RT).

A second input to the ballast controller IC 520 is the supply voltage VCC, which is selectively provided to the VCC pin of the ballast controller IC 520 to provide voltage VCC-ballast controller 176. Voltage VCC-ballast controller 176 is controlled by the ballast on/off switch 168. Ballast on/off switch 168 is implemented as a ballast controller switching transistor Q103. The emitter lead 546 of transistor Q103 is connected to the voltage VCC-ballast driver 164. Voltage VCC-ballast controller 176 is connected to Q103's collector lead via collector resistor R109. On its base side, Q103 is connected to voltage VCC-ballast driver 164 via the high-side ballast controller Vcc switch divider resistor 545. The ballast controller on/off signal 154 is input to the Q103 base via the low-side ballast controller Vcc switch divider resistor 548. Thus, the on/off ballast control signal 154 output by

the controller and amplifier circuit 150 can control the operation of the ballast controller IC 520, by disconnecting VCC to the ballast controller.

The overcurrent sensor circuit 160 includes an overcurrent sense transistor Q110 has its base connected to the VCC bus 134 via Vcc base line 539. The emitter of overcurrent sense transistor Q110 is connected via sense current limit resistor 536 to the voltage VCC-ballast driver 164 while a sense compensation capacitor 538 is connected between the emitter and the Vcc base line 539. Interposed between the VCC bus 134 and the voltage VCC-ballast driver 164 are a sense diode 532 connected in series with sense resistor 534. The collector of the transistor Q110 is connected to ground via an integration circuit comprising a sense integrator resistor 535 connected in series with a sense integrator capacitor C129. The capacitor signal 537, which is derived from the impact of the voltages at VCC buses 134, 164, is integrated by sense integrator resistor 535 and sense integrator capacitor C129. The voltage level across the sense integrator capacitor C129 is output ass the overcurrent signal 162, which is supplied to the control and amplifier circuit 150 whose embodiment 300 is described above with reference to Fig. 3.

The overcurrent sensor circuit 160 resets the strike sequence when the voltage of the bus filter capacitors 128a, 128b falls below a threshold value. The bus filter capacitors 128a, 128b are connected to the bus supplying power to the driver circuit 140 for the lamp 602. During lamp strike, the bus filter capacitors 128a, 128b provide the additional power required to start the lamp 602. If the lamp 602 fails to start, the bus filter capacitors 128a, 128b are depleted, with a corresponding drop in bus voltage below a threshold value. The threshold value of the voltage of the bus filter capacitors/bus is a voltage level that indicates that the lamp strike was unsuccessful. Another feature of the overcurrent sensor circuit 160 is circuit protection in case of power supply and/or bus filter capacitors failures that result in loss of normal voltage level.

The ballast controller IC 520 output drive signals 172 are sent to the ballast driver IC 580 belonging to the ballast driver circuit 140. As discussed below with reference to Fig. 6, the ballast driver circuit 140 receives these drive signals 172 to operate the lamp 602 via lamp power leads 144a, 144b.

Fig. 6 illustrates circuitry 600 including the ballast driver and voltage limiter circuit 140 for driving the lamp 602. The ballast driver integrated circuit 580 is provided with

power from voltage VCC-ballast driver 164 and is also connected to the -Main Bus 132b. In addition, as discussed above, the ballast driver integrated circuit receives driver signals 172 from the ballast controller circuit, and more particularly from the ballast controller chip 520. The ballast driver integrated circuit 580 has outputs connected to the gates of power transistors Q100 and Q101. Transistor Q100 is connected to power at +Main Bus 132a while transistor Q101 is connected to power at –Main Bus 132b. The outputs of power transistors Q100 and Q101 are tied together to form a resonant circuit driver signal 650. Meanwhile, a resonant circuit return signal (Cbus) 660 is formed at a node between bus filter capacitors 128a, 128b (see Fig. 1).

As seen in Fig. 6, the ballast driver and voltage limiter circuit 140 includes a resonant circuit 620 and a strike voltage limiter circuit 610. During lamp strike, a high voltage is developed across the lamp 602. It is desirable to limit the lamp strike voltage to ensure lamp longevity.

The resonant circuit 620 is configured as an LC circuit interposed between the ballast driver 580 and the lamp 602. The resonant circuit 620 has a resonant frequency equal to the frequency of the ballast driver 580. By matching the frequency of the ballast driver 580 to the resonant frequency of the resonant circuit 602, maximum power is transferred to the lamp 602. The resonant circuit 620 comprises an LC circuit inductor 622, an LC circuit run capacitor 624 and an LC circuit strike capacitor 626. The LC circuit strike capacitor 626 is in electrical parallel with the lamp 602.

The strike voltage limiter circuit 610 has a warmup/run voltage standoff high side varistor 612a (“first varistor 612a”), a strike voltage charge high side capacitor 614a (“first capacitor 614a”), a strike voltage limiter varistor 618 (“bridging varistor 618”), a strike voltage charge low side capacitor 612a (“second capacitor 612a”), and a warmup/run voltage standoff low side varistor 612b (“second varistor 612b”), connected across the LC circuit run capacitor 624.

As is known to those skilled in the art, a varistor has high resistance below a threshold voltage. When the voltage across the varistor exceeds the threshold, the varistor becomes conductive. To accommodate high voltages, multiple varistors may be connected in series. In some embodiments of the present invention, metal oxide varistors (MOV) may be used.

The connection of the bridging varistor 906 to each capacitor 614a, 614b also provides a connection for a corresponding diode 616a, 616b. The diodes 616a, 616b allow the capacitors 614a, 614b to be charged to a dc potential. Varistors 612a, 612b provide a voltage threshold sufficient to prevent the strike voltage limiter 620 from interfering with normal lamp running drive levels. When the cumulative potential across the capacitors 614a, 614b reaches the voltage limit of the bridging varistor 618, the bridging varistor 618 conducts, thereby limiting the lamp strike voltage to the voltage equal to the cumulative voltage ratings of the first and second varistors 612a, 612b and the bridging varistor 618. The peak of the voltage waveform overcomes the bridging varistor 618 to provide current flow across LC circuit run capacitor 624. This current prevents the continuing increase in resonant voltage development without increasing the drive current. Thus, it indirectly limits the driver demand in current and sizing for the application and allows the use of more economical driver switch devices that have typically lesser nC for faster switching and higher efficiency.

When lamp strike occurs, the lamp strike voltage is reached before the over-current signal is generated, with the delay being a result of the hold up capacitor 128a, 128b depletion. On the other side, with the strike being created by the frequency sweep of drive through the L/C resonant frequency, a finite dwell time at peak strike voltage is created by the L/C 'Q' and rate of the sweep. The hold up capacitor on the main bus is significantly of less charge than what would be required by the full sweep, and, therefore, the over-current is the source of the strike termination. This also prevents what is known as a false start of the lamp 602. For example, high intensity discharge (HID) lamps, under extreme uncontrolled conditions, have the capability of continuing the initial starting arc. The hold up depletion method of control prevents the arc from continuing.

After the lamp 602 strikes, the resonant LC circuit strike capacitor 626 is shunted by the relatively low effective impedance of the lamp 602. As a result, using one embodiment as an example, the 180KHz resonant frequency of the resonant circuit 610 is changed to 75KHz and becomes predominantly inductive because the drive frequency is on the upper slope of the curve. As the arc in the lamp 602 turns to a plasma, the maximum required lamp current is reduced from 4A to 2.6A at typical nominal run values. Given the drive impedance, the typical lamp 602 converts within a few minutes. Accordingly, adjustments

in power and/or brightness are made at a slow rate that is barely, if at all, perceptible. Further, to avoid stability issues, the rate of adjustment is less than the PFC power gain response characteristic. For example, the PFC dynamic power gain characteristic is set at 5Hz rate to support a typical strike and lamp run.

It can be seen from the foregoing that the voltage limiter 610 limits the strike voltage applied by the ballast circuit 140 when the lamp 602 starts. The voltage limiter 610 uses varistors to switch in circuit components, e.g., capacitors, that shifts the resonant circuit parameters based on voltage levels. When a certain voltage is reached, the varistors conduct and completes a circuit connected to the resonant circuit 620. The voltage limiter 610 changes the resonant frequency of the resonant circuit 620, which causes the voltage to the lamp 602 to be clamped at a maximum value.

As seen in Fig. 6, the ballast driver circuit 140 including the resonant circuit 610 and voltage limiter circuit 6100 is devoid of a resistor configured for detecting current conditions in the circuit 140, unlike in prior art ballast circuits. The absence of such a resistor helps mitigate power consumption and generation of heat in the ballast circuit 100.

While the present invention has been described with reference to one or more specific embodiments, the description is intended to be illustrative as a whole and is not to be construed as limiting the invention to the embodiments shown. It is appreciated that various modifications may occur to those skilled in the art that, while not specifically shown herein, are nevertheless within the scope of the invention.

List of Reference Numerals

100 – Ballast Circuit
110 – EMI and Filter Bridge Circuit
112a – inlet , N1
112b - inlet, N2
114 – inlet, Safety Ground
116 - PFC input capacitor
118a - rectified sinewave (+)
118b - rectified sinewave (-)
120 – Power Factor Controller
122 –bypass line
124 – bus divider, high side
125 – feedback/shutdown pin on PFC IC
126 – bus divider, low side
128a - bus filter capacitor high
128b - bus filter capacitor low
130 – Voltage Regulator Circuit
132a - +Main bus
132b – -Main bus
134 – Vcc bus
138 -- Vcc-Iso
140 – Ballast Driver Circuit
144a – Lamp Power Lead 1
144b – Lamp Power Lead 2
150 – Control and Amplifier Circuit
152 -- power correction feedback signal
154 – ballast controller on/off signal
156 – Dimmer Delay Control Signal
158 – PFC Current Sense signal (from Iavg pin of PFC IC)
160 – overcurrent sensor circuit

162 – over-current feedback signal
164 – Voltage VCC-ballast driver
168 -- ballast on-off switch
170 – Ballast Controller Circuit
172 – Drive Signals
174 – dimmer frequency adjustment signal
176 – Voltage VCC-ballast controller
180 – Dimmer Circuit
182a -- Dim input (+)
182b -- Dim input (-)
184 – dimmer Shunt Resistor
186 -- dimmer time delay switch
188 – dimmer bus correction feedback signal
200 -- Power Factor Controller Circuit
206 -- PFC current sense resistor
208 -- PFC Iavg resistor
210 – NCP1650 (ON Semiconductor)
300 – Controller and Amplifier Circuit
310 – Run comparator
314 -- Run comparator reference
319 -- Run status signal
320 – PLC Amp 1
322 – PLC Amp 1 Integrator
330 -- PLC Amp 2
332 -- PLC Amp 2 limiter
340 -- Strike Oscillator
342 -- Strike signal
350 -- Dim Delay Timer
360 -- Ballast Enable logic
400 – Dimmer Interface and Support Circuit
410 -- Voltage to Duty Cycle converter

414a,b -- Dim converter out

420 -- Dim converter Vcc regulator

420a -- Dim converter Vcc+

420b -- Dim converter Vcc-

430 -- T100 transformer

440 -- Opto isolator U104

442 -- Opto isolator U104 out

444 -- Opto isolator U104 enable

450 -- Opto isolator U105

452 -- Opto isolator U105 out

454 -- Opto isolator U105 enable

460 -- Opto isolator enable inverters

Q105 – first transistor enable inverter

Q106 – second transistor enable inverter

470 -- Dimmer frequency adjust level limiter

472 -- Dimmer frequency adjust integrator

480 -- Dimmer bus correction level limiter

482 -- Dimmer bus correction integrator

490 -- isolation barrier

500 -- Ballast Controller and Driver Circuit

511 -- ballast controller parameter pins

512 -- ballast controller setup sweep TC capacitor

514 -- ballast controller setup sweep TC resistor

516 -- ballast controller setup run frequency capacitor

518 -- ballast controller setup run frequency resistor A

520 -- ballast control IC

Q110 -- OC sense transistor

532 -- OC sense diode D116

C129 -- OC sense integrator capacitor

534 -- OC sense resistor R139

535 – OC sense integrator resistor

536 – OC sense current limit resistor

537 -- OC sense signal

538 – OC sense compensation capacitor

539 – Vcc line into sense transistor

Q103 -- Ballast controller Vcc switch transistor

545 -- high-side ballast controller Vcc switch divider resistor

546 -- Emitter lead of ballast controller transistor switch

R109 –Collector resistor of ballast controller transistor switch

548 -- low-side ballast controller Vcc switch divider resistor

580 – Ballast Driver IC IR2113

600 -- Ballast Driver Circuit

602 - Lamp

610 -- strike voltage limiter

612a -- warmup/run voltage standoff high side

612b --warmup/run voltage standoff low side

614a -- strike voltage charge capacitor high side

614b – strike voltage charge capacitor low side

616a -- strike rectifier diode high side

616b -- strike rectifier diode low side

618 -- strike voltage limiter MOV

620 -- resonant LC circuit

622 -- resonant LC circuit inductor

624 -- resonant LC circuit run capacitor

626 -- resonant LC circuit strike capacitor

650 – Resonant Circuit Driver Signal

660 – Resonant Circuit Return Signal (Cbus)

CLAIMS

What is claimed is:

1. An electronic ballast circuit for limiting lamp strike voltage, comprising:
a ballast driver circuit (140) comprising:
a resonant circuit (620) having a first resonant frequency and configured to drive a lamp (602); and
a voltage limiter circuit (610) connected to said resonant circuit (620).

2. The electronic ballast circuit for limiting lamp strike voltage, wherein
said first resonant frequency changes to a second resonant frequency when a lamp voltage exceeds a threshold voltage, whereby said lamp voltage is clamped to said threshold voltage.

3. The electronic ballast circuit according to claim 1, wherein:
the resonant circuit (620) comprises a first inductor (622) connected in series with a run capacitor (624) and a strike capacitor (626), with the lamp (602) connected across the strike capacitor (626); and
the voltage limiter circuit (610) is connected across the run capacitor (624).

4. The electronic ballast circuit according to claim 3, wherein the voltage limiter circuit (610) comprises:
a first varistor (612a), a strike voltage charge high side capacitor (614a) and a first diode (616a) connected in series between a high side of the run capacitor (624) and a common voltage (Cbus);
a second varistor (612b), a strike voltage charge low side capacitor (614b) and a second diode (616b) connected in series between a low side of the run capacitor (624) and said common voltage (Cbus);
wherein the first diode (616a) is arranged to conduct in a first direction and the second diode (616b) is arranged to conduct in a direction opposite to the first direction.

5. The electronic ballast circuit according to claim 4, wherein the voltage limiter circuit (610) further comprises:

a third varistor (618) bridging a first point located between the strike voltage charge high side capacitor (614a) and the first diode (616a) and a second point located between the strike voltage charge low side capacitor (614b) and the second diode (616b).

6. The electronic ballast circuit according to claim 4, wherein:

the common voltage (Cbus) is derived from a voltage divider formed by first and second capacitors (128a, 128b) connected across a pair of bus lines (132a, 132b).

7. The electronic ballast circuit according to claim 4, wherein:

the ballast driver circuit (140) devoid of a resistor configured for detecting current conditions therein to mitigate power consumption and generation of heat.

8. An electronic ballast circuit comprising:

a ballast controller circuit configured to output at least one drive signal;

a power factor correction circuit outputting a current sense signal reflective of a voltage;

a control and amplifier circuit configured to receive said current sense signal, provide a power correction feedback signal to the power factor correction circuit, and provide one or more output signals to control the ballast controller circuit;

a ballast driver circuit configured to receive said at least one drive signal from the ballast controller circuit, the ballast driver circuit comprising:

a resonant circuit that connectable to a lamp; and

a voltage limiter circuit configured to regulate behavior of the resonant circuit; and

an overcurrent sensor circuit configured to output a signal to the control and amplifier circuit to thereby indirectly control the ballast controller circuit via the control and amplifier circuit.

9. An electronic ballast circuit for limiting lamp strike voltage, comprising:

a power supply circuit (110);

a power factor controller circuit (120) connected to said power supply (110), said power factor controller circuit (120) comprising a PFC integrated chip (210) and a voltage divider.

10. The electronic ballast circuit for limiting lamp strike voltage according to claim 9, wherein said voltage divider comprises a first bus divider resistor (124) and a second bus divider resistor (126).

11. The electronic ballast circuit for limiting lamp strike voltage according to claim 10, further comprising a node disposed between said first bus divider resistor (124) and said second bus divider resistor (126).

12. The electronic ballast circuit for limiting lamp strike voltage according to claim 11, wherein said first bus divider resistor (124) is disposed between a first main bus (+Main bus 132a) and said node.

13. The electronic ballast circuit for limiting lamp strike voltage according to claim 11, wherein said second bus divider resistor (124) is disposed between a second main bus (-Main bus 132b) and said node.

14. An electronic ballast circuit for limiting lamp strike voltage, comprising:

a run comparator (310);

a strike oscillator (340) connected to said run comparator (310); and

ballast enable logic circuitry (360) connected to said run comparator (310) and said strike oscillator (340).

15. The electronic ballast circuit for limiting lamp strike voltage of claim 14, further comprising a dimmer delay timer circuitry (350) connected to said run comparator (310).

16. The electronic ballast circuit for limiting lamp strike voltage of claim 14, further comprising:

a power limit characterization (PLC) circuitry (317), said PLC circuitry (317) comprising: a PLC first amplifier 320, a PLC first amplifier integrator 322, a PLC second amplifier 330, and a PLC second amplifier limiter 332.

17. An electronic ballast circuit for limiting lamp strike voltage, comprising:

a dimmer converter voltage regulator (420);

a voltage-to-duty-cycle converter (410) connected to said dimmer converter voltage regulator (420);

a first opto-isolator (440) connected to said voltage-to-duty-cycle converter (410); and

a second opto-isolator (450) connected to said voltage-to-duty-cycle converter (410).

18. The electronic ballast circuit for limiting lamp strike voltage according to claim 17, further comprising a dimmer shunt resistor (184) disposed between said dimmer converter voltage regulator (420) and said voltage-to-duty-cycle converter (410).

19. The electronic ballast circuit for limiting lamp strike voltage according to claim 17, wherein said first opto-isolator (440) and said second opto-isolator (450) are connected in series.

20. The electronic ballast circuit for limiting lamp strike voltage according to claim 19, wherein a cathode of said first opto-isolator (440) is connected to an anode of said second opto-isolator (450).

21. The electronic ballast circuit for limiting lamp strike voltage according to claim 17, further comprising:

an opto-isolator enable inverter circuit (460) comprising a first enabling transistor (Q105) and a second enabling transistor (Q106),

wherein said first enabling transistor (Q105) is connected to said first opto-isolator

(440) and said second enabling transistor (Q106) is connected to said second opto-isolator (450).

22. The electronic ballast circuit for limiting lamp strike voltage according to claim 21, further comprising:

a dimmer frequency adjust level limiter (470) disposed between said first opto-isolator (440) and a dimmer frequency adjust integrator (472); and

a dimmer bus correction level limiter (480) disposed between said second opto-isolator (440) and a dimmer bus correction integrator (482).

23. An electronic ballast circuit for limiting lamp strike voltage, comprising:

an overcurrent sensor circuit (160);

a ballast controller integrated circuit (IC) (520) connected to said overcurrent sensor circuit (160); and

a ballast driver circuit (140) connected to said ballast controller IC (520).

24. The electronic ballast circuit for limiting lamp strike voltage according to claim 23, wherein said overcurrent sensor circuit (160) comprises an overcurrent sense transistor (Q110) connected to an integration circuit.

25. The electronic ballast circuit for limiting lamp strike voltage according to claim 24, wherein said integration circuit comprises a sense integrator resistor (535) connected in series with a sense integrator capacitor (C129).

26. The electronic ballast circuit for limiting lamp strike voltage according to claim 23, further comprising: a sense diode (532) connected in series with sense resistor (534).

27. The ballast circuit for limiting lamp strike voltage according to claim 23, wherein said ballast controller IC (520) further comprises:

a plurality of parameter pins (511) connected to ballast controller setup sweep TC capacitor (512), a ballast controller setup sweep TC resistor 514, a ballast controller setup run

frequency capacitor (516), and a ballast controller setup run frequency resistor (518).

28. The ballast circuit for limiting lamp strike voltage according to claim 23, wherein said ballast controller IC (520) further comprises:

a ballast controller switching transistor (Q103) comprising an emitter lead (546), wherein said ballast controller switching transistor (Q103) is connected to a collector resistor (R109), a ballast controller Vcc switch divider resistor (545), and a ballast controller Vcc switch divider resistor (548).

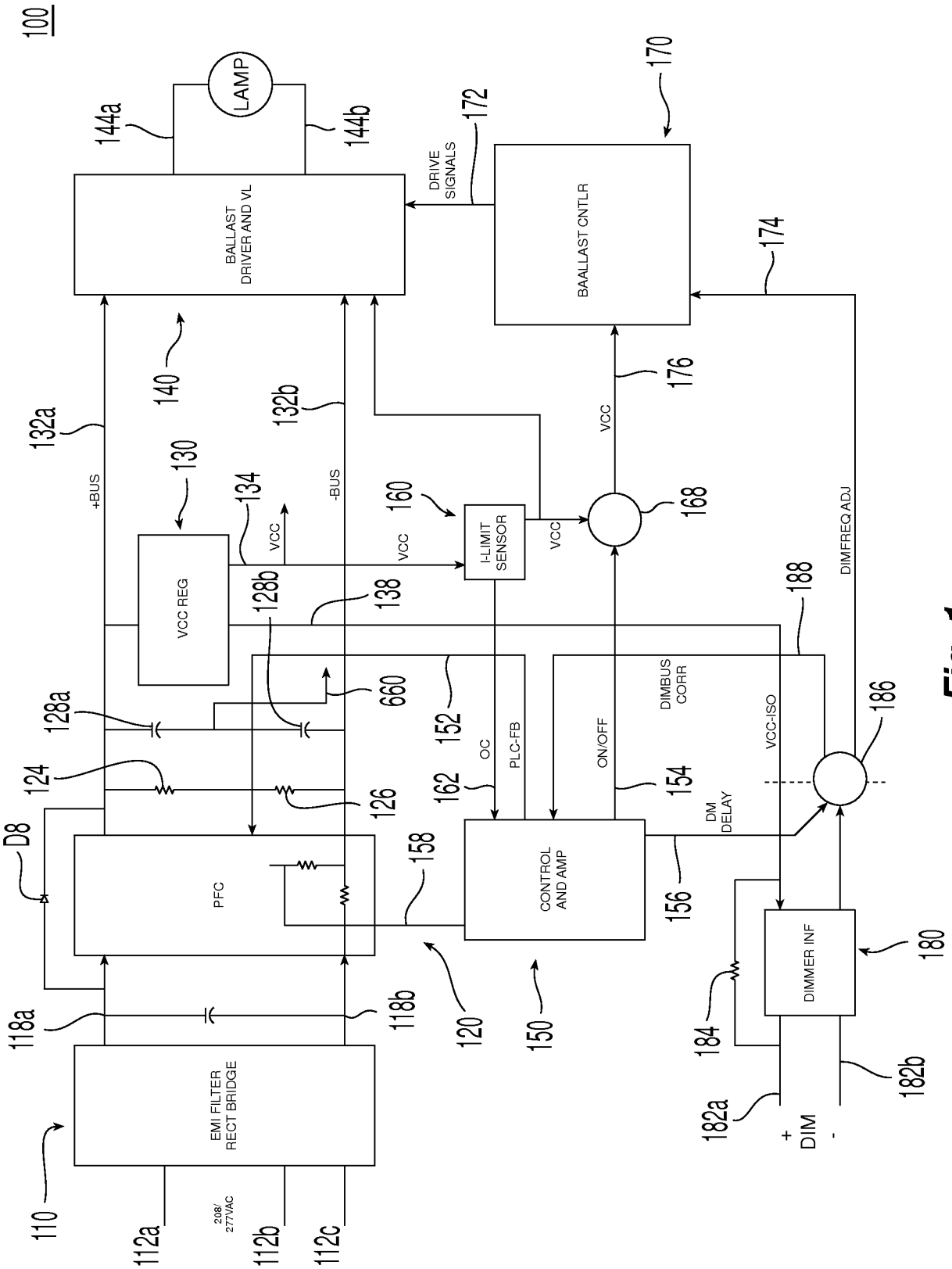

100
LAMP
144a
144b
BALLAST DRIVER AND VL
DRIVE SIGNALS
172
BAALLAST CNTLR
170
174
140
132a
132b
+BUS
-BUS
130
134
VCC REG
VCC
160
I-LIMIT SENSOR
168
176
128b
138
188
DIMFREQ ADJ
660
128a
124
126
152
OC
PLC-FB
ON/OFF
DIMBUS CORR
VCC-ISO
186
162
154
DM DELAY
D8
PFC
158
CONTROL AND AMP
156
DIMMER INF
180
118a
118b
120
150
184
182a
182b
+ DIM -
110
EMI FILTER RECT BRIDGE
208/ 277VAC
112a
112b
112c

Fig. 1

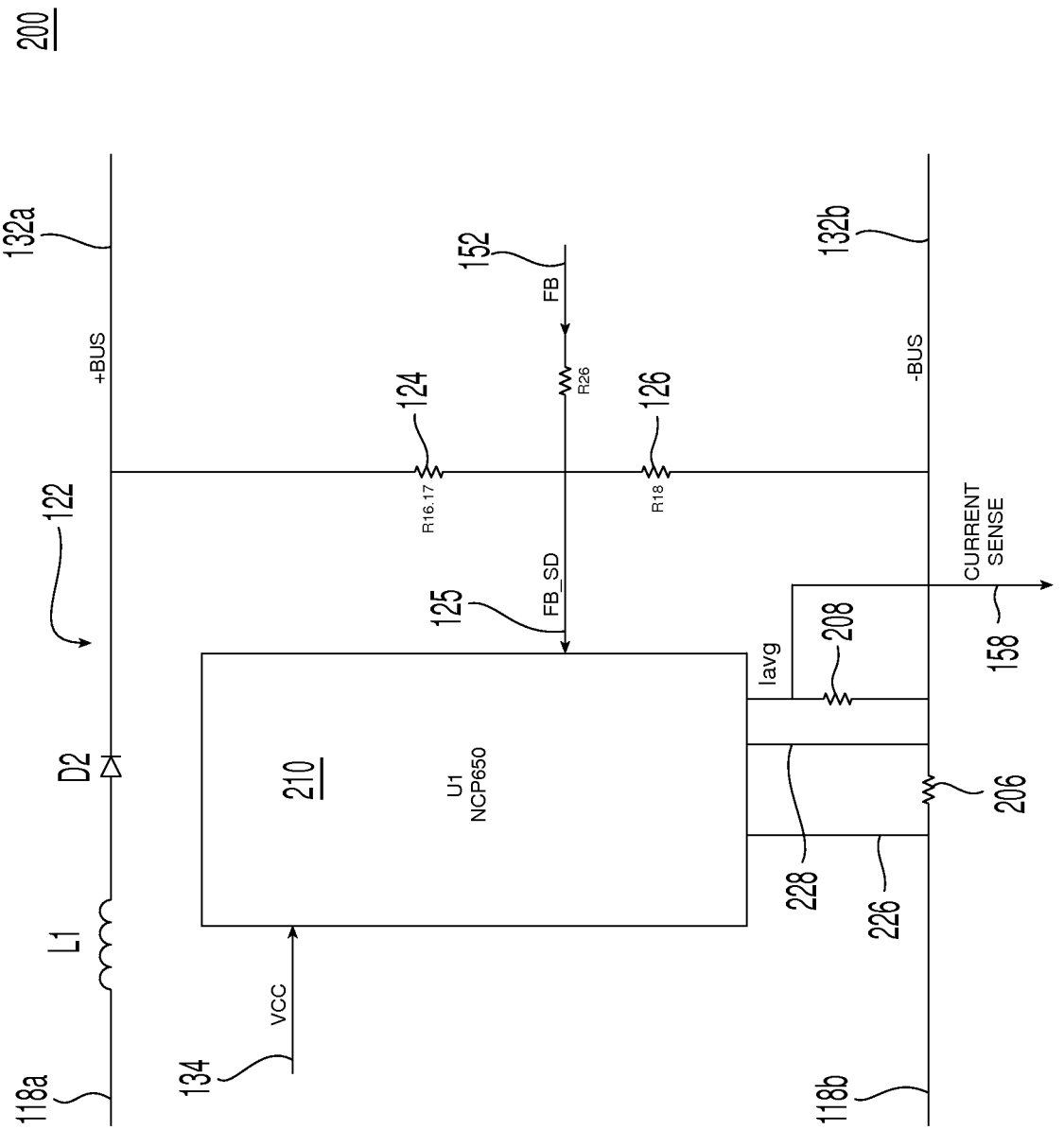

200
132a
+BUS
152
FB
132b
-BUS
124
R16.17
R26
126
R18
122
125
FB_SD
CURRENT SENSE
158
208
Iavg
D2
210
U1
NCP650
206
L1
228
226
VCC
134
118a
118b
PFC

Fig. 2

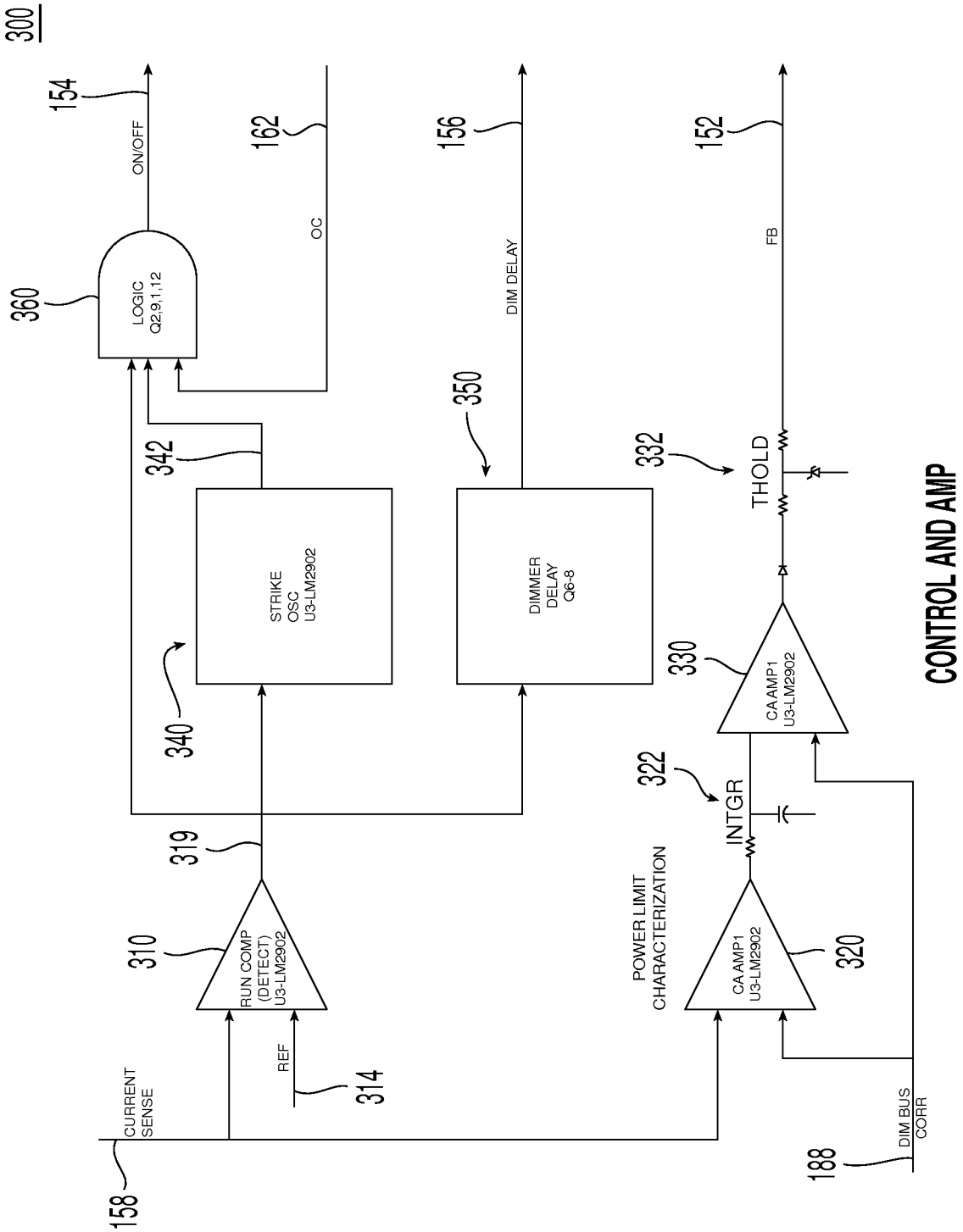

300
154
ON/OFF
162
OC
156
DIM DELAY
152
FB
360
LOGIC
Q2,9,11,12
350
342
332
THOLD
STRIKE
OSC
U3-LM2902
DIMMER
DELAY
Q6-8
340
330
CAAMP1
U3-LM2902
322
INTGR
319
310
RUN COMP
(DETECT)
U3-LM2902
POWER LIMIT
CHARACTERIZATION
CAAMP1
U3-LM2902
320
REF
314
CURRENT
SENSE
158
188
DIM BUS
CORR
CONTROL AND AMP

Fig. 3

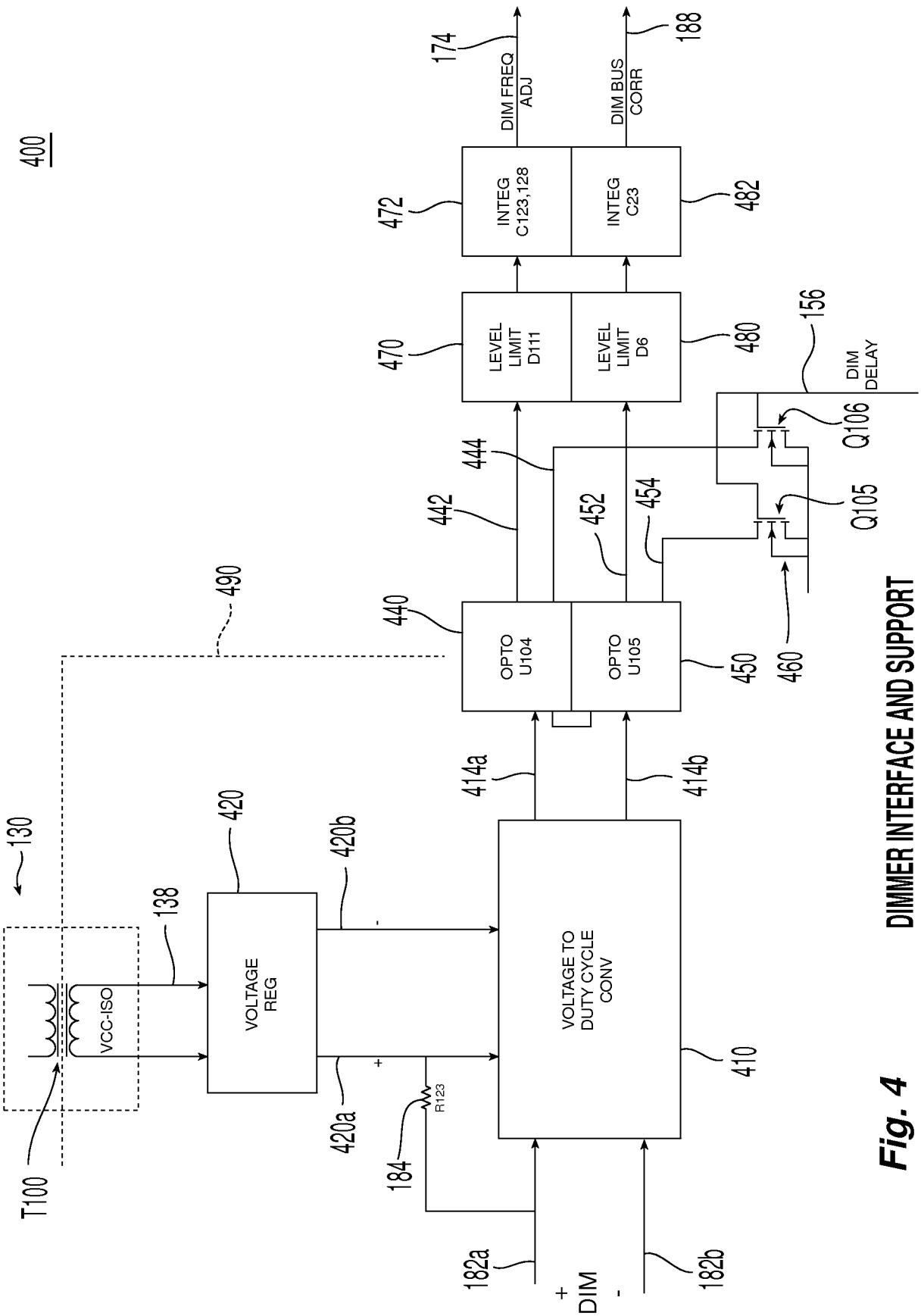


Fig. 4 DIMMER INTERFACE AND SUPPORT

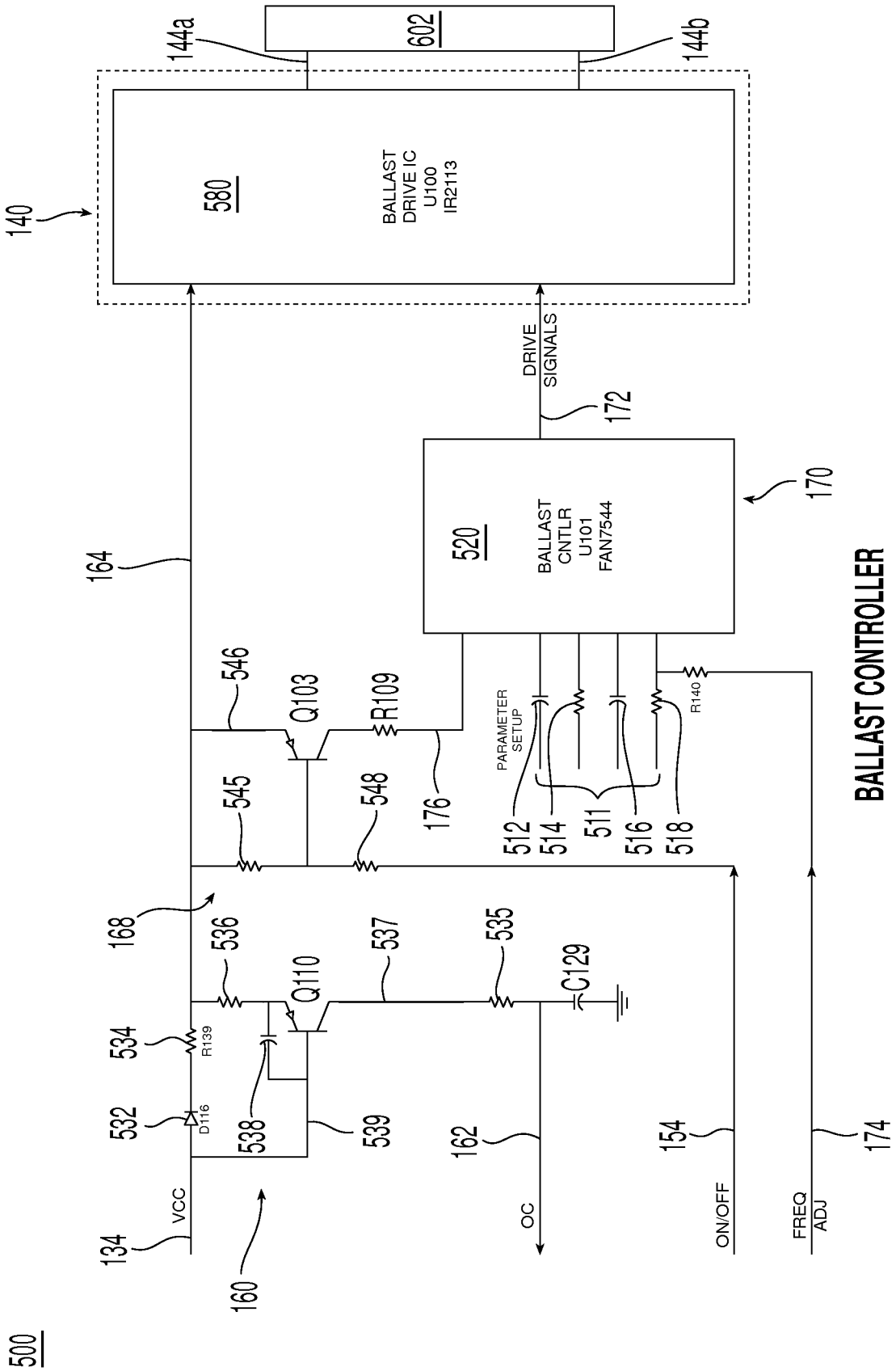

500
140
580
BALLAST DRIVE IC U100 IR2113
144a
602
144b
DRIVE SIGNALS
172
170
520
BALLAST CNTLR U101 FAN7544
BALLAST CONTROLLER
164
546
Q103
R109
545
548
176
PARAMETER SETUP
512
514
511
516
518
R140
168
536
537
535
Q110
C129
534
R139
532
D116
538
539
162
154
174
VCC
134
160
OC
ON/OFF
FREQ ADJ

Fig. 5

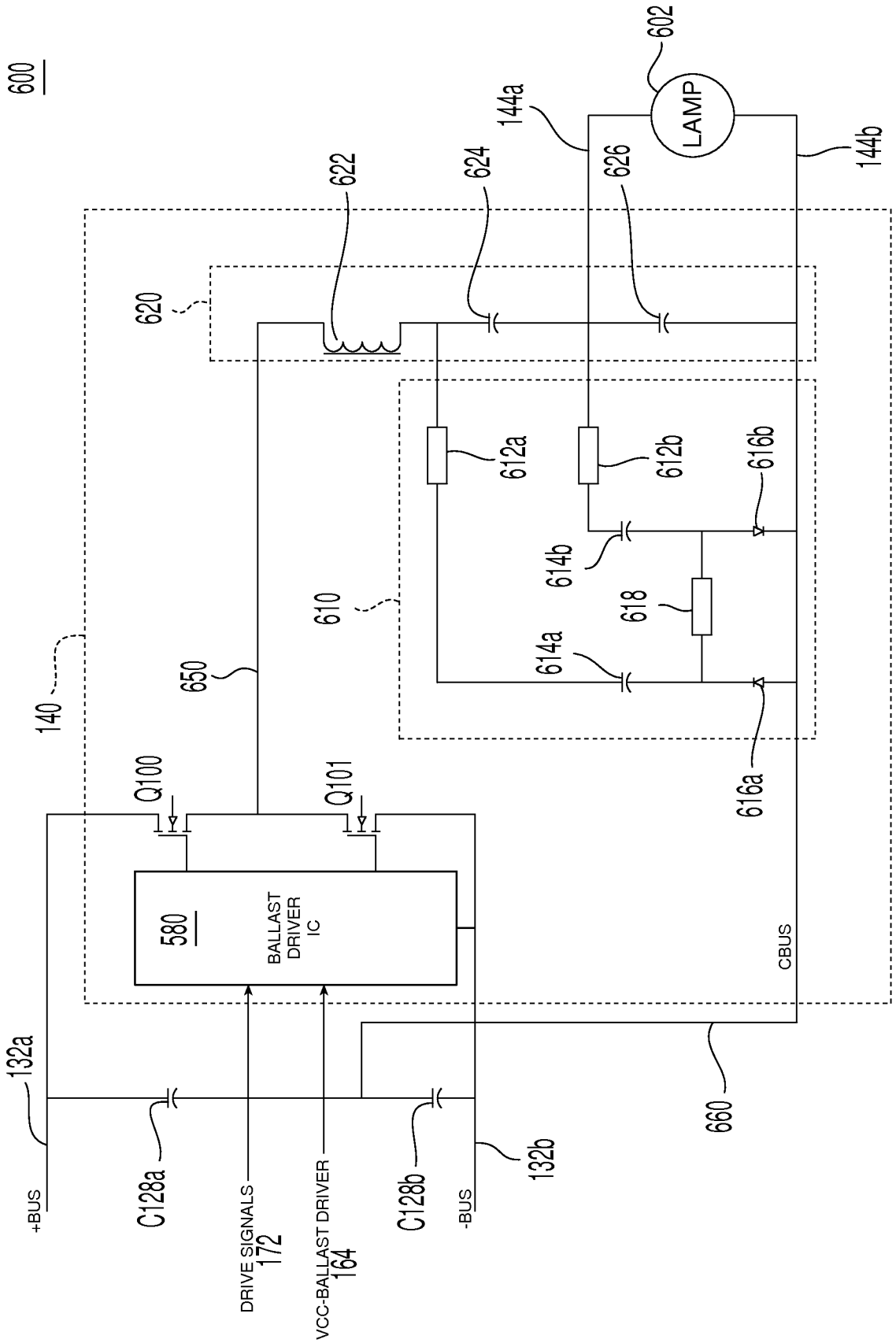
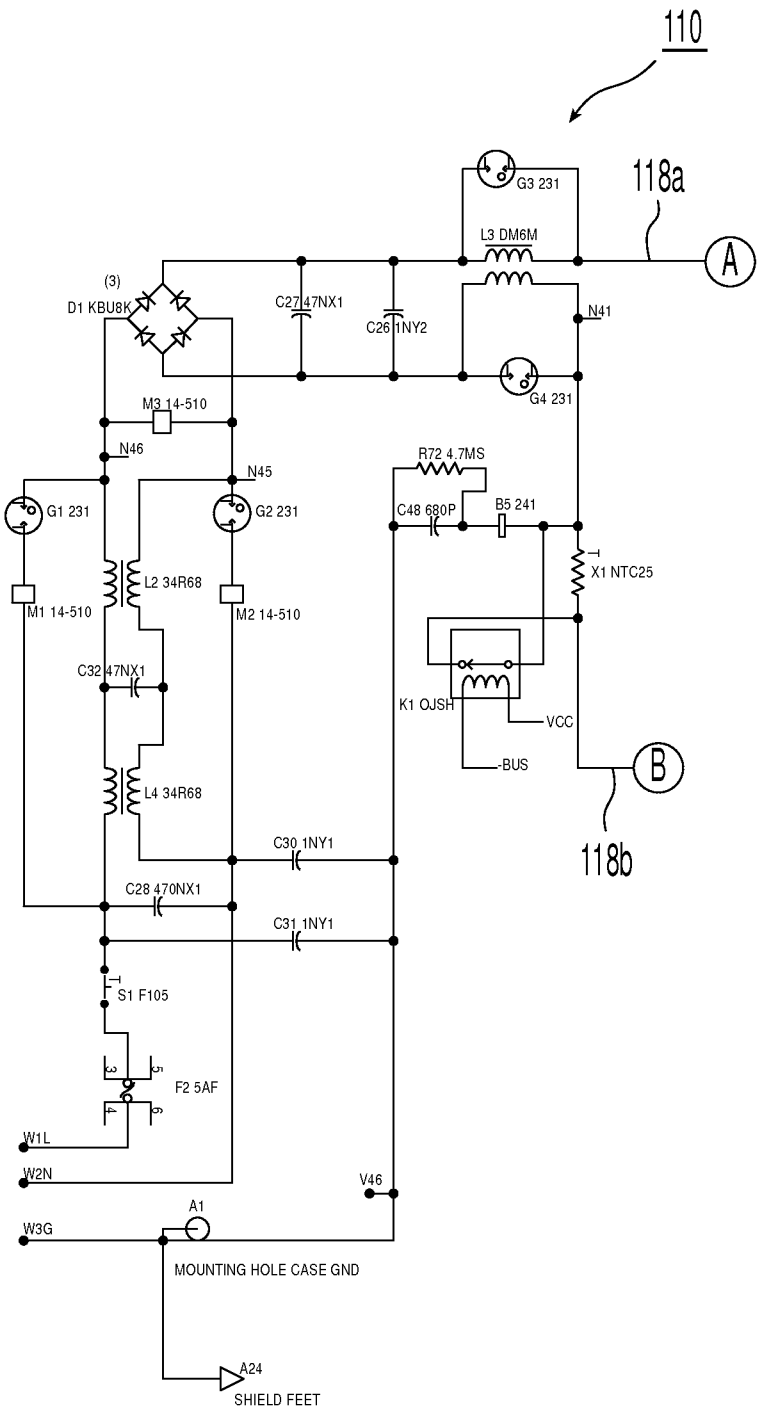
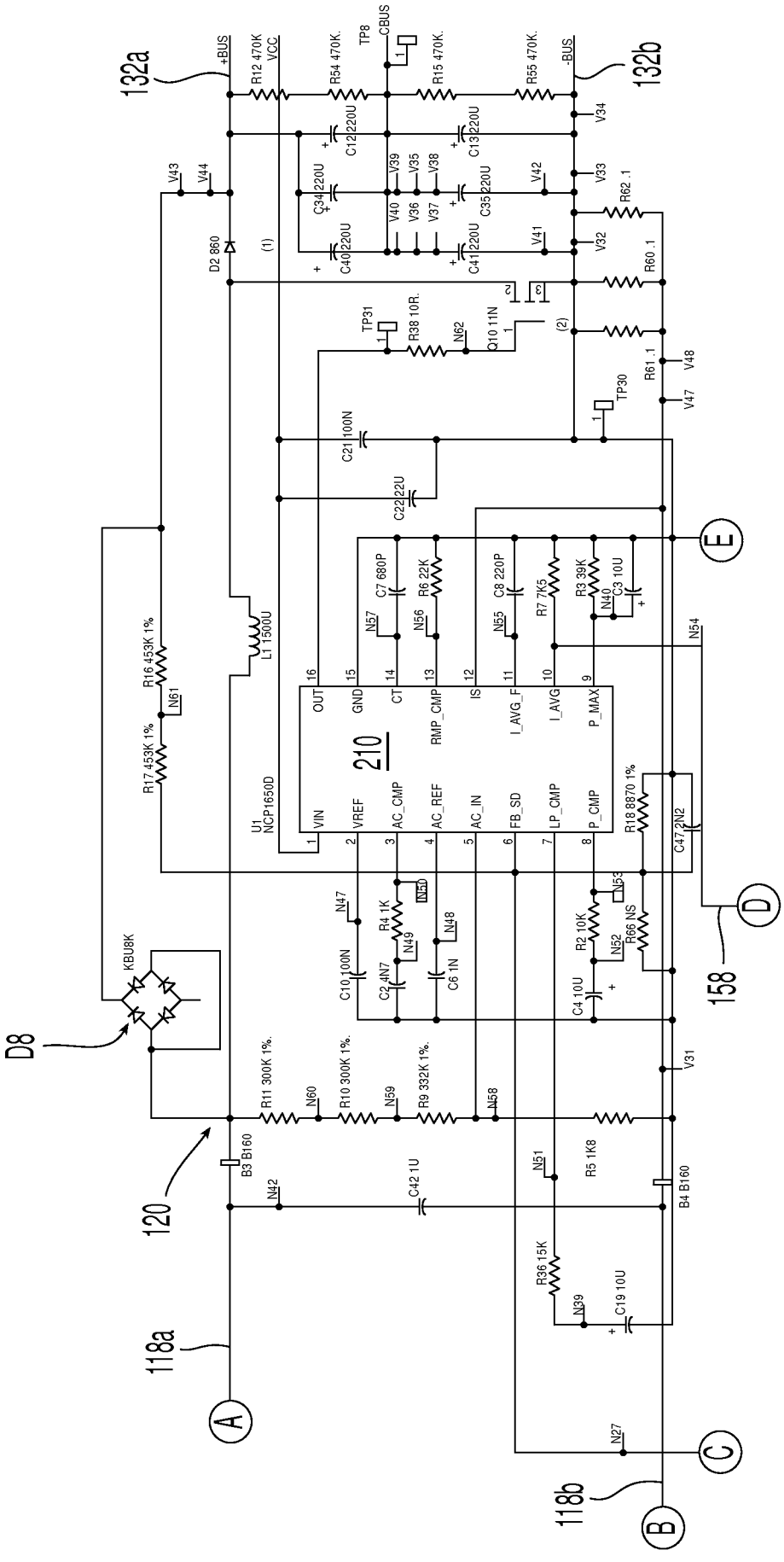


Fig. 6 BALLAST DRIVER AND VL



EMI Filter & Rectifier Bridge

Fig. 7



Power Factor Correction Circuit

Fig. 8

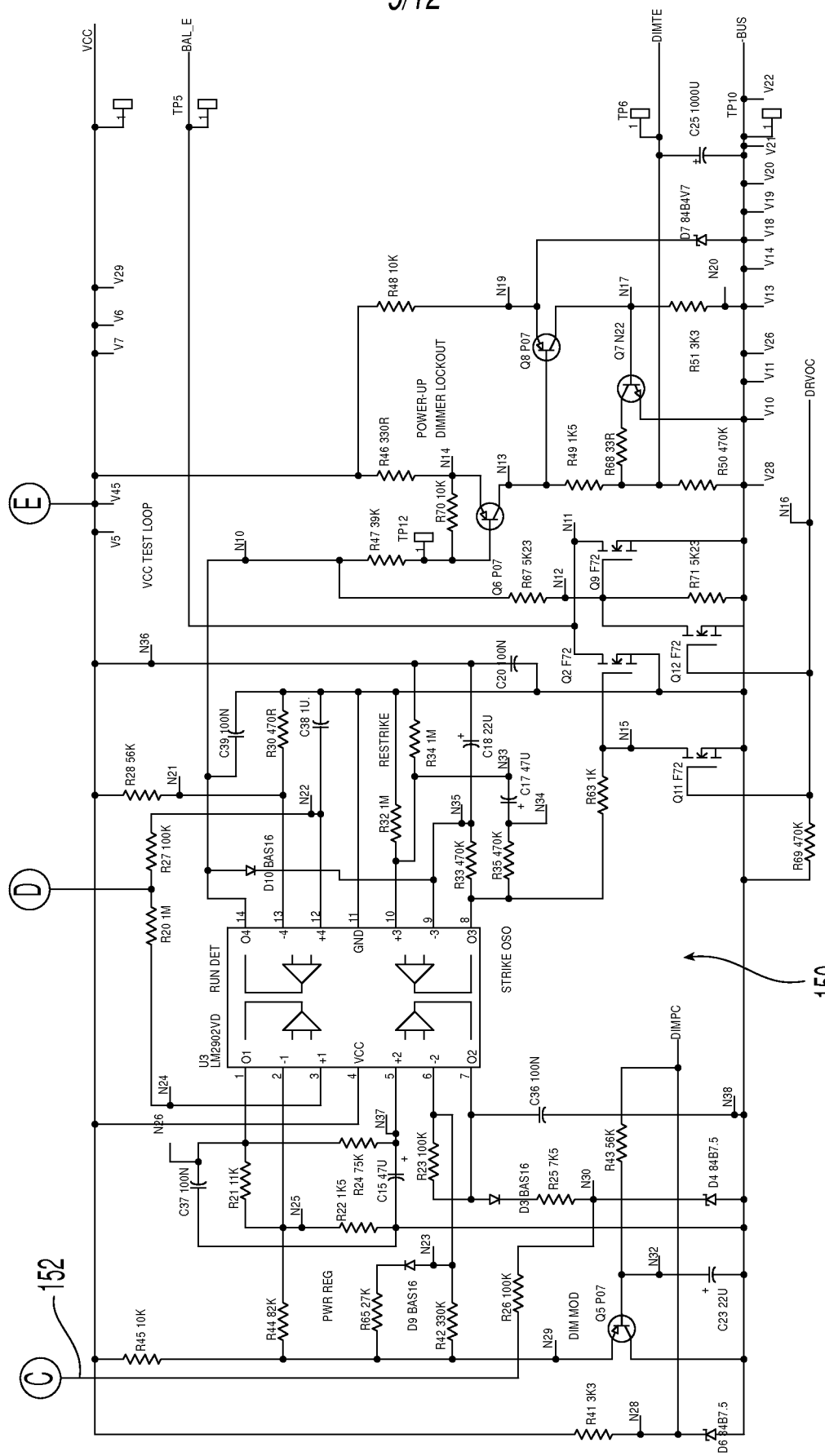

VCC
BAL_E
TP5
DIMTE
TP6
BUS
TP10
C25 1000U
V22
V21
V20
V19
V18
V14
V13
V26
V11
V10
V28
V29
V6
V7
V45
V5
VCC TEST LOOP
D7 84B4V7
N20
R48 10K
N19
N17
Q8 P07
Q7 N22
R51 3K3
R46 330R
POWER-UP
DIMMER LOCKOUT
N14
N13
R49 1K5
R68 33R
R50 470K
DRVOC
N16
R47 39K
TP12
R70 10K
Q6 P07
R67 5K23
N12
N11
Q9 F72
R71 5K23
N10
N36
C20 100N
Q2 F72
Q12 F72
C39 100N
R30 470R
C38 1U.
RESTRIKE
R34 1M
C18 22U
N33
C17 47U
N34
N15
R63 1K
Q11 F72
R28 56K
N21
N22
R32 1M
N35
R33 470K
R35 470K
R69 470K
R27 100K
D10 BAS16
R20 1M
RUN DET
STRIKE OSO
U3
LM2902VD
O4
O3
O1
O2
VCC
GND
DIMPC
N24
N26
N37
N38
C36 100N
C37 100N
R21 11K
R24 75K
C15 47U
R23 100K
R43 56K
D4 84B7.5
N25
R22 1K5
D3 BAS16
R25 7K5
N30
N23
N32
R44 82K
PWR REG
R65 27K
D9 BAS16
R42 330K
R26 100K
DIM MOD
Q5 P07
C23 22U
R45 10K
N29
R41 3K3
N28
D6 84B7.5
150
152
C
D
E
Control and Amplification Circuitry

Fig. 9

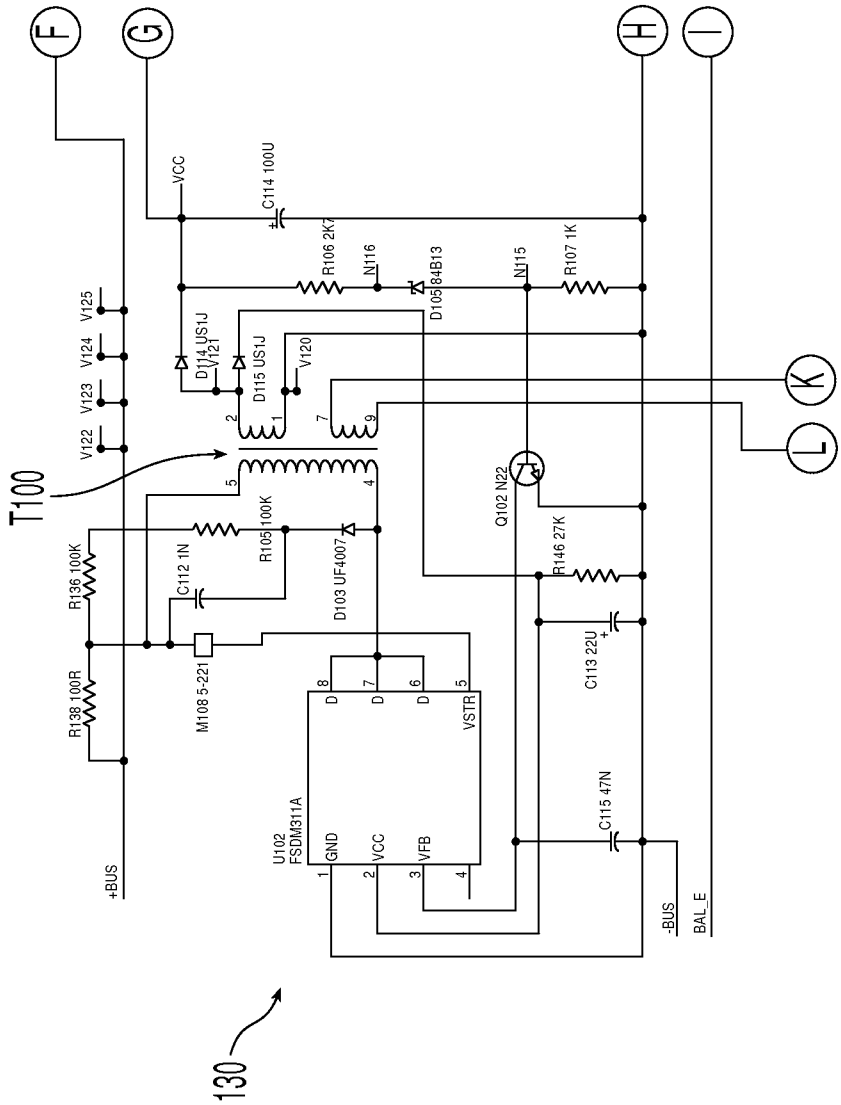


Fig. 10 Voltage Regulator

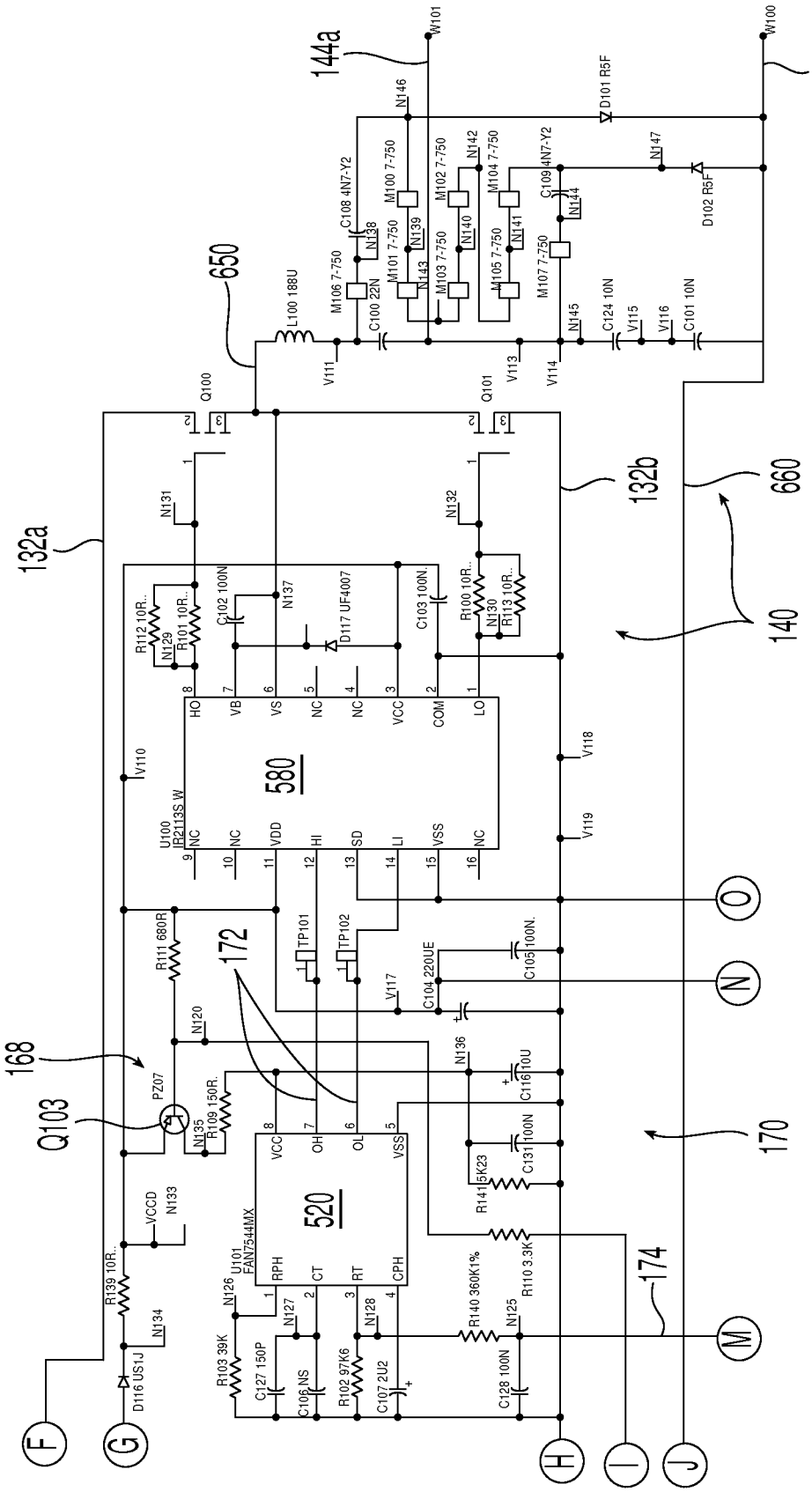

144a
144b
650
660
132a
132b
140
168
Q103
172
170
174
580
520
U100 IR2113S W
U101 FAN7544MX
Q100
Q101
L100 188U
D101 R5F
D102 R5F
D117 UF4007
D116 US1J
PZ07
TP101
TP102
M100 7-750
M101 7-750
M102 7-750
M103 7-750
M104 7-750
M105 7-750
M106 7-750
M107 7-750
C108 4N7-Y2
C109 4N7-Y2
C100 22N
C101 10N
C102 100N
C103 100N.
C104 220UE
C105 100N.
C106 NS
C107 2U2
C116 10U
C124 10N
C127 150P
C128 100N
C131 100N
R100 10R..
R101 10R..
R102 97K6
R103 39K
R109 150R.
R110 3.3K
R111 680R
R112 10R..
R113 10R..
R139 10R..
R140 360K1%
R141 5K23
VCCD
Ballast Controller & Ballast Driver

Fig. 11

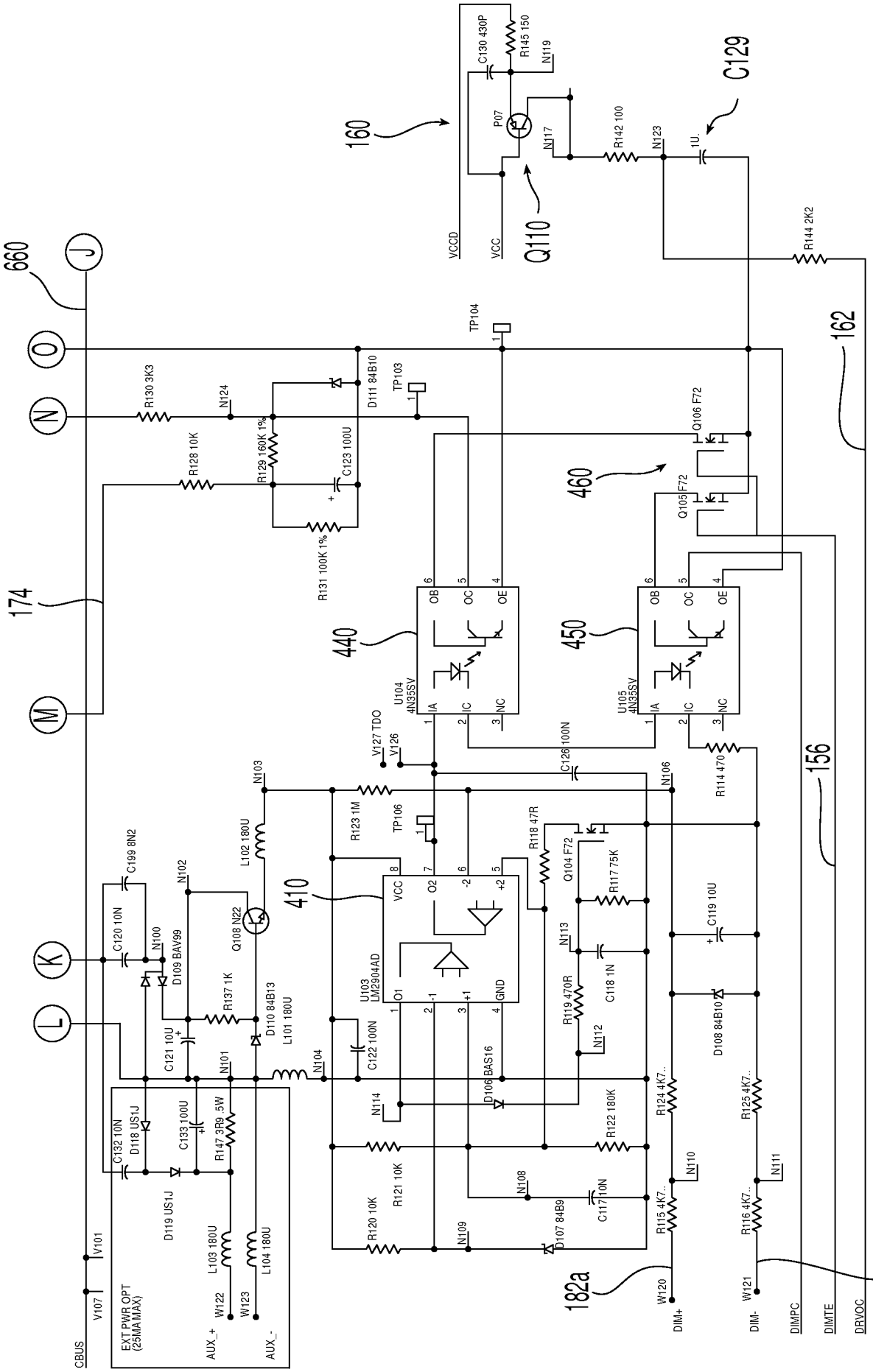


Fig. 12

Dimmer Circuit & Current Limit Sensor

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/055189

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H05B 37/02 (2011.01)
USPC - 315/224
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H05B 37/02, H05B 41/14 (2011.01)
USPC - 315/224, 225, 247, 291, 307

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO EAST System (US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT), Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ----- Y	US 2002/0141129 A1 (RIBARICH) 03 October 2002 (03.10.2002) entire document	1, 23 ------ 2, 3, 8, 24-28
Y	US 2003/0094908 A1 (NERONE et al) 22 May 2003 (22.05.2003) entire document	2
Y	US 2004/0263089 A1 (CONTENTI et al) 30 December 2004 (30.12.2004) entire document	3, 14-16
Y	US 2008/0272748 A1 (MELANSON) 06 November 2008 (06.11.2008) entire document	8
Y	US 2008/0180037 A1 (SRIMUANG) 31 July 2008 (31.07.2008) entire document	8
Y	US 2004/0155635 A1 (INABA) 12 August 2004 (12.08.2004) entire document	24, 25
Y	US 6,262,542 B1 (KIM et al) 17 July 2001 (17.07.2001) entire document	25
Y	US 2001/0054887 A1 (BARETICH et al) 27 December 2001 (27.12.2001) entire document	26
Y	US 2008/0042595 A1 (RIBARICH) 21 February 2008 (21.02.2008) entire document	27
Y	US 2006/0261739 A1 (LEE et al) 23 November 2006 (23.11.2006) entire document	28
Y	US 6,211,623 B1 (WILHELM et al) 03 April 2001 (03.04.2001) entire document	14-16
Y	US 2007/0040516 A1 (CHEN) 22 February 2007 (22.02.2007) entire document	15, 17-22

☒ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 February 2011	01 MAR 2011
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/055189

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,121,734 A (SZABADOS) 19 September 2000 (19.09.2000) entire document	16-22

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/055189

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See extra sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☒ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

1-8, 14-28

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/055189

Continuation of Box III.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claims 1-8 and 23-28, drawn to an apparatus including a ballast driver circuit having a resonant circuit having a first resonant frequency and configured to drive a lamp; and a voltage limiter/overcurrent circuit connected to the resonant circuit.

Group II, claims 9-13, drawn to an apparatus including a power factor controller circuit comprising a PFC integrated chip and a voltage divider.

Group III, claims 14-16, drawn to an apparatus including ahaving a resonant circuit having a first resonant frequency and configured to drive a lamp; and a voltage limiter/overcurrent circuit connected to the resonant circuit.

Group IV, claims 17-22, drawn to an apparatus including a first opto-isolator connected to a voltage-to-duty-cycle converter and a second opto-isolator connected to said voltage-to-duty-cycle converter.

The inventions listed as Groups I, II, III, or IV do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the special technical feature of the Group I invention: a ballast driver circuit having a resonant circuit having a first resonant frequency and configured to drive a lamp; and a voltage limiter/overcurrent circuit connected to the resonant circuit as claimed therein is not present in the invention of Groups II, III, or IV as a novel special technical feature. The special technical feature of the Group II invention: a power factor controller circuit comprising a PFC integrated chip and a voltage divider as claimed therein is not present in the invention of Groups I, III, or IV. The special technical feature of the Group III invention: having a resonant circuit having a first resonant frequency and configured to drive a lamp; and a voltage limiter/overcurrent circuit connected to the resonant circuit as claimed therein is not present in the invention of Groups I, II, or IV. The special technical feature of the Group IV invention: a first opto-isolator connected to a voltage-to-duty-cycle converter and a second opto-isolator connected to said voltage-to-duty-cycle converter as claimed therein is not present in the invention of Groups I, II, or III.

Groups I, II, III, and IV, lack unity of invention because even though the inventions of these groups require the technical feature of an electronic ballast circuit comprising: a ballast controller circuit; a power factor correction circuit; a ballast driver circuit; and an overcurrent sensor circuit, this technical feature is not a special technical feature as it does not make a contribution over the prior art in view of US 2004/0263089 A1 (CONTENTI et al) figure 1; abstract; and paragraphs 13-14, 18, and 27-28.

Since none of the special technical features of the Group I, II, III or IV inventions are found in more than one of the inventions, unity of invention is lacking.