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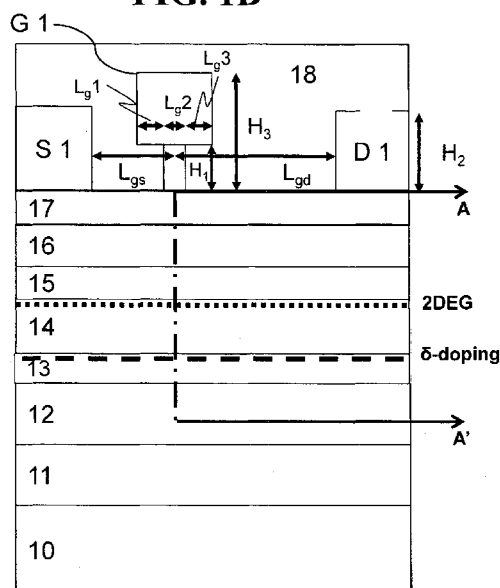

(57) Abstract: A semiconductor device includes a semiconductor structure including a first doped layer (16) for forming a carrier channel having a carrier charge, a second doped layer (13) having a conductivity type identical to a conductivity type of the first doped layer, a barrier layer arranged in proximity to the semiconductor structure via the second doped layer, wherein the barrier layer includes a doped layer (11) having a conductivity type opposite to the conductivity type of the second doped layer, and a set of electrodes for providing and controlling the carrier charge in the carrier channel.

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[DESCRIPTION]

[Title of Invention]

SEMICONDUCTOR DEVICE AND METHOD FOR DESIGNING SEMICONDUCTOR DEVICE

[Technical Field]

[0001]

This invention relates generally to semiconductor devices, and more particularly to semiconductor devices with high linearity-transconductance.

[Background Art]

[0002]

A nitride semiconductor device is used for high-power and high-frequency applications, due to its outstanding combination of fundamental physical properties, such as large band gaps, large breakdown fields, high electron mobilities, etc. In order to achieve the gain and efficiency requirements at K-band and above, the natural way is to achieve low gate capacitance by reducing gate length. However, GaN high electron mobility transistors (HEMTs) are vulnerable to short-channel effects like all field effect transistors (FETs) when gate length scales below 0.2μm. The short-channel effects take the form of a drain dependent pinch-off voltage, the loss of saturation on output current including a linearity of a transconductance, a large off-state drain leakage current and low breakdown voltage.

[0003]

Linearity of a transconductance is an important factor for RF power amplifiers due to the large dynamic range in the variable envelop of the modulation signals. An ideally linear FET device would possess constant drain transconductance over a wide range of input gate–source voltages. The

problems in achieving flat transconductance are related to (1) small absolute distance between 2DEG and gate, (2) the increase of the access resistance at high drain current levels caused by quasi-saturation of the electron velocity, and (3) large transverse electric-field (E-field) *perpendicular* to the channel and the barrier/channel interface at the high current levels.

[0004]

Thus, there is a need for a GaN material transistor structure that provides a high electron mobility channel having a linear transconductance with suppressed short channel effect for RF applications.

[Summary of Invention]

[0005]

Some embodiments are based on recognition that a way of improving the linearity of a transcondcutance of a transistor is related to modifying the access resistance using multichannel heterostructures or forming a minor channel near a main channel using composite-channel design. Another possible way is to create a minor channel by introducing n-doped layer below the channel layer of AlGaN/GaN HEMT with an n-GaN layer introduced in a buffer layer.

[0006]

Some embodiments of a semiconductor device according to the invention semiconductor device comprises a semiconductor structure including a first doped layer for forming a carrier channel having a carrier charge; a second doped layer having a conductivity type identical to a conductivity type of the first doped layer; a barrier layer arranged in proximity to the semiconductor structure via the second doped layer, wherein the barrier layer includes a partially doped layer having a conductivity type opposite to

the conductivity type of the second doped layer; and a set of electrodes for providing and controlling the carrier charge in the carrier channel.

[0007]

Another embodiment of the invention discloses that a semiconductor device comprises a semiconductor structure including a channel layer, first barrier layers for providing a carrier charge, wherein the channel layer is undoped layer and the first barrier layers consist of a undoped barrier, a first n-type doped barrier and another undoped barrier; a second n-type doped layer adjacent to the channel; a second barrier layer arranged in proximity to the semiconductor structure via the second n-type doped layer, wherein the second barrier layer includes at least partially p-typed doped layer; and a set of electrodes for controlling the carrier charge in the carrier channel.

[0008]

Still another embodiment of the invention discloses a method for designing a semiconductor device. The method comprises selecting a III-V semiconductor heterostructure including a channel layer and first barrier layers for providing a carrier charge wherein the channel layer is undoped layer and the first barrier layers consist of a undoped barrier, a first n-type doped barrier and another undoped barrier, wherein a bandgap of a material of the first barrier layers is selected so as to be greater than a bandgap of a material of the channel layer; arranging a second n-type doped layer adjacent to the channel layer; selecting a second barrier layer of a III-V semiconductor in proximity to the channel layer via the second n-type doped layer, wherein the second barrier layer includes a partially p-typed doped layer; and providing a set of electrodes for controlling the carrier charge in the carrier channel.

[0009]

The forgoing and other objects, features and effects of the invention will become more apparent from the following detailed description of the embodiments with reference to the attached drawings.

[Brief Description of Drawings]

[0010]

[Fig. 1A]

FIG. 1A shows a designing process of a semiconductor device having a semiconductor structure including a channel and barrier layers.

[Fig. 1B]

FIG. 1B shows a cross-sectional diagram of a semiconductor device according to some embodiments of the invention.

[Fig. 1C]

FIG. 1C shows a cross-sectional diagram of a semiconductor device according to some embodiments of the invention.

[Fig. 2]

FIG. 2 shows a comparison of conduction band diagrams of a conventional HEMT structure and a proposed HEMT structure.

[Fig. 3]

FIG. 3 shows a comparison of transfer characteristics of a conventional HEMT structure and a proposed HEMT structure with a 18nm or 25nm barrier and Lg_2=200nm.

[Fig. 4A]

FIG. 4A shows I-V characteristics of a conventional HEMT structure with Lg_2=200nm.

[Fig. 4B]

FIG. 4B shows I-V characteristics of a proposed HEMT structure with

Lg_2=200nm.

[Fig. 5]

FIG. 5 shows a comparison of current gain cutoff frequencies of a conventional HEMT structure and proposed HEMT structure with a 18nm or 25nm barrier layer; Lg_2=200nm, V_{ds}=3V and the ac simulation was conducted at f = 1 MHz.

[Fig. 6]

FIG. 6 shows a comparison of current gain cutoff frequencies as a function of gate length in conventional structure and proposed structure with 18 or 25nm barrier. V_{ds}=3V and the ac simulation was conducted at f = 1 MHz.

[Fig. 7]

FIG. 7 shows a comparison of drain induced barrier lowering as a function of gate length in conventional structure and proposed structure with 18 or 25nm barrier. V_{th} is defined when I_{ds} reaches 0.1mA/mm.

[Fig. 8]

FIG. 8 shows transconductance profiles of HEMTs with delta-doped layer inserted.

[Description of Embodiments]

[0011]

Various embodiments of the invention are described hereafter with reference to the figures. It would be noted that the figures are not drawn to scale elements of similar structures or functions are represented by like reference numerals throughout the figures. It should be also noted that the figures are only intended to facilitate the description of specific embodiments of the invention. They are not intended as an exhaustive description of the invention or as a limitation on the scope of the invention. In addition, an aspect

described in conjunction with a particular embodiment of the invention is not necessarily limited to that embodiment and can be practiced in any other embodiments of the invention.

[0012]

Some embodiments are based on recognition that a semiconductor device is consisted of an i-n-i barrier, a delta-doped n-GaN layer inserted in a buffer and a back barrier, which can provide (a) a high device linearity of transconductance, and suppress (b) short channel effect.

[0013]

The short channel effects originate from poor confinement of electrons in the channel, resulting in current flowing within the bulk of the GaN layer. A back barrier structure can be used to improve carrier confinement, which prevents electron punch-through and suppress short channel effect. The back-barrier structure for the electron confinement enhancement can be a p-type GaN or some materials having a larger bandgap than the bandgap of GaN.

[0014]

Improving the linearity of a transconductance of a transistor can be realized by creating a minor channel through inserting an n-doped layer in buffer layer. However, due to the large polarization field in AlGaN/GaN HEMT, and the limitation of uniform doping density in n-GaN inserted layer, it would be very hard to form a secondary channel to achieve good device linearity. Delta doping (δ-doping) can be a technique to significantly increase doping density, as the maximum uniform doping density is limited by the available Si source. Si delta-doping in GaN layer can provide a sheet concentration as high as 1×10^{12} cm^{-2} to 2×10^{13} cm^{-2}, while the Si uniform-doping in GaN can only achieve concentration up to a few 10^{19} cm^{-3} which is

equivalent a range of a sheet concentration < 10^{12} cm^{-2}. In addition, high density uniform doping in GaN would introduce a significant amount of strain which can cause cracking of layers, while Si delta-doping is a method to reduce tensile stress as well as obtaining high doping density. Moreover, Si δ-doping has other benefits in enhancing electron mobility, decreasing defect densities and reducing threading edge dislocation density.

[0015]

In some embodiments, a semiconductor device is formed on a substrate and includes a back barrier layer, an unintentional doped buffer layer, an inserted n-type δ-doped layer, an unintentionally doped channel layer, an i-n-i barrier layer, and a source electrode, a drain electrode and a T-shape gate electrode on the barrier layer, and a passivation layer over the top of the whole device. The semiconductor device may be an AlGaN/GaN high-electron-mobility transistor (HEMT), which provides advantages in achieving ultra-flat transconductance, suppressing short channel effect and obtaining large on-state current.

[0016]

More specifically, the semiconductor device may include a back barrier layer on a substrate, followed by an unintentional doped buffer, then an inserted n-type δ-doped layer, an unintentional doped channel layer, an i-n-i barrier layer, and then a source electrode, a drain electrode and a T-shape gate electrode on the barrier layer, and a passivation layer over the top of the whole device. A major channel (or major electron channel) is formed by polarization between barrier layer and channel layer, and a minor channel is formed by arranging a heavily n-type δ-doped layer. The major channel may be referred to as a first channel and the minor channel may be referred to as a second

channel. The barrier layer is a stack of a thin unintentionally doped layer, an n-doped layer followed by another thin unintentionally doped layer. In the following, proposed HEMT structures in accordance with some embodiments of the invention will be described.

[0017]

Some embodiments of the invention are based on a recognition that a semiconductor device is designed for a power amplifier by selecting a semiconductor heterostructure that includes channel and barrier layers. For instance, a method for designing the semiconductor device includes selecting a III-V semiconductor heterostructure including a channel layer and first barrier layers for providing a carrier charge, wherein the channel layer is undoped layer and the first barrier layers consist of a undoped barrier, a first n-type doped barrier and another undoped barrier,wherein a bandgap of a material of the first barrier layers is selected so as to be greater than a bandgap of a material of the channel layer. Further, a second n-type doped layer adjacent to the channel layer is arranged, and a second barrier layer of a III-V semiconductor is arranged in proximity to the channel layer via the second n-type doped layer, wherein the second barrier layer includes a partially p-typed doped layer, and then the structure of the semiconductor device is obtained by providing a set of electrodes for the semiconductor heterostructure for controlling the carrier charge in the carrier channel.

[0018]

FIG. 1A shows a method for designing a semiconductor device having a semiconductor structure including a channel and barrier layers.

[0019]

A semiconductor structure which includes a channel layer and barrier

layers is determined (selected) for manufacturing a semiconductor device. The semiconductor device can be applied for an RF power amplifier. After selecting the semiconductor structure in step 100, such as a transistor structure including the channel and barrier layers, materials of the channel layer and barrier layers are selected in step 110. Subsequently, the geometrical parameters, such as thicknesses of the layers, positions of doping layers in the semiconductor structure are determined in steps 120 and 130. In this case, the geometrical parameters may include sizes of a gate electrode, a source electrode, and a drain electrode. Further, doping densities of doped layers and a partially doped barrier layer in the semiconductor structure as well as impurities of the first and second doping layers and the partially doped barrier layer, amounts of compositions in compound semiconductor materials are determined. For instance, the n-type doping layer may be silicon (Si) doped layers, and the p-type doping layer may be a magnesium (Mg) or carbon (C) doped layer.

[0020]

Based on the determinations above, an energy band structure (band structure) of the semiconductor device is simulated. For instance, the band structure may be calculated (simulated) from the channel layer to the partially doped barrier layer. A device performance is simulated based on the semiconductor structure described above. After simulating a device performance in step 140, a linearity of a transconductance of the semiconductor device is characterized based on a transconductance profile as a function of voltages between the gate and source electrodes at a predetermined constant drain voltage. According to an evaluation result of the device performance, steps 120 and 130 may be performed repeatedly.

[0021]

FIG. 1B and FIG. 1C show a cross-sectional diagram of a semiconductor device according to some embodiments of the invention. The figures illustrate a structure of a high-electron mobility transistor (HEMT) as an example of the semiconductor device.

[0022]

FIG. 1B is the cross-sectional diagram of a semiconductor device according to some embodiments of the invention. The semiconductor device includes a substrate layer 10. The substrate layer 10 may be Si, SiC, sapphire and diamond. Further, the substrate layer 10 can be a single substrate layer or include multiple layers such as transition layers between substrate layer and the doped layer 11. The doped layer 11 is a back-barrier layer that is fully or partially doped by impurities with a conductivity type opposite to the conductivity type of the carrier channel 14.

[0023]

According to some embodiments of the invention, various methods can be adopted for the formation of a substrate region 10 (substrate10), including but not limiting to a Chemical Vapor Deposition (CVD), a Metal-Organic Chemical Vapor Deposition (MOCVD), a DC plasma CVD. The back-barrier layer 11 is disposed on the substrate region 10, with an exemplary thickness of 2μm. The material of layer 11 can be p-GaN, AlGaN, InGaN and p-diamond. For the doped layer 11 as p-GaN, it can be doped with Mg or C dopants with an exemplary doping density in the range from 1×10^{16} cm^{-3} to 1×10^{19} cm^{-3}; For layer 11 as AlGaN or InGaN, it can be intrinsic with Al content/In content in the range from 0.04 to 0.1; For layer 11 as p-diamond, it can be doped with p-type dopants such as B with an exemplary doping density in a range from

1×10^{16} cm^{-3} to 1×10^{21} cm^{-3}. The dopants in the layer 11 can be added during epitaxial growth or can be added by ion implantation after the layer 11 is formed.

[0024]

An unintentionally-doped (UID) semiconductor buffer layer 12 (region 12) is disposed on the back-barrier layer 11 with an exemplary thickness of 100nm to 200nm. The material of the UID semiconductor buffer layer 12 can be III-nitride or III-arsenide materials. An n-type doped semiconductor layer 13 is disposed on the UID buffer layer 12. The n-type doped semiconductor layer 13 may be referred to as a second doped layer 13. The n-type doped semiconductor layer 13 can be a thin n-doped layer or an n-type delta-doped layer. In one embodiment, materials of the doped layer 13 can be Si delta-doped GaN layer with sheet doping density in the range from 1×10^{12} cm^{-2} to 1×10^{13} cm^{-2}, and the thickness of delta-doped GaN layer is in the range from monolayer to a few multilayers (2.5 Å to 10 Å). According to some embodiments, various methods can be adopted for the formation of Si delta-doped GaN layer 13 with a high n-doping density, including but not limiting to a chemical vapor deposition (CVD), a metal-organic chemical vapor deposition (MOCVD), a molecular beam epitaxy (MBE) and a metal-organic vapor phase epitaxy (MOVPE).

[0025]

In some embodiments of the inventnion, a thickness of the first doped layer is greater than a thickness of the second doped layer.

[0026]

An unintentionally-doped (UID) channel layer 14 is disposed on the n-type doped semiconductor layer 13. The thickness of the channel layer 14 may

be in a range from 10nm to 40nm. In some embodiments, the material of the channel layer 14 can be III-V materials.

[0027]

An unintentionally-doped compound semiconductor barrier layer 15 is disposed on the channel layer 14. The thickness of the barrier layer 15 may be a few nanometers (2 nm to 4 nm). The material of the barrier layer 15 has a different lattice constant and bandgap energy compared to the material of the channel layer 14. In some embodiments, a 2DEG channel is formed at the heterostructure of the barrier layer 15 and the channel layer 14 due to polarizations. In some cases, the materials of barrier layer 15 and channel layer 14 can be AlGaN and GaN, InAlN and GaN, AlN and GaN, or InAlGaN and GaN. An n-doped compound semiconductor barrier layer 16 is disposed on the unintentionally-doped layer 15 with doping density ranging from 1×10^{18} cm^{-3} to 3×10^{18} cm^{-3}, and with thickness ranging from 13nm to 20nm. The n-doped compound semiconductor barrier layer 16 may be referred to as a first doped layer 16.

[0028]

Another unintentionally-doped semiconductor barrier layer 17 is disposed on the n-type semiconductor barrier layer 16, with an exemplary thickness of a few nanometers (2 nm to 4 nm). The material of semiconductor layers 15, 16 and 17 are preferred to be the same and can be compound III-V semiconductor materials such as AlGaN, InAlN and InAlGaN. Further, the semiconductor layers 15, 16 and 17 may be referred as an i-n-i barrier layer or a barrier layer. The barrier layer may have a total thickness ranging from 18nm to 25nm, in which a thickness of the n-type semicondutor barrier layer 16 is varied between 13nm and 20nm.

[0029]

In some embodiments of the invention, the unintentionally-doped semiconductor barrier layers 15 and 17 may be referred to as the first barrier layers, and the back barrier 11 may be referred to as the second barriers. In this case, the materials of the first and second barrier layers may be selected such that a lattice mismatch between the barrier layers and the channel layer is in range of approximately ±1 percent of the lattice constant of the channel layer. This selection can be effective to reduce crystal strain and defects in the semiconductor device structure.

[0030]

According to some embodiments, various methods can be adopted for the formation of the compound semiconductor layer 14 to the UID barrier layer 17, including but not limiting to a chemical vapor deposition (CVD), a metal-organic chemical vapor deposition (MOCVD), a molecular beam epitaxy (MBE) and a metal-organic vapor phase epitaxy (MOVPE).

[0031]

In some embodiments of the invention, the substrate 10 may be selected for supporting the layers 11 through 17 and such that a thermal conductivity of the substrate 10 is greater than at least one of materials of the channel layer 14 and the barrier layer 11. Further, the materials of the first and second barrier layers may be selected such that a lattice mismatch between lattice constants of the first and second barrier layers and a lattice constant of the channel layer is in range of approximately ±1 percent of the lattice constant of the channel layer, which reduces crystal defects in the semiconductor device.

[0032]

The set of electrodes includes the source electrode S 1, the T-shape gate

electrode G 1 and drain electrode D 1. The left part of T-shape gate electrode L_g1 can be fixed at 0.05 μm. In some embodiments, the center part of T-shape gate electrode L_g2 and the right part of T-shape gate electrode L_g3 can be in the range of 0.05 μm to 0.5 μm and 0.1 μm to 0.3 μm, respectively. In one embodiment, the distance between the barrier layer 17 to the lower side of the gate electrode H_1, the height of source/drain electrode H_2 and the height of T-gate electrode H_3 are 0.1 μm, 0.2 μm and 0.3 μm, respectively. In some embodiments, the material to form source/drain electrode S 1/D 1 can be Ti/Al/Ni/Au metal stack for ohmic contact, and Schottky T-gate electrode G 1 can be formed by Ni/Au metal stack or Pt metal.

[0033]

In some other embodiments, a dielectric layer 18 (dielectric region 18) can be formed as a passivation layer. The dielectric layer 18 can include a single or multiple insulating layers, with the materials including but not limiting to Al_2O_3, SiO_2, AlN, SiN_x, HfO_2, nanocrystalline diamond.

[0034]

According to some embodimenets of the invention, FIG. 1B and FIG. 1C show an example device structure referred to as a proposed semiconductor deivce, which has layers having sized and compositions as follows:

Substrate layer 10: SiC

Back-barrier layer 11: 1.8 μm p-GaN with doping density of 1×10^{17} cm^{-3}

Unintentionally-doped (UID) buffer layer 12: 0.2 μm UID-GaN layer

n-type delta-doped semiconductor layer 13: 1 nm n-GaN with doping density of 6×10^{19} cm^{-3}

Unintentionally-doped (UID) channel layer 14: 25 nm UID-GaN layer

Unintentionally-doped barrier layer 15: 3nm UID-$Al_{0.3}Ga_{0.7}N$ layer

n-doped barrier layer 16: 13nm or 20nm n-$Al_{0.3}Ga_{0.7}N$ layer with doping density of 2×10^{18} cm^{-3}

Unintentionally-doped barrier layer 17: 2nm UID-$Al_{0.3}Ga_{0.7}N$ layer

Dielectric layer 18: 0.5 μm Si_3N_4

Distance between layer 17 to the lower side of gate electrode H_1: 0.1 μm

Source/Drain electrode S 1/D 1 height H_2: 0.2 μm

Gate electrode G 1 height H_3: 0.3 μm

Thickness of left part of T-shape gate electrode L_g1: 0.05 μm

Thickness of center part of T-shape gate electrode L_g2: 0.2 μm

Thickness of right part of T-shape gate electrode L_g3: 0.1 μm

[0035]

FIG. 2 shows simulated conduction band diagrams of the cross-line AA' within the proposed device of FIG. 1C. For comparison, a reference structure referred as a conventional HEMT, in which the delta-doped layer 13 is not included and the layers 11 and 16 are undoped layers, is also simulated. As shown, at the interface between the heterostructure formed by layers 14 and 15, the conduction band E_c dips below the Fermi level E_F at equbibrium as indicated as a first conduction band edge in the figure, which provides a main channel. The electrons are induced at the hetero structure due to the piezoelectric polarization and spontaneous polarization that form a 2DEG sheet charge region at the heterostructure. Further, in the proposed HEMT, electrons are also provided from the n-doped layer 16 to the main channel. In the conventional HEMT, the conduction band is relatively flat from the channel layer 14 to the UID buffer layer 12 since the delta-doped layer 13 and the doped back-barrier layer 11 are not introduced. As a result, the electrons in the 2DEG channel would easily spill over to the buffer layer 12 under bias

conditions, resulting in current flowing within the GaN buffer layer. The situation would be more serious when the gate length is small (under 0.2μm), in which the short channel effect would dominate in transistor operations. By introducing a heavily n-type delta-doped GaN layer 13, a minor channel can be created in the proposed HEMTs, which would greatly improve access resistance therefore enhance the linearity of the transconductance. The minor channel at a second conduction band edge provides additional electrons as carrier charges. Under the bias conditions during transistor operations, additional electrons in the minor channel are smoothly tranferred to the main channel in a wide range of biases applied to the gate and source electrodes. This carrier transfer mechanism greatly improves the linearity of the transconductance. In a case of the conventional HEMT, in which the n-type delta-doped layer 13 is not introduced, the electrons in the main channel become insufficient in the wide bias range, which results in a poor linearity of the transconductance as indicated in FIG. 3.

[0036]

In some embodiments, a distance of the first conduction band edge from the Fermi level is selected so as to be greater than a distance of the second conduction edge from the Fermi level at an equilibrium condition (non-biased condition).

[0037]

The n-doped layer 16 is formed for eliminating the influence of the delta-doped layer 13 on the 2DEG to provide a high carrier density in the major channel. And the back-barrier layer 11 is a p-type GaN, which pulls up the conduction band of buffer layer 12, resulting in much better electron confinement in both major and minor channel. The carrier spill-over and short

channel effect can be suppressed to some extents.

[0038]

FIG. 3 shows the simulated transfer characteristics at V_{ds}=3V of the proposed HEMT with a 18nm thick or 25nm thick i-n-i barrier layer (the layers 15, 16 and 17) and the conventional HEMT. The threshold voltages (V_{th}) of the conventional HEMT and the proposed HEMTs with 18nm and 25nm barrier layers are -5.8V, -7.9V and -10.8V, respectively. The threshold voltages of the proposed HEMTs shift to the negative side from the positive side. The shifts of the threshold voltages are due to the formation of the minor channels and more electrons residing under the gate electrode. FIG. 3 indicates that nearly flat transconductances (g_m) are achieved over a wide gate bias (V_{gs}) range of -7V to -1.5V, and -10V to -4.6V for the proposed HEMT with a 18nm or a 25nm barrier layer, respectively.

[0039]

The proposed HEMTs having a 25nm barrier layer and a 18nm barrier layer provide transconductances (g_m) with ultra-flat regions remaining close to respective great values of the g_m over a wide range of gate–source voltages (V_{gs}). The flat region of a transconductance reflects to a linearity of amplification of a transistor. Accordingly, the transconductance characteristics of the proposed HEMTs are desirable features for achieving linear operation of the large-signal power amplifiers.

[0040]

A transconductance of a conventional HEMT, which does not include the δ-doped layer, the doped back barrier layer and the doped barrier, is also shown in FIG. 3 for comparison. It is indicated that the transconductance of the conventional HEMT does not have a flat region, in contrast to the proposed

HEMTs, which show a superior linearity of the transconductance.

[0041]

FIG. 3 also indicates that the proposed HEMTs have other advantages in suppressing short channel effect as well as obtaining large on-state currents.

[0042]

FIG. 4A and FIG. 4B show I_d-V_d characteristics of the conventional HEMT and the proposed HEMT with a 18nm barrier layer (layers 15, 16 and 17), respectively. The center part of T-gate L_g2 is fixed at 0.2μm and a thermal model is enabled for both cases. A typical behavior is observed on the conventional HEMT with a small gate length: The loss of saturation in the output characteristic caused by the inability of the short gate to completely deplete the electric charge in the channel. This behavior is eliminated on the proposed HEMT due to the enhanced carrier confinement by adding a back-barrier layer 11. In addition, the maximum output currents at V_{gs}=0V for conventional HEMT and proposed HEMT are 1.97 A/mm and 1.52 A/mm, respectively. The higher output current presents on the proposed HEMT is due to an effect of a minor channel formed by by the delta-doping layer 13 and smooth carrir communication between the two channels achieved by optimizing the thickness of the channel layer 14.

[0043]

FIG. 5 shows current gain cutoff frequences as a function of V_{gs} of the conventional HEMT and proposed HEMTs with 18nm and 25nm barrier layers (layer 15, 16 and 17) for comparison. In this case, two proposed HEMT structures having a 18nm and a 25nm barrier layer with a gate length Lg_2=200nm are indicated.

[0044]

Device transfer characteristics were simulated in ac mode at V_{ds}=3V, and a transconductance g_m and gate capacitances C_{gd} and C_{gs} were extracted as a function of V_{gs}. The intrinsic cutoff frequency f_T was calculated by:

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1 + 2(C_{gd}/C_{gs})}}$$

[0045]

As shown in FIG. 5, plateau regions (flat regions) of g_m are obtained for the proposed HEMTs with 18nm and 25nm barrier layers over the gate biases V_{gs} from -7V to -2.5V and -10V to -5V. In contrast, the conventional HEMT does not have a plateau region of g_m and shows the peak at V_{gs}=-3.7V and drops significantly with V_{gs}. The highly flat f_T (plateau region of g_m) behaviors on the proposed HEMTs are due to the flat g_m achieved, and remain close to respective peak values when V_{gs} varies. These charateristics of f_T are desirable features for achieving linear operations of the large-signal power amplifiers.

[0046]

FIG. 6 shows the maximum intrinsic cutoff frequency $f_{T.max}$ as a function of center gate length L_g2. The intrinsic cutoff frequency f_T was calculated for each V_{gs} and the peak f_T was extracted. As shown, $f_{T.max}$ increases with decreasing the center gate length L_g2. This increase is due to smaller gate capacitances. In addition, a 20% lower $f_{T.max}$ is observed in the proposed HEMT with a 18nm barrier, since there is a trade-off between improving device linearity and enhancing $f_{T.max}$ in the proposed HEMT. FIG. 6 also indicates that further increase of $f_{T.max}$ would be achieved by scaling L_g2 down below 0.1μm, however, short channel effect would become more serious. It needs to further improve carrier confinement and optimize the ratio between L_g2 and a barrier thickness (region 15, 16 and 17) to suppress the short channel

effect.

[0047]

FIG. 7 shows the value of drain-induced barrier lowering (DIBL) (defined as V_{th}/V_{ds} and V_{ds} of 1 and 10 V used in the simulation) as a function of center gate length L_g2 in the conventional HEMT and the proposed HEMTs with or without the back barrier layer 11. The drain-induced barrier lowering (DIBL) is a short-channel effect in FETs referring originally to a reduction of a threshold voltage of the transistor at higher drain voltages, which needs to keep as low as possible for device operations. In the proposed HEMT structure without the back barrier layer 11, the DIBL is more serious than the conventional HEMT due to the lowering of the conduction band in the buffer layer 12 caused by the delta-doped layer 13. The back barrier layer 11 is essential to solve the trade-off between improving linearity and suppressing the short channel effect when the delta-doped layer 13 is introduced. Thanks to the back barrier layer 11 introduced in the proposed HEMT, the proposed HEMTs with a short gate show not only a much smaller value of DIBL but also a significant improvement in the subthreshold slope (shown in FIG. 3).

[0048]

A combination of the thickness of the unintentionally doped buffer layer 12 and the doping density of the back barrier layer 11 is chosen to achieve better carrier confinements as well as higher linearity of operations.

[0049]

FIG. 8 shows transconductance profiles of the HEMTs with and without delta-doped layer 13. No back barrier layer 11 added because of a comparison purpose.

[0050]

If the unintentionally doped (UID) layer 12 is too thin, and/or the doping density of the back-barrier layer 11 is too high, the conduction band in the location of the delta-doped layer 13 would be pulled up without forming a minor channel, resulting in a poor linearity of device operations. On the other hand, if the UID layer 12 is too thick, and/or the doping density of the back-barrier layer 11 is too low, the short channel effect would greatly affect the device performance of the HEMT due to the failure of channel carrier confinement. In some embodiments, the thickness of the unintentionally doped layer 12 can be chosen from 100nm to 200nm, and the doping density in the p-GaN back-barrier layer 11 can be chosen from 5×10^{16} cm^{-3} to 5×10^{17} cm^{-3}.

[0051]

The thickness of the UID channel layer 14 should can be designed as follows. With increasing in the thickness of the UID channel layer 14, the wider region of the transconductance (g_m) would be achieved. However, the transconductance g_m profile tends to show a two-peak behavior rather than a flat region when the thickness of the channel layer 14 increases beyond a threshold thickness. In some cases, the channel layer 14 can be in a range from 20nm to 30nm. It is due to the creation of a relatively wide barrier between the major channel and the minor channel, resulting in a double channel device that avoids the communication between the two channels. The preferred thickness of UID channel layer 14 may be fromed between 20nm and 30nm.

[0052]

The doping density of the delta-doped layer 13 should also be carefully designed to the improve device linearity. Too high or too low delta-doped density would result in a two-peak behavior rather than a flat region. A preferable range of the sheet doping density of delta-doped layer 13 may be

from 4×10^{12} cm^{-2} to 6×10^{12} cm^{-2}. Overall, the linearity performance and carrier confinement are determined by the combination of thicknesses of the unintentionally doped layer 12, the UID channel layer 14, and the doping densities of the back-barrier layer 11 and the delta-doped layer 13.

[0053]

The above-described embodiments of the present invention can be implemented in any of numerous ways. For example, the embodiments may be implemented using hardware, software or a combination thereof. When implemented in software, the software code can be executed on any suitable processor or collection of processors, whether provided in a single computer or distributed among multiple computers. Such processors may be implemented as integrated circuits, with one or more processors in an integrated circuit component. Though, a processor may be implemented using circuitry in any suitable format.

[0054]

Also, the embodiments of the invention may be embodied as a method, of which an example has been provided. The acts performed as part of the method may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

[0055]

Use of ordinal terms such as “first,” “second,” in the claims to modify a claim element does not by itself connote any priority, precedence, or order of one claim element over another or the temporal order in which acts of a method are performed, but are used merely as labels to distinguish one claim

element having a certain name from another element having a same name (but for use of the ordinal term) to distinguish the claim elements.

[CLAIMS]

[Claim 1]

A semiconductor device, comprising:

a semiconductor structure including a first doped layer for forming a carrier channel having a carrier charge;

a second doped layer having a conductivity type identical to a conductivity type of the first doped layer;

a barrier layer arranged in proximity to the semiconductor structure via the second doped layer, wherein the barrier layer includes a partially doped layer having a conductivity type opposite to the conductivity type of the second doped layer; and

a set of electrodes for providing and controlling the carrier charge in the carrier channel.

[Claim 2]

The semiconductor device of claim 1, wherein the second doped layer is a delta doping (δ-doping) layer having an n-type doping density greater than a doping density of the partially doped layer of the barrier layer.

[Claim 3]

The semiconductor device of claim 1, wherein the second doped layer is a delta doping (δ-doping) layer having an n-type doping density greater than a doping density of the first doped layer.

[Claim 4]

The semiconductor device of claim 1, wherein a thickness of the first doped layer is greater than a thickness of the second doped layer.

[Claim 5]

The semiconductor device of claim 1, wherein a thickness of the

partially doped layer is greater than a thickness of the second doped layer.

[Claim 6]

The semiconductor device of claim 1, wherein the second doped layer is a delta doping (δ-doping) layer having an n-type doping density ranging from 4×10^{19} cm^{-3} to 6×10^{19} cm^{-3}.

[Claim 7]

The semiconductor device of claim 1, wherein the second doped layer is arranged away from the carrier charge of the carrier channel in a range from 10nm to 30nm.

[Claim 8]

The semiconductor device of claim 1, wherein the carrier channel is formed of an undoped channel layer having a thickness in a range from 20nm to 30nm.

[Claim 9]

The semiconductor device of claim 1, wherein a doping density of the partially doped layer in the barrier layer is in a range from 5×10^{16} cm^{-3} to 5×10^{17} cm^{-3}.

[Claim 10]

The semiconuctor device of claim 1, wherein the barrier layer includes an unintentionally doped layer having a thickness ranging form 100nm to 200nm, and wherein the unintentionally doped layer is arranged between the second carrier channel and the partially doped layer.

[Claim 11]

The semiconductor device of claim 1, wherein the semiconductor structure comprises:

an undoped channel layer forming the carrier channel; and

undoped top barrier layers with the first doped layer disposed between the undoped top barrier layers for providing the carrier charge from the first doped layer to the carrier channel.

[Claim 12]

The semiconductor device of claim 11, wherein a material of the undoped channel layer and a material of the second doped layer are formed of an identical material.

[Claim 13]

The semiconductor device of claim 1, wherein the semiconductor structure is a semiconductor heterostructure including a III-V channel layer and a III-V barrier layer having the first doped layer, wherein a bandgap of the III-V barrier layer is greater than a bandgap of the III-V channel layer such that the carrier charge is provided to the III-V channel layer from the first doped layer of the III-V barrier layer.

[Claim 14]

The semiconductor device of claim 13, wherein a material of the III-V channel layer includes one or combination of gallium nitride (GaN) and indium gallium nitride (InGaN), and a material of III-V barrier layer includes one or combination of aluminum gallium nitride (AlGaN), indium aluminum nitride (InAlN), aluminum nitride (AlN) and indium aluminum gallium nitride (InAlGaN).

[Claim 15]

A semiconductor device, comprising:

a semiconductor structure including a channel layer and first barrier layers for providing a carrier charge wherein the channel layer is undoped layer and the first barrier layers consist of a undoped barrier, a first n-type

doped barrier and another undoped barrier;

a second n-type doped layer adjacent to the channel;

a second barrier layer arranged in proximity to the semiconductor structure via the second n-type doped layer, wherein the second barrier layer includes at least partially p-typed doped layer; and

a set of electrodes for controlling the carrier charge in the carrier channel.

[Claim 16]

A method for designing a semiconductor device, comprising:

selecting a III-V semiconductor heterostructure including a channel layer and first barrier layers for providing a carrier charge, wherein the channel layer is undoped layer and the first barrier layers consist of a undoped barrier, a first n-type doped barrier and another undoped barrier, wherein a bandgap of a material of the first barrier layers is selected so as to be greater than a bandgap of a material of the channel layer;

arranging a second n-type doped layer adjacent to the channel layer;

selecting a second barrier layer of a III-V semiconductor in proximity to the channel layer via the second n-type doped layer, wherein the second barrier layer includes a partially p-typed doped layer; and

providing a set of electrodes for controlling the carrier charge in the carrier channel.

[Claim 17]

The method of claim 16, wherein materials of the first and second barrier layers are selected such that a lattice mismatch between lattice constants of the first and second barrier layers and a lattice constant of the channel layer is in range of approximately ±1 percent of the lattice constant of

the channel layer.

[Claim 18]

The method of claim 16, further comprising:

selecting a substrate for supporting the second barrier layer and such that a thermal conductivity of the substrate is greater than at least one of materials of the channel layer and the first and second barrier layers.

[Claim 19]

The method of claim 16, wherein the channel layer has a first conduction band edge and a second conduction band edge, wherein at an equilibrium condition, a distance of the first conduction band edge from a Fermi level is selected so as to be greater than a distance of the second conduction edge from the Fermi level.

[Claim 20]

The method of claim 19, wherein the first conduction band edge is connected with a conduction band of one of the barrier layers and the second conduction band edge is connected with a conduction band of the second n-type doped layer.

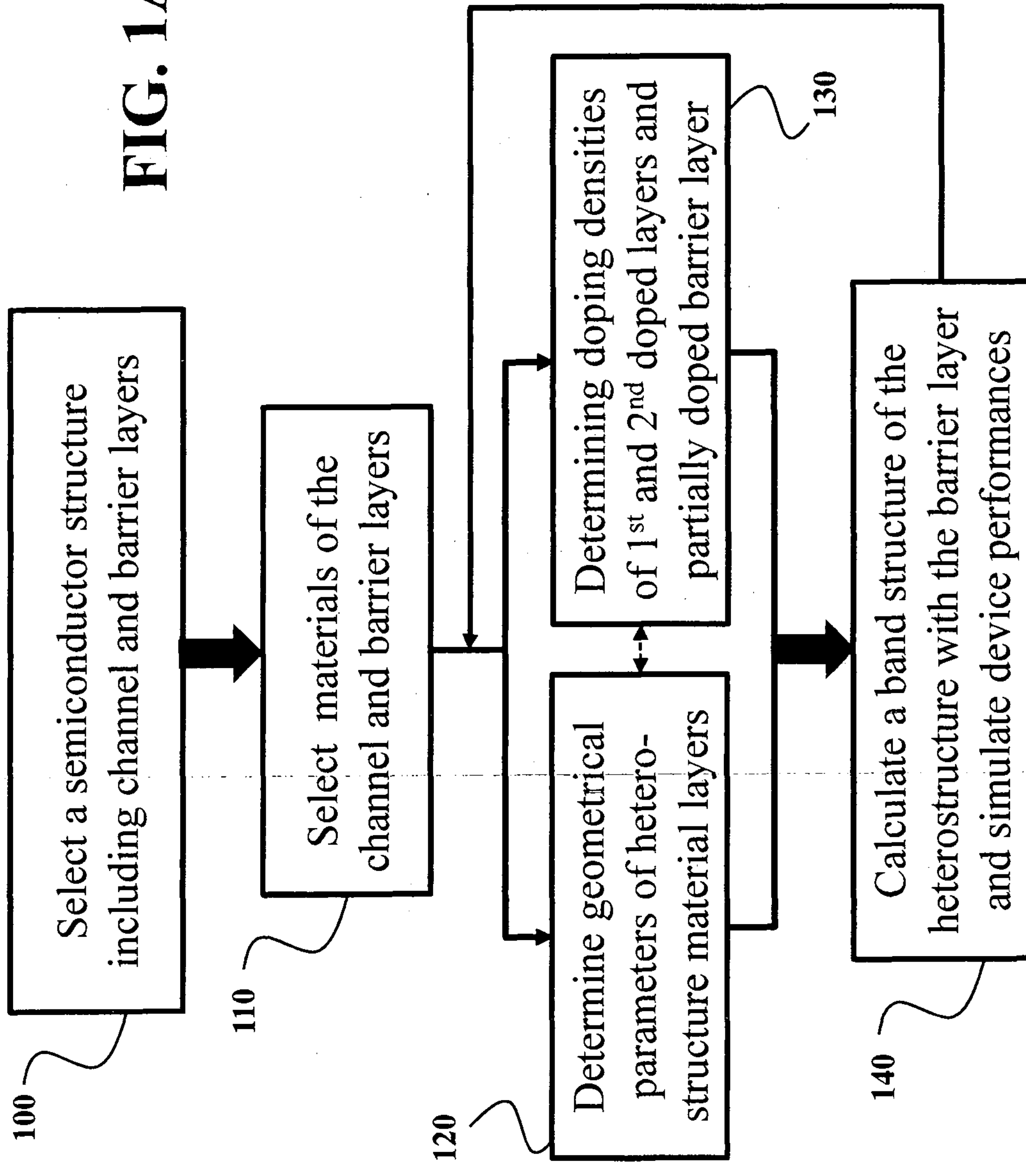

FIG. 1A

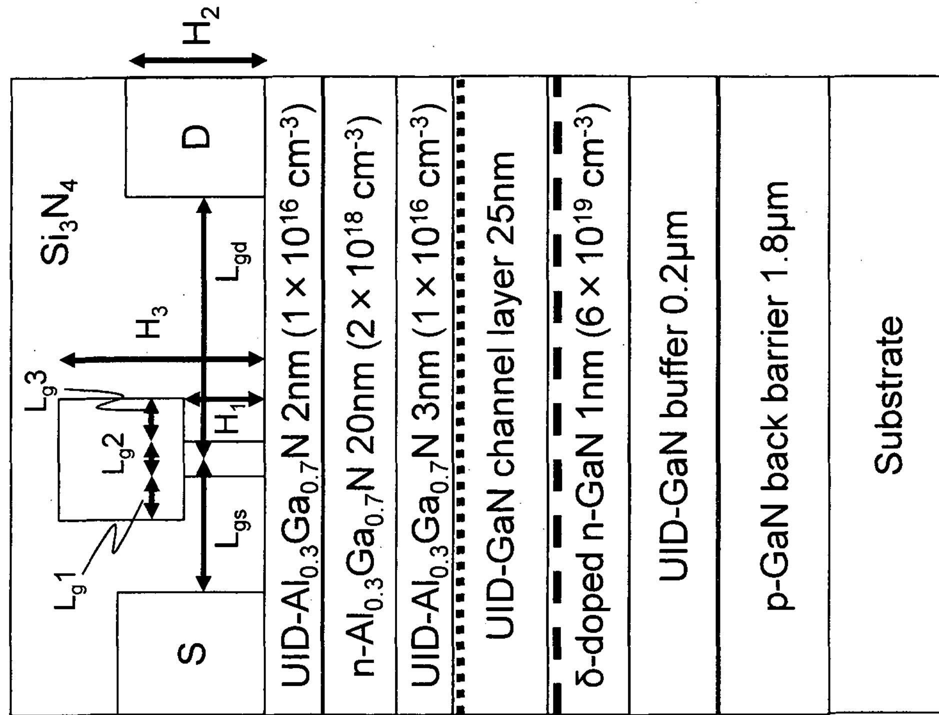

FIG. 1C

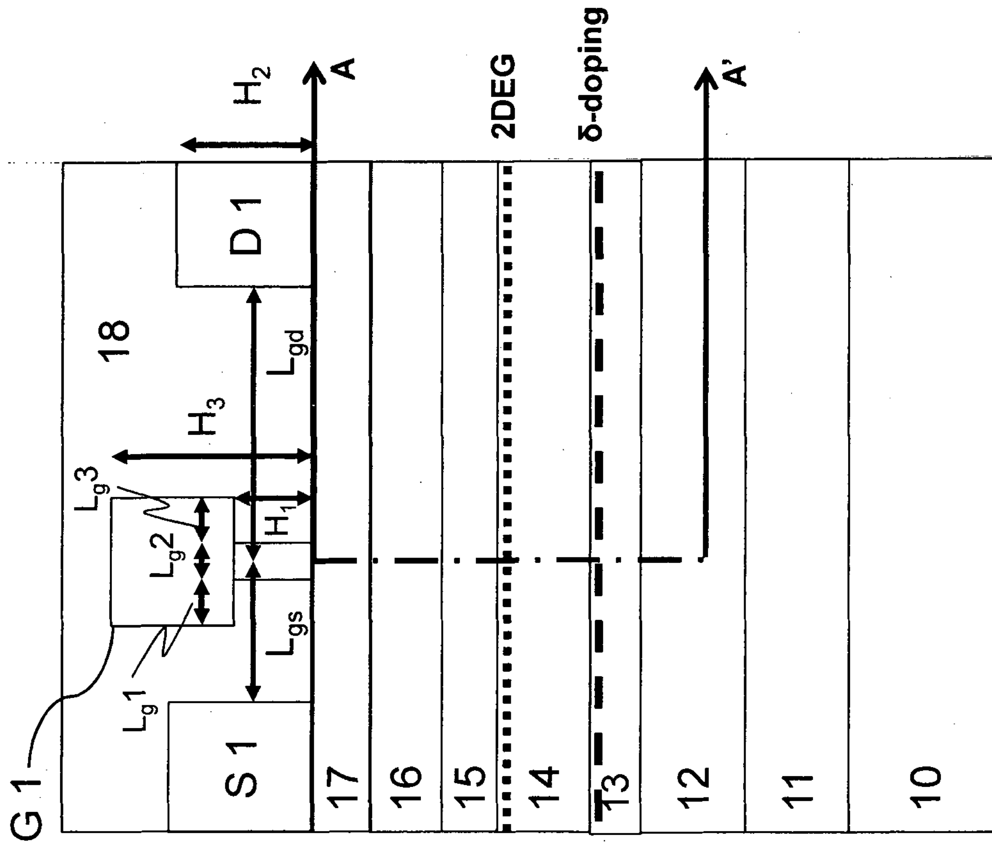

FIG. 1B

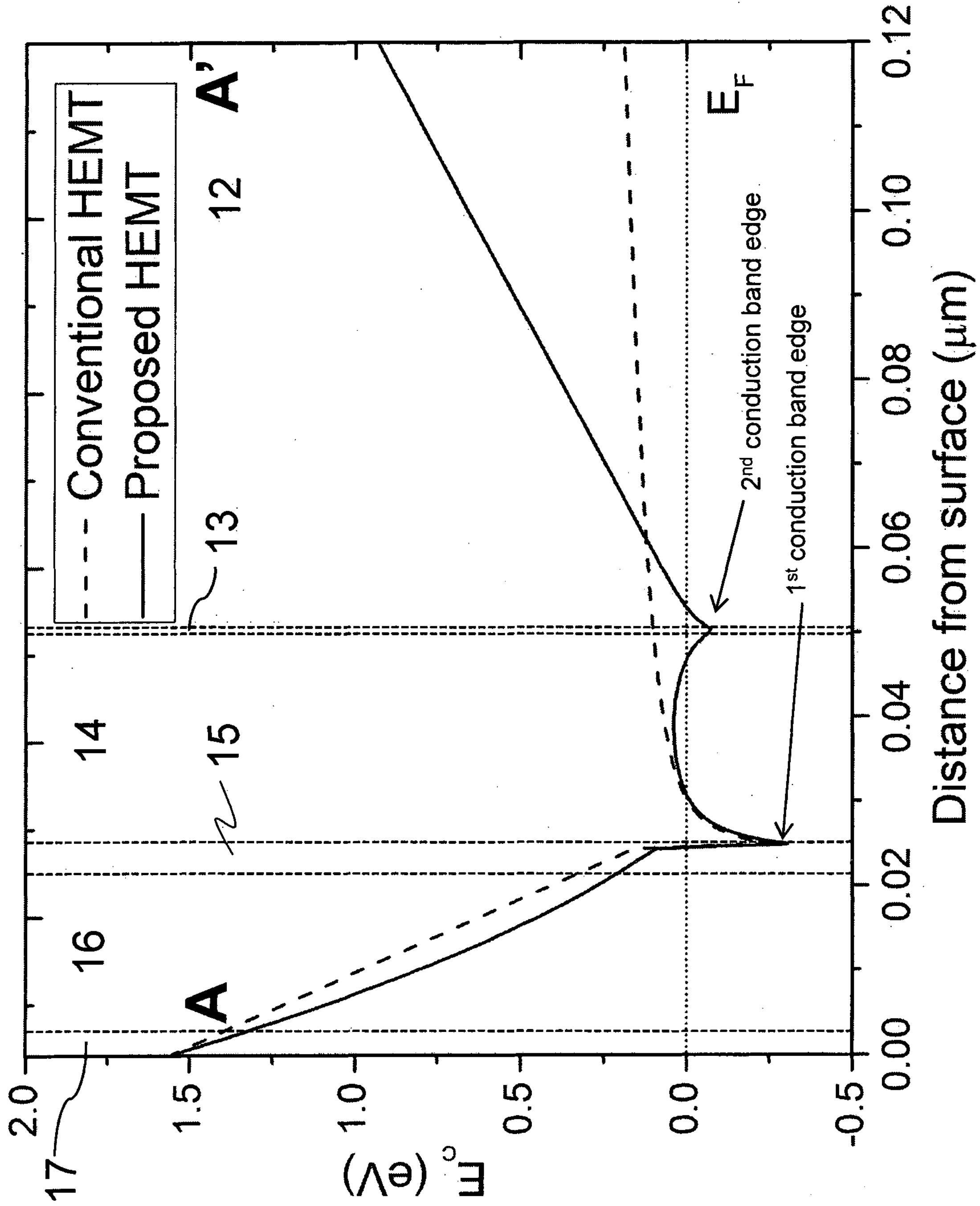

FIG. 2

Proposed HEMT, 25nm barrier
Proposed HEMT, 18nm barrier
Conventional HEMT

I_{ds} (A/mm)

0.0 0.5 1.0 1.5

g_m (S/mm)

0.0 0.2 0.4 0.6 0.8

V_{GS} (V)

-12 -10 -8 -6 -4 -2 0

FIG. 3

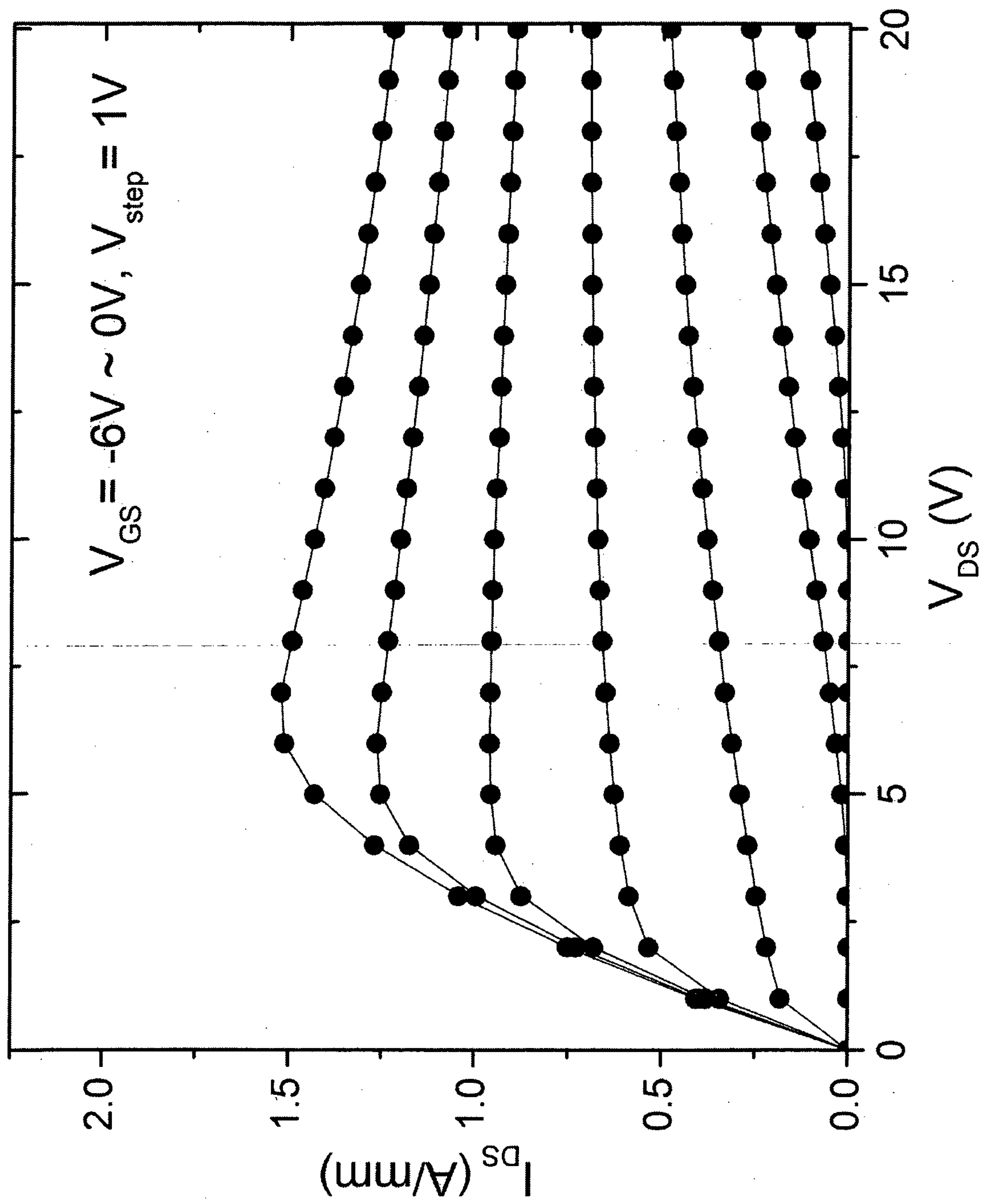

FIG. 4A

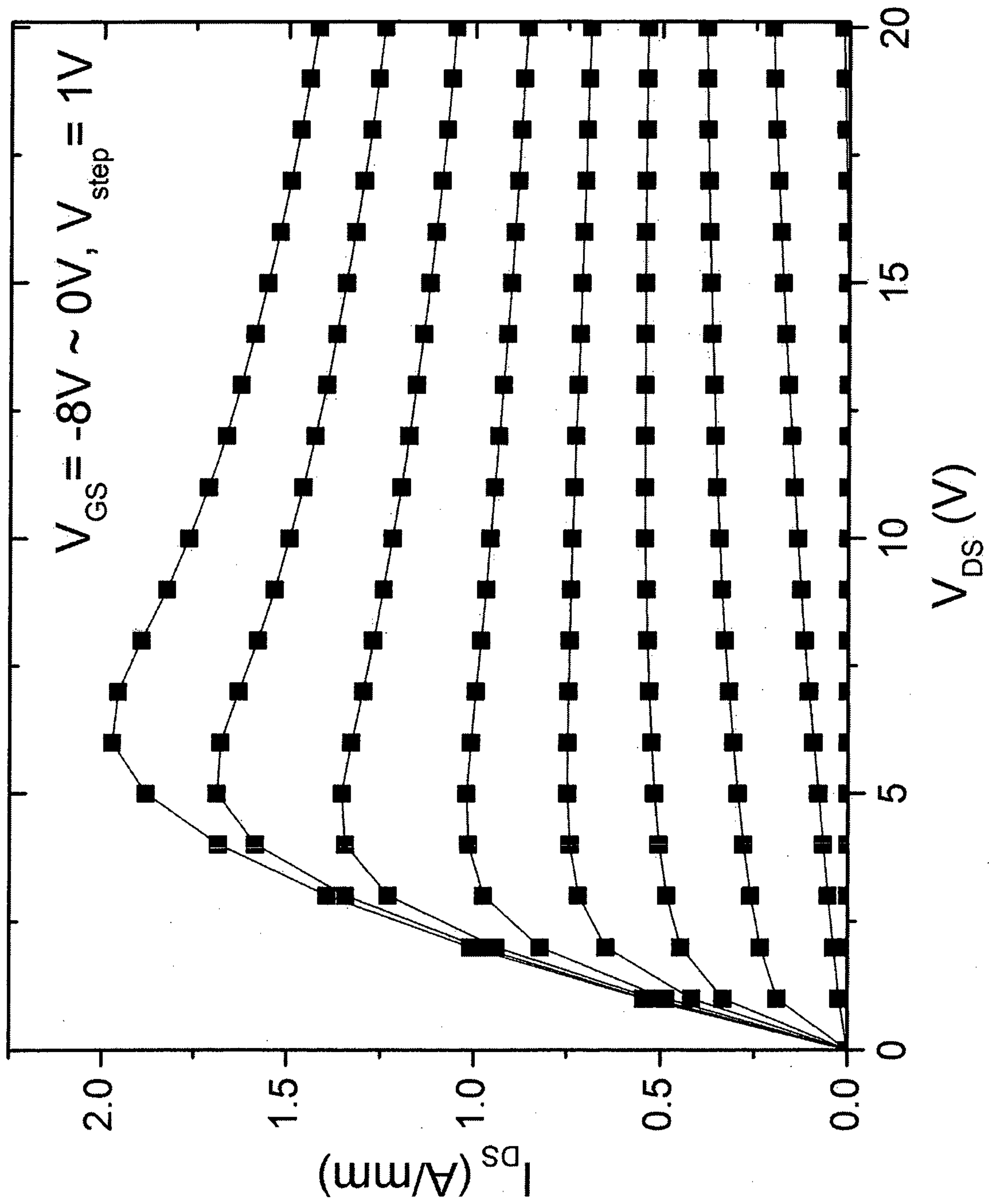

FIG. 4B

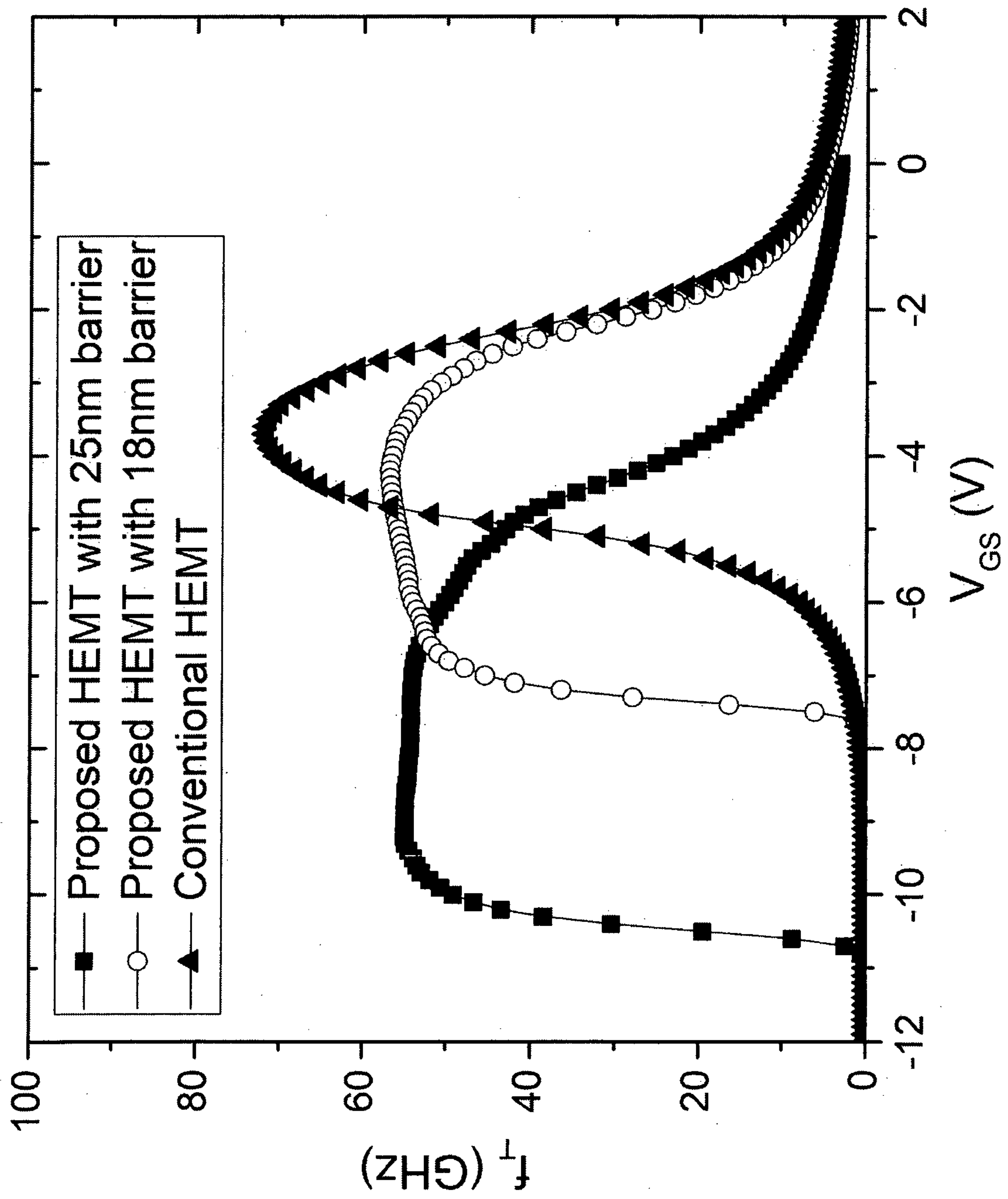

FIG. 5

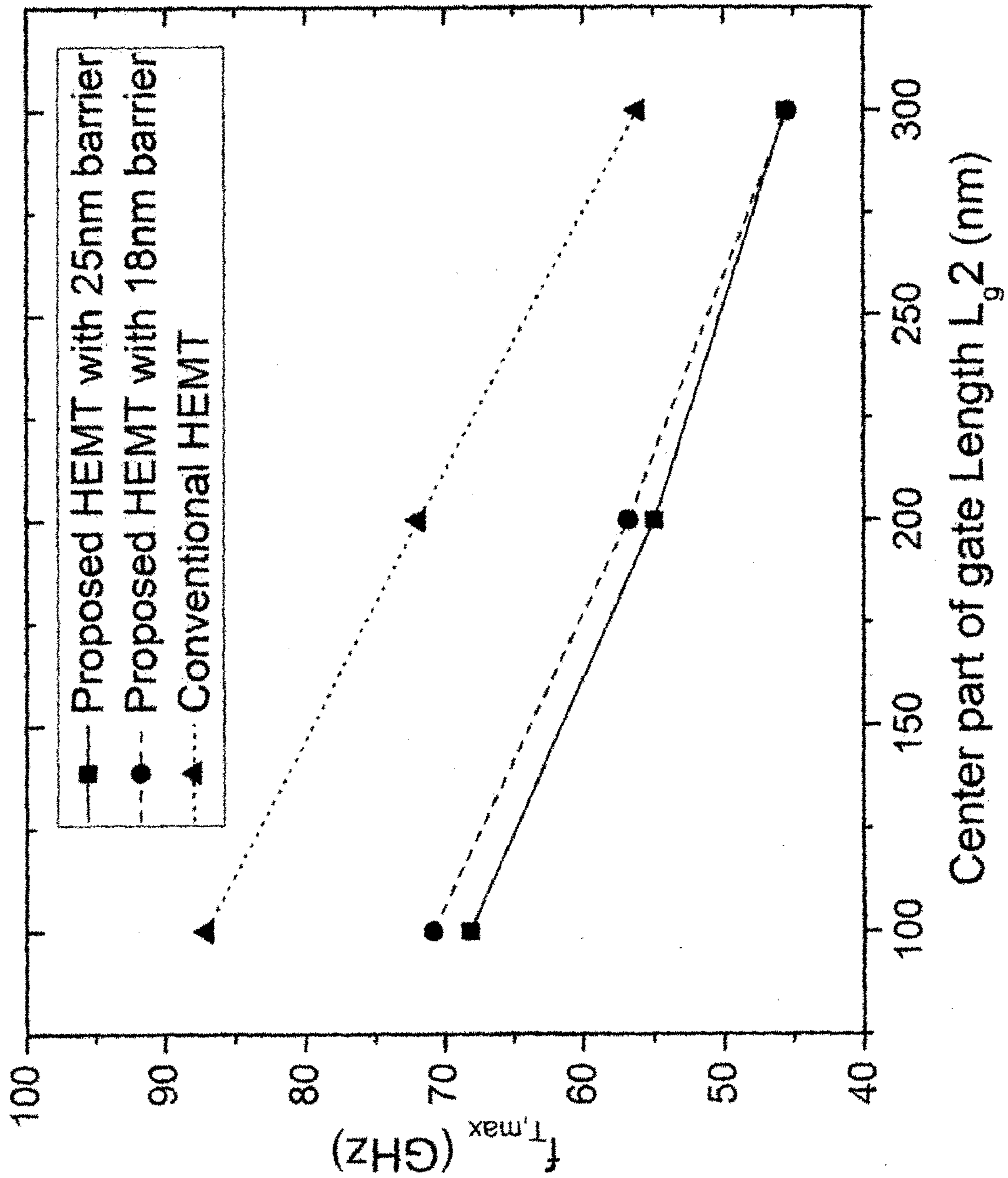

FIG. 6

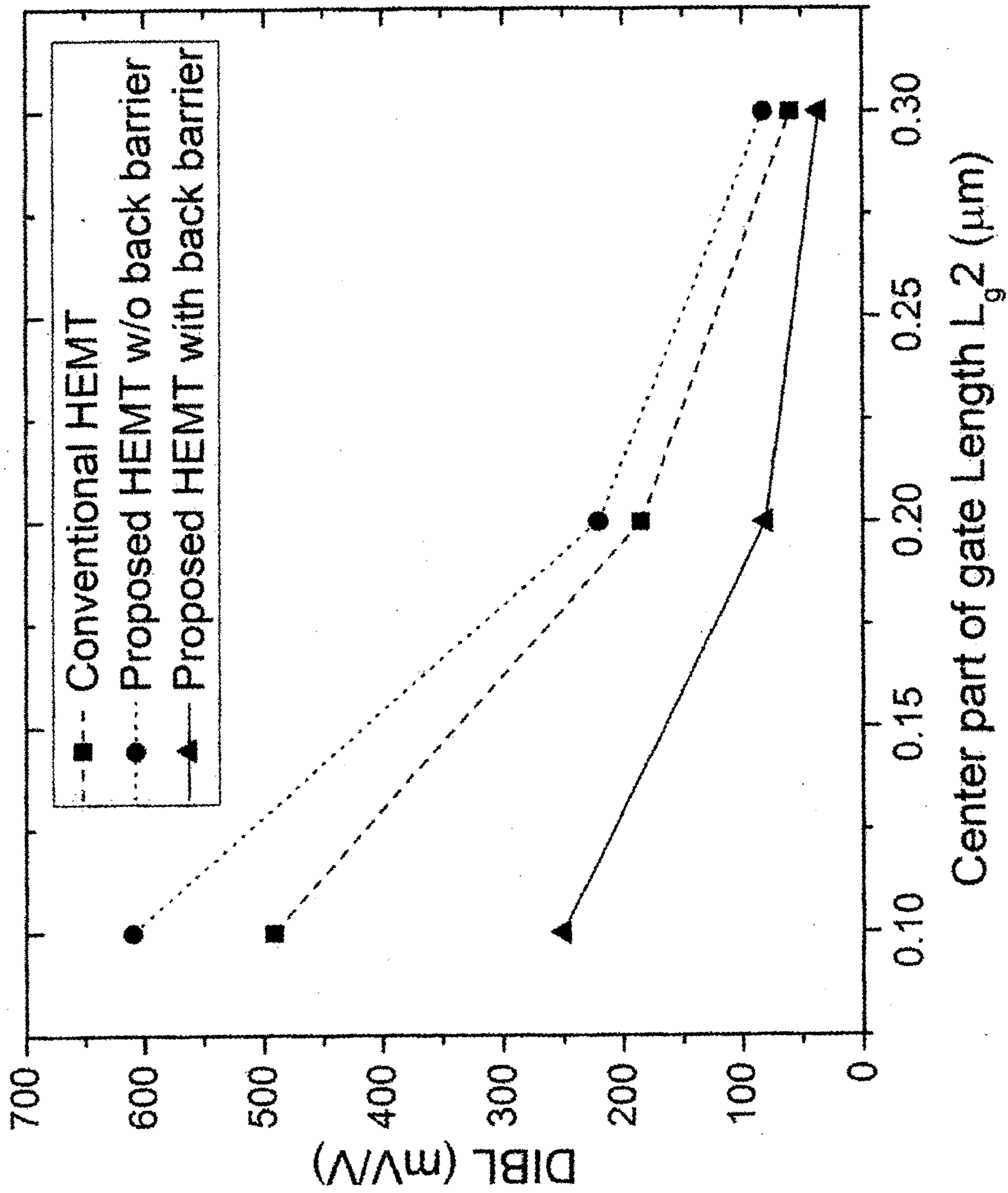

FIG. 7

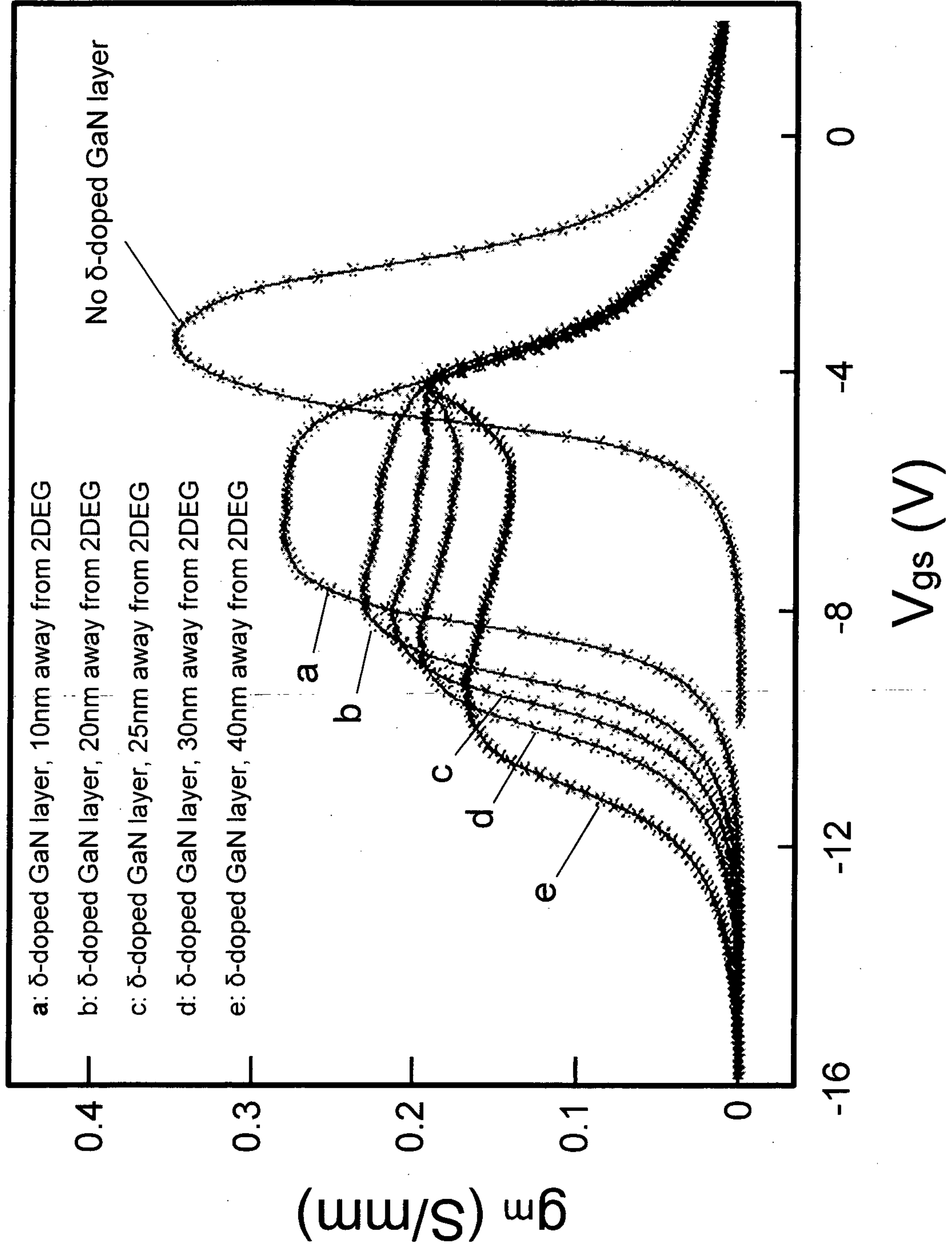

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/JP2017/036048

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/778 H01L29/36
ADD. H01L29/10 H01L29/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KR 2010 0089464 A (SILTRON INC [KR]) 12 August 2010 (2010-08-12) paragraphs [0029], [0037] - [0040]; figure 1	1-20
X	US 2006/255364 A1 (SAXLER ADAM W [US] ET AL) 16 November 2006 (2006-11-16) figures 1, 3-5 and associated text	1-20
A	US 2001/017370 A1 (SHEPPARD SCOTT THOMAS [US] ET AL) 30 August 2001 (2001-08-30) paragraphs [0024], [0026], [0028]; figure 1	11,15-20
A	US 2002/096692 A1 (NAKAMURA FUMIHIKO [JP] ET AL) 25 July 2002 (2002-07-25) figures 1, 12	3,10,11, 15-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
24 January 2018	02/02/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Moehl, Sebastian

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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