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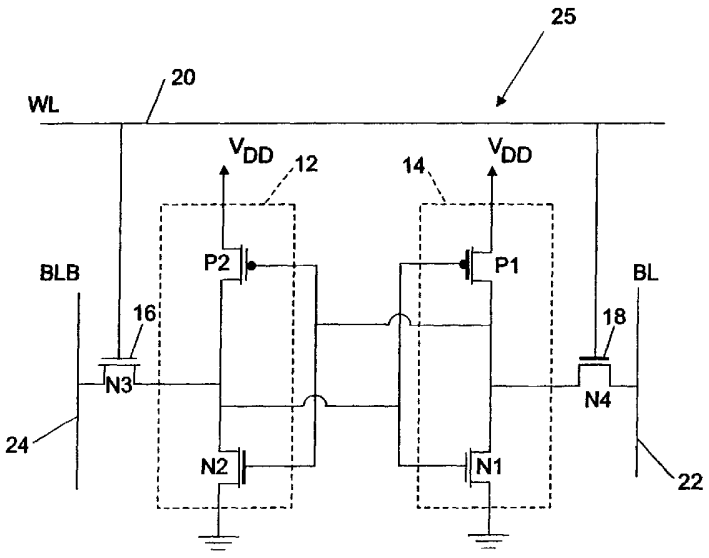
(54) Title: LOW LEAKAGE ASYMMETRIC SRAM CELL DEVICES



(57) Abstract: Asymmetric SRAM cell designs exploiting data storage patterns found in ordinary software programs wherein most of the bits stored are zeroes for data and instruction streams. The asymmetric SRAM cell designs offer lower leakage power with little impact on latency. In asymmetric SRAM cells, selected transistors are "weakened" to reduce leakage current when the cell is storing a zero. Transistor weakening may be achieved by using higher voltage threshold transistors, by varying transistor geometries, or other means. In addition, a novel sense amplifier design is provided that leverages the asymmetric nature of the asymmetric SRAM cells to offer cell read times that are comparable with conventional symmetric SRAM cells. Lastly, cache memory designs are provided that are based on asymmetric SRAM cells offering leakage power reduction while maintaining high performance, comparable noise margins, and stability with respect to conventional cache memories.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/25084

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G11C 11/00, 7/00, 07/02, 11/34
US CL : 365/154

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 365/ 181, 184, 188, 205, 207

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
East: US Pat, US PG PUB, EPO, JPO, DERWENT, and IBM_TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US Pat 5,363,328, aabstract, fig. 2 and col. 4, line 40 - col. 5, line 7	1, 2, 6-8, 9
X	US Pat 5,144,582 (Steele) 01 September 1992 (01.09.19920, figs 5, 8, col. 4, lines 51-64.	1-2, 6
Y	US 6,317,362 B1 (Nomura et al.) 13 November 2001 (13.11.2001), fig. 1, col. 3, line 12 - col. 4, line 40 and col. 5, line 38 - col. 6, line 63.	1-13
A	US 6,275,433 B1 (Forbes) 14 August 2001 (14.08.2001), fig. 6, col. 10, line 46 - col. 12, line 9.	1-13
Y,P	US 6,466,489 B1 (Ieong et al.) 15 October 2002 (15.10.2002), abstract, figs 5x, col. 8, lines 37-40	1-13
X	US 5,583,821 (Rose et al.) 10 December 1996 (10.12.1996), figs. 2, 3, see entire reference	1-2, 6
A	US 5,774,411 (Hsieh et al.) 30 June 1998 (30.06.1998), see entire reference	1-13
X	US 6,198,656 B1 (Zhang) 06 March 2001 (06.03.2001), see entire reference for asymetrical SRAM cell and asymetrical sense amp.	1-13
X	US 5,949,256 (Zhang et al.), 07 September 1999 (07.09.1999), see entire reference for application of asymmetrical sense amplifier	3-5, 9-13

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INTERNATIONAL SEARCH REPORT

C. (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
&	US 5,608,681 (Priebe et al.), 04 March 1997 (04.03.1997), see entire document.	3-5
X	US 5,355,333 (Pascucci), 11 October 1994 (11.10.1994), see entire document for application of asymmetrical sense amplifier	3-5, 6, 9-13