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(54) **Title:** DETERMINING RESISTIVE STATE OF MEMRISTORS

(57) **Abstract:** Example implementations relate to determining resistive state of memristors in a crossbar memory. For example, a method includes biasing each row of memristors and each column of memristors of the crossbar memory with a first voltage, and biasing a target column of memristors corresponding to the memristor with a second voltage to determine background current flowing through the target column of memristors. The method also includes increasing the first voltage for the reference array of memristors up to a third voltage such that the current flowing through the target column is a first current, and switching between the third voltage of the reference array of memristors and the first voltage of a target row of memristors corresponding to the memristor. The method also includes determining a second current flowing through the target column and comparing the second current with the first current to identify the resistive state of the memristor.



DETERMINING RESISTIVE STATE OF MEMRISTORS

BACKGROUND

[0001] A memristor, or a memristive device, is a resistive switching device that can be programmed to be in different resistive states, such as a low resistive state and a high resistive state. The different resistive states can be programmed by applying a programming energy, such as a voltage. After programming, the state of the memristor remains stable and can be read over a specified time period. Thus, memristors can be used to store digital data. For example, the low resistive state may indicate a logical high, or a binary "1", while the high resistive state may indicate a logical low, or a binary "0". The resistive state of a memristor can also be changed from a logical low to a logical high, and vice versa, to switch between the "0" storage and the "1" storage in the memristor.

BRIEF DESCRIPTION OF DRAWINGS

[0002] The detailed description is provided with reference to the accompanying figures. In the figures, the left-most digit(s) of a reference number identifies the figure in which the reference number first appears. The same numbers are used throughout the drawings to reference like features and components.

[0003] Fig. 1 illustrates an example system to determine resistive state of memristors in a crossbar memory, according to an example implementation of the present subject matter;

[0004] Fig. 2 illustrates a memory controller to determine resistive state of the memristors in the crossbar memory, according to an example implementation of the present subject matter;

[0005] Fig. 3 illustrates a current-voltage relationship of a memristor, while determining resistive state memristors in the crossbar memory, according to an example implementation of the present subject matter;

[0006] Fig. 4 illustrates an example circuit for determining resistive state memristors in the crossbar memory, according to an example implementation of the present subject matter;

[0007] Fig. 5 illustrates an example method of determining resistive state memristors in the crossbar memory, according to an example implementation of the present subject matter.

DETAILED DESCRIPTION

[0008] The present subject matter relates to techniques for reading stored digital data from an array based memory arrangement having memory devices in a crossbar configuration. The memory devices may be memristive devices, also referred to as memristors, hereinafter. In a crossbar configuration, the array based memory has a first set of substantially parallel nanowires on top, and a second set of substantially parallel nanowires, aligned at about 90° to the first set, at bottom. A memristor is disposed at each point of intersection of the top and the bottom nanowires to form a row-column arrangement of memristors. For the sake of explanation, the crossbar configuration of memristors may be referred to as a crossbar memory, and memristors in a row or a column of the crossbar configuration may be referred to as an array of memristors, hereinafter.

[0009] The memristors in the crossbar memory can be programmed to different resistive states such that each resistive state may represent digital data in binary form, i.e., in the form of 0's and 1's. Resistive state of a memristor may be indicative of a state of one bit of the digital data. In operation, by applying a predefined switching voltage across a memristor, the resistive state of the memristor may be changed for storing digital values, '1' or '0'. For example, the memristor can be set to a low resistive state to represent a binary '1' by applying the switching voltage, or can be set to a high resistive state to represent a binary

'0' by applying another voltage, for example, another switching voltage in the opposite polarity.

[0010] For retrieving the digital data stored in a crossbar memory, each memristor is read to determine its resistive state. For the sake of explanation, a memristor to be read has been referred to as a 'target memristor', hereinafter. Similarly, the row and column in which the target memristor lies, is referred to as target row and target column, respectively. A target memristor is selected uniquely by selecting the corresponding target row and the corresponding target column of the crossbar memory and a read voltage is applied across the target row and the target column to determine the resistive state of the selected memristor.

[0011] While the read voltage is applied across the target row and the target column, sneak currents, also referred to as background currents, develop in other rows and columns of the crossbar memory. Generation of the background currents, passing through the crossbar memory, make it difficult to read the resistance state of the target memristor accurately, thereby leading to read and/or write failure of the target memristor and the crossbar memory. Generally, selectors are used with the memristors of the crossbar memory to isolate each memristor from other memristors and to reduce the background currents developed within the crossbar memory. A selector may have a threshold voltage, which may be a minimum voltage that may activate the selector. In other words, the application of a voltage that is equal or larger than the threshold voltage of the selector may switch the selector from an insulating state to a conducting state.

[0012] A selector generally exhibits nonlinear current-voltage characteristics. Such characteristics of the selector can further vary from one selector to another due to the geometry and the local condition variations during the fabrication process. For example, a threshold voltage of the selector can vary from one array to another. These variations in current-voltage characteristics of different selectors result in supply of different voltages to different memristors even when a common voltage is applied across a target row or a target column. Therefore, an attempt to read different target memristor by supplying a second

voltage to the respective target row and the respective target column would result in generation of different currents by each target memristor. Such variations in generated current may result in erroneous determination of resistive states of the memristors, thereby resulting in errors in determination of the digital data.

[0013] According to an implementation of the present subject matter, techniques of determining resistive state of memristors in a crossbar memory are described. The crossbar memory may include memristors arranged in a crossbar configuration, such that each memristor may represent a binary value of '0' or '1'. With the implementation of the present subject matter, accurate resistive state of each of the memristor, within the crossbar memory, may be determined. Further, with the implementation of the present subject matter, resistive state of the memristors can be read without any errors even in situations where different selectors coupled with the memristors have variation in their current-voltage characteristics.

[0014] In an example implementation of the present subject matter, the crossbar memory may include a reference array of memristors from amongst the different rows of memristors. For example, a couple of rows of the crossbar memory may be identified to be reference array of memristors. In an implementation of the present subject matter, the reference array of memristors may include at least two staggered rows of memristors. Such reference array of memristors may be utilized for determination of conditions that result in generation of a first current, based on which the resistive state of a target memristor may be identified. The manner in which the resistive state of the target memristor may be identified has been explained with the following example implementations of the present subject matter.

[0015] According to an implementation of the present subject matter, to read the resistive state of the target memristor, a first voltage may be applied to the rows and columns of memristors of the crossbar memory. Further, the target column of memristors, corresponding to the target memristor may be biased to a second voltage. The biasing of the target column may lead to generation of background current in the crossbar memory due to potential difference between

the target column and the other rows of memristors. In said implementation of the present subject matter, the difference between the first voltage and the second voltage may be less than the threshold voltage of the selector coupled to the memristors, such that the selector may be in an insulating stage.

[0016] In an example, the generated background current may be allowed to stabilize and be subsequently measured to identify the value of background current being developed within the crossbar memory at the application of first voltage and the second voltage at different rows and columns of memristors.

[0017] Upon determination of the background current, the voltage supplied to the reference array of memristors may be increased from the first voltage to a third voltage, such that the current flowing from the target column is equal to a first current. The first current can be understood to be a combination of a bias current and the background current. The bias current may be a predetermined current corresponding to the memristors of the crossbar memory.

[0018] In an example implementation of the present subject matter, the bias current may be predetermined based on the resistive state of the reference array. For example, if the reference array of memristors is in a low resistive state, the bias current may be predetermined to a value, while the reference array of memristors is in a high resistive state, the bias current may be predetermined to another value.

[0019] Subsequent to the determination of the third voltage, the biasing of the target row may be switched from the first voltage to the third voltage, and the biasing of the reference array of memristors may be switched from the third voltage to the first voltage. The switching of the voltages may draw a second current from the target column, depending on the resistive state of the target memristor. Accordingly, the second current, upon its stabilization, may be determined.

[0020] In an example implementation of the present subject matter, the second current may be compared with the first current to determine the resistive state of the target memristor. For example, if the first current is based on a bias current where the reference array of memristors is in low resistive state, then a

difference, greater than a threshold value, between the second current and the first current would indicate that the target memristor is in high resistive state.

[0021] Therefore, the implementation of the described techniques allow for accurate determination of the resistive state of the target memristor. Also, since the reference array of memristors are in the vicinity of the target memristor, similar behavior of selectors can be observed, thereby providing reliable determination of the resistive state of the target memristor by comparison of first current corresponding to the reference array of memristors and the second current.

[0022] The above techniques are further described with reference to Fig. 1 to Fig. 5. It should be noted that the description and the figures merely illustrate the principles of the present subject matter along with examples described herein and, should not be construed as a limitation to the present subject matter. It is thus understood that various arrangements may be devised that, although not explicitly described or shown herein, embody the principles of the present subject matter. Moreover, all statements herein reciting principles, aspects, and implementations of the present subject matter, as well as specific examples thereof, are intended to encompass equivalents thereof.

[0023] Fig. 1 schematically illustrates a computing system 102, also referred to as a system 102, hereinafter, implementing a crossbar memory 104, according to an example implementation of the present subject matter. The system 102 may also implement a memory controller 106 to control the crossbar memory 104. The memory controller 106 may further include a voltage control unit 108 and an analysis unit 110 to determine resistive state of memristors in the crossbar memory 104.

[0024] The memory controller 106 may be an electrical device or component that, in addition to other functions, operates or controls the crossbar memory 104. The implementation of memory controller 106 may include hardware-based components, such as a microchip, chipset, or electronic circuit, such as a processor, microprocessor, or some other programmable device. For example, the memory controller 106 may include a circuit, such as the example circuit shown in Fig 4.

[0025] Similarly, the voltage control unit 108 may be a module, engine, or device that, in addition to other functions, manages voltages applied to different elements of the crossbar memory 104. The implementation of voltage control unit 108 may include hardware-based components, such as a microchip, chipset, or electronic circuit, such as a processor, microprocessor, or some other programmable device.

[0026] Further, the analysis unit 110 may be a module, engine, or device that, in addition to other functions, analyzes currents and voltages to determine resistive states of memristors within the crossbar memory 104. The implementation of the analysis unit 110 may include hardware-based components, such as a microchip, chipset, or electronic circuit, such as a processor, microprocessor, or some other programmable device.

[0027] In an example implementation of the present subject matter, the crossbar memory 104 may be a configuration of substantially parallel and substantially perpendicular lines with memristors and other components coupled between lines at cross-points. Such architecture is generally referred to as a crossbar configuration or cross-point array configuration.

[0028] Accordingly, the crossbar memory may include a plurality of rows of memristors 120-1, 120-2, ..., 120-N. For the ease of explanation, the rows of memristors 120-1, 120-2, ..., 120-N have been commonly referred to as rows of memristors 120, and have been individually referred to as a row of memristors 120. Similarly, the crossbar memory may include a plurality of columns of memristors 122-1, 122-2, ..., 122-M. For the ease of explanation, the columns of memristors 122-1, 122-2, ..., 122-M have been commonly referred to as columns of memristors 122, and have been individually referred to as columns of memristors 122.

[0029] Each memristor 124 may be coupled between a unique combination of one row of memristors 120 and one column of memristors 122. In other words, no memristor 124 share a row of memristors 120 and a column of memristors 124.

[0030] Each row of memristors 120 may be an electrically conducting line that carries current throughout the crossbar memory 104. The rows of memristors 120 may be in parallel to each other, generally with equal spacing. Similarly, column of memristors 122 may also be conducting lines parallel to each other, and perpendicular to the rows of memristors 120. Rows of memristors 120 and the column of memristors 122 may be made of conducting materials, such as platinum (Pt), tantalum (Ta), hafnium (Hf), zirconium (Zr), aluminum (Al), cobalt (Co), nickel (Ni), iron (Fe), niobium (Nb), molybdenum (Mo), tungsten (W), copper (Cu), titanium (Ti), tantalum nitrides (Ta_{Nx}), or titanium nitrides (Ti_{Nx}).

[0031] As explained before, the memristor 124 may be coupled between row of memristors 120 and the column of memristors 122, which may mean forming a continuous electrical connection between a row of memristors 120, the memristor 124, and the column of memristors 122.

[0032] In an implementation of the present subject matter, the memristor 124 may be an electrical component that may change resistance when a voltage is applied across it or a current is driven through it. Furthermore, the memristor 124 may “memorize” its last resistance. In this manner, each memristor 124 may be set to at least two states and may switch from a first state to a second state when a predetermined voltage is applied. In some examples, the predetermined voltage may be a minimum voltage that is to be applied to drive a current above a switching current that switches the memristor 124 from one state to the other. In some examples, the memristor 124 may include one or more of, a phase change memory, spin-transfer torque memory, or other forms of memory.

[0033] In some examples, each memristor 124 may be based on a variety of materials. For instance, the memristor 124 may be oxide-based, meaning that at least a portion of the memristor 124 is formed from an oxide-containing material. The memristor 124 may also be nitride-based, meaning that at least a portion of the memristor 124 is formed from a nitride-containing composition. Furthermore, the memristor 124 may be oxy-nitride based, meaning that a portion of the memristor is formed from an oxide-containing material and that a portion of the memristor 124 is formed from a nitride-containing material.

[0034] In some examples, the memristor 124 may be formed based on tantalum oxide (TaOx) or hafnium oxide (HfOx) compositions. In some other examples, materials of memristors may include titanium oxide, yttrium oxide, niobium oxide, zirconium oxide, aluminum oxide, calcium oxide, magnesium oxide, dysprosium oxide, lanthanum oxide, silicon dioxide, or other like oxides. Further examples include nitrides, such as aluminum nitride, gallium nitride, tantalum nitride, and silicon nitride. In addition, other functioning memristors may be employed in the practice of the implementations discussed herein.

[0035] In an example implementation, the memristor 124 may exhibit non-linear current-voltage characteristics. In other words, when an applied voltage is changed across the memristor 124, the current passing through the memristor 124 changes disproportionately to the change in voltage. In some examples, the memristor 124 may also include a selector (not shown) coupled in series with the memristor 124. The selector may be an electrical component placed in series with other components, such as the memristor 124, to control the overall electrical properties of the resulting combination. The selector may have a threshold voltage, which may be a minimum voltage that may activate the selector. In other words, the application of a voltage that is equal to or greater than the threshold voltage may switch the selector from an insulating state to a conducting state. Various selectors may be suitable for the implementations described herein. For example, selectors may be based on oxides, nitrides, oxy-nitrides, sulfides, selenides, tellurides, arsenides, and antimonides.

[0036] In an example implementation of the present subject matter, the crossbar memory 104 may include at least one row of memristors 120 as a reference array of memristors. For example, row of memristors 120-1 may be utilized as the reference array of memristors, also referred to as reference array of memristors 126.

[0037] The arrangement of the reference array of memristors may vary from one implementation to other. For example, in an implementation, the first row and the last row of memristors 120, of the crossbar memory 104, may be set as the reference array of memristors 126. In another implementation, one or more

staggered rows of memristors may be set as the reference array of memristors 126. In yet another implementation, middle rows of memristors 120, within the crossbar memory 104, may be set as the reference array of memristors 126. Therefore, the reference array of memristors 126 may be assigned in different ways to provide a suited representation of other memristors 124 of the crossbar memory 104.

[0038] The reference array of memristors 126 may be utilized by the memory controller 106 to determine reference value of voltages and currents, which may then be compared with voltage and currents through target column of the crossbar memory 104 to determine the resistive state of the memristors 124.

[0039] As defined earlier, for the sake of understanding, the memristor 124 for which the memory controller 106 determines the resistive state is referred to as the target memristor, and the row and column corresponding to the target memristor are referred to as the target row of memristors and the target column of memristors, respectively. For example, a memristor 'A' may be referred to as the target memristor and the row of memristors 120-2 would be referred to as the target row of memristors. Further, the column of memristors 122-2 may be referred to as the target column of memristors.

[0040] The manner in which the memory controller 106 may determine resistive state of the target memristors may be further explained with reference to forthcoming figures.

[0041] Referring to Fig. 2, the memory controller 106 of the system 102 may determine the resistive state of target memristor of the crossbar memory 104. According to an implementation of the present subject matter, the voltage control unit 108 may determine a voltage value for the reference array of memristors 126 that generates a first current through the target column of memristors 122, to determine the resistive state of the target memristor 'A'. To this end, the voltage control unit 108 of the memory controller 106 may apply a first voltage to each of the rows of memristors 120 and each of the columns of memristors 122. In an example implementation, the voltage control unit 108 may also apply a second voltage to the target column of memristors 122-2. In an example, the difference

between the first voltage applied to the rows and columns of memristors and the second voltage applied to the target column of memristors 122, may be less than a threshold voltage of the selector corresponding to the target memristor 'A'.

[0042] The application of first voltage to all the rows of memristors 120 and columns of memristors 122, other than the target column of memristors 122-2, and application of second voltage to the target column of memristors may generate background current in the crossbar memory 104. The background current may flow through the target column of memristors 122-2 and may be sampled. The background current can be understood as the sneak current which flows through the rows and columns of the crossbar memory 104. In an implementation of the present subject matter, upon application of the first voltage and the second voltage, current through the target column 122-2 may be sampled by the memory controller 106. The sampled current may then be stored as background current and be utilized for further reference.

[0043] The voltage control unit 106, upon sampling the background current, may modify the voltage applied to the reference array of memristors 126. In an example implementation, the voltage may be modified to a third voltage such that the current passing through the target column 122-2 is equal to a first current. In the example implementation of the present subject matter, the first current may be a combination of the background current and a bias current.

[0044] The bias current can be understood as a predetermined current that is smaller than a switching current of the target memristor 'A' to not to disturb any previously resistive state of the memristor. Also, to correctly distinguish between the high resistive state and low resistive state of the target memristor 'A', the bias current would be predetermined to a higher value than a current drawn at the application of a threshold voltage to the selector corresponding to the target memristor.

[0045] In one example implementation of the present subject matter, the memory controller 106 may sample the third voltage and store the third voltage for further reference. It would be noted that since the biasing of the reference array of memristors 126 with the third voltage may allow flow of the first current

through the target column 122-2, the voltage control unit 108 may modify the bias voltage of the reference array of memristors such that the current being sampled through the target column of memristors 122-2 is identified to be substantially equal to the first current.

[0046] In an example, the memristors of the reference array 126 may be set in a low resistive state, and accordingly, the voltage control unit 108 may determine the third voltage to be the voltage at which memristors 124 of the target column 122 allow flow of the first current, while the memristors of the reference array 126 are in a low resistive state. In another example implementation of the present subject matter, the memristors of the reference array 126 may be set in a high resistive state, and accordingly, the voltage control unit 108 may determine the third voltage to be the voltage at which memristors 124 of the target column 122 allow flow of the first current, while the memristors of the reference array are in a high resistive state.

[0047] Upon determination of the third voltage, the voltage control unit 108 may provide the third voltage to the target row of memristors 120-2, corresponding to the target memristor 'A'. The voltage control unit 108 may also change the voltage being supplied to the reference array of memristors to either the first voltage, or to a voltage, other than the third voltage.

[0048] The biasing of the target row of memristor 120-2 with the third voltage may drive a current through the target column 122-2. In one example implementation of the present subject matter, the voltage control unit 108 may sample such current as the second current.

[0049] It would be noted that in a crossbar memory 104, the current flowing through the target column of memristors 122 is dependent on the voltage applied to the target row of memristors and the target column of the memristors corresponding to the target memristor, along with the resistive state of the target memristor. Accordingly, the analysis unit 110 may compare the first current and the second current to determine the resistive state of the target memristor 'A'. For the sake of explanation, the analysis of the currents, by the analysis unit 110, to

determine the resistive state of the target memristor has been explained with reference to Fig. 3.

[0050] Fig. 3 includes a graph depicting current-voltage behavior of a memristor with a selector, corresponding to the target memristor. The Y axis of the graph depicts current while the X axis of the graph depicts the voltage. Accordingly, for an applied voltage, the current drawn from the memristor is plotted on the graph. As would be noted, the current-voltage behavior of the target memristor is non-linear. Referring to Fig. 3, line 302 depicts a low resistive state characteristic of the target memristor while line 304 depicts a high resistive state characteristic of the target memristor. Further, the line 306 depicts the switching behavior of the memristor from the low resistive state to the high resistive state. The voltage at which the switching may occur has been depicted as threshold voltage (V_{th}), and a switching current observed at the application of the V_{th} is depicted by I_{sw} .

[0051] It would be appreciated that while the target memristor shows current-voltage characteristics as depicted by line 302 when it is in its low resistance state, the target memristor would show current-voltage characteristics as depicted by line 304, while the memristor is in high resistive state.

[0052] As explained earlier, the reference array of memristors 126 are set in a low resistive state, and while the reference array of memristors 126 are in the low resistive state, the current-voltage characteristic is depicted by line 302. Accordingly, I_1 depicts the current flowing through the reference cell when the third voltage (V_3) is applied to the reference array of memristors 126. The total current through the target column, which is the sum of the I_{BIAS} and the background current from the unselected rows, is measured as the first current (I_1). While the third voltage is noted, the third voltage is also applied to the target row of memristors 120-2 to sample the second current (I_2). In such situation, the analysis unit 110 may compare I_1 and I_2 to determine the resistive state of the target memristor. Although I_2 has been depicted to be smaller than the I_1 , it may be noted that I_2 may also be sampled to be equal to I_1 , in some example implementations of the present subject matter.

[0053] It may also be noted that the voltage applied to the target memristor is in reference to the voltage applied to the target column of memristors. Accordingly, the voltages at which different currents are sampled, have been depicted in reference to the voltage of the target column of memristors (V_2).

[0054] In an example implementation of the present subject matter, if the analysis unit 110 determines the current I_1 and I_2 to be substantially similar, the analysis module 110 may determine the target memristor to be in the low resistive state. However, if the analysis module identifies the I_2 to be less than I_1 , the analysis module 110 may determine the target memristor to be in a high resistive state.

[0055] Therefore, based on the comparison of the first current and the second current, the analysis module 110 may determine the resistive state of the target memristor.

[0056] In Fig. 4, implementation of the memory controller 106 along with different components of the voltage control unit 108 and the analysis unit 110 is depicted. In an example, implementation, the crossbar memory 104 may include two staggered rows of reference array of memristors. For the sake of explanation, reference memristors of the reference array of memristors are depicted with a square block (■). Similarly, for the sake of explanation, the memristors of the target column of memristors are depicted with triangular blocks (▲), and the target memristor is depicted with a circular block (●).

[0057] As explained earlier, the crossbar memory 104 is coupled with the memory controller 106 that includes the voltage control unit 108 and the analysis unit 110. The voltage control unit 108 and the analysis unit 110 may include different circuits, such as a bias current circuit, a sampling circuit, and bias voltage circuit to provide different voltages to the rows and columns of memristors within the crossbar memory 104. All the rows of memristors and columns of memristors may first be biased with the first voltage (V_1), while the target column of memristors is biased with the second voltage (V_2). The sampling circuit may sample the background current in such condition, and store it for further reference. The reference array of memristors may then be biased up to the third

voltage (V_3) such that the current flowing through the target column of memristors is substantially equal the first current (I_1). As described earlier, the first current (I_1) may be a cumulative of the background current and the bias current. In an example implementation of the present subject matter, the bias current may be supplied by the bias current circuit.

[0058] Upon determination of the third voltage (V_3), the voltages between the reference array of memristors and the target row of memristors may be switched, such that the target row of memristors is biased with the third voltage (V_3). The application of the third voltage (V_3) to the target row of memristors may generate the second current (I_2). Thereafter, based on the comparison of the first current (I_1) and the second current (I_2), the resistive state of the target memristor may be determined.

[0059] Fig. 5 illustrates a method 500 to determine the resistive state of a memristor of a crossbar memory 104. The order in which the method 500 is described is not intended to be construed as a limitation, and any number of the described method blocks may be combined in any order to implement the method 500, or an alternative method. Furthermore, the method 500 may be implemented by electronic circuits, or processor(s) through any suitable hardware, or combination thereof.

[0060] It may be understood that steps of the method 500 may be performed by programmed units, such as the memory controller 106. The steps of the methods 500 may be executed based on instructions stored within such programmed units, as will be readily understood.

[0061] Referring to Fig. 5, in an implementation of the present subject matter, at block 502, each row of memristors and each column of memristors of a crossbar memory is biased with a first voltage. In an implementation of the present subject matter, at least one row of memristors is a reference array of memristors.

[0062] At block 504, a target column of memristors corresponding to a memristor to be read, is biased with a second voltage to determine background

current flowing through the target column of memristors. As described earlier, the memristor to be read is defined as a target memristor and, the row of memristors corresponding to the target memristor is referred to as the target row of memristors. Similarly, the column of memristors corresponding to the target memristor is referred to as the target column of memristors.

[0063] At block 506, the first voltage for the reference array of memristors is varied up to a third voltage, such that a current flowing through the target column is about a first current. In an example implementation, the first current may be a combination of the background current and a bias current.

[0064] At block 508, the third voltage of the reference array of memristors is switched with the first voltage of the target row of memristors, such that the target row of memristors is biased with the third voltage.

[0065] At block 510, a second current flowing through the target column, where the target column is biased with the second voltage. In an implementation of the present subject matter, the second current may be sampled and stored for further reference.

[0066] At block 512, the second current may be compared with the first current to identify the resistive state of the memristor. In an example implementation of the present subject matter, if the second current is substantially same as the first current, the memristor may be determined to be in a low resistive state. However, if the second current is identified to be smaller than the first current, the memristor may be determined to be in a high resistive state.

[0067] Although implementations of present subject matter have been described in language specific to structural features and/or methods, it is to be understood that the present subject matter is not necessarily limited to the specific features or methods described. Rather, the specific features and methods are disclosed and explained in the context of a few implementations for the present subject matter.

We claim:

1. A method for identifying resistive state of a memristor in a crossbar memory, the method comprising:
 - biasing each row of memristors and each column of memristors of the crossbar memory with a first voltage, wherein at least one row of memristors is a reference array of memristors;
 - biasing a target column of memristors corresponding to the memristor with a second voltage to determine background current flowing through the target column of memristors;
 - varying the first voltage for the reference array of memristors up to a third voltage such that a current flowing through the target column of memristors is about a first current, wherein the first current is a combination of the background current and a bias current;
 - switching between the third voltage of the reference array of memristors and first voltage of a target row of memristors corresponding to the memristor such that the reference array of memristors is biased with the first voltage and the target row of memristors is biased with the third voltage;
 - determining a second current flowing through the target column of memristors, wherein the target column of memristors is biased with the second voltage; and
 - comparing the second current with the first current to identify the resistive state of the memristor.
2. The method as claimed in claim 1, wherein memristors of the reference array of memristors are programmed to a low resistive state.
3. The method as claimed in claim 1, each memristor within the crossbar memory is coupled with a selector and the selector exhibits non-linear current-voltage behavior.

4. The method as claimed in claim 3, wherein a difference between the first voltage and the second voltage is less than threshold voltage of a corresponding selector coupled to the memristor.
5. The method as claimed in claim 1, wherein the comparing comprises:
 - computing a difference between the second current and the first current; and
 - identifying the resistive state of the memristor to be a low resistive state when the difference is below a threshold value.
6. The method as claimed in claim 1, wherein the comparing comprises:
 - computing a difference between the second current and the first current; and
 - identifying the resistive state of the memristor to be a high resistive state when the difference is above a threshold value.
7. A system comprising:
 - a crossbar memory, wherein the crossbar memory comprises rows and columns of memristors arranged in a crossbar arrangement, and wherein at least a row from amongst the rows of memristors is a reference array of memristors; and
 - a memory controller, coupled to the crossbar memory, for identifying resistive state of a memristor in the crossbar memory, wherein the memory controller comprises:
 - a voltage control unit to:
 - provide a first voltage to each of the rows of memristors and each column of memristors, and a second voltage to a target column of memristors corresponding to the memristor;
 - sample a background current flowing through the target column of memristors;

modify the first voltage for the reference array of memristors to a third voltage such that a current flowing through the target column is about a first current, the first current being cumulative of the background current and a bias current, wherein the bias current is a predetermined current; and

switch between the third voltage of the reference array of memristors and the first voltage of a target row of memristors corresponding to the memristor such that the reference array is biased with the first voltage and the target row is biased with the third voltage; and

an analysis unit coupled to the voltage control unit to:

determine a second current flowing through the target column, wherein the target column is biased with the second voltage;

compute a difference between the second current and the first current; and

identify the resistive state of the memristor to be a low resistive state when the difference is below a threshold value.

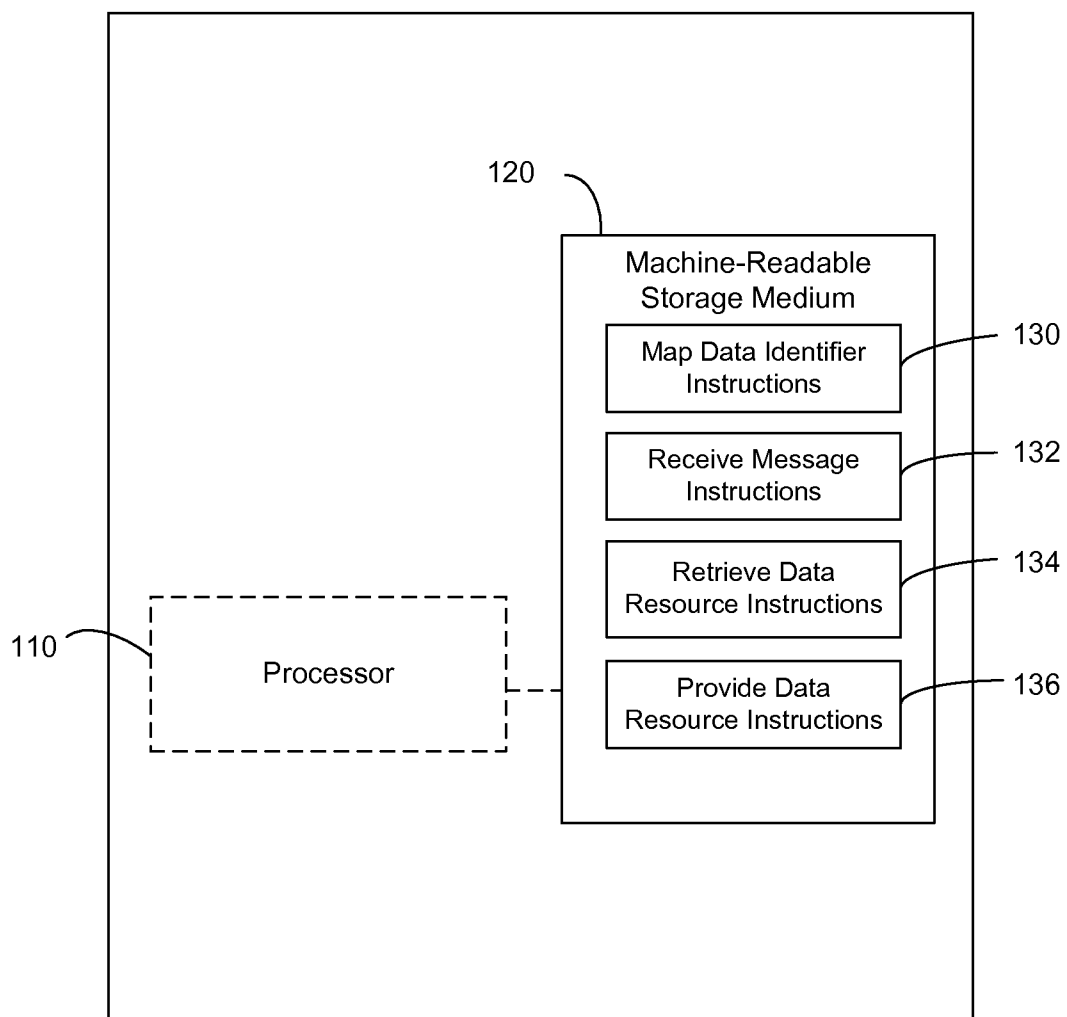
8. The system as claimed in claim 7, wherein the reference array of memristors include at least two staggered rows of memristors.
9. The system as claimed in claim 8, wherein memristors of the reference array of memristors are alternatively programmed to a low resistive state and a high resistive state.
10. The system as claimed in claim 7, wherein each memristor within the crossbar memory is coupled with a selector, wherein the selector exhibits non-linear current-voltage behavior, and wherein a difference between the

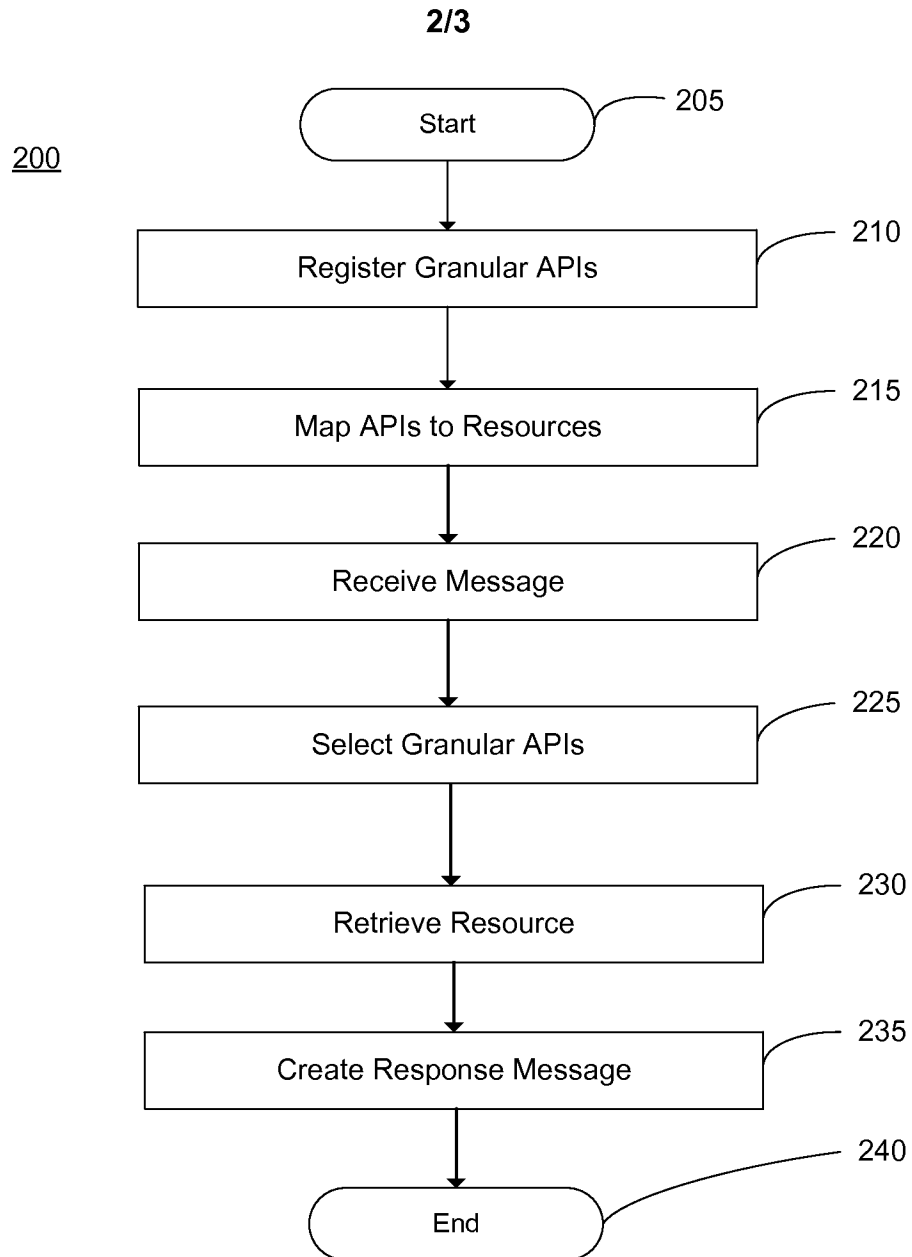
first voltage and the second voltage is less than threshold voltage of a corresponding selector coupled to the memristor.

11. The system as claimed in claim 7, wherein the reference array of memristors exhibit similar current-voltage characteristics as that of current-voltage characteristics of the memristor.
12. A memory controller of a crossbar memory, for identifying resistive state of a memristor in the crossbar memory, the memory controller comprising:
 - a voltage control unit to:
 - provide a first voltage to each of rows of memristors and each of columns of memristors, and a second voltage to a target column of memristors corresponding to the memristor;
 - sample a background current flowing through the target column of memristors;
 - increase the first voltage for a reference array of memristors to a third voltage such that the current flowing through the target column is about a first current, wherein the first current is a combination of the background current and a bias current, and wherein the bias current is a predetermined current; and
 - switch between the third voltage of the reference array of memristors and the first voltage of a target row of memristors corresponding to the memristor such that the reference array is biased with the first voltage and the target row is biased with the third voltage; and
 - an analysis unit coupled to the voltage control unit to:
 - sample a second current flowing through the target column, wherein the target column is biased with the second voltage; and
 - determine the resistive state of the memristor by comparing the second current with the first current.

13. A memory controller as claimed in claim 12, wherein each memristor of the crossbar memory is coupled with a selector, wherein the selector exhibits non-linear current-voltage behavior.
14. The memory controller as claimed in claim 12, wherein the analysis unit is further to identify the resistive state of the memristor to be a low resistive state when the difference is below a threshold value.
15. The memory controller as claimed in claim 12, wherein the analysis unit is further to identify the resistive state of the memristor to be a high resistive state when the difference is above a threshold value.

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100**FIG. 1**

**FIG. 2**

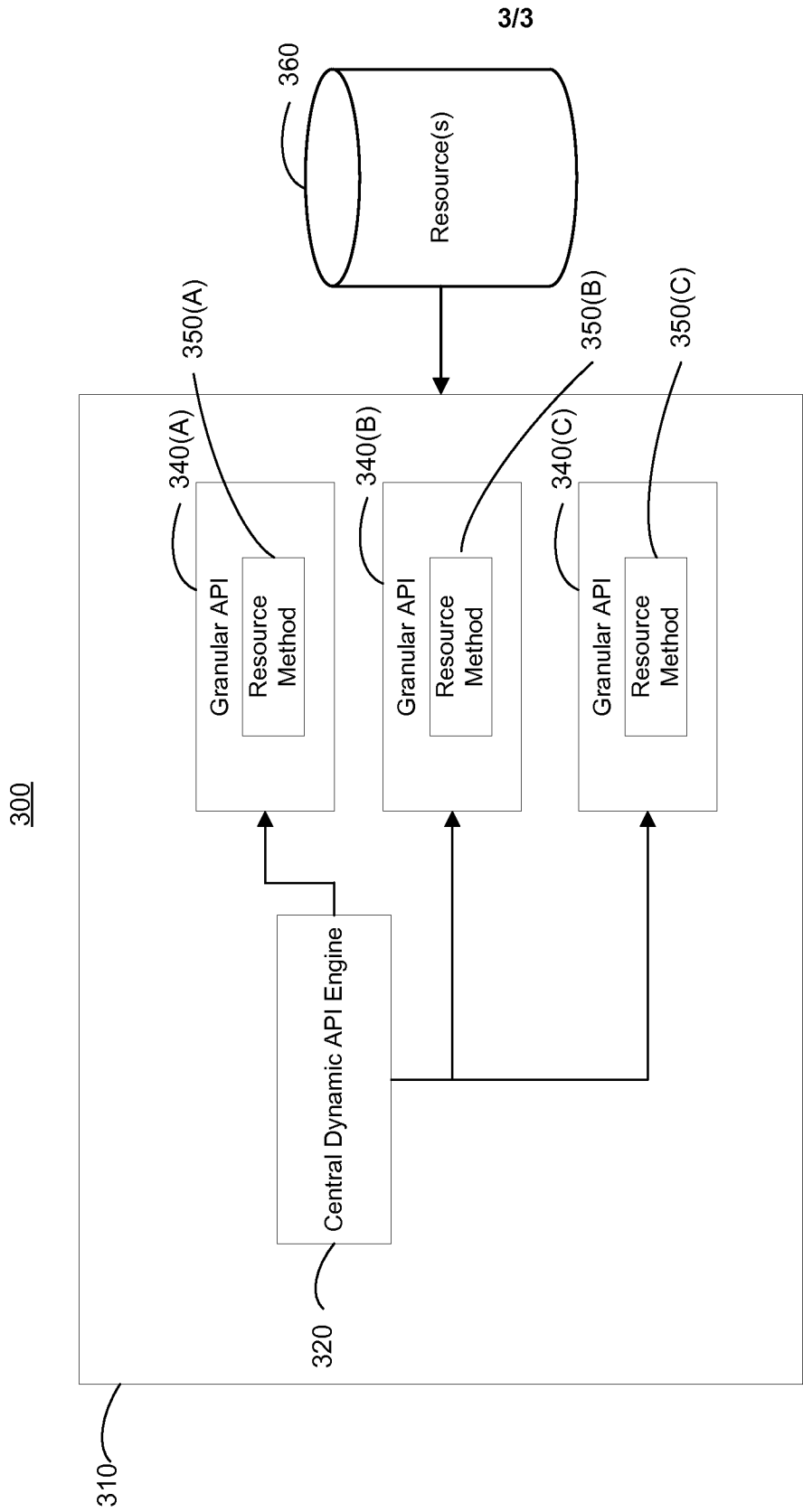


FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/026281**A. CLASSIFICATION OF SUBJECT MATTER****G11C 13/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 13/00; G11C 11/02; H03K 19/173; G11C 5/14; G11C 11/21; G11C 7/06; G11C 7/12; G11C 11/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: crossbar, array, reference, row, column, biasing, background, current, voltage, resistive, state, switching, comparing, memristor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0241075 A1 (YOOCHARN JEON) 28 August 2014 See paragraphs [0050]-[0051]; and figures 4A-4C, 5A-5C.	1-15
A	US 2014-0133211 A1 (HAGOP NAZARIAN et al.) 15 May 2014 See paragraphs [0032], [0035]; and figure 1.	1-15
A	US 2014-0028347 A1 (WARREN ROBINETT et al.) 30 January 2014 See paragraphs [0068]-[0069]; and figure 15.	1-15
A	US 2013-0010521 A1 (RICHARD CARTER) 10 January 2013 See paragraphs [0025]-[0026]; and figure 5.	1-15
A	US 2011-0286259 A1 (FREDERICK PERNER) 24 November 2011 See paragraphs [0030]-[0040]; and figure 2.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

14 January 2016 (14.01.2016)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/026281

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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