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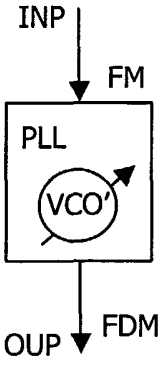
(54) Title: PHASE LOCKED LOOP DEMODULATOR WITH GAIN CONTROL



(57) Abstract: The invention relates to a demodulator to demodulate frequency-modulated signals FM including a phase locked loop PLL including at least a phase detector, a loop filter and a voltage controlled oscillator function VCO', characterized in that said voltage controlled oscillator function VCO' has modifiable gain. The invention allows to eliminate drawbacks presented by the conventional use of a complex gain modifiable amplifier at the input of demodulated signal processing means. Application: demodulation of modulated signals: wireless phone, home network.

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"Phase locked loop demodulator with gain control."

Field of the invention

The invention relates to the field of demodulation of modulated signals and amplification of demodulated signals obtained. More particularly, the invention relates to architecture of a circuit or a set of circuits realizing these functions. In its different applications, the invention notably relates to the reception of modulated signals like, for example, radio signals, telecommunication signals, telephone signals, audio base-band signals, wireless analog signals, video signals etc... The invention then also relates to any receiving system for such signals. Such receiving systems or devices can be a phone in wireless standard, DECT for example, a radio receiver, a wireless controller... Low cost wireless communications can also profit from the invention. The invention also proposes also a method for demodulating a modulated signal and amplifying the demodulated signal obtained.

Background of the Invention

Fig.1 presents a standard architecture of the demodulation of a modulated signal followed by an amplification of the demodulated signal obtained.

Such a standard architecture is for example implemented and described in the data sheet of UAA3515 from Philips semiconductors. In such architecture the demodulation is realized by a demodulator DEM using a conventional phase locked loop including a phase detector PDT, a loop filter LFI and a voltage controlled oscillator function VCO. Then the demodulated signal FDM is applied to a first amplifier stage G1 comprising a high gain amplifier G∝ and passive elements C1, R1 and R2. In integrated circuit technology, the use of passive elements generally implies the use of at least two connection pins P1 and P2 as shown in Fig.1. Then the output of the amplifier stage G1 is conventionally connected using an intermediate filter INF to a second amplifier stage G2 including a complex gain control amplifier GGC. This second amplifier stage is then connected to a processor PRO that processes the signal so that this signal can be used.

Such architecture presents the drawbacks that two connection pins are needed, external components are needed that are found on a PCB and moreover impose their time constant (this time constant is even greater than the R1C1 multiplication and has to be high so as not

to deform the audio signal), the presence is needed of a complex gain control amplifier that often deteriorate noise floor characteristics.

Summary of the Invention

It is an object of the present invention to propose a new architecture realizing the demodulation of modulated signals and the amplification of the demodulated signal obtained, which architecture does not have the drawbacks of the above-presented architecture and enables an enhanced quality for the signals finally used.

To this end, the invention proposes a demodulator to demodulate frequency-modulated signals including a Phase locked loop including at least a phase detector, a loop filter and a voltage controlled oscillator function VCO, characterized in that said voltage controlled oscillator function VCO has modifiable gain.

Said modifiable gain being implemented in the voltage controlled oscillator function VCO allows the frequency variations of the Frequency-modulated signals to be amplified. Consequently, the demodulated frequency-modulated signals are amplified when output from the phase locked loop. The modifiable gain can be implemented in various ways within the voltage controlled oscillator function.

According to an advantageous embodiment, the modifiable gain of said voltage controlled oscillator function VCO is modifiable using a programmable transconductance. In this advantageous embodiment the voltage controlled oscillator function VCO is controlled by the current output from a programmable transconductance. Said programmable transconductance allows the transformation of a voltage into current, said transformation generating a current as low as amplification desires. The less important said output current of said programmable transconductance is, the most important the amplification versus the frequency variations is. Said advantageous embodiment is particularly adapted to standard Intermediate Frequencies IF used in wireless communication: 450kHz, 10.7MHz.

According to a preferred embodiment of the invention, the programmable transconductance includes a fixed transconductance and a current multiplier, the output of said programmable transconductance being the output of a summation unit that sums a combination of at least one output of said multiplier.

In an advantageous implementation, said second current is taken from an intermediate output of said current multiplier using digitally programmable switches and preferentially MOS switches. The command of said MOS switches may then be provided by a digital

command on a given number of bits for example, said bits corresponding to the activation of said MOS switches.

The invention also relates to an electronic device able to receive frequency-modulated signals characterized in that demodulation of said signals is realized by a demodulator as described above. A method for demodulating frequency-modulated signals according to the invention is also proposed and includes the steps of applying said frequency-modulated signals at the input of a phase locked loop includes at least a phase detector, a loop filter and a voltage controlled oscillator function VCO, increases frequency variations by increasing gain of the voltage controlled oscillator function VCO having a modifiable gain and produces demodulated signals at the output of said phase locked loop.

Brief Description of the Drawings

The invention is described hereafter in detail with reference to the diagrammatic Figures wherein:

Fig.1 represents the standard architecture of a demodulator followed by amplification of demodulated signals according to the state of the art;

Fig.2 represents the new architecture of a demodulator with integrated gain control according to the invention;

Fig.3 represents an advantageous embodiment of means to modify the gain of the voltage controlled oscillator function according to the invention using a programmable transconductance;

Fig.4 represents a preferred use of the programmable transconductance;

Fig.5 illustrates a receiving device according to the invention;

Fig.6 is a block diagram of a method to demodulate a signal according to the invention, said block diagram also describing schematically the invention according to the abstract.

Description of embodiments

Fig.1 represents the standard architecture of a demodulator DEM followed by amplification of demodulated signals according to the state of the art in a specific second amplifier stage G2 including a complex gain control amplifier GGC. This Figure has been described above.

In an application, the demodulator receives frequency-modulated signal:

$FM = A \cdot \cos [2\pi f_c t + (f_{dev}/f_{mod}) \sin(2\pi f_{mod} t)]$.

f_{dev} is the deviation of the frequency, f_{mod} is the modulation frequency, f_c the central frequency of the Voltage Controlled Oscillator function VCO. Said central frequency f_c may be the inherent oscillation frequency of an oscillator included in the function VCO or a divided-by-M own oscillation frequency of an oscillator included in the function VCO, said inherent oscillation frequency being equal to several times M of the central frequency fc, and said oscillator being followed by a divide-by-M divider. In this case, the function VCO is considered to include the divider. Any structure known for a voltage controlled oscillator function VCO allowing having a frequency centered on the modulation frequency of the received signals can be implemented in the state of the art and in the invention. The invention includes supplementary features independently of such means to center the frequency of the voltage controlled oscillator function on the modulation frequency.

The audio processor PRO input signal is then:

(f_{dev}/K_{VCO}). G1 . G2 . sin $(2\pi f_{mod}t)$.

K_{VCO} is the gain of the VCO, this gain is fixed in the state of the art. G1 and G2 represent here the value gain of the two amplifier stages G1 and G2. The gain G2 is modifiable to adapt the amplification of the signal input in the audio processor PRO. The amplitude of the modification of the gain is advantageously centered on a mean value that corresponds to the most commonly required level of amplification by an exploitation system implemented at the output of the audio processor PRO. Such an exploitation system can be, for example, an earpiece with loudspeaker. The modification of the gain of amplifier stage G2 then enables to increase and decrease the gain around this mean value.

Such architecture presents some drawbacks. This architecture conventionally needs external passive elements R1, R2, C1 and two output pins in order to realize connections with those external passive elements. This architecture is limited in terms of settle time by the R1, C1 time constant. It has a major impact on the standby mode of a telephone for example. This architecture also needs a complex gain control amplifier GGC in the second amplifier stage G1. The DC offset of such a complex amplifier GGC limits the audio processor noise floor performances. As the gain control is used after an output pin, the signal level on this output pin is lower than in the invention. It makes the architecture less robust to the ground audio bounce on PCB. The invention allows to avoid all these drawbacks by providing a high-quality demodulation and amplification of the demodulated signals with a very simple new architecture.

The main function achieved by the invention is the demodulation of frequency-modulated signals with gain control of the output signals directly done in the phase locked loop within the voltage controlled oscillator function VCO.

Fig.2 represents the new architecture of a demodulator DEM' with integrated gain control according to the invention. The phase locked loop includes a voltage controlled oscillator function VCO' with modifiable gain. This modifiable gain allows to increase or decrease the gain of the voltage controlled oscillator function VCO' to adapt the level of the input of an audio processor PRO directly in the phase locked loop. Such a modifiable gain voltage controlled oscillator function VCO' can be implemented in various ways.

An advantageous embodiment is then proposed in Fig.3. This embodiment is particularly adapted to standard Intermediate Frequencies IF modulated signals (450kHz, 10.7MHz for example). The voltage controlled oscillator function VCO' includes a Relaxation Oscillator RO. Relaxation Oscillators are known to one skilled in the art. It is constituted by a capacitor, which is charged and discharged by a current. This charge and discharge represent the period of the oscillator. As seen hereinabove, said relaxation oscillator RO can, independently of the invention, be followed by a current divider to center the frequency of the voltage controlled oscillator function VCO' on the modulation frequency of the received signals. The functioning of the Relaxation Oscillator RO is controlled by the sum of two currents: I that conventionally enables the frequency of the VCO' to be centered on the modulation frequency and IGM coming from the phase locked loop and representing the frequency variations due to the frequency modulation. According to the invention, the current IGM passes through a programmable transconductance GM1. According to programmation data PG, the transconductance GM1 has the ability to provide a dependence on the programmation data PG, more or less important current IGM for a given voltage difference between the output of said loop filter and a reference voltage VREF. Then the gain of the voltage controlled oscillator function VCO' is proportional to the value of the programmable transconductance GM1. A particular and preferred use of the programmable transconductance GM1 will be presented in the following.

Fig.4 presents a preferred use of the programmable transconductance GM1. Said programmable transconductance GM1 includes a fixed transconductance GM2 conventionally known in the state of the art. The output of this fixed transconductance is a current IGM2. As explained above in the description of Fig.1, the amplification needed is generally dedicated to adapt the level of the input signal of the audio processor in order to obtain usable signals at the

output of this audio processor. According to the architecture of the invention represented in Fig.2, the audio processor input signal is equal to:

(f_{dev}/K_{VCO}). G . sin $(2\pi f_{mod}t)$.

K_{VCO} is modifiable here. Its value has to be centered on a value that enables a mean value that corresponds to the most commonly required level of amplification by an exploitation system implemented at the output of the audio processor PRO. The amplitude of variation of K_{VCO} can also be determined. For example, it is then considered in the following that the current IGM2 is a maximum value for IGM that corresponds to a maximum of K_{VCO} and consequently to a minimum of the audio processor input signal. Then, said programmable transconductance GM1 advantageously includes also a binary weighted current multiplier MUL presenting, in this particular example, a ratio $1/2^N$ with N = 1 to n at each of its outputs. Such a definition here means that a current equal to IGM2/ 2^n is provided on output n of the multiplier MUL, n being included in interval [1:N]. In this embodiment, conventional current multiplication means like current mirrors can be used in the invention. According to the preferred embodiment of the invention, switches S[n] are connected to the multiplier outputs. Said switches are then linked to a summation unit SUM. The switches are controlled by programmation data PG made of n bits. It has to be noted that, in Figure 4, a single output n and a single switch are represented for clarity. A summation unit SUM is connected to said switches. The summation unit SUM output current IGM is equal to IGM2 x $\sum_{n/PG} (1/2^n)$. For example, for programmation data PG in 3-bit-code 101, the output current IGM is: IGM2 x (1 x ½ + 0 x ¼ + 1 x 1/8) = 0.625 IGM2. Said outputs can also be permanently connected to the summation unit SUM.

The summation unit SUM can sum as many currents as there are permanently connected outputs, or outputs connected via a switch. Any combination of the outputs of the multiplier MUL is possible according to the invention. Any kind of output of a multiplier may also be used according to the invention. Multiplier MUL outputs may be any kind of multiple of the multiplier input current IGM2. Amplitude of modification of IGM is then defined by an interval of current, defined by limits that can be taken by the sum. Said interval is advantageously centered on the above-invoked mean value.

It may also happen that IGM2 is a minimum value that corresponds to the higher possible required gain. In this case, the multiplier, for example, provides IGM2 and the summation is an integer multiple of IGM2. A multiplier according to the invention can also provide any multiple of IGM2 at its outputs, said multiples being then summed according to the invention.

In this case, for example, $IGM = IGM2 \times \sum_{n/PG} 2^{n-1}$. For example, for a 3-bit-code 101, the output current is: IGM2 x (1 x 4 + 0 x 2 + 1 x 1) = 7 x IGM2.

According to the invention, the voltage controlled oscillator function VCO' includes a multiplier. The modification of the gain of the voltage controlled oscillator function VCO' is then realized using commutation of currents. The decreasing of the gain results in an amplification of the frequency variations in the Relaxation Oscillator VCO for a given signal. Consequently, the formed demodulated signal FDM is amplified in a customizable way regarding what would have been obtained with a fixed transconductance GM2. The change of the gain of the voltage controlled oscillator function VCO' generates a change in the output gain. It has to be noted that the gain of the amplifier of the first amplifier stage in the architecture of the state of the art has to be high (conventionally around 20) while the gain of G needs generally to be around 1 or 2.

The invention enables to reduce the time necessary to establish a balance in the receiving chain of a reception device compared to the state of the art. Effectively, the invention allows not to be limited by the time constant of external elements. The invention allows not to have external elements. The invention allows to reduce the silicon size required to realize functions of gain control amplification more than 100 times (no complex gain control amplifier). The invention allows not to need a complex gain control amplifier. The DC offset of the latter amplifier induces limitations in the noise floor performance of the audio processor. According to the invention, the DC offset of the amplification is removed before the audio processor by the AC coupling realized by the filter INF in Figure 2. As the gain control is implemented before the output pin, the signal level on this pin is higher than in the state-of-the-art architecture. It makes the architecture more robust relative to the ground audio bounce on PCB.

Consequently, the new architecture according to the invention provides an amplification equivalent to the one realized in the state of the art without having the drawbacks of the latter. In summary, the invention allows improvements concerning silicon occupation, audio quality, pinning count, external components and PCB area. System consumption is also reduced as the settling time of the receiver is reduced (no more time constant). Effectively, the standby time being reduced, the consumption is reduced.

Fig.5 illustrates a receiving device according to the invention. This Figure is a highly schematic representation of such a receiving device. It includes at least an antenna ANT at least able to receive frequency-modulated signals FM (Radio-Frequency RF or other), a

demodulator DEM' according to the invention, a receiving chain RX with a processing unit PROC. Said receiving chain RX and demodulator DEM' are advantageously connected to an audio system AUD and allow the use of demodulated signals FDM. This can be an earpiece with a loudspeaker LSP. Advantageously the receving device also includes a transmission chain TX advantageously linked to the processing unit PROC and to the audio system AUD. This is the case with telephone for example. Then the audio system also includes a microphone MIC for example.

Fig.6 is a block diagram of a method to demodulate a signal according to the invention, said block diagram also describing schematically the invention according to the abstract. A method for demodulating frequency-modulated signals according to the invention includes the step INP of applying frequency-modulated signals FM to an input of a phase locked loop PLL which includes at least a phase detector, a loop filter and a Voltage controlled oscillator function VCO', the step of amplifying frequency variations by modifying/decreasing gain of the voltage controlled oscillator function VCO', said voltage controlled oscillator function VCO' having a modifiable gain, the step OUP of producing demodulated signals FDM at an output of the phase locked loop PLL.

The architecture strictly as disclosed in Fig.2 and the embodiments presented in Figures 3 and 4 are not exclusive. Other alternative architectures and embodiments may be derived in accordance with principles of the invention defined in the Claims to accomplish the same objectives.

CLAIMS :

1. A demodulator to demodulate frequency-modulated signals including a phase locked loop including at least a phase detector, a loop filter and a voltage controlled oscillator function VCO, characterized in that said voltage controlled oscillator function VCO has a modifiable gain.

2. A demodulator as claimed in Claim 1, wherein the gain of said voltage controlled oscillator function VCO is modifiable using a programmable transconductance.

3. A demodulator as claimed in Claim 2, wherein the programmable transconductance includes a fixed transconductance, a current multiplier, the output of said programmable transconductance being the output of a summation unit that sums a combination of at least one output of said multiplier.

4. A demodulator as claimed in Claim 3, wherein said second current is taken from an intermediate output of said current multiplier using digitally programmable switches.

5. A demodulator as claimed in Claim 4, wherein said switches are MOS switches.

6. An electronic device able to receive frequency-modulated signals characterized in that demodulation of said signals is realized by a demodulator as claimed in one of the Claims 1 to 5.

7. A method for demodulating frequency-modulated signals including the steps of :
   - applying said frequency-modulated signals at the input of a phase locked loop including at least a phase detector, a loop filter and a voltage controlled oscillator function VCO,

- increasing frequency variations by increasing gain of the voltage controlled oscillator function VCO having a modifiable gain,
- producing demodulated signals at the output of said the phase locked loop.

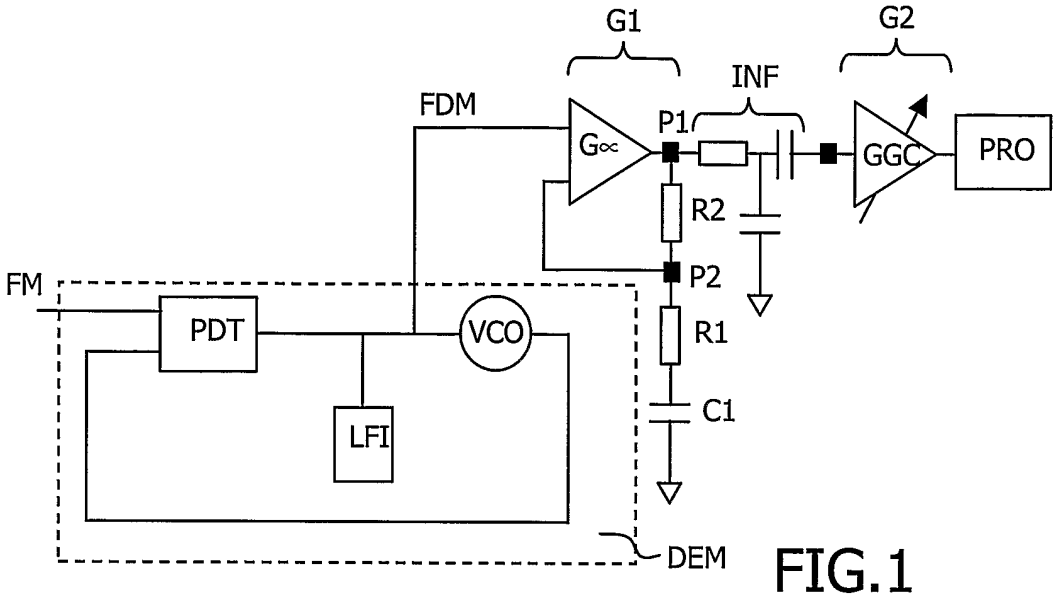
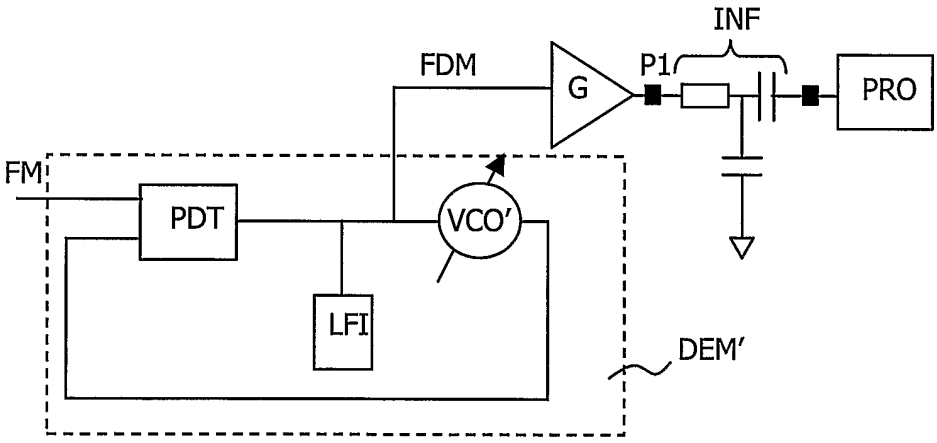

G1
G2
INF
FDM
P1
G∝
GGC
PRO
R2
P2
FM
PDT
VCO
R1
LFI
C1
DEM

FIG.1


INF
FDM
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P1
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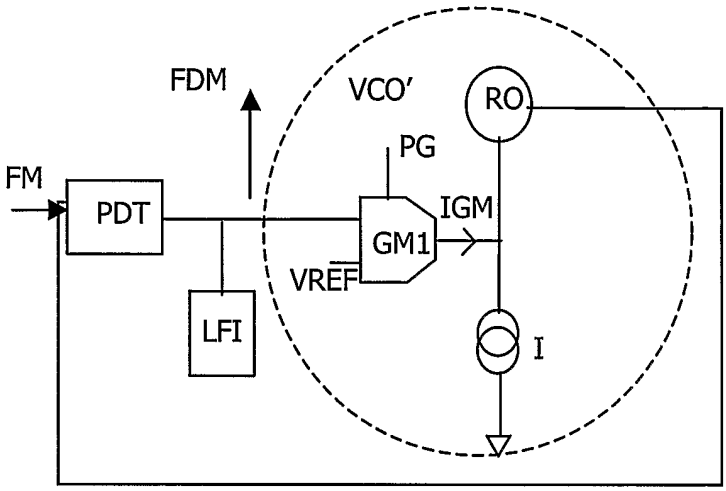
FM
PDT
VCO'
LFI
DEM'

FIG.2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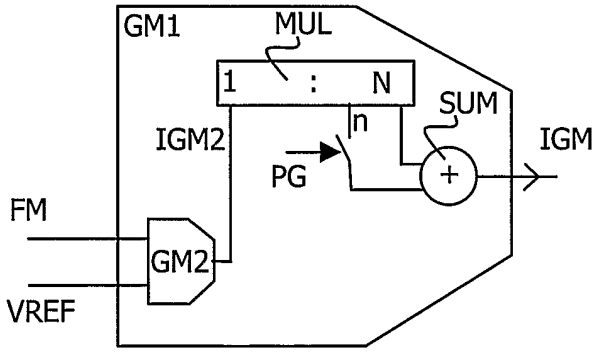
VCO'
RO
PG
FM
PDT
IGM
GM1
VREF
LFI
I

FIG.3


GM1
MUL
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n
SUM
IGM2
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IGM
FM
GM2
VREF

FIG.4

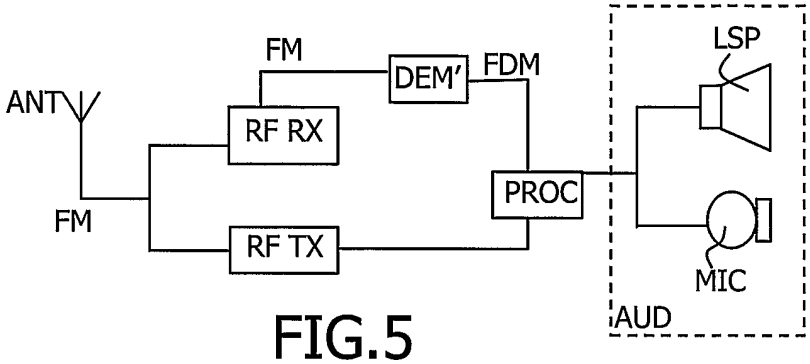
FM
DEM'
FDM
LSP
ANT
RF RX
PROC
FM
RF TX
MIC
AUD

FIG.5

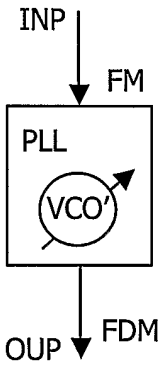
INP
FM
PLL
VCO'
OUP
FDM

FIG.6

INTERNATIONAL SEARCH REPORT

PCT/IB 03/04508

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03D3/24

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03D H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 459 653 A (J. SETO) 17 October 1995 (1995-10-17) column 2, line 61 -column 4, line 50; claim 10; figure 4B	1,7
Y	EP 0 645 891 A (SGS THOMSON MICROELECTRONICS LTD) 29 March 1995 (1995-03-29) column 2, line 30 -column 5, line 40; figures 1,2	1,7
A	US 6 404 294 B1 (I. SHA) 11 June 2002 (2002-06-11) column 3, line 21 -column 5, line 4; figures 5,7,8	1,7

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search	Date of mailing of the international search report
15 March 2004	23/03/2004

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 757 433 A (SGS THOMSON MICROELECTRONICS S.A.) 5 February 1997 (1997-02-05) column 5, line 6 - line 32 column 6, line 4 - line 39 column 7, line 24 -column 8, line 50; figures 1-3	1,7
A	EP 1 244 215 A (BROADCOM CORP.) 25 September 2002 (2002-09-25) column 8, line 34 -column 12, line 22; figures 3-8	1,7

INTERNATIONAL SEARCH REPORT

PCT/IB 03/04508

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5459653 A	17-10-1995	CA 2105107 A1	24-12-1994
EP 645891 A	29-03-1995	DE 69429485 D1	31-01-2002
		EP 0645891 A1	29-03-1995
		JP 7170176 A	04-07-1995
		US 5446411 A	29-08-1995
US 6404294 B1	11-06-2002	NONE	
EP 757433 A	05-02-1997	FR 2737626 A1	07-02-1997
		DE 69600658 D1	22-10-1998
		DE 69600658 T2	04-02-1999
		EP 0757433 A1	05-02-1997
		US 5828266 A	27-10-1998
EP 1244215 A	25-09-2002	US 2002135428 A1	26-09-2002
		EP 1244215 A1	25-09-2002
		US 2003206065 A1	06-11-2003