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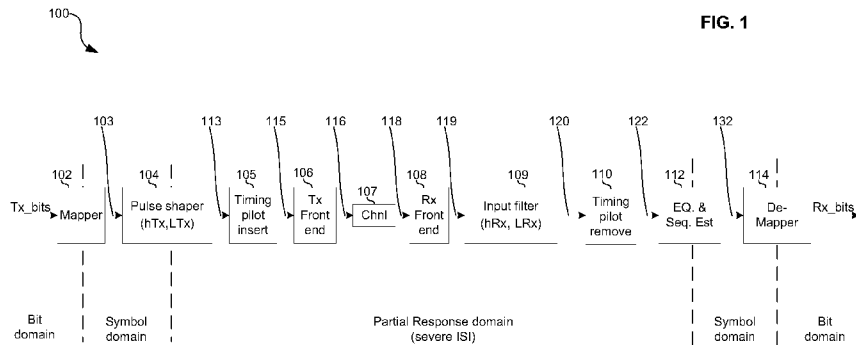
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(54) Title: HIGHLY-SPECTRALLY-EFFICIENT RECEIVER



(57) Abstract: A receiver may be operable to receive a QAM-based, inter- symbol correlated (ISC) signal at a signal-to-noise ratio of between 29 dB and 31dB and process the QAM- based, ISC signal to output estimated symbols at a symbol error rate of between 2×10^{-1} and 1×10^{-3} . The QAM-based, ISC signal may be a partial response signal generated by passing a first signal through a partial response pulse shaping filter. The partial response pulse shaping filter may provide greater capacity than a capacity achieved by passing the first signal through a root-raised-cosine-based pulse shaping filter. The receiver may comprises an input filter, and the processing of the QAM-based, ISC signal may comprises filtering the QAM-based, ISC signal via a filter configured to achieve a de-sired total partial response in combination with the partial response pulse shaping filter.

HIGHLY-SPECTRALLY-EFFICIENT RECEIVER

CLAIM OF PRIORITY

[0001] This patent application makes reference to, claims priority to and claims benefit from:

United States Provisional Patent Application Serial No. 61/662,085 entitled "Apparatus and Method for Efficient Utilization of Bandwidth" and filed on June 20, 2012;

United States Provisional Patent Application Serial No. 61/726,099 entitled "Modulation Scheme Based on Partial Response" and filed on November 14, 2012;

United States Provisional Patent Application Serial No. 61/729,774 entitled "Modulation Scheme Based on Partial Response" and filed on November 26, 2012; and

United States Provisional Patent Application Serial No. 61/747,132 entitled "Modulation Scheme Based on Partial Response" and filed on December 28, 2012.

[0002] Each of the above-identified applications is hereby incorporated herein by reference in its entirety.

INCORPORATION BY REFERENCE

[0003] This patent application also makes reference to:

United States Patent Application Serial No.: 13,754,964, titled "Low-Complexity, Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/755,972, titled "Multi-Mode Transmitter for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No.: 13/756,010, titled "Multi-Mode Receiver for Highly-Spectrally-Efficient Communications," and filed on January 31, 2013;

United States Patent Application Serial No. 13/756,079 titled “Pilot Symbol Generation for Highly-Spectrally-Efficient Communications,” and filed on January 31, 2013; and United States Patent Application Serial No. 13/755,052 titled “Pilot Symbol-Aided Sequence Estimation for Highly-Spectrally-Efficient Communications,” and filed on January 31, 2013.

[0004] Each of the above stated applications is hereby incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0005] Aspects of the present application relate to electronic communications.

BACKGROUND

[0006] Existing communications methods and systems are overly power hungry and/or spectrally inefficient. Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such approaches with some aspects of the present method and system set forth in the remainder of this disclosure with reference to the drawings.

BRIEF SUMMARY

[0007] Methods and systems are provided for low-complexity, highly-spectrally efficient communications, substantially as illustrated by and/or described in connection with at least one of the figures, as set forth more completely in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a block diagram depicting an example system configured for low-complexity, highly-spectrally-efficient communications.

[0009] FIG. 2 is a block diagram depicting an example equalization and sequence estimation circuit for use in a system configured for low-complexity, highly-spectrally-efficient communications.

[0010] FIG. 3 is a block diagram depicting an example sequence estimation circuit for use in a system configured for low-complexity, highly-spectrally-efficient communications.

[0011] FIG. 4 is a block diagram depicting an example metric calculation circuit for use in a system configured for low-complexity, highly-spectrally-efficient communications.

[0012] FIGS. 5A–5D depict portions of an example sequence estimation process performed by a system configured for low-complexity, highly-spectrally-efficient communications.

[0013] FIGS. 6A and 6B depict an example survivor selection process that is an alternative to the process depicted in FIG. 5D.

[0014] FIG. 7 is a diagram illustrating initialization of the sequence estimation process.

[0015] FIGS. 8A depicts an example implementation of the phase buffer shown in FIG. 3.

[0016] FIGS. 8B depicts an example implementation of the symbol buffer shown in FIG. 3.

[0017] FIG. 8C depicts contents of an example symbol buffer over a plurality of iterations of a sequence estimation process.

[0018] FIG. 8D depicts generated signals corresponding to the symbol buffer contents shown in FIG. 8C.

[0019] FIG. 9 depicts Symbol Error Rate (SER) vs. SNR for a receiver using aspects of this disclosure and for a conventional QAM receiver.

[0020] FIG. 10 depicts spectral efficiency for a receiver using aspects of this disclosure and a conventional DVB-S receiver.

DETAILED DESCRIPTION

[0021] As utilized herein the terms "circuits" and "circuitry" refer to physical electronic components (i.e. hardware) and any software and/or firmware ("code") which may configure the hardware, be executed by the hardware, and or otherwise be associated with the hardware. As used herein, for example, a particular processor and memory may comprise a first "circuit" when executing a first one or more lines of code and may comprise a second "circuit" when executing a second one or more lines of code. As utilized herein, "and/or" means any one or more of the items in the list joined by "and/or". As an example, "x and/or y" means any element of the three-element set $\{(x), (y), (x, y)\}$. As another example, "x, y, and/or z" means any element of the seven-element set $\{(x), (y), (z), (x, y), (x, z), (y, z), (x, y, z)\}$. As utilized herein, the term "exemplary" means serving as a non-limiting example, instance, or illustration. As utilized herein, the terms "e.g.," and "for example" set off lists of one or more non-limiting examples, instances, or illustrations. As utilized herein, circuitry is "operable" to perform a function whenever the circuitry comprises the necessary hardware and code (if any is necessary) to perform the function, regardless of whether performance of the function is disabled, or not enabled, by some user-configurable setting.

[0022] FIG. 1 is a block diagram depicting an example system configured for low-complexity, highly-spectrally-efficient communications. The system 100 comprises a mapper circuit 102, a pulse shaping filter circuit 104, a timing pilot insertion circuit 105, a transmitter front-end circuit 106, a channel 107, a receiver front-end 108, a filter circuit 109, a timing pilot removal circuit 110, an equalization and sequence estimation circuit 112, and a de-mapping circuit 114. The components 102, 104, 105, and 106 may be part of a transmitter (e.g., a base station or access point, a router, a gateway, a mobile device, a server, a computer, a computer peripheral device, a table, a modem, a set-top box, etc.), the components 108, 109, 110, 112, and 114 may be part of a receiver (e.g., a base station or access point, a router, a gateway, a mobile device, a server, a computer, a computer

peripheral device, a table, a modem, a set-top box, etc.), and the transmitter and receiver may communicate via the channel 107.

[0023] The mapper 102 may be operable to map bits of the Tx_bitstream to be transmitted to symbols according to a selected modulation scheme. The symbols may be output via signal 103. For example, for an quadrature amplitude modulation scheme having a symbol alphabet of N (N-QAM), the mapper may map each $\text{Log}_2(N)$ bits of the Tx_bitstream to single symbol represented as a complex number and/or as in-phase (I) and quadrature-phase (Q) components. Although N-QAM is used for illustration in this disclosure, aspects of this disclosure are applicable to any modulation scheme (e.g., amplitude shift keying (ASK), phase shift keying (PSK), frequency shift keying (FSK), etc.). Additionally, points of the N-QAM constellation may be regularly spaced (“on-grid”) or irregularly spaced (“off-grid”). Furthermore, the symbol constellation used by the mapper may be optimized for best bit-error rate performance that is related to log-likelihood ratio (LLR) and to optimizing mean mutual information bit (MMIB). The Tx_bitstream may, for example, be the result of bits of data passing through a forward error correction (FEC) encoder and/or an interleaver. Additionally, or alternatively, the symbols out of the mapper 102 may pass through an interleaver.

[0024] The pulse shaper 104 may be operable to adjust the waveform of the signal 103 such that the waveform of the resulting signal 113 complies with the spectral requirements of the channel over which the signal 113 is to be transmitted. The spectral requirements may be referred to as the “spectral mask” and may be established by a regulatory body (e.g., the Federal Communications Commission in the United States or the European Telecommunications Standards Institute) and/or a standards body (e.g., Third Generation Partnership Project) that governs the communication channel(s) and/or standard(s) in use. The pulse shaper 104 may comprise, for example, an infinite impulse response (IIR) and/or a finite impulse response (FIR) filter. The number of taps, or

“length,” of the pulse shaper 104 is denoted herein as L_{Tx} , which is an integer. The impulse response of the pulse shaper 104 is denoted herein as h_{Tx} . The pulse shaper 104 may be configured such that its output signal 113 intentionally has a substantial amount of inter-symbol interference (ISI). Accordingly, the pulse shaper 104 may be referred to as a partial response pulse shaping filter, and the signal 113 may be referred to as a partial response signal or as residing in the partial response domain, whereas the signal 103 may be referred to as residing in the symbol domain. The number of taps and/or the values of the tap coefficients of the pulse shaper 104 may be designed such that the pulse shaper 104 is intentionally non-optimal for additive white Gaussian noise (AWGN) in order to improve tolerance of non-linearity in the signal path. In this regard, the pulse shaper 104 may offer superior performance in the presence of non-linearity as compared to, for example, a conventional near zero positive ISI pulse shaping filter (e.g., root raised cosine (RRC) pulse shaping filter). The pulse shaper 104 may be designed as described in one or more of: the United States patent application titled “Design and Optimization of Partial Response Pulse Shape Filter,” the United States patent application titled “Constellation Map Optimization For Highly Spectrally Efficient Communications,” and the United States patent application titled “Dynamic Filter Adjustment For Highly-Spectrally-Efficient Communications,” each of which is incorporated herein by reference, as set forth above.

[0025] It should be noted that a partial response signal (or signals in the “partial response domain”) is just one example of a type of signal for which there is correlation among symbols of the signal (referred to herein as “inter-symbol-correlated (ISC) signals”). Such ISC signals are in contrast to zero (or near-zero) ISI signals generated by, for example, raised-cosine (RC) or root-raised-cosine (RRC) filtering. For simplicity of illustration, this disclosure focuses on partial response signals generated via partial response filtering. Nevertheless, aspects of this disclosure are applicable to other ISC

signals such as, for example, signals generated via matrix multiplication (e.g., lattice coding), and signals generated via decimation below the Nyquist frequency.

[0026] The timing pilot insertion circuit 105 may insert a pilot signal which may be utilized by the receiver for timing synchronization. The output signal 115 of the timing pilot insertion circuit 105 may thus comprise the signal 113 plus an inserted pilot signal (e.g., a sine wave at $1/4 \times f_{\text{baud}}$, where f_{baud} is the symbol rate). An example implementation of the pilot insertion circuit 105 is described in the United States patent application titled "Timing Synchronization for Reception of Highly-Spectrally-Efficient Communications," which is incorporated herein by reference, as set forth above.

[0027] The transmitter front-end 106 may be operable to amplify and/or upconvert the signal 115 to generate the signal 116. Thus, the transmitter front-end 106 may comprise, for example, a power amplifier and/or a mixer. The front-end may introduce non-linear distortion and/or phase noise (and/or other non-idealities) to the signal 116. The non-linearity of the circuit 106 may be represented as F_{nlTx} which may be, for example, a polynomial, or an exponential (e.g., Rapp model). The non-linearity may incorporate memory (e.g., Volterra series).

[0028] The channel 107 may comprise a wired, wireless, and/or optical communication medium. The signal 116 may propagate through the channel 107 and arrive at the receive front-end 108 as signal 118. Signal 118 may be noisier than signal 116 (e.g., as a result of thermal noise in the channel) and may have higher or different ISI than signal 116 (e.g., as a result of multi-path).

[0029] The receiver front-end 108 may be operable to amplify and/or downconvert the signal 118 to generate the signal 119. Thus, the receiver front-end may comprise, for example, a low-noise amplifier and/or a mixer. The receiver front-end may introduce non-linear distortion and/or phase noise to the signal 119. The non-linearity of the circuit 108 may be represented as F_{nlRx} which may be, for example, a polynomial, or an

exponential (e.g., Rapp model). The non-linearity may incorporate memory (e.g., Volterra series).

[0030] The timing pilot recovery and removal circuit 110 may be operable to lock to the timing pilot signal inserted by the pilot insertion circuit 105 in order to recover the symbol timing of the received signal. The output 122 may thus comprise the signal 120 minus (i.e., without) the timing pilot signal. An example implementation of the timing pilot recovery and removal circuit 110 is described in the United States patent application titled “Timing Synchronization for Reception of Highly-Spectrally-Efficient Communications,” which is incorporated herein by reference, as set forth above.

[0031] The input filter 109 may be operable to adjust the waveform of the partial response signal 119 to generate partial response signal 120. The input filter 109 may comprise, for example, an infinite impulse response (IIR) and/or a finite impulse response (FIR) filter. The number of taps, or “length,” of the input filter 109 is denoted herein as L_{Rx} , an integer. The impulse response of the input filter 109 is denoted herein as h_{Rx} . The number of taps, and/or tap coefficients of the input filter 109 may be configured based on: a non-linearity model, \widehat{F}_{nl} , signal-to-noise ratio (SNR) of signal 120, the number of taps and/or tap coefficients of the Tx partial response filter 104, and/or other parameters. The number of taps and/or the values of the tap coefficients of the input filter 109 may be configured such that noise rejection is intentionally compromised (relative to a perfect match filter) in order to improve performance in the presence of non-linearity. As a result, the input filter 109 may offer superior performance in the presence of non-linearity as compared to, for example, a conventional near zero positive ISI matching filter (e.g., root raised cosine (RRC) matched filter). The input filter 109 may be designed as described in one or more of: the United States patent application titled “Design and Optimization of Partial Response Pulse Shape Filter,” the United States patent application titled “Constellation Map Optimization For Highly Spectrally

Efficient Communications,” and the United States patent application titled “Dynamic Filter Adjustment For Highly-Spectrally-Efficient Communications,” each of which is incorporated herein by reference, as set forth above.

[0032] As utilized herein, the “total partial response (h)” may be equal to the convolution of h_{Tx} and h_{Rx} , and, thus, the “total partial response length (L)” may be equal to $L_{Tx} + L_{Rx} - 1$. L may, however, be chosen to be less than $L_{Tx} + L_{Rx} - 1$ where, for example, one or more taps of the Tx pulse shaper 104 and/or the Rx input filter 109 are below a determined level. Reducing L may reduce decoding complexity of the sequence estimation. This tradeoff may be optimized during the design of the system 100.

[0033] The equalizer and sequence estimator 112 may be operable to perform an equalization process and a sequence estimation process. Details of an example implementation of the equalizer and sequence estimator 112 are described below with respect to FIG. 2. The output signal 132 of the equalizer and sequence estimator 112 may be in the symbol domain and may carry estimated values of corresponding transmitted symbols (and/or estimated values of the corresponding transmitted information bits of the Tx_bitstream) of signal 103. Although not depicted, the signal 132 may pass through an interleaver en route to the de-mapper 114. The estimated values may comprise soft-decision estimates, hard-decision estimates, or both.

[0034] The de-mapper 114 may be operable to map symbols to bit sequences according to a selected modulation scheme. For example, for an N-QAM modulation scheme, the mapper may map each symbol to $\log_2(N)$ bits of the Rx_bitstream. The Rx_bitstream may, for example, be output to a de-interleaver and/or an FEC decoder. Alternatively, or additionally, the de-mapper 114 may generate a soft output for each bit, referred as LLR (Log-Likelihood Ratio). The soft output bits may be used by a soft-decoding forward error corrector (e.g. a low-density parity check (LDPC) decoder).

The soft output bits may be generated using, for example, a Soft Output Viterbi Algorithm (SOVA) or similar. Such algorithms may use additional information of the sequence decoding process including metrics levels of dropped paths and/or estimated bit probabilities for generating the LLR, where $LLR(b) = \log\left(\frac{P_b}{1-P_b}\right)$, where P_b is the probability that bit $b=1$.

[0035] In an example implementation, components of the system upstream of the pulse shaper 104 in the transmitter and downstream of the equalizer and sequence estimator 112 in the receiver may be as found in a conventional N-QAM system. Thus, through modification of the transmit side physical layer and the receive side physical layer, aspects of the invention may be implemented in an otherwise conventional N-QAM system in order to improve performance of the system in the presence of non-linearity as compared, for example, to use of RRC filters and an N-QAM slicer.

[0036] FIG. 2 is a block diagram depicting an example equalization and sequence estimation circuit for use in a system configured for low-complexity, highly-spectrally-efficient communications. Shown are an equalizer circuit 202, a signal combiner circuit 204, a phase adjust circuit 206, a sequence estimation circuit 210, and non-linearity modeling circuits 236a and 236b.

[0037] The equalizer 202 may be operable to process the signal 122 to reduce ISI caused by the channel 107. The output 222 of the equalizer 202 is a partial response domain signal. The ISI of the signal 222 is primarily the result of the pulse shaper 104 and the input filter 109 (there may be some residual ISI from multipath, for example, due to use of the least means square (LMS) approach in the equalizer 202). The error signal, 201, fed back to the equalizer 202 is also in the partial response domain. The signal 201 is the difference, calculated by combiner 204, between 222 and a partial response signal 203 that is output by non-linearity modeling circuit 236a. An example implementation of

the equalizer is described in the United States patent application titled “Feed Forward Equalization for Highly-Spectrally-Efficient Communications,” which is incorporated herein by reference, as set forth above.

[0038] The carrier recovery circuit 208 may be operable to generate a signal 228 based on a phase difference between the signal 222 and a partial response signal 207 output by the non-linearity modeling circuit 236b. The carrier recovery circuit 208 may be as described in the United States patent application titled “Coarse Phase Estimation for Highly-Spectrally-Efficient Communications,” which is incorporated herein by reference, as set forth above.

[0039] The phase adjust circuit 206 may be operable to adjust the phase of the signal 222 to generate the signal 226. The amount and direction of the phase adjustment may be determined by the signal 228 output by the carrier recovery circuit 208. The signal 226 is a partial response signal that approximates (up to an equalization error caused by finite length of the equalizer 202, a residual phase error not corrected by the phase adjust circuit 206, non-linearities, and/or other non-idealities) the total partial response signal resulting from corresponding symbols of signal 103 passing through pulse shaper 104 and input filter 109.

[0040] The buffer 212 buffers samples of the signal 226 and outputs a plurality of samples of the signal 226 via signal 232. The signal 232 is denoted $\underline{PR1}$, where the underlining indicates that it is a vector (in this case each element of the vector corresponds to a sample of a partial response signal). In an example implementation, the length of the vector $\underline{PR1}$ may be Q samples.

[0041] Input to the sequence estimation circuit 210 are the signal 232, the signal 228, and a response \hat{h} . Response \hat{h} is based on h (the total partial response, discussed above). For example, response \hat{h} may represent a compromise between h (described above) and a

filter response that compensates for channel non-idealities such as multi-path. The response \hat{h} may be conveyed and/or stored in the form of $L_{Tx} + L_{Rx} - 1$ tap coefficients resulting from convolution of the L_{Tx} tap coefficients of the pulse shaper 104 and the L_{Rx} tap coefficients of the input filter 109. Alternatively, response \hat{h} may be conveyed and/or stored in the form of fewer than $L_{Tx} + L_{Rx} - 1$ tap coefficients—for example, where one or more taps of the L_{Tx} and L_{Rx} is ignored due to being below a determined threshold. The sequence estimation circuit 210 may output partial response feedback signals 205 and 209, a signal 234 that corresponds to the finely determined phase error of the signal 120, and signal 132 (which carries hard and/or soft estimates of transmitted symbols and/or transmitted bits). An example implementation of the sequence estimation circuit 210 is described below with reference to FIG. 3.

[0042] The non-linear modeling circuit 236a may apply a non-linearity function \widehat{F}_{nl} (a model of the non-linearity seen by the received signal en route to the circuit 210) to the signal 205 resulting in the signal 203. Similarly, the non-linear modeling circuit 236b may apply the non-linearity function \widehat{F}_{nl} to the signal 209 resulting in the signal 207. \widehat{F}_{nl} may be, for example, a third-order or fifth-order polynomial. Increased accuracy resulting from the use of a higher-order polynomial for \widehat{F}_{nl} may tradeoff with increased complexity of implementing a higher-order polynomial. Where F_{nlTx} is the dominant non-linearity of the communication system 100, \widehat{F}_{nl} modeling only F_{nlTx} may be sufficient. Where degradation in receiver performance is above a threshold due to other non-linearities in the system (e.g., non-linearity of the receiver front-end 108) the model \widehat{F}_{nl} may take into account such other non-linearities

[0043] FIG. 3 is a block diagram depicting an example sequence estimation circuit for use in a system configured for low-complexity, highly-spectrally-efficient communications. Shown are a candidate generation circuit 302, a metrics calculation circuit 304, a candidate selection circuit 306, a combiner circuit 308, a buffer circuit 310,

a buffer circuit 312, a phase adjust circuit 314, and convolution circuits 316a and 316b. The sequence estimation process described with respect to FIG. 3 is an example only. Many variations of the sequence estimation process are also possible. For example, although the implementation described here uses one phase survivor per symbol survivor, another implementation may have PSu (e.g., $PSu < Su$) phase survivors that will be used commonly for each symbol survivor.

[0044] For each symbol candidate at time n , the metrics calculation circuit 304 may be operable to generate a metric vector $D_n^1 \dots D_n^{M \times Su \times P}$ based on the partial response signal PR1, the signal 303a conveying the phase candidate vectors PC_n¹...PC_n^{M×Su×P}, and the signal 303b conveying the symbol candidate vectors SC_n¹...SC_n^{M×Su×P}, where underlining indicates a vector, subscript n indicates that it is the candidate vectors for time n , M is an integer equal to the size of the symbol alphabet (e.g., for N-QAM, M is equal to N), Su is an integer equal to the number of symbol survivor vectors retained for each iteration of the sequence estimation process, and P is an integer equal to the size of the phase alphabet. In an example implementation, the size of phase alphabet is three, with each of the three symbols corresponding to one of: a positive shift, a negative phase shift, or zero phase shift, as further described below with respect to FIGS. 5A–5D and in the United States patent application titled “Fine Phase Estimation for Highly Spectrally Efficient Communications,” which is incorporated herein by reference, as set forth above. In an example implementation, each phase candidate vector may comprise Q phase values and each symbol candidate vector may comprise Q symbols. An example implementation of the metrics calculation block is described below with reference to FIG. 4.

[0045] The candidate selection circuit 306 may be operable to select Su of the symbol candidates SC_n¹...SC_n^{M×Su×P} and Su of the phase candidates PC_n¹...PC_n^{M×Su×P} based on the metrics $D_n^1 \dots D_n^{M \times Su \times P}$. The selected phase candidates are referred to as the phase

survivors $\underline{PS}_n^1 \dots \underline{PS}_n^{Su}$. Each element of each phase survivors $\underline{PS}_n^1 \dots \underline{PS}_n^{Su}$ may correspond to an estimate of residual phase error in the signal 232. That is, the phase error remaining in the signal after coarse phase error correction via the phase adjust circuit 206. The best phase survivor \underline{PS}_n^1 is conveyed via signal 307a. The S_u phase survivors are retained for the next iteration of the sequence estimation process (at which time they are conveyed via signal 301b). The selected symbol candidates are referred to as the symbol survivors $\underline{SS}_n^1 \dots \underline{SS}_n^{Su}$. Each element of each symbol survivors $\underline{SS}_n^1 \dots \underline{SS}_n^{Su}$ may comprise a soft-decision estimate and/or a hard-decision estimate of a symbol of the signal 232. The best symbol survivor \underline{SS}_n^1 is conveyed to symbol buffer 310 via the signal 307b. The S_u symbol survivors are retained for the next iteration of the sequence estimation process (at which time they are conveyed via signal 301a). Although, the example implementation described selects the same number, S_u , of phase survivors and symbol survivors, such is not necessarily the case. Operation of example candidate selection circuits 306 are described below with reference to FIGs. 5D and 6A–6B.

[0046] The candidate generation circuit 302 may be operable to generate phase candidates $\underline{PC}_n^1 \dots \underline{PC}_n^{M \times S_u \times P}$ and symbol candidates $\underline{SC}_n^1 \dots \underline{SC}_n^{M \times S_u \times P}$ from phase survivors $\underline{PS}_{n-1}^1 \dots \underline{PS}_{n-1}^{S_u}$ and symbol survivors $\underline{SS}_{n-1}^1 \dots \underline{SS}_{n-1}^{S_u}$, wherein the index $n-1$ indicates that they are survivors from time $n-1$ are used for generating the candidates for time n . In an example implementation, generation of the phase and/or symbol candidates may be as, for example, described below with reference to FIGs. 5A and 5B and/or in the United States patent application titled “Joint Sequence Estimation of Symbol and Phase with High Tolerance of Nonlinearity,” which is incorporated herein by reference, as set forth above.

[0047] The symbol buffer circuit 310 may comprise a plurality of memory elements operable to store one or more symbol survivor elements of one or more symbol survivor vectors. The phase buffer circuit 312 may comprise a plurality of memory elements operable to store one or more phase survivor vectors. Example implementations of the buffers 310 and 312 are described below with reference to FIGS. 8A and 8B, respectively.

[0048] The combiner circuit 308 may be operable to combine the best phase survivor, \underline{PS}_n^1 , conveyed via signal 307a, with the signal 228 generated by the carrier recovery circuit 208 (Fig. 2) to generate fine phase error vector \underline{FPE}_n^1 , conveyed via signal 309, which corresponds to the finely estimated phase error of the signal 222 (Fig. 2). At each time n, fine phase error vector \underline{FPE}_{n-1}^1 stored in phase buffer 312 may be overwritten by \underline{FPE}_n^1 .

[0049] The phase adjust circuit 314 may be operable to adjust the phase of the signal 315a by an amount determined by the signal 234 output by phase buffer 312, to generate the signal 205.

[0050] The circuit 316a, which performs a convolution, may comprise a FIR filter or IIR filter, for example. The circuit 316a may be operable to convolve the signal 132 with response \hat{h} , resulting in the partial response signal 315a. Similarly, the convolution circuit 316b may be operable to convolve the signal 317 with response \hat{h} , resulting in the partial response signal 209. As noted above, response \hat{h} may be stored by, and/or conveyed to, the sequence estimation circuit 210 in the form of one or more tap coefficients, which may be determined based on the tap coefficients of the pulse shaper 104 and/or input filter 109 and/or based on an adaptation algorithm of a decision feedback equalizer (DFE). Response \hat{h} may thus represent a compromise between

attempting to perfectly reconstruct the total partial response signal (103 as modified by pulse shaper 104 and input filter 109) on the one hand, and compensating for multipath and/or other non-idealities of the channel 107 on the other hand. In this regard, the system 100 may comprise one or more DFEs as described in one or more of: the United States patent application titled “Decision Feedback Equalizer for Highly-Spectrally-Efficient Communications,” the United States patent application titled “Decision Feedback Equalizer with Multiple Cores for Highly-Spectrally-Efficient Communications,” and the United States patent application titled “Decision Feedback Equalizer Utilizing Symbol Error Rate Biased Adaptation Function for Highly-Spectrally-Efficient Communications,” each of which is incorporated herein by reference, as set forth above.

[0051] Thus, signal 203 is generated by taking a first estimate of transmitted symbols, (an element of symbol survivor \underline{SS}_n^1), converting the first estimate of transmitted symbols to the partial response domain via circuit 316a, and then compensating for non-linearity in the communication system 100 via circuit 236a (FIG. 2). Similarly, signal 207 is generated from a second estimate of transmitted symbols (an element of symbol survivor \underline{SS}_n^1) that is converted to the partial response domain by circuit 316b to generate signal 209, and then applying a non-linear model to the signal 209b to compensate for non-linearity in the signal path.

[0052] FIG. 4 is a block diagram depicting an example metric calculation circuit for use in a system configured for low-complexity, highly-spectrally-efficient communications. Shown is a phase adjust circuit 402, a convolution circuit 404, and a cost function calculation circuit 406. The phase adjust circuit 402 may phase shift one or more elements of the vector $\underline{PR1}$ (conveyed via signal 232) by a corresponding one or more values of the phase candidate vectors $\underline{PC}_n^1 \dots \underline{PC}_n^{M \times S \times P}$. The signal 403 output by

the phase adjust circuit 402 thus conveys a plurality of partial response vectors $\underline{PR2}_n^1 \dots \underline{PR2}_n^{M \times Su \times P}$, each of which comprises a plurality of phase-adjusted versions of $\underline{PR1}$.

[0053] The circuit 404, which performs a convolution, may comprise a FIR filter or IIR filter, for example. The circuit 404 may be operable to convolve the symbol candidate vectors $\underline{SC}_n^1 \dots \underline{SC}_n^{M \times Su \times P}$ with \hat{h} . The signal 405 output by the circuit 404 thus conveys vectors $\underline{SCPR}_n^1 \dots \underline{SCPR}_n^{M \times Su \times P}$, each of which is a candidate partial response vector.

[0054] The cost function circuit 406 may be operable to generate metrics indicating the similarity between one or more of the partial response vectors $\underline{PR2}_n^1 \dots \underline{PR2}_n^{M \times Su \times P}$ and one or more of the vectors $\underline{SCPR}_n^1 \dots \underline{SCPR}_n^{M \times Su \times P}$ to generate error metrics $D_n^1 \dots D_n^{M \times Su \times P}$. In an example implementation, the error metrics may be Euclidean distances calculated as shown below in equation 1.

$$D_n^i = \left| \left(\underline{SCPR}_n^i \right) - \left(\underline{PR2}_n^i \right) \right|^2 \quad \text{EQ. 1}$$

for $1 \leq i \leq M \times Su \times P$.

[0055] FIGS. 5A–5D depict portions of an example sequence estimation process performed by a system configured for low-complexity, highly-spectrally-efficient communications. In FIGS. 5A–5D it is assumed, for purposes of illustration, that $M=4$ (a symbol alphabet of $\alpha, \beta, \chi, \delta$), $Su=3$ (three symbol survivors are selected each iteration), $Psu=Su$ (three phase survivors are selected each iteration), $P=3$ (a phase alphabet of plus, minus, and zero), and that Q (vector length) is 4.

[0056] Referring to FIG. 5A, there is shown phase and symbol survivors from time $n-1$ on the left side of the figure. The first step in generating symbol candidates and phase

candidates from the survivors is to duplicate the survivors and shift the contents to free up an element in each of the resulting vectors called out as 502 on the right side of FIG. 5A. In the example implementation depicted, the survivors are duplicated $M \cdot P - 1$ times and shifted one element.

[0057] Referring to FIG. 5B, the next step in generating the candidates is inserting symbols in the vacant elements of the symbol vectors and phase values in the vacant elements of the phase vectors, resulting in the symbol candidates and phase candidate for time n (called out as 504 in FIG. 5B). In the example implementation depicted, each of the M possible symbol values is inserted into $S_u \cdot P$ symbol candidates, and each of the P phase values may be inserted into $M \cdot S_u$ candidates. In the example implementation depicted, θ_5 is a reference phase value calculated based on phase survivor \underline{PS}_{n-1}^1 . For example, θ_5 may be the average (or a weighted average) of the last two or more elements of the phase survivor \underline{PS}_{n-1}^1 (in the example shown, the average over the last two elements would be $(\theta_5 + 0)/2$). In the example implementation depicted, $\theta_4 = \theta_5 - \Delta\theta$, and $\theta_6 = \theta_5 + \Delta\theta$, where $\Delta\theta$ is based on: the amount of phase noise in signal 226, slope (derivative) of the phase noise in signal 226, signal-to-noise ratio (SNR) of signal 226, and/or capacity of the channel 107. Similarly, in the example implementation shown, θ_8 is a reference phase value calculated based on phase survivor \underline{PS}_{n-1}^2 , $\theta_7 = \theta_8 - \Delta\theta$, $\theta_9 = \theta_8 + \Delta\theta$, θ_{11} is a reference phase value calculated based on phase survivor \underline{PS}_{n-1}^3 , $\theta_{10} = \theta_{11} - \Delta\theta$, and $\theta_{12} = \theta_{11} + \Delta\theta$.

[0058] Referring to FIG. 5C, as described above with reference to FIG. 4, the symbol candidates are transformed to the partial response domain via a convolution, the reference signal \underline{PR}_1 is phase adjusted, and then the metrics $D_n^1 \dots D_n^{M \times S_u \times P}$ are calculated based on the partial response signals $\underline{PR}_n^1 \dots \underline{PR}_n^{M \times S_u \times P}$ and $\underline{SCPR}_n^1 \dots \underline{SCPR}_n^{M \times S_u \times P}$.

[0059] Referring to FIG. 5D, the metrics calculated in FIG. 5C are used to select which of the candidates generated in FIG. 5B are selected to be the survivors for the next iteration of the sequence estimation process. FIG. 5D depicts an example implementation in which the survivors are selected in a single step by simply selecting Su candidates corresponding to the Su best metrics. In the example implementation depicted, it is assumed that metric D_n^{14} is the best metric, that D_n^{16} is the second best metric, and that D_n^{30} is the third-best metric. Accordingly, symbol candidate \underline{SC}_n^{14} is selected as the best symbol survivor, \underline{PC}_n^{14} is selected as the best phase survivor, symbol candidate \underline{SC}_n^{16} is selected as the second-best symbol survivor, \underline{PC}_n^{16} is selected as the second-best phase survivor, symbol candidate \underline{SC}_n^{30} is selected as the third-best symbol survivor, and \underline{PC}_n^{30} is selected as the third-best phase survivor. The survivor selection process of FIG. 5D may result in selecting identical symbol candidates which may be undesirable. A survivor selection process that prevents redundant symbol survivors is described below with reference to FIGS. 6A and 6B.

[0060] FIGS. 6A and 6B depict an example survivor selection process that is an alternative to the process depicted in FIG. 5D. In FIG. 6A, the candidates generated in FIG. 5B and the metrics calculated in FIG. 5C are used to select the best phase candidate for each symbol candidate (selected candidates are called out by reference designator 602). In FIG. 6B, the best Su of the candidates selected in FIG. 6A are selected as the survivors for the next iteration of the sequence estimation process. In the example implementation depicted, it is assumed that metric D_n^6 is the best metric, that D_n^5 is the second-best metric, and that D_n^{25} is the third-best metric. Accordingly, symbol candidate \underline{SC}_n^6 is selected as the best symbol survivor, \underline{PC}_n^6 is selected as the best phase survivor, symbol candidate \underline{SC}_n^5 is selected as the second-best symbol survivor, \underline{PC}_n^5 is selected as

the second-best phase survivor, symbol candidate \underline{SC}_n^{25} is selected as the third-best symbol survivor, and \underline{PC}_n^{25} is selected as the third-best phase survivor.

[0061] Although the implementations described with reference to FIGS 5A–6B use one phase survivor per symbol survivor. Other example implementations may use PSu (e.g., $PSu < Su$) phase survivors that are used commonly for each symbol survivor. In such an implementation, each of the phase survivors $\underline{PS}_{n-1}^1 \dots \underline{PS}_{n-1}^{PSu}$ may be duplicated P times to generate phase successors, and then duplicated $M \cdot Su$ times to be associated with corresponding symbols successors. The number of symbol candidates in such an implementation would be $M \cdot Su \cdot PSu \cdot P$.

[0062] FIG. 7 is a diagram illustrating initialization of the sequence estimation process. In FIG. 7 it is again assumed, for illustration, that $M=4$ (a symbol alphabet of $\alpha, \beta, \chi, \delta$), $Su=3$ (three symbol survivors are selected each iteration), $PSu=Su$ (three phase survivors are selected each iteration), $P=3$ (a phase alphabet of plus, minus, and zero), and that Q (vector length) is 4. On the far left of FIG. 7 is shown symbol survivors 702 after receipt of a preamble sequence. Because the preamble is a deterministic sequence, all symbol survivors are forced to the same values. From the survivors 702 are generated the candidates 704 and metrics 706 are calculated based on the candidates 704. In the example implementation shown, since the survivors were all the same, there are only four unique symbol candidates. The metrics for the four candidates are, respectively, D1, D2, D3, and D4. Accordingly, if the three candidates corresponding to the best three metrics were chosen, then the three candidates corresponding to D1 would all be chosen and the survivors for the next iteration would again all be identical. Accordingly, the three best, non-redundant symbol candidates are selected (as indicated by the heavy lines). Consequently, one of the candidates having the metric value D1 is selected, one of the candidates having the metric value D2 is selected, and one of the candidates having

metric value D3 is selected, such that three non-redundant survivors are used for the next iteration.

[0063] FIGs. 8A depicts an example implementation of the phase buffer shown in FIG. 3. In the example implementation depicted, the depth of the phase buffer 312 is Q and the phase value stored at element q is represented as Z_q , for q from 1 to Q . In the example implementation depicted, the value stored in element $q3$ is output as the signal 234. For each iteration of the sequence estimation process, Q elements of the phase buffer 312 storing Q values of \underline{PS}_{n-1}^1 may be overwritten with Q values of \underline{PS}_n^1 .

[0064] FIGs. 8B depicts an example implementation of the symbol buffer shown in FIG. 3. In the example implementation depicted, the value(s) stored in one or more elements starting with index $q1$ (e.g., values stored in elements $q1$ through $q1+L$) is/are output as the signal 317 and the value(s) stored in one or more elements starting with index $q2$ (e.g., values stored in elements $q2$ through $q2+L$) is/are output as the signal 132. Because the value(s) output as the signal 317 start from a lower-indexed element of the symbol buffer, the delay between receiving a signal sample and outputting the corresponding value of signal 317 is shorter than the delay between receiving a signal sample and outputting the corresponding value of the signal 132. Because the value(s) output as the signal 132 start from a higher-indexed element, however, it/they is/are likely to be less error-prone. These concepts are further illustrated with reference to in FIGS. 8C and 8D. In an example implementation, $q2$ is equal to $q3$.

[0065] FIG. 8C depicts contents of an example symbol buffer over a plurality of iterations of a sequence estimation process. In the example implementation shown in FIG. 8C, the symbol buffer 310 comprises four elements with the signal 317 corresponding to the contents of the first element (for simplicity of illustration, in FIGS. 8C and 8D, it is assumed only one element is output as signal 317 on each iteration) and the signal 132 corresponding to the fourth element (for simplicity of illustration, in

FIG.S. 8C and 8D, it is assumed only one element is output as signal 132 on each iteration). In the example implementation depicted, during each iteration of the sequence estimation process, candidates are generated by duplicating the survivors from the previous iteration, shifting the values by one element, and the appending a new value into the vacated element. Accordingly, ideally each survivor would differ from the previous survivor only in the lowest-indexed element (corresponding to the most-recent symbol). Where other elements of the most-recent survivor differ from corresponding elements of the previous survivor, such difference indicates that there is an error in those elements (either in the most-recent survivor or in the previous survivor). Given the convolutional nature of the partial response signal, symbols at higher indexes in the buffer are more reliable. Thus the symbol values will tend to converge as they move toward the right in FIG. 8C.

[0066] Shown are the contents of example symbol buffer 310 at times $n-3$, $n-2$, $n-1$, and n . At time $n-3$, a symbol survivor having values $\alpha, \beta, \chi, \delta$ is stored in the symbol buffer 310. Accordingly, as shown in FIG. 8D, the value of signal 317 at time $n-3$ is ' α ' and the value of signal 132 is ' δ .' At time $n-2$, a new symbol survivor having values $\delta, \beta, \beta, \chi$ is stored in the symbol buffer 310. Accordingly, as shown in FIG. 8D, the value of signal 317 at time $n-2$ is ' δ ' and the value of signal 132 is ' χ .' At time $n-1$, a new symbol survivor having values $\chi, \delta, \beta, \beta$ is stored in the symbol buffer 310. Accordingly, as shown in FIG. 8D, the value of signal 317 at time $n-1$ is ' χ ' and the value of signal 132 is ' β .' At time n , a new symbol survivor having values $\beta, \chi, \delta, \beta$ is stored in the symbol buffer 310. Accordingly, as shown in FIG. 8D, the value of signal 317 at time n is ' β ' and the value of signal 132 is ' β .' Thus, in the example scenario depicted in FIG. 8C, the value in the first element of the symbol buffer 310 at time $n-3$ was erroneous and the symbol did not converge until it reached the second element ($q=2$) of the buffer 310. That is, at time $n-2$ the symbol changed from α to β and then remained β at times $n-1$

and n. This illustrates the consequence of taking signal 317 from the first element of the symbol buffer 310 and taking the signal 132 from the fourth element of the symbol buffer 312. Namely, the signal 317 has less delay than the signal 132 but is also more error prone than the signal 132.

[0067] In FIG. 8D, the values of the signals are shown for times n-3 to time n+3. The dashed lines illustrate the delay between the signal 317 and the signal 132.

[0068] FIG. 9 depicts Symbol Error Rate (SER) vs. SNR for a receiver using aspects of this disclosure and for a conventional QAM receiver. For purpose of FIG. 9, gross spectral efficiency has been set to 10bits/sec/Hz and channel spacing has been 28 MHz (which is just one example of a channel spacing as might be defined by a standards and/or regulatory body such as the FCC and ETSI). Line 1002 represents ideal (i.e., without AWGN or phase noise) performance of a conventional QAM receiver receiving a QAM1024 signal and line 1004 represents ideal performance of a receiver using aspects of this disclosure receiving a “PR10” (which uses a QAM32 constellation and partial response shaping to achieve a capacity gain of 2). Line 1006 represents performance of the conventional QAM receiver, and line 1008 represents performance of the PR10 receiver, with SSB phase noise of -90dBc/Hz at frequency offset of 100KHz. The phase noise model has a fixed slope of -20dB/dec. Line 1010 represents performance of the conventional QAM receiver, and Line 1012 represents performance of the PR10 receiver, under combined phase noise and non-linear distortion. The non-linear distortion model is saturated 3rd order, without memory, where φ was selected to be 30° to create the polynomial saddle point, which is the clipping (saturation) point:

$$y = \begin{cases} x \cdot (1 - r \cdot e^{j\varphi} \cdot |x|^2), & x < x_{sat} \\ y_{sat} & , x \geq x_{sat} \end{cases}$$

$$y_{sat} = x_{sat} \cdot (1 - r \cdot e^{j\varphi} \cdot |x_{sat}|^2)$$

and r is set according to the desired distortion level (e.g., power backoff setting).

[0069] In the ideal scenario, the PR10 receiver as shown performs 3.5dB better than the QAM receiver as shown around SER of 3×10^{-2} , which is a practical reference for BER of 10^{-6} with FEC rate around 0.95. Both receivers as shown are using symbols Pilot Over Head (POH) of 5%, which may stabilize **phase** recovery in presence of sever phase noise. The PR10 receiver as shown is estimating phase noise using the HPSE but the QAM receiver shown is using perfect decisions (i.e., genie aided) for carrier recovery loop (for all other demodulating purposes it uses the symbol pilots and tentative decisions). The phase noise degrades the QAM receiver by 1dB but the PR10 receiver by only 0.4dB. The transmitted power of the PR10 receiver shown is higher by 4.5dB than for the QAM receiver shown. Nevertheless, the combined phase noise and non-linear distortion degrades the QAM receiver shown by 2.2dB while it affects the PR10 receiver shown by only 0.6dB. The overall SER improvement of the PR10 receiver shown is around 5.3dB but the PR10 receiver shown has error correlation due to the nature of partial response (memory) hence, the FEC gain for the PR10 receiver shown is 1dB below the FEC gain of the QAM receiver shown. Therefore the practical sensitivity benefit is limited to 4.3dB. Tx power benefit of the PR10 receiver shown relative to the QAM receiver shown is 4.5dB, thus the total contribution to the system gain by using the PR10 receiver shown instead of the QAM receiver shown is 8.8dB. But due to spectral mask limitations the Tx power must be below $P_{1dB} - 4.5dB$ so that the spectral re-growth will not exceed the applicable spectral mask, therefore the practical benefit in Tx power of the PR10 receiver shown vs. the QAM receiver shown is 3dB and the overall system gain benefit of using the PR10 receiver instead of the QAM receiver shown is 7.3dB. With the use of crest factor reduction (CFR) and pre-distortion methods the Tx power for the PR10 receiver shown may increase without violating the applicable spectral mask and the system gain benefit resulting from use of the PR10 receiver shown instead of the QAM receiver shown may approach 8.8dB.

[0070] In the presence of non-linear distortion and phase noise, the performance of the near-zero ISI QAM receiver is practically determined by the SINAD (Signal to Noise and Distortion) level that consists of the AWGN, phase noise and non-linear distortion. Although the non-linear distortion isn't an AWGN interference, it may be practically considered like an AWGN because it has an in-band response which is almost flat and the distortion may be modeled as an additive component. The phase noise for small phase error may be modeled as an additive component as well. Although the phase noise isn't flat, assuming it has a small variance comparing to the AWGN, it may be considered as an additive contributor to the AWGN. Therefore, as a practical approximation, the overall SINAD may be expressed as the ratio of signal power to the sum of the variances of AWGN, in-band non-linear distortion and phase noise (rad). This is the manner in which SINAD is used herein. For the near-zero ISI receiver, SER performance vs. SINAD is very close to the SER performance vs. SNR for equal SNR and SINAD values (e.g., SINAD of 32dB will generate similar SER as SNR of 32dB).

[0071] The PR based modulation is using models of non-linear distortion and phase noise, thus by considering these interferences as part of the signal rather than as noise contributors, systems using PR-based modulation as described herein may perform significantly better in the presence of non-linearities

[0072] FIG. 10 depicts spectral efficiency for a receiver using aspects of this disclosure and a conventional DVB-S receiver. FIG. 10 is showing spectral efficiency based on BER simulations of 10^{-6} . A receiver using aspects of this disclosure to receive a "PR5" signal (based on QPSK and partial response shaping providing capacity gain of 2.5) is compared to a conventional receiver receiving DVBS-2 standard modulations 8PSK, 16APSK and 32APSK with FEC of LDPC with length of 64000 bits. The PR5 receiver is using RS(1024,931) which has rate of 0.91 and interleaver with size of 6144x6 words (word consists of 10bits), thus the latency is 61440 bits which is a little bit smaller

than the 64000 bits of LDPC. The curves 1004, 1006, 1008 represent ideal (i.e., without phase noise and POH=0%) of the DVBS-2 receiver. The curves 1010, 1012, 1014 represent performance of the DVBS-2 receiver with phase noise. The circle 1018 represents ideal (i.e., without phase noise and POH=0%) performance of the PR5 receiver. Curves 1010, 1012, and 1014 and circle 1018 are under SSB phase noise power level of -85dBc/Hz at frequency offset of 100KHz, with a slope of -20dB/dec and POH of 5%. The phase noise degrades performance of the DVBS-2 receiver by 1dB, which pushes the curves 1004, 1006, and 1008 to the right, and the POH of 5% pulls the curves 1004, 1006, and 1008 down by 5% (thus arriving at curves 1010, 1012, and 1014). The total gap from the Shannon capacity bound to curves 1010, 1012, and 1014 is 3-4dB. The PR5 receiver has spectrum efficiency of 4.32 bits/sec/Hz ($5 \times 0.95 \times 0.91$) and it performs up to 0.4dB from the capacity bound which is 4.3dB better than the DVBS-2 receiver receiving a 32APSK signal under same conditions.

[0073] In various example implementation, a receiver may receive a QAM-based, inter-symbol correlated (ISC) signal at a signal-to-noise-and-distortion ratio (SINAD) and process the received QAM-based, ISC signal to output information at a particular rate (i.e. a particular net spectral efficiency) with a symbol error rate lower or equal to $1e-2$. The SINAD may comprise a noise component and a distortion component. The SINAD without the distortion component may corresponds to a first SNR. The first SNR may be higher, by less than 7dB, than a second SNR that corresponds to the Shannon capacity limit needed to achieve the particular rate of information. In the example scenario depicted in FIG. 9, the information rate (or net spectral efficiency) is 9 bits/sec/Hz, the first SNR is 30.5 dB (for the SNR corresponding to SER of $1e-2$) and the second SNR is 27.1 dB (which is the Shannon capacity for 9bits/sec/Hz)

[0074] The QAM-based, ISC signal may be a partial response signal generated by passing a first signal through a partial response pulse shaping filter (e.g., 104). The

partial response pulse shaping filter may provide greater spectral efficiency than a spectral efficiency achieved by passing the first signal through a root-raised-cosine-based pulse shaping filter. The receiver may comprises an input filter; and the processing of the QAM-based, ISC signal may comprise filtering the QAM-based, ISC signal via a filter configured to achieve a desired total partial response in combination with the partial response pulse shaping filter. The receiver may comprise a non-linear modeling circuit (e.g., 236a and 236b), and the processing of the QAM-based, ISC signal may comprise equalizing the QAM-based, ISC signal via an equalizer (e.g., 122) controlled based on a feedback signal (e.g., 201) generated via the non-linear modeling circuit. The non-linear modeling circuit may be configured based on a non-linearity of a front-end of the receiver (e.g., 106). The QAM-based, ISC signal may enables an increased QAM symbols baud rate by a factor of more than 1.3 relative to a QAM symbols baud rate enabled by a corresponding QAM-based, near-zero inter-symbol interference (ISI) signal. The QAM-based, ISC signal may be based on an N-QAM symbol constellation, where N is an integer. The QAM-based, ISC signal may comprise pilot symbols and information symbols as described in, for example, United States Patent Application Serial No. 13/756,079 titled "Pilot Symbol Generation for Highly-Spectrally-Efficient Communications," and/or United States Patent Application Serial No. 13/755,052 titled "Pilot Symbol-Aided Sequence Estimation for Highly-Spectrally-Efficient Communications," each of which is incorporated herein by reference, as set forth above. The QAM-based, ISC signal complies with a channel spacing set by the European Telecommunications Standards Institute (ETSI) and/or the Federal Communications Commission (FCC) (e.g., EN 302 217 related to fixed wireless communications). The QAM-based, ISC signal complies with spectral mask limitations set by the European Telecommunications Standards Institute (ETSI) and/or the Federal Communications Commission (FCC) (e.g., EN 302 217 related to fixed wireless communications).

[0075] The present method and/or system may be realized in hardware, software, or a combination of hardware and software. The present method and/or system may be realized in a centralized fashion in at least one computing system, or in a distributed fashion where different elements are spread across several interconnected computing systems. Any kind of computing system or other apparatus adapted for carrying out the methods described herein is suited. A typical combination of hardware and software may be a general-purpose computing system with a program or other code that, when being loaded and executed, controls the computing system such that it carries out the methods described herein. Another typical implementation may comprise an application specific integrated circuit or chip.

[0076] The present method and/or system may also be embedded in a computer program product, which comprises all the features enabling the implementation of the methods described herein, and which when loaded in a computer system is able to carry out these methods. Computer program in the present context means any expression, in any language, code or notation, of a set of instructions intended to cause a system having an information processing capability to perform a particular function either directly or after either or both of the following: a) conversion to another language, code or notation; b) reproduction in a different material form.

[0077] While the present method and/or system has been described with reference to certain implementations, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the scope of the present method and/or system. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the present disclosure without departing from its scope. Therefore, it is intended that the present method and/or system not be limited to the particular implementations disclosed, but that the present

method and/or system will include all implementations falling within the scope of the appended claims.

CLAIMS

What is claimed is:

1. A method comprising:
 - receiving, in a receiver, a QAM-based, inter-symbol correlated (ISC) signal at a signal-to-noise-and-distortion ratio (SINAD) ; and
 - processing, in said receiver, said QAM-based, ISC signal to output information at a particular rate with a symbol error rate lower or equal to $1e-2$, wherein:
 - said SINAD comprises a noise component and a distortion component;
 - said noise component is equal to said distortion component;
 - said SINAD without said distortion component corresponds to a first SNR;
 - said first SNR is higher, by less than 7dB, than a second SNR that corresponds to the Shannon capacity limit needed to achieve said particular rate of information.
2. The method of claim 1, wherein said QAM-based, ISC signal is a partial response signal generated by passing a first signal through a partial response pulse shaping filter.
3. The method of claim 2, wherein said partial response pulse shaping filter provides greater spectral efficiency than a spectral efficiency achieved by passing said first signal through a root-raised-cosine-based pulse shaping filter.
4. The method of claim 2, wherein:
 - said receiver comprises an input filter; and

said processing said QAM-based, ISC signal comprises filtering said QAM-based, ISC signal via a filter configured to achieve a desired total partial response in combination with said partial response pulse shaping filter.

5. The method of claim 1, wherein:

said receiver comprises a non-linear modeling circuit; and

said processing said QAM-based, ISC signal comprises equalizing said QAM-based, ISC signal via an equalizer controlled based on a feedback signal generated via said non-linear modeling circuit.

6. The method of claim 5, wherein said non-linear modeling circuit is configured based on a non-linearity of a front-end of said receiver.

7. The method of claim 5, wherein said QAM-based, ISC signal enables an increased QAM symbols baud rate by a factor of more than 1.3 relative to a QAM symbols baud rate enabled by a corresponding QAM-based, near-zero inter-symbol interference (ISI) signal.

8. The method of claim 1, wherein said QAM-based, ISC signal is based on an N-QAM symbol constellation, where N is an integer.

9. The method of claim 1, wherein said QAM-based, ISC signal is comprises pilot symbols and information symbols.

10. The method of claim 1, wherein said QAM-based, ISC signal complies with a channel spacing set by the European Telecommunications Standards Institute (ETSI) and/or the Federal Communications Commission (FCC).

11 The method of claim 1, wherein said QAM-based, ISC signal complies with spectral mask limitations set by the European Telecommunications Standards Institute (ETSI) and/or the Federal Communications Commission (FCC).

12. A system comprising:

a receiver operable to:

receive a QAM-based, inter-symbol correlated (ISC) signal at a signal-to-noise-and-distortion ratio (SINAD) ; and

process said QAM-based, ISC signal to output information at a particular rate with a symbol error rate lower or equal to $1e-2$, wherein:

said SINAD comprises a noise component and a distortion component;

said noise component is equal to said distortion component;

said SINAD without said distortion component corresponds to a first SNR;

said first SNR is higher, by less than 7dB, than a second SNR that corresponds to the Shannon capacity limit needed to achieve said particular rate of information.

13. The system of claim 12, wherein said QAM-based, ISC signal is a partial response signal generated by passing a first signal through a partial response pulse shaping filter.

14. The system of claim 13, wherein said partial response pulse shaping filter provides greater spectral efficiency than a spectral efficiency achieved by passing said first signal through a root-raised-cosine based pulse shaping filter.

15. The system of claim 13, wherein:
said receiver circuit comprises an input filter; and
said processing of said QAM-based, ISC signal comprises a filtering of said QAM-based, ISC signal via a filter configured to achieve a desired total partial response in combination with said partial response pulse shaping filter.

16. The system of claim 12, wherein:
said receiver circuit comprises a non-linear modeling circuit; and
said processing of said QAM-based, ISC signal signal comprises equalization of said QAM-based, ISC signal via an equalizer controlled based on a feedback signal generated via sad non-linear modeling circuit.

17. The system of claim 16, wherein said non-linear modeling circuit is configured based on a non-linearity of a front-end of said receiver.

18. The system of claim 16, wherein said QAM-based, ISC signal enables an increased QAM symbols baud rate by a factor of more than 1.3 relative to a QAM symbols baud rate enabled by a corresponding QAM-based, near-zero inter-symbol interference (ISI) signal.

19. The system of claim 12, wherein said QAM-based, ISC signal is based on an N-QAM symbol constellation, where N is an integer.

20. The system of claim 12, wherein said QAM-based, ISC signal comprises pilot symbols and information symbols.

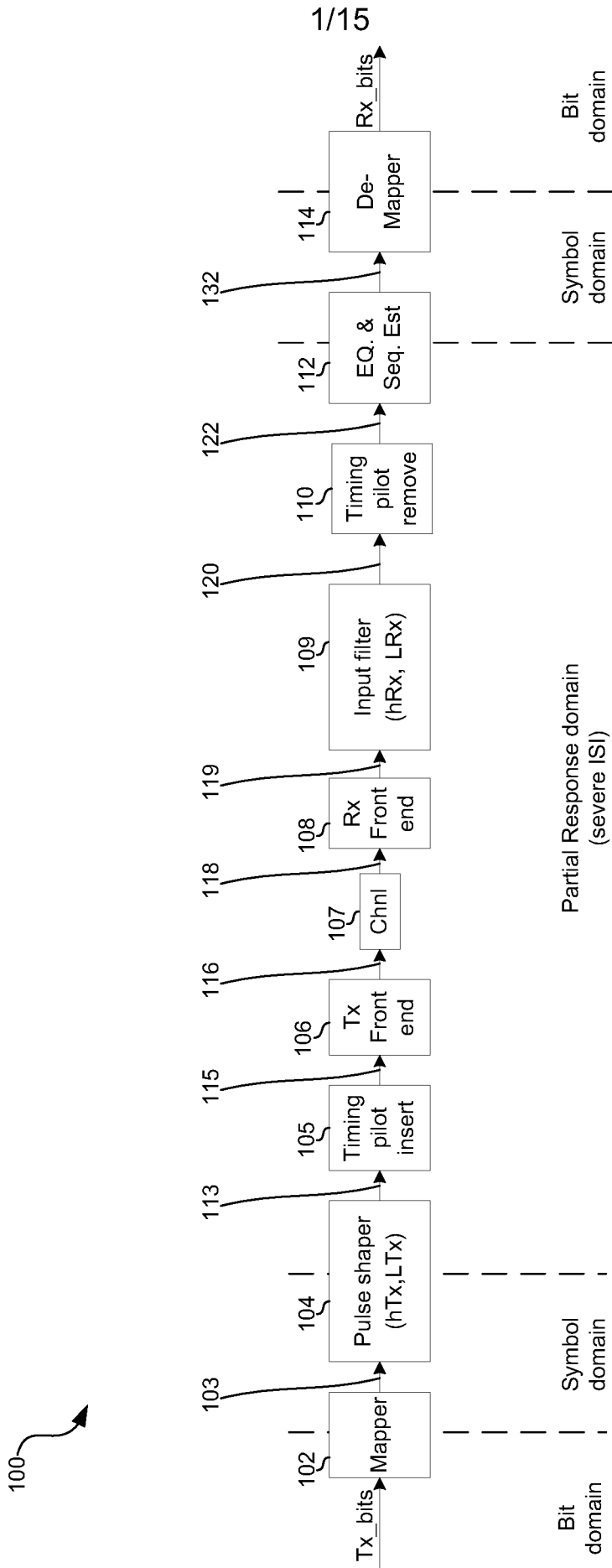


FIG. 1

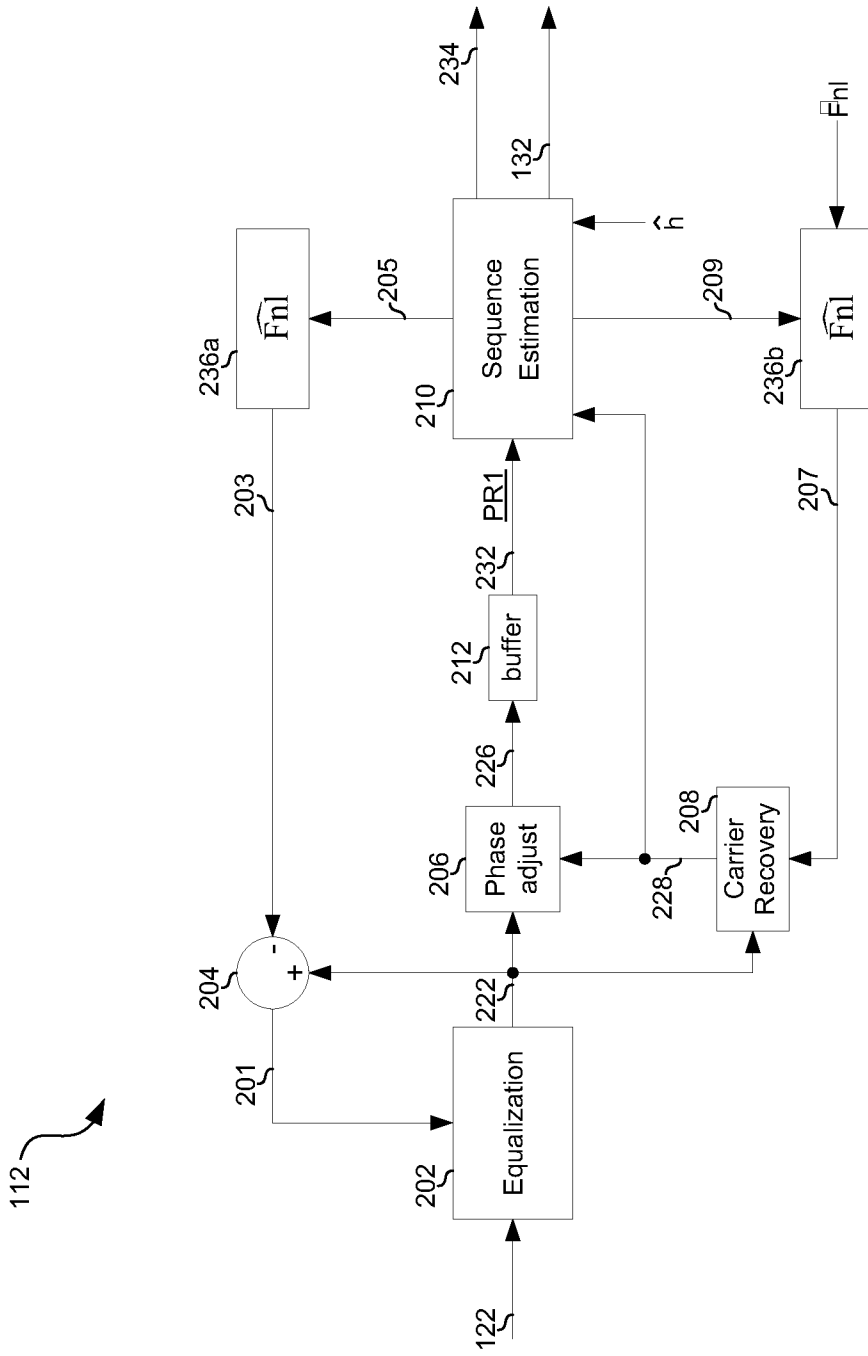


FIG. 2

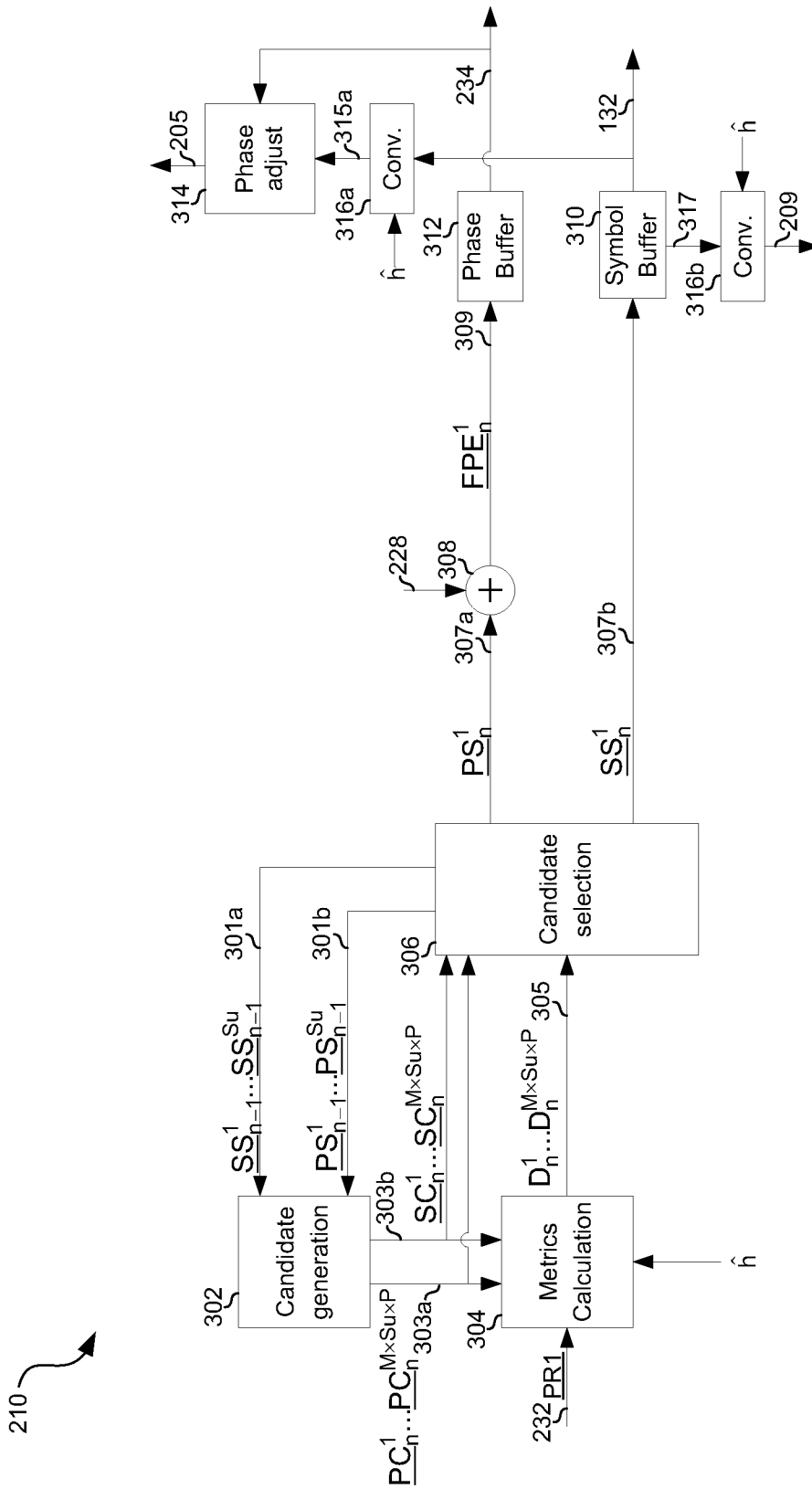


FIG. 3

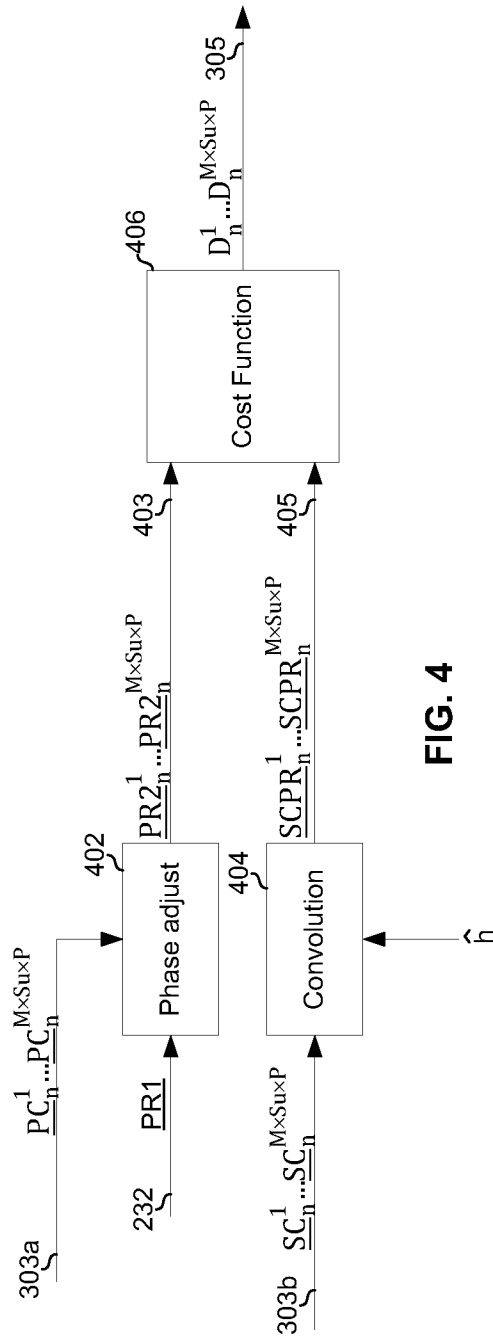


FIG. 4

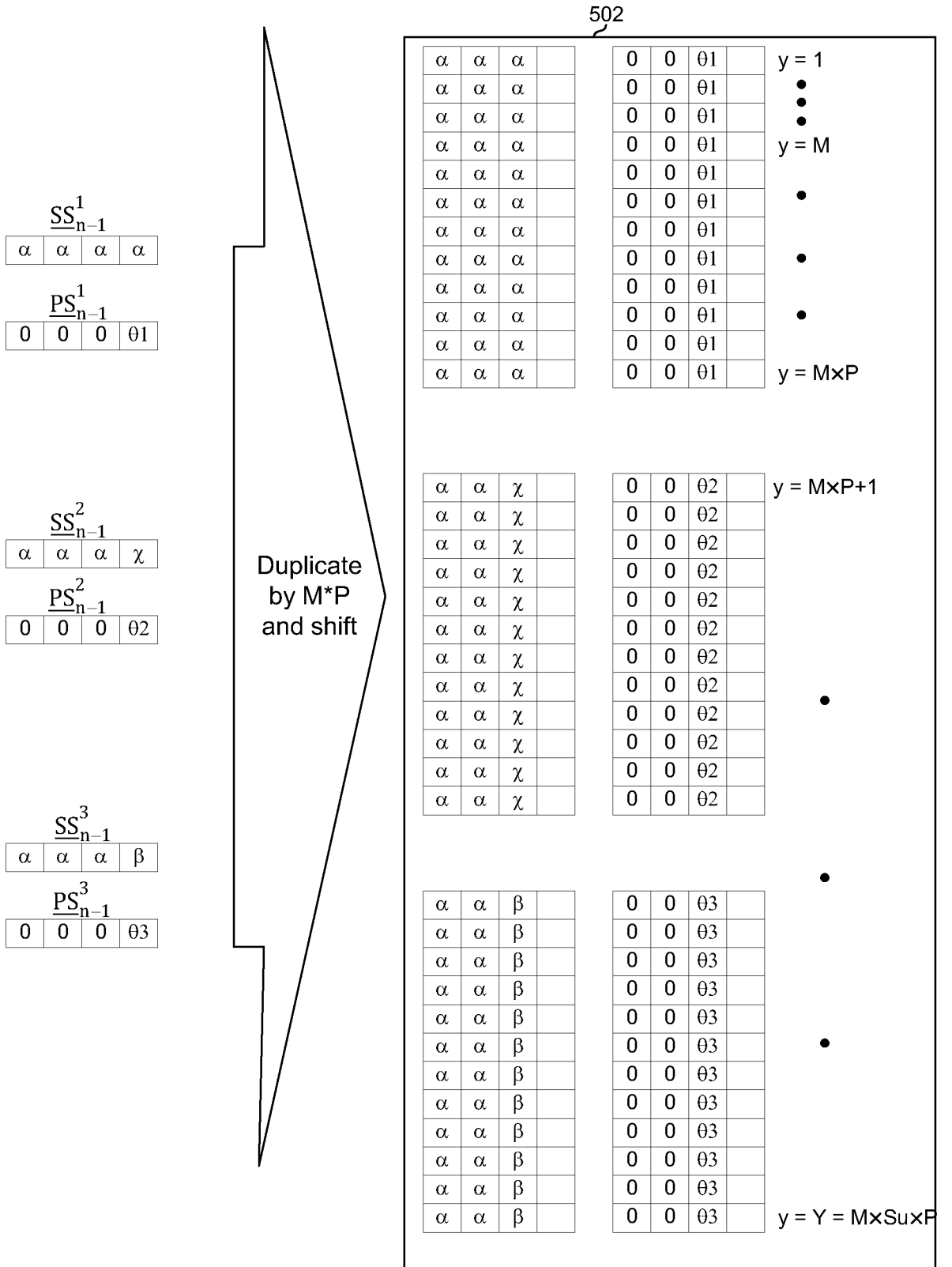
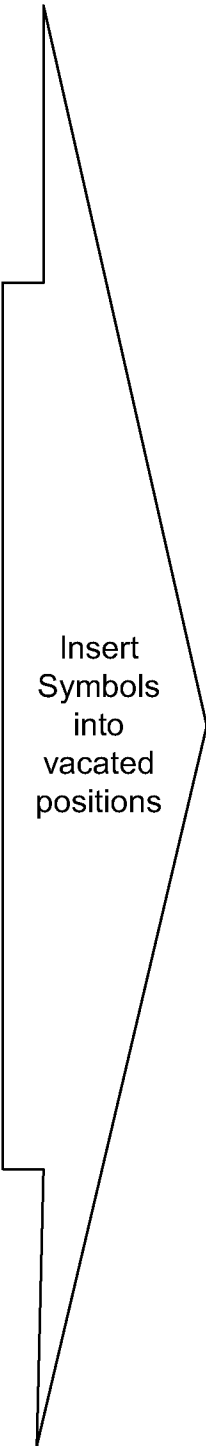


FIG. 5A

504

502
(FIG. 5A)



\underline{SC}_n				\underline{PC}_n				
α	α	α	α	0	0	01	04	$y = 1$
α	α	α	β	0	0	01	04	•
α	α	α	χ	0	0	01	04	•
α	α	α	δ	0	0	01	04	$y = M$
α	α	α	α	0	0	01	05	•
α	α	α	β	0	0	01	05	•
α	α	α	χ	0	0	01	05	•
α	α	α	δ	0	0	01	05	•
α	α	α	α	0	0	01	06	•
α	α	α	β	0	0	01	06	•
α	α	α	χ	0	0	01	06	•
α	α	α	δ	0	0	01	06	$y = M \times P$
α	α	χ	α	0	0	02	07	$y = M \times P + 1$
α	α	χ	β	0	0	02	07	•
α	α	χ	χ	0	0	02	07	•
α	α	χ	δ	0	0	02	07	•
α	α	χ	α	0	0	02	08	•
α	α	χ	β	0	0	02	08	•
α	α	χ	χ	0	0	02	08	•
α	α	χ	δ	0	0	02	08	•
α	α	χ	α	0	0	02	09	•
α	α	χ	β	0	0	02	09	•
α	α	χ	χ	0	0	02	09	•
α	α	χ	δ	0	0	02	09	•
α	α	β	α	0	0	03	010	•
α	α	β	β	0	0	03	010	•
α	α	β	χ	0	0	03	010	•
α	α	β	δ	0	0	03	010	•
α	α	β	α	0	0	03	011	•
α	α	β	β	0	0	03	011	•
α	α	β	χ	0	0	03	011	•
α	α	β	δ	0	0	03	011	•
α	α	β	α	0	0	03	012	•
α	α	β	β	0	0	03	012	•
α	α	β	χ	0	0	03	012	•
α	α	β	δ	0	0	03	012	$y = Y = M \times SuxP$

FIG. 5B

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**Metrics
Calculation
Block**

504
(FIG. 5B)

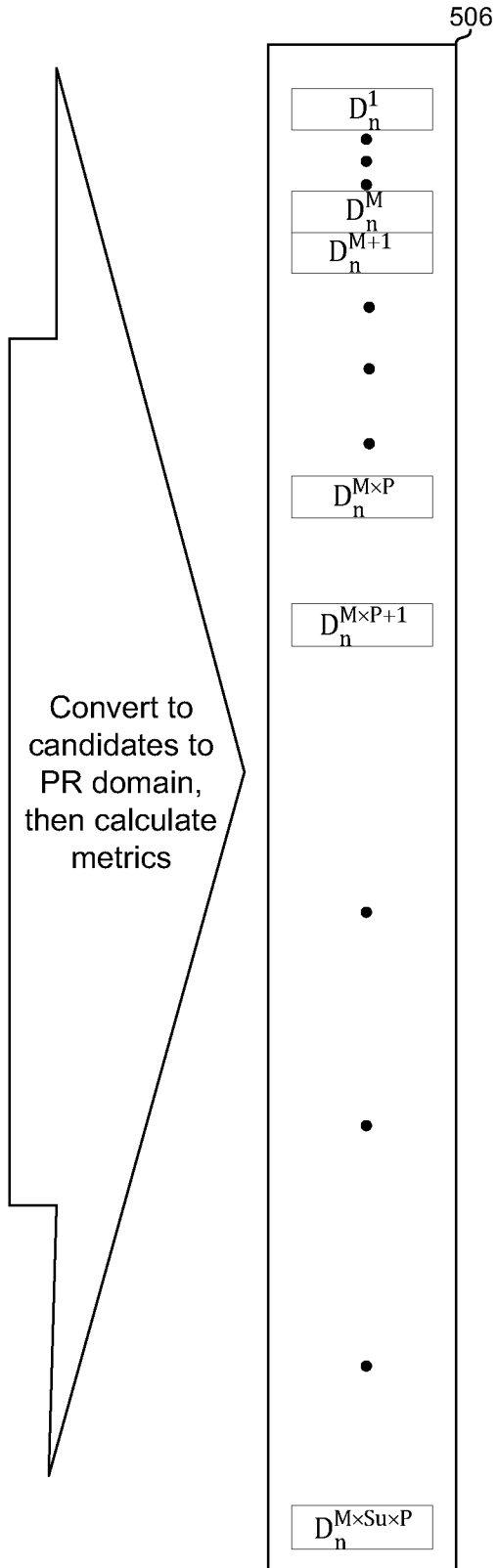


FIG. 5C

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One-Step Candidate Selection.

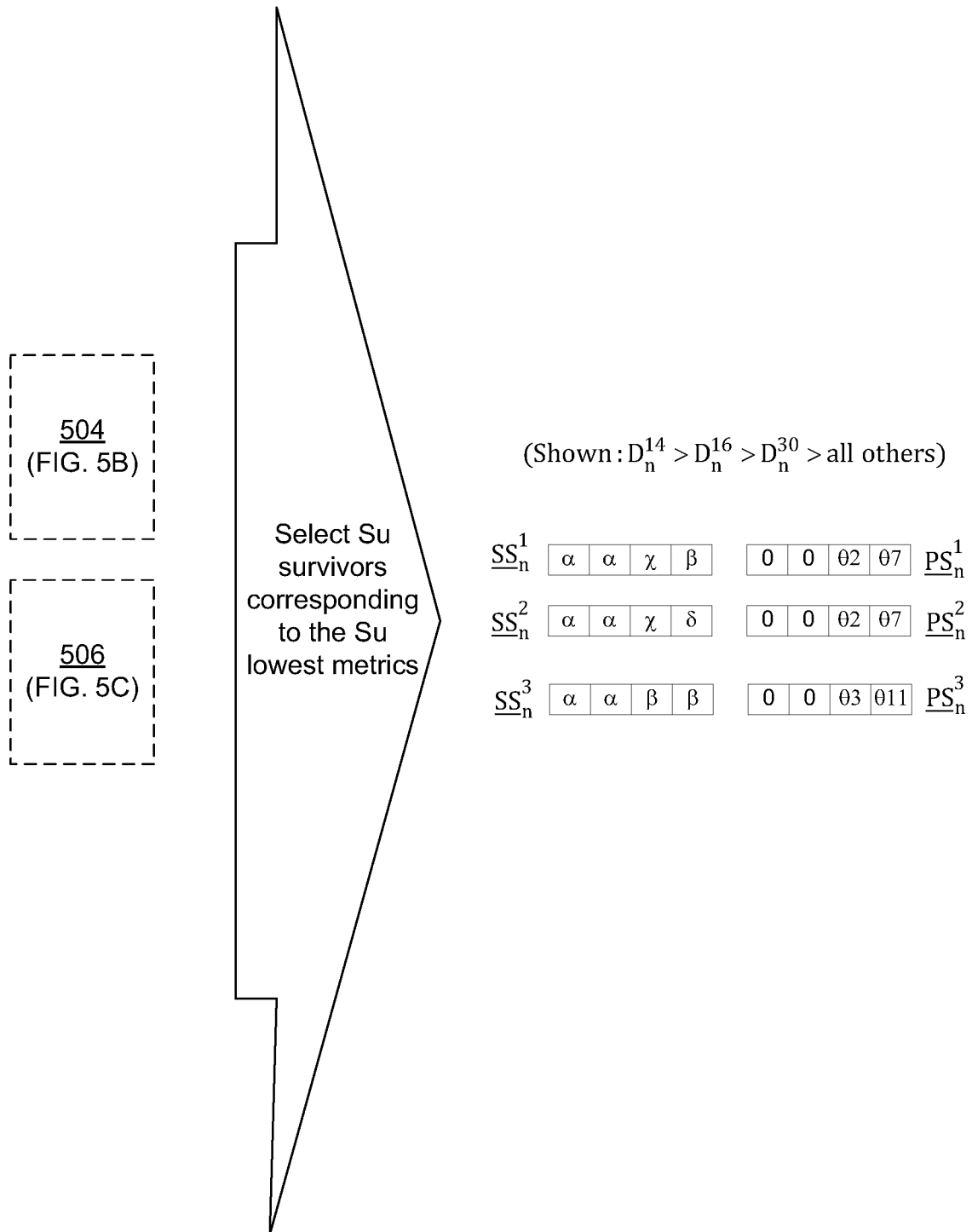


FIG. 5D

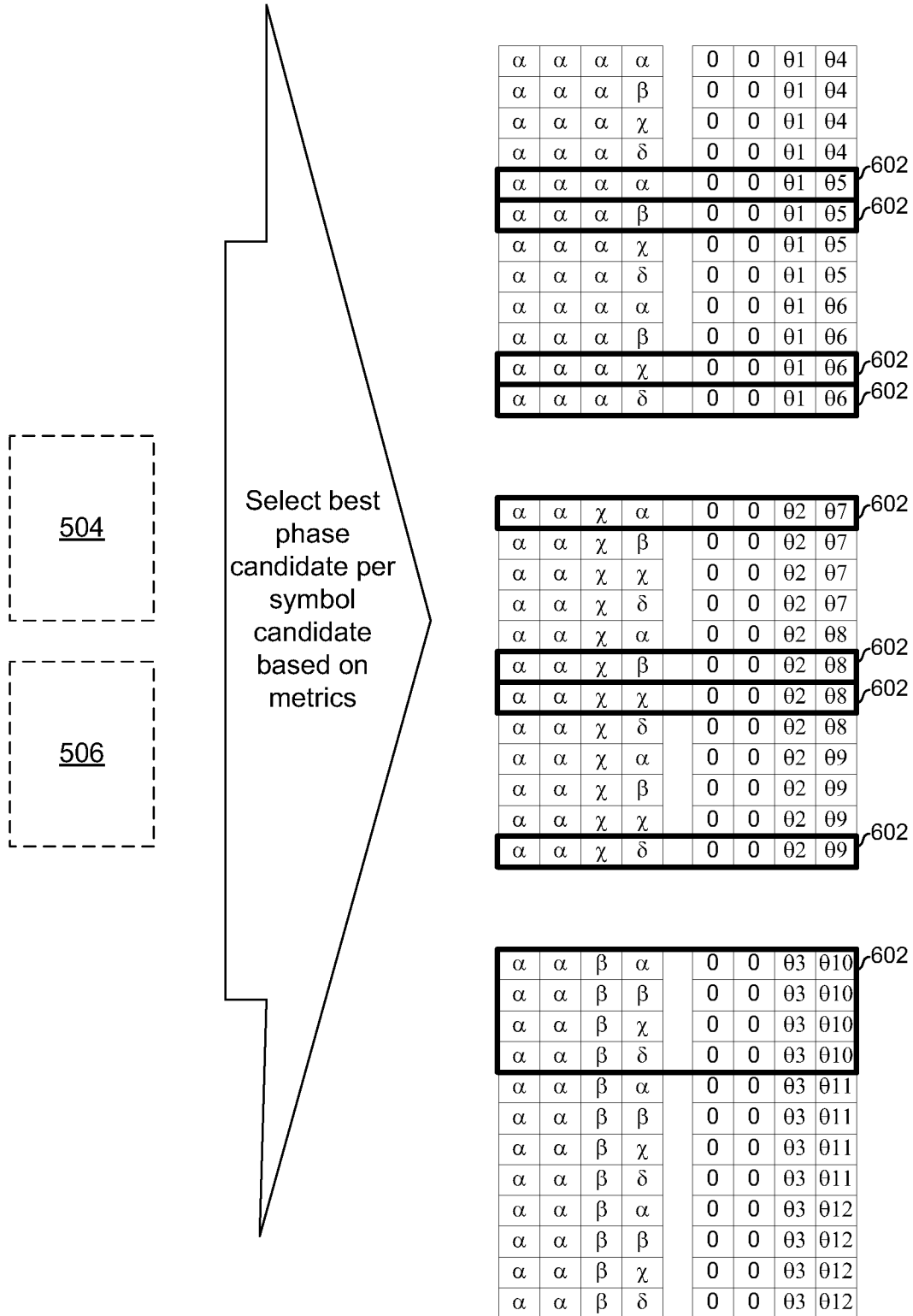
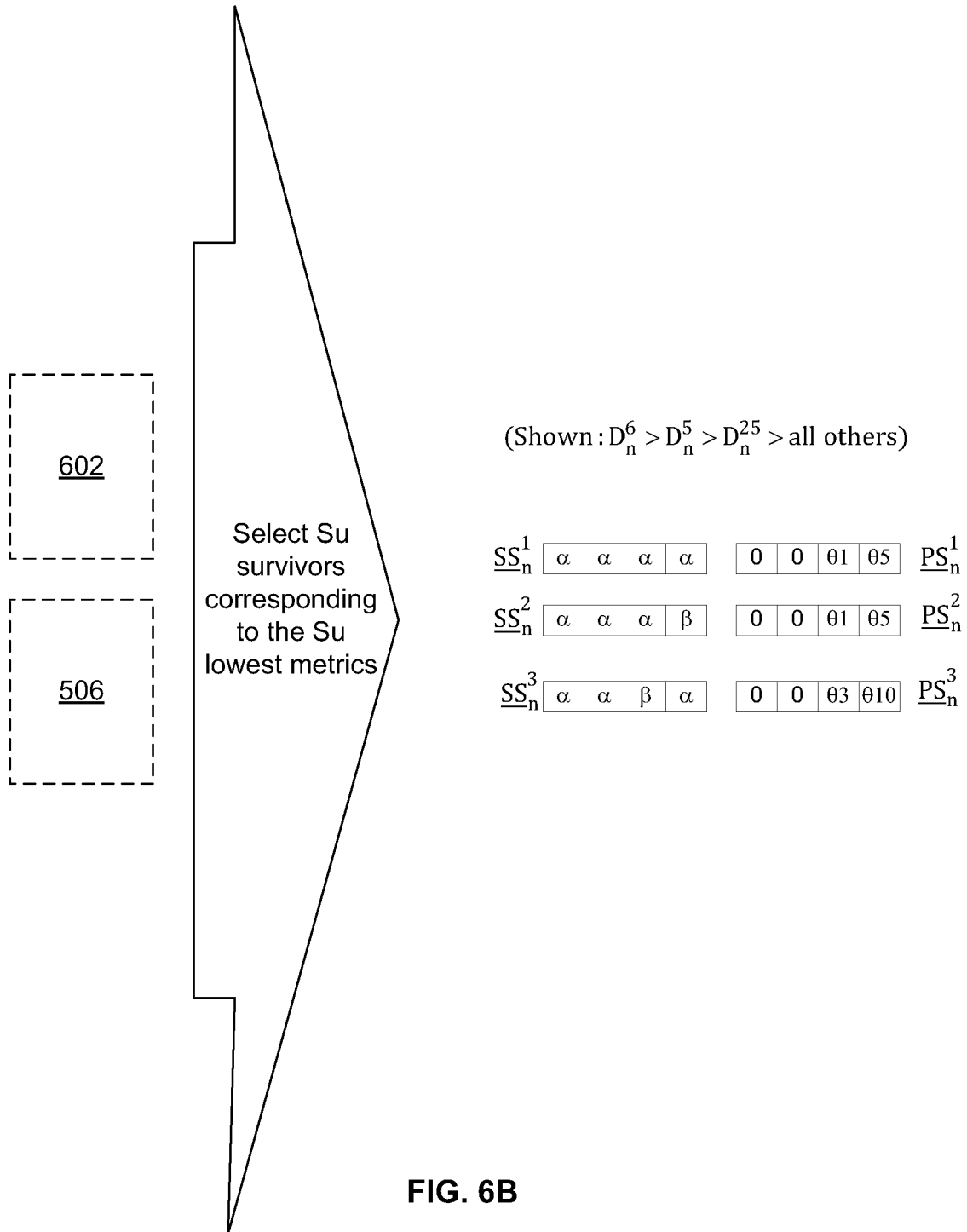


FIG. 6A



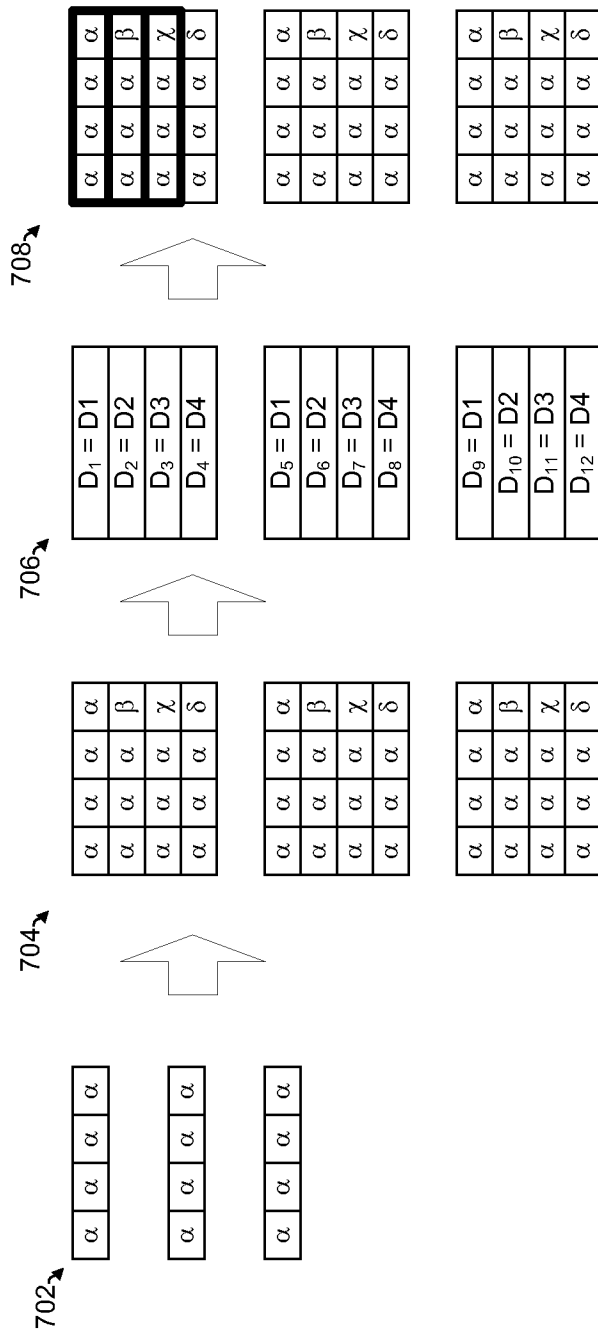


FIG. 7

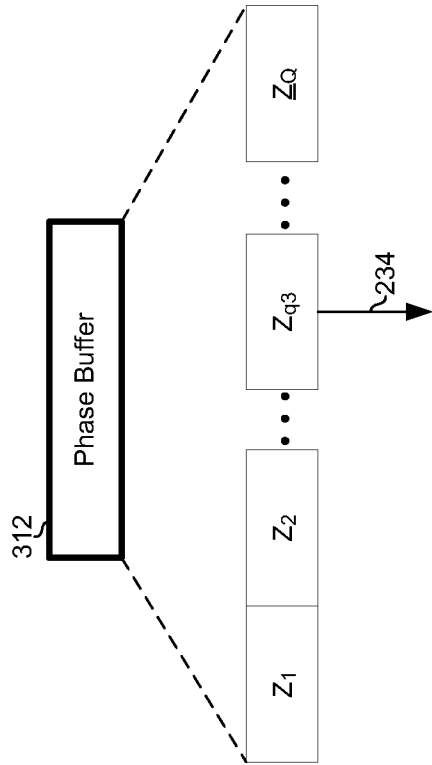


FIG. 8A

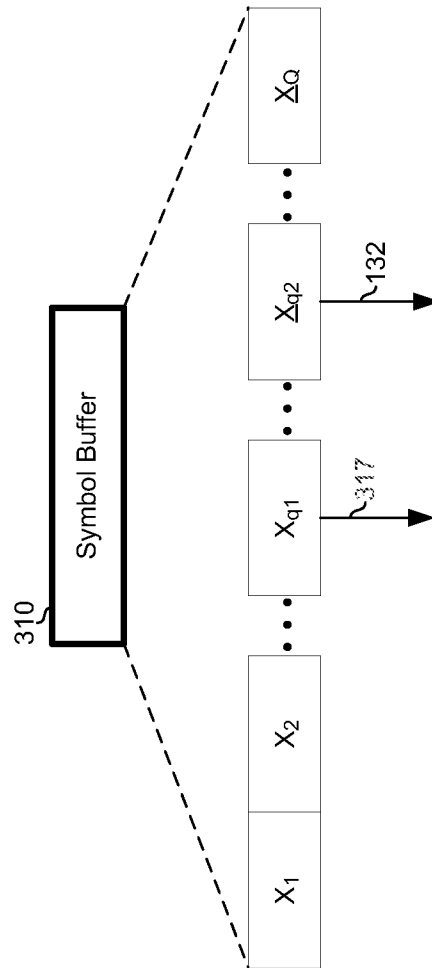


FIG. 8B

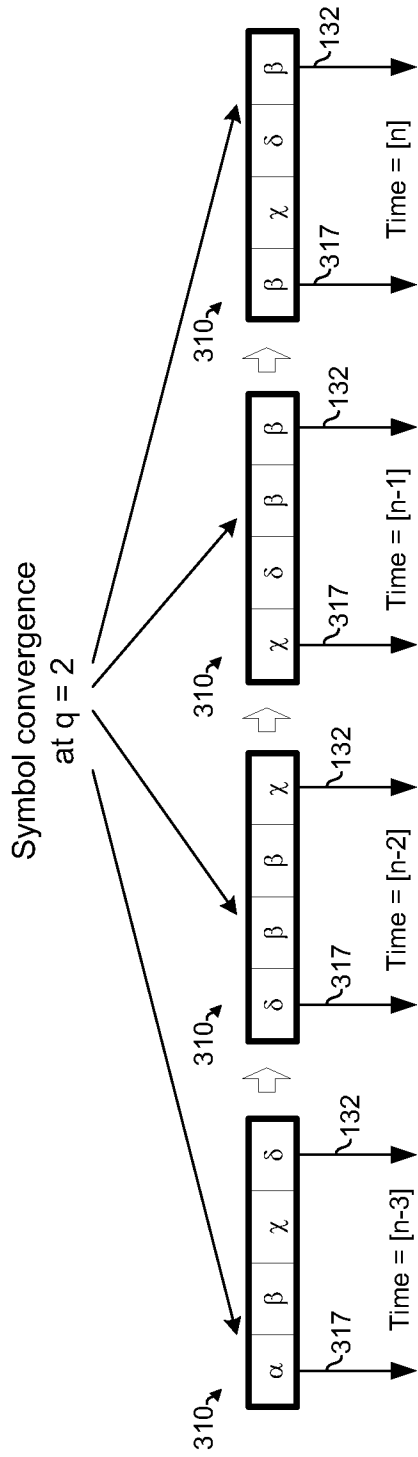


FIG. 8C

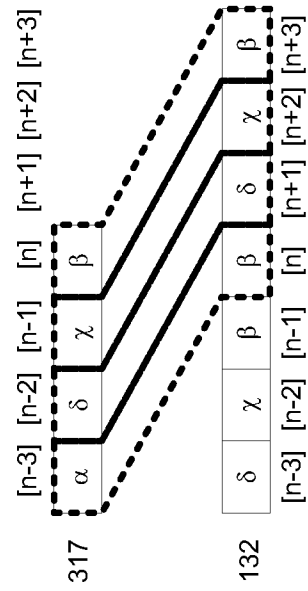


FIG. 8D

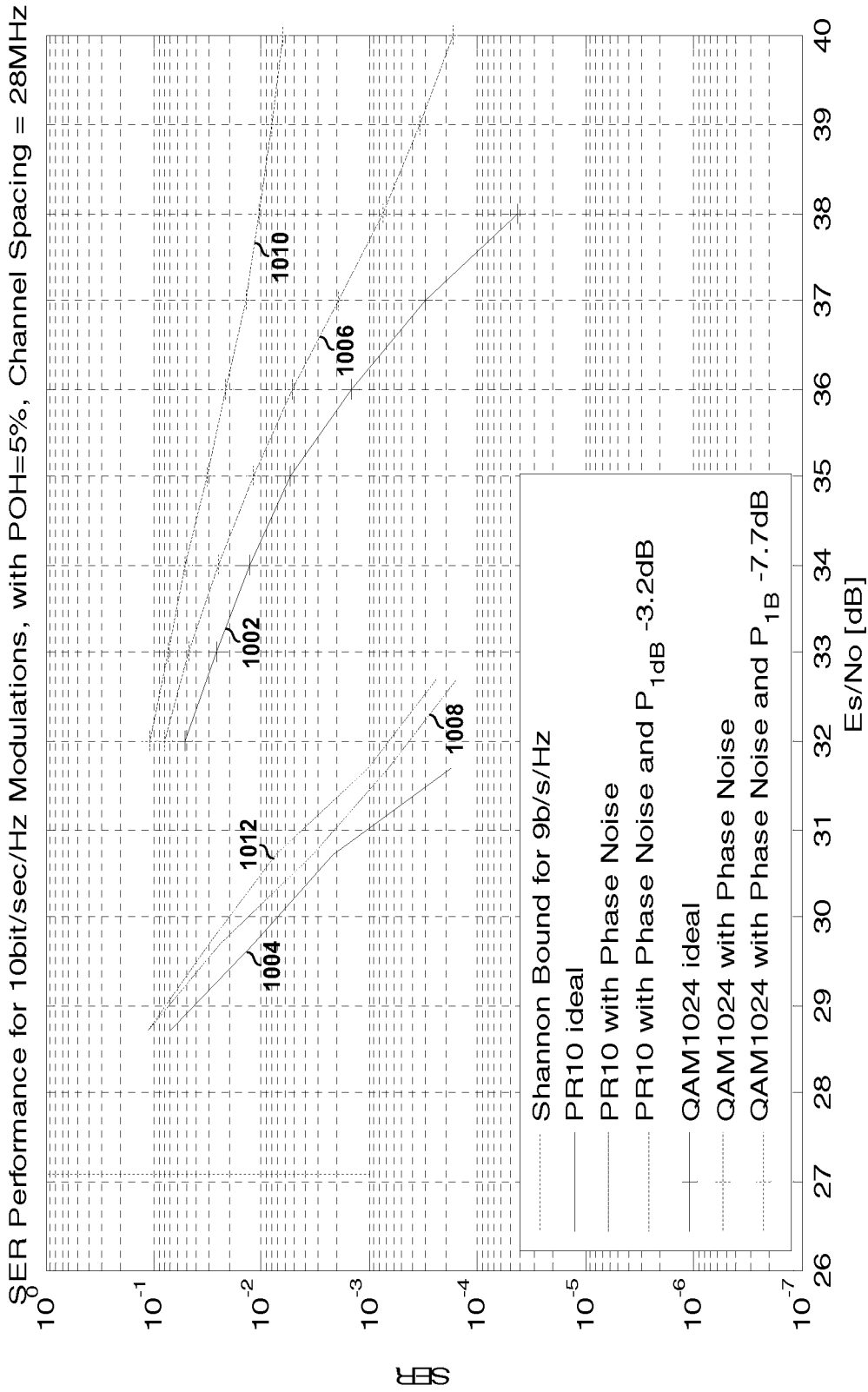


FIG. 9

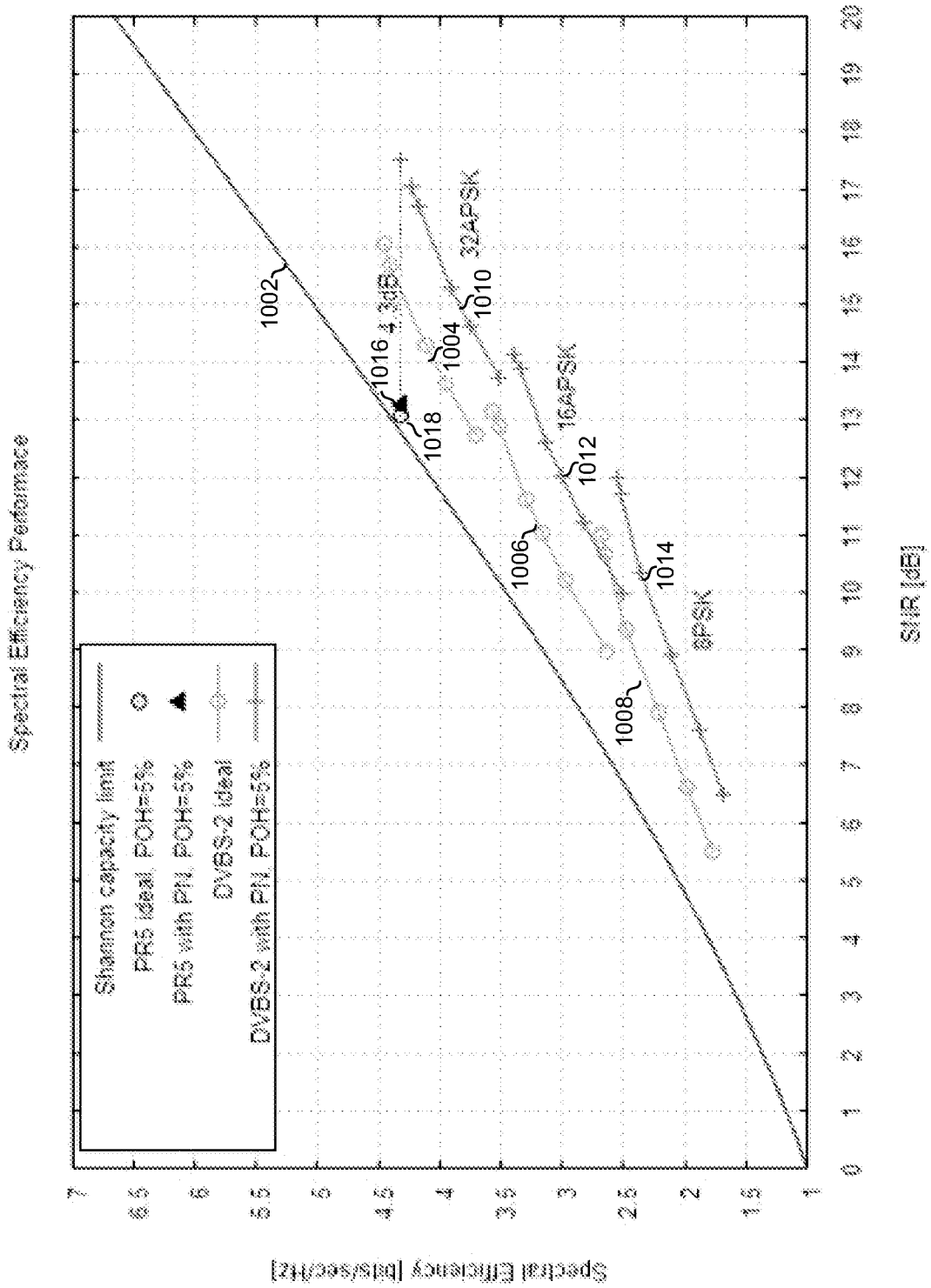


FIG. 10