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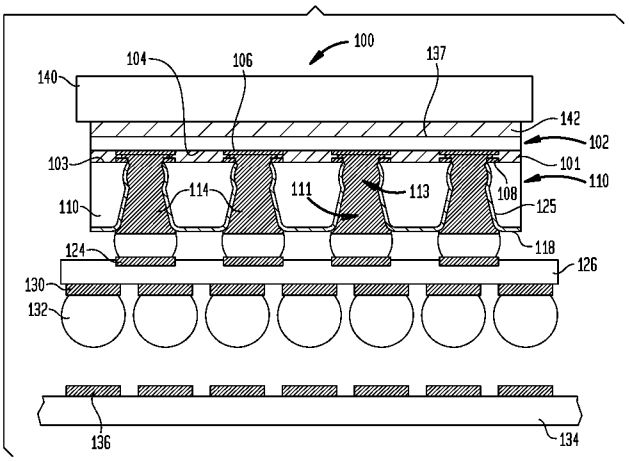
[Continued on next page]

(54) **Title**: MICROELECTRONIC ASSEMBLY WITH PLURAL STACKED ACTIVE CHIPS HAVING THROUGH - SILICON VIAS FORMED IN STAGES

FIG. 1



(57) **Abstract**: A microelectronic assembly 100 is provided in which first and second electrically conductive pads 108, 106 exposed at front surfaces of first and second microelectronic elements 110, 102, respectively, are juxtaposed, each of the microelectronic elements embodying active semiconductor devices. An electrically conductive element 114 may extend within a first opening 111 extending from a rear surface 118 of the first microelectronic element 110 towards the front surface 103 thereof, within a second opening 113 extending from the first opening 111 towards the front surface 103 of the first microelectronic element 110, and within a third opening 180 extending through at least one of the first and second pads 108, 106 to contact the first and second pads. Interior surfaces 121, 123 of the first and second openings 111, 113 may extend in first and second directions relative to the front surface 103 of the first microelectronic element 110, respectively, to define a substantial angle.

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MICROELECTRONIC ASSEMBLY WITH PLURAL STACKED ACTIVE CHIPS HAVING THROUGH - SILICON VIAS FORMED IN STAGES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of the filing date of United States Patent Application No. 13/051,414 filed March 18, 2011, which claims the benefit of United States Provisional Patent Application No. 61/419,037 filed December 2, 2010, the disclosures of which are hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to packaging of microelectronic devices, especially the packaging of semiconductor devices.

[0003] Microelectronic devices generally comprise a thin slab of a semiconductor material, such as silicon or gallium arsenide, commonly called a die or a semiconductor chip. Semiconductor chips are commonly provided as individual, prepackaged units. In some unit designs, the semiconductor chip is mounted to a substrate or chip carrier, which is in turn mounted on a circuit panel, such as a printed circuit board.

[0004] The active circuitry is fabricated in a first face of the semiconductor chip (*e.g.*, a front surface). To facilitate electrical connection to the active circuitry, the chip is provided with bond pads on the same face. The bond pads are typically placed in a regular array either around the edges of the die or, for many memory devices, in the die center. The bond pads are generally made of a conductive metal, such as copper, or aluminum, around 0.5 micron (μm) thick. The bond pads could include a single layer or multiple layers of metal. The size of the bond pads will vary with the device type but will typically measure tens to hundreds of microns on a side.

[0005] Through-silicon vias (TSVs) can be used to provide electrical connections between the front surface of a semiconductor chip on which bond pads are disposed, and a rear surface of a semiconductor chip opposite the front surface. Conventional TSV holes may reduce the portion of the first face that can be used to contain the active circuitry. Such a reduction in the available space on the first face that can be used for active circuitry may increase the amount of silicon required to produce each semiconductor chip, thereby potentially increasing the cost of each chip.

[0006] Size is a significant consideration in any physical arrangement of chips. The demand for more compact physical arrangements of chips has become even more intense with the rapid progress of portable electronic devices. Merely by way of example, devices commonly referred to as "smart phones" integrate the functions of a cellular telephone with powerful data processors, memory and ancillary devices such as global positioning system receivers, electronic cameras, and local area network connections along with high-resolution displays and associated image processing chips. Such devices can provide capabilities such as full internet connectivity, entertainment including full-resolution video, navigation, electronic banking and more, all in a pocket-size device. Complex portable devices require packing numerous chips into a small space. Moreover, some of the chips have many input and output connections, commonly referred to as "I/O's." These I/O's must be interconnected with the I/O's of other chips. The interconnections should be short and should have low impedance to minimize signal propagation delays. The components which form the interconnections should not greatly increase the size of the assembly. Similar needs arise in other applications as, for example, in data servers such as those used in internet search engines. For example, structures which provide numerous short, low-impedance

interconnects between complex chips can increase the bandwidth of the search engine and reduce its power consumption.

[0007] Despite the advances that have been made in semiconductor via formation and interconnection, further improvements can be made to enhance the processes for making connections between front and rear chip surfaces, and to the structures which can result from such processes.

SUMMARY OF THE INVENTION

[0008] In accordance with an aspect of the invention, a microelectronic assembly can include a first microelectronic element having a front surface and a first electrically conductive pad exposed at the front surface, a second microelectronic element having a front surface and a second electrically conductive pad exposed thereat, and an electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the front surface thereof. The front surfaces of the first and second microelectronic elements can face one another. The first and second pads can be juxtaposed. Each of the microelectronic elements can embody active semiconductor devices. The electrically conductive element can also extend within a second opening extending from the first opening towards the front surface of the first microelectronic element. The electrically conductive element can also extend within a third opening extending through at least one of the first and second pads. Interior surfaces of the first and second openings can extend in first and second directions relative to the front surface of the first microelectronic element, respectively, to define a substantial angle. The electrically conductive element can contact the first and second pads.

[0009] In a particular embodiment, the third opening can extend from the second opening through at least the first pad of the first microelectronic element. In one embodiment, the

third opening can extend through each of the first and second pads. In an exemplary embodiment, the third opening can extend from a second surface of the second microelectronic element through at least the second pad of the second microelectronic element. In a particular embodiment, the electrically conductive element can include at least one of a metal or a conductive compound of a metal between juxtaposed surfaces of the first and second pads. In one embodiment, the electrically conductive element can conform to a contour of at least a portion of the interior surface of at least one of the first or second openings.

[0010] In an exemplary embodiment, the electrically conductive element may not conform to a contour of at least a portion of the interior surface of at least one of the first or second openings. In a particular embodiment, the electrically conductive element can conform to a contour of at least a portion of an interior surface the third opening. In one embodiment, the electrically conductive element may not conform to a contour of at least a portion of the interior surface of the third opening. In an exemplary embodiment, the first opening in the first microelectronic element and the opening in the second microelectronic element can be tapered, becoming smaller in opposite directions from one another.

[0011] In accordance with another aspect of the invention, a microelectronic assembly can include a first microelectronic element having a first surface and an electrically conductive pad exposed at the first surface, a second microelectronic element having a first surface facing the first surface of the first microelectronic element and an electrically conductive pad exposed at the first surface and juxtaposed with the conductive pad of the first microelectronic element, and an electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the first surface thereof.

Each of the microelectronic elements can embody active semiconductor devices. The electrically conductive element can also extend within a second opening extending through at least one of the juxtaposed electrically conductive pads. The electrically conductive element can include at least one of a metal or a conductive compound of a metal between juxtaposed surfaces of the pads.

[0012] In one embodiment, the first opening can include a third opening extending from the rear surface of the first microelectronic element towards the first surface thereof and a fourth opening extending from the third opening in a direction towards the first surface of the first microelectronic element. Interior surfaces of the third and fourth openings can extend in first and second directions relative to the first surface, respectively, to define a substantial angle. In a particular embodiment, the second opening can extend through the pad of the first microelectronic element. In an exemplary embodiment, the second opening can include a third opening extending from the rear surface of the second microelectronic element towards the first surface of the second microelectronic element. The second opening can extend through the pad of the second microelectronic element.

[0013] In accordance with yet another aspect of the invention, a microelectronic assembly can include a first microelectronic element having a front surface and an electrically conductive pad exposed at the front surface, a second microelectronic element having a front surface facing the front surface of the first microelectronic element and an electrically conductive pad exposed at the front surface and juxtaposed with the conductive pad of the first microelectronic element, and an electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the front

surface thereof. Each of the microelectronic elements can embody active semiconductor devices. The electrically conductive element can also extend within a second opening extending from a rear surface of the second microelectronic element towards the front surface thereof. Interior surfaces of the first and second openings can extend in first and second directions relative to the front surface, respectively, to define a substantial angle. The electrically conductive element can extend through at least one of the juxtaposed pads, and can contact the pads.

[0014] In accordance with still another aspect of the invention, a microelectronic assembly can include a first microelectronic element having a front surface and a first electrically conductive pad exposed at the front surface, and a first electrically conductive element extending along the front surface away therefrom, a second microelectronic element having a front surface facing the front surface of the first microelectronic element, a second electrically conductive element extending within an opening extending from a rear surface of the first microelectronic element towards the front surface thereof, and a third electrically conductive element extending within an opening extending from a rear surface of the second microelectronic element towards the front surface thereof. The second microelectronic element can also have a second electrically conductive pad exposed at the front surface thereof and juxtaposed with a portion of the first electrically conductive element. The first and second microelectronic elements can embody active semiconductor devices. The second conductive element can contact the first conductive pad. The third conductive element can extend through an opening in the second conductive pad and can contact the second conductive pad and the first conductive element.

[0015] In a particular embodiment, the opening in the first microelectronic element can include a first opening extending from a rear surface of the first microelectronic element towards the front surface thereof, and a second opening extending from the first opening towards the front surface of the first microelectronic element. Interior surfaces of the first and second openings can extend in first and second directions relative to the front surface, respectively, to define a substantial angle. The second conductive element can contact the first and second pads. In one embodiment, the opening in the second microelectronic element can include a first opening extending from a rear surface of the second microelectronic element towards the front surface thereof, and a second opening extending from the first opening towards the front surface of the second microelectronic element. Interior surfaces of the first and second openings extend in first and second directions relative to the front surface, respectively, to define a substantial angle. The second conductive element can contact the first and second pads.

[0016] In an exemplary embodiment, the second and third conductive elements can be spaced apart from one another in a direction along the front surfaces of the microelectronic elements. In a particular embodiment, the first conductive element can have an upper surface exposed at the front surface of the second microelectronic element and the second conductive element can contact at least a portion of the upper surface. In one embodiment, at least a portion of the first conductive element can be an electrically conductive trace. In an exemplary embodiment, the microelectronic assembly can also include a third microelectronic element having a front surface facing the rear surface of the second microelectronic element, and a fourth electrically conductive element extending within an opening extending from the rear surface of the third microelectronic element. The third conductive

element can extend through the conductive pad of the third microelectronic element and can contact the second conductive element.

[0017] In one embodiment, the microelectronic assembly can also include one or more fourth microelectronic elements each stacked to overlie the rear surface of the third microelectronic element and being electrically coupled with the third conductive element thereof. Each fourth microelectronic element can have a front surface facing the rear surface of the third or fourth microelectronic element adjacent thereto. The microelectronic assembly can have a fifth electrically conductive element extending within at least an opening extending from the rear surface of the fourth microelectronic element and extending through the conductive pad of such fourth microelectronic element and contacting the conductive element extending through the microelectronic element adjacent thereto.

[0018] Further aspects of the invention can provide systems that incorporate microelectronic structures according to the foregoing aspects of the invention, and one or more other electronic components electrically connected to the structures. For example, the system may also include a housing, said structure and said other electronic components being mounted to said housing. Systems according to preferred embodiments in this aspect of the invention may be more compact than comparable conventional systems.

[0019] In accordance with another aspect of the invention, a method of fabricating a microelectronic assembly can include the steps of: (a) assembling a first microelectronic element with a second microelectronic element such that a first surface of the first microelectronic element faces a first surface of the second microelectronic element, each of the microelectronic elements embodying active semiconductor devices, such that electrically conductive pads exposed at the

first surfaces of the microelectronic elements are juxtaposed with each other, and (b) then forming an electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the first surface thereof, within a second opening extending from the first opening towards the first surface of the first microelectronic element, and within a third opening extending through at least one of the juxtaposed electrically conductive pads, wherein interior surfaces of the first and second openings extend in first and second directions relative to the first surface respectively defining a substantial angle, the electrically conductive element contacting the juxtaposed electrically conductive pads.

[0020] In a particular embodiment, the step of forming the electrically conductive element can include depositing at least one of metal or a conductive compound of a metal onto juxtaposed surfaces of the pads. In one embodiment, the step of forming the electrically conductive element can include forming an undercut between the juxtaposed surfaces of the pads. The step of depositing can deposit the at least one of a metal or a conductive compound of metal within the undercut. In an exemplary embodiment, the third opening can extend from a second surface of the second microelectronic element through at least the juxtaposed pad of the first microelectronic element.

[0021] In one embodiment, the third opening can extend through at least the juxtaposed pad of the second microelectronic element. In a particular embodiment, the step of forming the electrically conductive element can include forming the first opening and then forming the third opening by different processes. In an exemplary embodiment, the electrically conductive element can conform to a contour of an interior surface of at least one of the first and second openings. In one embodiment, the electrically conductive

element may not conform to a contour of an interior surface of at least one of the first and second openings.

[0022] In accordance with yet another aspect of the invention, a method of fabricating a microelectronic assembly can include the steps of: (a) assembling a first microelectronic element with a second microelectronic element such that a first surface of the first microelectronic element faces a first surface of the second microelectronic element, each of the microelectronic elements embodying active semiconductor devices, such that electrically conductive pads exposed at the first surfaces of the microelectronic elements are juxtaposed with each other, and (b) then forming an electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the first surface thereof and within a second opening extending through at least one of the juxtaposed electrically conductive pads, the forming of the electrically conductive element including depositing at least one of a metal or a conductive compound of a metal onto juxtaposed surfaces of the pads.

[0023] In an exemplary embodiment, the step of forming the electrically conductive element can include forming an undercut between the juxtaposed surfaces of the pads. The step of depositing can deposit the at least one of a metal or a conductive compound of metal within the undercut. In one embodiment, the first opening can include a third opening extending from the rear surface of the first microelectronic element towards the first surface thereof and a fourth opening extending from the opening to the second opening. Interior surfaces of the first and second openings can extend in first and second directions relative to the first surface respectively defining a substantial angle. The second opening can extend through the pad of the first microelectronic element. In a particular embodiment, the second opening can

include a third opening extending from the rear surface towards the first surface of the first microelectronic element and a fourth opening extending from the third opening through the pad of the second microelectronic element.

[0024] In accordance with still another aspect of the invention, a method of fabricating a microelectronic assembly can include the steps of: (a) assembling a first microelectronic element with a second microelectronic element such that a first surface of the first microelectronic element faces a first surface of the second microelectronic element, each of the microelectronic elements embodying active semiconductor devices, such that electrically conductive pads exposed at the first surfaces of the microelectronic elements are juxtaposed with each other, and (b) then forming an electrically conductive element extending within a first opening extending from a second surface of the first microelectronic element towards the first surface thereof, within a second opening extending from a second surface of the second microelectronic element towards the first surface thereof, wherein interior surfaces of the first and second openings extend in first and second directions relative to the first surface respectively defining a substantial angle, the electrically conductive element extending through at least one of the juxtaposed pads and contacting the pads.

[0025] In accordance with another aspect of the invention, a method of fabricating a microelectronic assembly can include the steps of: (a) assembling a first microelectronic element with a second microelectronic element such that a first surface of the first microelectronic element faces a first surface of the second microelectronic element, each of the microelectronic elements embodying active semiconductor devices, such that an electrically conductive pad exposed at the first surface of one of the microelectronic elements is juxtaposed with a first conductive element exposed at the

first surface of another of the microelectronic elements, and (b) then forming a second electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the first surface thereof, within a second opening extending from the first opening towards the first surface of the first microelectronic element, and within a third opening extending through at least one of the pad or the first electrically conductive element, wherein interior surfaces of the first and second openings extend in first and second directions relative to the first surface respectively defining a substantial angle, the second conductive element contacting the pad and the first electrically conductive element.

[0026] In a particular embodiment, the pad can be a first pad exposed at the first surface of the first microelectronic element and the second microelectronic element can include a second electrically conductive pad spaced in a direction along the first surface of the second microelectronic element from the first pad. The first conductive element can extend along the first surface of the second microelectronic element and can be electrically coupled with the second pad. In one embodiment, the pad can be a first pad exposed at the first surface of the second microelectronic element and the first microelectronic element can include a second electrically conductive pad spaced in a direction along the first surface of the first microelectronic element from the first pad. The first conductive element can extend along the first surface of the first microelectronic element and can be electrically coupled with the second pad. In an exemplary embodiment, the second conductive element can extend through the first pad.

[0027] In one embodiment, the second pad can have an upper surface facing in a direction away from the second microelectronic element and the first conductive element can contact at least a portion of the upper surface of the second

pad. In a particular embodiment, the method can also include forming the first conductive element in contact with at least a portion of the upper surface of the second pad before step (a). In an exemplary embodiment, at least a portion of the first conductive element can be an electrically conductive trace extending along the surface of the first microelectronic element in a direction between the second pad and a location of the first microelectronic element juxtaposed with the first pad.

[0028] In an exemplary embodiment, the third opening can extend through the first pad and a portion of the second conductive element can further extend within the third opening and can contact the first pad. In one embodiment, a portion of the second conductive element can further extend within an opening extending from a rear surface of the second microelectronic element through the second pad. In a particular embodiment, the method can also include assembling a third microelectronic element with the first and second microelectronic elements such that a first surface of the third microelectronic element faces the second surface of the second microelectronic element, and then forming a third electrically conductive element extending within at least an opening extending from the second surface of the third microelectronic element. The third conductive element can extend through the conductive pad of the third microelectronic element and can contact the second conductive element.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] Fig. 1 is a sectional view illustrating a microelectronic assembly in accordance with an embodiment of the invention, positioned for attachment with a circuit panel.

[0030] Fig. 1A is a fragmentary sectional view showing an enlarged view in greater detail of a conductive element in a microelectronic assembly in accordance with an embodiment of the invention.

[0031] Fig. 2 is a sectional view illustrating a microelectronic assembly in accordance with an embodiment of the invention, as mounted to a circuit panel.

[0032] Fig. 3 is plan view further illustrating a microelectronic assembly in accordance with an embodiment of the invention.

[0033] Fig. 4 is a sectional view illustrating a microelectronic assembly in accordance with a variation of the embodiment of the invention shown in Fig. 1.

[0034] Figs. 5 and 6 are sectional views illustrating stages in a method of fabricating a microelectronic assembly according to an embodiment of the invention.

[0035] Figs. 7, 8, 9, and 10 are fragmentary sectional views illustrating stages subsequent to the stage shown in Fig. 6, in a method of fabricating a microelectronic assembly according to an embodiment of the invention.

[0036] Fig. 11 is a fragmentary sectional view illustrating a stage of fabricating a microelectronic assembly according to an embodiment of the invention which can occur after or before the stages of fabrication illustrated in Figs. 7, 8, 9 and 10.

[0037] Fig. 12 is a fragmentary sectional view illustrating a microelectronic assembly according to a variation of the embodiment illustrated in Fig. 11.

[0038] Fig. 13 is a fragmentary sectional view illustrating a microelectronic assembly according to another variation of the embodiment illustrated in Fig. 11.

[0039] Fig. 14 is a fragmentary sectional view illustrating a microelectronic assembly according to another variation of the embodiment illustrated in Fig. 11.

[0040] Fig. 15 is a fragmentary sectional view illustrating a microelectronic assembly according to another variation of the embodiment illustrated in Fig. 11.

[0041] Figs. 16, 17, 18, and 19 are fragmentary sectional views illustrating stages subsequent to the stage shown in

Fig. 6, in a method of fabricating a microelectronic assembly according to a variation of the embodiment of the invention shown in Figs. 7, 8, 9 and 10.

[0042] Fig. 20 is a fragmentary sectional view illustrating a microelectronic assembly according to another embodiment of the invention.

[0043] Fig. 21 is a fragmentary sectional view illustrating a microelectronic assembly according to a variation of the embodiment of the invention shown in Fig. 20.

[0044] Fig. 22 is a fragmentary sectional view illustrating a microelectronic assembly according to another embodiment of the invention.

[0045] Fig. 23 is a fragmentary sectional view illustrating a microelectronic assembly according to a variation of the embodiment shown in Fig. 22.

[0046] Fig. 24 is a fragmentary sectional view illustrating a microelectronic assembly according to another embodiment of the invention.

[0047] Fig. 25 is a fragmentary sectional view illustrating a microelectronic assembly according to a variation of the embodiment of the invention shown in Fig. 24.

[0048] Fig. 26 is a schematic depiction of a system according to one embodiment of the invention.

DETAILED DESCRIPTION

[0049] Fig. 1 illustrates a microelectronic assembly 100 in accordance with an embodiment of the invention. The microelectronic package includes a microelectronic element 102, e.g., an integrated circuit embodied in a semiconductor chip, which can include silicon, an alloy of silicon, or other semiconductor material such as a III-V semiconductor material or II-VI semiconductor material. As seen in the enlarged view of Fig. 1A, the chip 102 has a front surface 104, also referred to as a contact-bearing face, being a major surface of the chip, with a first region 105 of the chip at the front

face. The first region 105 typically includes a dielectric region, which typically includes a plurality of wiring layers having dielectric layers disposed between and around the wiring layers. In a particular embodiment, the dielectric region can include one or more layers of dielectric material having a low dielectric constant, i.e., a "low-k" dielectric layer. Low-k dielectric materials include porous silicon dioxide, carbon-doped silicon dioxide, polymeric dielectrics, and porous polymeric dielectrics, among others. In a porous low-k dielectric layer, the dielectric layer can have substantial porosity, which reduces the dielectric constant of the dielectric material relative to a nonporous layer of the same material. Dielectric materials typically have a dielectric constant significantly above 1.0, but air which occupies open spaces within a porous dielectric material has a dielectric constant of about 1.0. In this way, some dielectric materials can achieve reductions in the dielectric constant by having substantial porosity.

[0050] However, some low-k dielectric materials, such as polymeric dielectric materials and porous dielectric materials, withstand much less mechanical stress than traditional dielectric materials. Particular types of operating environments and ways that the microelectronic element may be tested can present stress at or near a limit that the low-k dielectric material can tolerate. The microelectronic assemblies described herein provide improved protection for the low-k dielectric layer of a microelectronic element by moving the locations where stress is applied to the microelectronic element away from the low-k dielectric layer within region 105. In this way, manufacturing, operation and testing apply much reduced stresses to the low-k dielectric layer, thus protecting the low-k dielectric layer.

[0051] Layer 105 also includes active semiconductor devices (e.g., transistors, diodes, or other active devices), which

are ultimately connected by the wiring layers with a plurality of electrically conductive pads 106 at the front face. When the chip is a silicon-on-insulator ("SOI") type chip, the first region 105 may also include a buried dielectric layer which underlies the active semiconductor devices. The first region 105 may separate a second region 107 of the chip from the front face 104. The first region typically has a thickness of 0.1 micron to 5 microns, and typically cannot be thinned. The second region 107 typically consists essentially of semiconductor material (typically either monocrystalline or polycrystalline) and typically has a thickness under 20 microns, the thickness typically being determined by the degree to which an initial semiconductor wafer has been thinned during processing. In one embodiment, the chip may have only the first region 105 and the second region 107 may not be present.

[0052] As further seen in Fig. 1, another microelectronic element 110, a semiconductor chip embodying active semiconductor devices, is mounted with the microelectronic element 102 such that front surfaces 103, 104 of the microelectronic elements face one another. As shown in Fig. 1, a plurality of electrically conductive pads 108 of microelectronic element 110 can be juxtaposed with the conductive pads 106 of microelectronic element 102. The microelectronic elements typically are bonded together, such as with an adhesive 101. Other possible bonding materials can include glass, which in a particular embodiment, can be doped and can have a glass transition temperature below 500 °C. Typically, microelectronic element 110 consists essentially of the same semiconductor material as the other microelectronic element 102. As further seen in Fig. 1, microelectronic element 110 can have a plurality of conductive via elements extending through openings in the microelectronic element for

providing electrically conductive connections with the conductive pads 108, and 106.

[0053] The vias can be "staged vias" having multiple stages between a rear surface of one of the microelectronic elements and at least one conductive pad thereof, or alternatively, can be single stage vias, In one example, microelectronic element 110 can have a plurality of first openings 111 which extend from an exposed outwardly-facing surface 118 towards the chip front surface 104. A plurality of second openings 113 can extend from respective first openings 111 to respective conductive pads 106 of the chip. As further seen in Fig. 1A, at locations where the first and second openings meet, interior surfaces 121, 123 of the first and second openings extend at different angles 140, 142 relative to a plane defined by the major surface 104, which is the same as the angles 140, 142 relative to any plane 135 parallel to the major surface. Thus, the interior surfaces of the first and second openings extend in first and second directions, respectively, to define a substantial angle.

[0054] A plurality of conductive elements 114 extend within the first and second openings and are electrically coupled to the conductive pads 106, 108. The conductive elements 114 typically are insulated from other portions of chip 110 by an insulating layer 125 which can line interior surfaces 121, 123 of the first and second openings. The conductive elements 114 typically are exposed at an exposed outwardly-facing surface 118 of microelectronic element 110. In one example, the conductive elements 114 can include metal features which are formed by depositing a metal in contact with exposed surfaces of the conductive pads 106, 108. Various metal deposition steps can be used to form the conductive elements, as described in further detail below.

[0055] As further seen in Fig. 1, the conductive elements 114 can be conductively bonded, similar to a flip-chip manner,

to contacts 124 exposed at a surface of a dielectric element 126, such as through masses 128 of a bond metal, e.g., solder, tin, indium, or a combination thereof. In turn, the dielectric element can have a plurality of terminals 130 for further electrically connecting the package 100 to corresponding contacts 136 of a circuit panel 134, such as through conductive masses 132, e.g., solder balls, projecting away from the dielectric element 126. Fig. 1 illustrates the package 100 prior to joining the circuit panel 134 thereto. Fig. 2 illustrates a microelectronic assembly which includes the package 100 and the circuit panel 134 joined thereto.

[0056] A heat spreader 140 may be thermally coupled to a rear surface 137 of microelectronic element 102, such as through a thermally conductive material 142, e.g., a thermally conductive grease, thermally conductive adhesive, or a joining metal having a relatively low melting temperature such as solder, tin, indium, gold, or other material. When the thermally conductive material 142 is also electrically conductive, such as a metal or conductive compound of a metal, a dielectric layer (not shown) can separate the rear surface 137 of the microelectronic element 102 from such thermally and electrically conductive material 142.

[0057] Fig. 3 is a view looking toward the rear surface 118 of the microelectronic element 110 of the package illustrating conductive elements 114 exposed at the rear surface, which are shown arranged in an area array. As also shown in Fig. 3, the conductive elements 114 extend within second openings 123 and are connected to conductive pads 108 exposed at the front surface 103 (Fig. 1) of microelectronic element 110, which can also be arranged in an area array. Alternatively, when the conductive pads 108 of microelectronic element have a different arrangement, such as can be arranged adjacent peripheral edges 114, or can be arranged centrally to the

front surface, the conductive elements 114 typically have a matching pattern.

[0058] Fig. 4 illustrates a microelectronic package 150 according to another embodiment of the invention. As seen in Fig. 4, microelectronic element 102 may further include conductive elements 152 extending within openings 153 extending from a rear surface 154 of microelectronic element 102, the conductive elements 152 contacting the conductive pads 106. As further shown in Fig. 4, some conductive pads 106a may not be in contact with a conductive element 152 extending within an opening 153 in the microelectronic element. One or more conductive elements 152b may be electrically connected with a metallic heat spreader 140 or ground plane through an electrically and thermally conductive material 142 between them. However, other conductive elements 152a can be electrically isolated from such heat spreader or ground plane by a dielectric layer 144.

[0059] Referring to Fig. 5, a method of making a microelectronic package will now be described. As illustrated therein, a semiconductor wafer 160 or a portion of a wafer having a plurality of microelectronic elements 102 attached together as dicing lanes 164, is arranged such that a front surface 104 thereof faces a front surface 103 of another wafer 162 having a plurality of microelectronic elements 110 attached together at the dicing lanes 164. The wafers 160, 162 can be aligned such that multiple pairs of, or even all conductive pads 106, 108 of each wafer are juxtaposed with one another. Thereafter, as shown in Fig. 6, the wafers 160, 162 are bonded together, such as by an adhesive 101. Then, a thickness of wafer 160 can be reduced, such as by grinding, lapping, or polishing.

[0060] Fig. 7 is a fragmentary view illustrating a further step in processing in which staged openings 166 are created in the wafer 162 which includes microelectronic elements 110.

Fig. 7 shows a stage of processing after the staged opening 166 has been defined. Specifically, a staged opening 166 includes a first opening 168 extending from a rear surface 118 of microelectronic element 110 towards a front surface 103 thereof. A second opening 170 extends from the first opening towards the front surface. The microelectronic element will include many such staged openings 166, within each of which a conductive element 114 can be formed. In one example, the staged opening can be formed by a series of steps, which can include etching, laser patterning, mechanically milling, micro-particle abrasion, e.g., from a directed stream of particles, typically referred to as "sandblasting", or a combination or series of such steps. The interior surfaces 121, 123 of the openings can have the arrangement as described above relative to Fig. 1A. The process of forming the first and second openings can be as generally described in any or all of United States Patent Publication No. 20080246136A1, or United States applications, each filed July 23, 2010: Application Nos. 12/842,717, 12/842,612, 12/842,669; 12/842,692; 12/842,587, the disclosures of which are incorporated herein by reference.

[0061] The process of forming the staged opening can be performed selectively with respect to a dielectric region 172 of the wafer 162 disposed between a semiconductor region 174 and the pad 108 such that the opening does not go through the dielectric layer 174. The dielectric region 172 can include a passivation layer, one or more dielectric layers in which wiring layers of the wafer can be disposed, or both the passivation layer and such dielectric layer. For ease of reference, any or all of these can be referred to hereinafter alternatively as the "passivation layer" 172. Thereafter, as seen in Fig. 8, an opening 176 can be formed which extends through the passivation layer 172.

[0062] Before or after forming the opening 176 in the passivation layer 172, a dielectric layer 178 (Fig. 9) can be formed which extends along the interior surfaces 121, 123 of the staged opening and which contacts the rear surface 118 of the wafer. In one example, an electrophoretic deposition technique can be used to form a dielectric coating 178 conformally with respect to the interior surfaces 121, 123 of the openings and the surface 118. In this way, the conformal dielectric coating may be deposited only onto exposed conductive and semiconductive surfaces of the assembly. During deposition, the semiconductor device wafer is held at a desired electric potential and an electrode is immersed into the bath to hold the bath at a different desired potential. The assembly is then held in the bath under appropriate conditions for a sufficient time to form an electrodeposited conformal dielectric layer 178 on exposed surfaces of the device wafer which are conductive or semiconductive. Electrophoretic deposition can occur so long as a sufficiently strong electric field is maintained between the surface to be coated thereby and the bath. As the electrophoretically deposited coating is self-limiting in that after it reaches a certain thickness governed by parameters, e.g., voltage, concentration, etc. of its deposition, deposition stops.

[0063] Electrophoretic deposition typically forms a continuous and uniformly thick conformal coating on conductive and/or semiconductive exterior surfaces of the assembly. In addition, the electrophoretic coating can be deposited so that it does not form on the remaining dielectric layer 172 overlying the bottom surface 192 of the conductive pad 108, due to its dielectric (nonconductive) property. Stated another way, a property of electrophoretic deposition is that is does not form on a layer of dielectric material overlying a conductor provided that the layer of dielectric material has sufficient thickness, given its dielectric properties.

Typically, electrophoretic deposition will not occur on dielectric layers having thicknesses greater than about 10 microns to a few tens of microns. In a particular example, the conformal dielectric layer 178 can be formed from a cathodic epoxy deposition precursor. Alternatively, a polyurethane or acrylic deposition precursor could be used.

[0064] In further processing, an opening 180 can be formed in the pad 108, such as by etching through the conductive pad 108 in a manner performed selectively to the dielectric bonding material 101, e.g., adhesive, after which the bonding material exposed within such opening 180 can be removed to expose the underlying conductive pad 106 of wafer 160.

[0065] Thereafter, as seen in Fig. 10, one or more layers 182 of conductive material, e.g., a metal, can be deposited onto the exposed portion of pad 106 and in contact with pad 108 and dielectric layer 178. The metal can be deposited by various ways, such as sputtering, physical or chemical vapor deposition, which may or may not be plasma assisted, atomic layer deposition, plating, a combination thereof, or other method. A dielectric layer 184 may be deposited onto the metal layer 182, and a pad metal layer 186 may then be deposited or otherwise formed on one or more exposed surfaces the dielectric layer to form the conductive element 114 shown in Fig. 10.

[0066] Thereafter, referring to Fig. 11, further processing can be performed to form an opening 153 extending from the rear surface 154 of the microelectronic element 102 to expose a lower surface 189 of the pad 106 which faces toward the rear surface 154 of the microelectronic element 102. Such opening 153 then is lined with a dielectric layer 188 (Fig. 11), and then the conductive element 152 is formed therein, such as by depositing one or more metal layers on the dielectric layer 188, as described above. As seen in Fig. 11, one or more of the openings in the microelectronic elements can be tapered.

For example, the openings 153 and 121 can be tapered such that widths 157, 158 of these openings, respectively, become smaller in opposite directions 155, 156. The same may also be true of openings 153 and 123 being tapered in opposite directions 155, 156.

[0067] Fig. 11 illustrates an example in which the conductive elements 114, 152 substantially fill the spaces within the respective openings and are non-hollow in that they do not contain interior cavities of non-metal material. However, as seen in Fig. 10, and further in Fig. 12, the conductive elements 114b, 152c can be hollow.

[0068] Fig. 12 further illustrates a particular example in which the conductive element 152c extending through the microelectronic element 102 extends through the conductive pad 106 to contact an upper surface 190 of pad 108 which faces pad 106. The structure in Fig. 12 can be made by a variation of the above-described process in which the conductive element 114b is formed on the lower surface 192 of the pad 108 following the staged shown in Fig. 8, and in which an opening is formed in the pad 106 which extends to the upper surface of pad 108, in a similar manner to the processing described above (Figs. 9-10) for forming an opening in pad 108.

[0069] As further seen in Fig. 13, it is not necessary that the conductive elements in wafer 162 be non-hollow. For example, a conductive element can have one or more portions 152d, 152e extending along the dielectric layer 188 lining the opening 153. In one example, portions 152d, 152e can be portions of a continuous layer which fully covers an interior surface of the opening 153. In another example, the portions 152d, 152e, can represent distinct features which may not be connected together along the interior surface 153, but which may be connected to a surface of one or more of the pads 106, 108.

[0070] In each of the embodiments illustrated in Figs. 1,2,4, and 10-13, the conductive elements conform to contours of the interior surfaces 121, 123, and 153 of the openings in the microelectronic elements 102, 110. However, in another embodiment, a conductive element need not conform to the contours of interior surfaces of the openings. For example, Fig. 14 shows an embodiment in which a conductive element 214 does not conform to the contours of either of the interior surfaces 123, 121 of the openings in microelectronic element 110. Such conductive element may be formed, for example, by forming a dielectric region 216 which fills the space within the openings, then forming an aperture which extends through the dielectric region, and thereafter depositing a metal within the aperture to form a metal column extending from the pad 106 of microelectronic element 102. Subsequently, a conductive pad 218 can be formed to overlie the dielectric region 216. In a variation thereof, the dielectric layer 178 lining the openings 121, 123 can be omitted because the dielectric region 216 adequately insulates the conductive element 214 from the semiconductor material exposed at the interior surfaces 121, 123 of the openings.

[0071] Fig. 15 illustrates a variation of Fig. 14 which further includes a conductive element 252 extending through an opening 253 in the microelectronic element 102. Like conductive element 214, conductive element 252 does not conform to a contour of an interior surface of the opening 253 within which it extends. It will be appreciated that the conductive elements can have various combinations, in which at least a part of one or more conductive elements conforms to a contour of an interior surface of the opening within which it extends, and does not conform to an interior surface of another part of, or another opening, in a microelectronic element.

[0072] Referring now to Figs. 16-19, in a further variation, after forming an opening, e.g., a staged opening as illustrated in Fig. 16, a process is applied which removes the material, e.g., bonding material, between juxtaposed surfaces 206, 208 of the conductive pads. For example, an etchant can be used to remove the bonding material from between the juxtaposed surfaces of the pads. Then, as further illustrated in Fig. 18, when forming the conductive element 314, a metal or conductive compound of a metal is deposited in areas between the juxtaposed surfaces 206, 208 of the conductive pads. Fig. 19 further illustrates a structure as seen in Fig. 18, after a further conductive element 352 has been formed. As in the above-described embodiments, the vias extending through microelectronic element 110 can be either single-stage vias or can be multiple-stage vias, as seen, for example, in Fig. 18.

[0073] Fig. 20 illustrates a further variation in which a conductive pad 306 of a microelectronic element 302 has a conductive element 312 extending away therefrom along the front surface 304 of the microelectronic element 302. For example, the conductive element 312 can include an electrically conductive pad in area 312a and an electrically conductive trace 312b which connects the pad 312a to the pad 306. The conductive element 312 is juxtaposed with a conductive pad 308 of another microelectronic element 310. A second conductive element 324 can extend through an electrically conductive pad 308 at a front surface 303 of the other microelectronic element 310 and be in contact with the conductive element 312. As further seen in Fig. 20, a further electrically conductive element 334 can extend through a thickness of microelectronic element 302 and be in contact with pad 306. Such conductive elements 312, 324, 334 can each be electrically insulated from other conductive features, e.g., pads, other traces, or from the bodies of the

microelectronic elements by dielectric layers disposed at the front surfaces 303, 304 and dielectric layers disposed within the openings through which the conductive elements 324, 334 extend.

[0074] In a particular embodiment, the conductive element 312 can be applied as a feature of a redistribution layer formed on a wafer during back-end-of-line ("BEOL") processing or subsequent thereto. The arrangement seen in Fig. 20 can be used, for example, in situations in which the location at least one of the conductive pads 306 of a microelectronic element does not match the location of at least one other conductive pad 308 of another microelectronic element. In this way, electrical connections can be made between microelectronic elements 302, 310 without requiring the locations of bond pads on each microelectronic element to match in ways permitting the bond pads to be juxtaposed. In a particular embodiment, one microelectronic element can be a logic chip such as a processor, for example, and another microelectronic element can be a memory chip, i.e., one that has a memory storage element therein. A memory storage element includes a multiplicity of memory cells together with circuitry for reading from and writing to the memory cells.

[0075] Fig. 21 shows a variation of the embodiment shown in Fig. 20, in which a conductive element 412 extends away from a conductive pad 408 of a microelectronic element 410, such conductive element being juxtaposed with conductive pad 406 of another microelectronic element 402. In this case, a conductive element 434 extends through the conductive pad 406 and is in contact with conductive element 412. Figs. 20 and 21 illustrate further variations in which any or all of the conductive elements 324, 334, 424, 434 may be hollow as seen in Fig. 20, or non-hollow as seen in Fig. 21.

[0076] Fig. 22 illustrates a further embodiment in which additional microelectronic elements 502 are each stacked and

bonded together with microelectronic elements 102, 110 similar to Fig. 1, in an assembly 500 in which conductive elements 552 extending through a thickness of each microelectronic element 502 are electrically connected through openings in pads 506 of each additional microelectronic element 502. In this variation, the conductive element 514 extends through the pad 108.

[0077] Fig. 23 illustrates a variation of such embodiment in which the conductive element 614 is in contact with the pad 108 but another conductive element 652 extends through pad 106 and is in contact with the pad 108. Fig. 23 further shows a variation in which the conductive element 614 is hollow.

[0078] Fig. 24 further illustrates a variation in which the opening 712 in microelectronic element 710 is a single-stage opening extending from a rear surface 718 thereof through pad 708 and exposing a portion of the conductive pad 706. Such opening can have a uniform taper between the rear surface 718 and pad 708, as seen in Fig. 24. Fig. 24 illustrates an embodiment in which the conductive element 714 is in contact with an upper surface 716 of the pad 706, and conductive element 752 is in contact with a lower surface 726 of such pad 706.

[0079] Fig. 25 illustrates a variation of the embodiment of Fig. 24 in which the conductive element 714 extends through openings in both microelectronic elements 710, 702 including through both conductive pads 706, 708.

[0080] The structure and fabrication of the microelectronic assemblies and incorporation thereof into higher-level assemblies can include structure, and fabrication steps which are described in one or more of the following commonly owned co-pending applications each filed on December 2, 2010: U.S. Provisional Application No. 61/419,033; and U.S. Nonprovisional Application No. 12/958,866; and the following U.S. applications each filed July 23, 2010: Application Nos.

12/842,717; 12/842,651; 12/842,612; 12/842,669; 12/842,692; and 12/842,587; the disclosures of all such applications being incorporated by reference herein.

[0081] The structures discussed above provide extraordinary three-dimensional interconnection capabilities. These capabilities can be used with chips of any type. Merely by way of example, the following combinations of chips can be included in structures as discussed above: (i) a processor and memory used with the processor; (ii) plural memory chips of the same type; (iii) plural memory chips of diverse types, such as DRAM and SRAM; (iv) an image sensor and an image processor used to process the image from the sensor; (v) an application-specific integrated circuit ("ASIC") and memory. The structures discussed above can be utilized in construction of diverse electronic systems. For example, a system 1300 (Fig. 26) in accordance with a further embodiment of the invention includes a structure 1306 as described above in conjunction with other electronic components 1308 and 1310. In the example depicted, component 1308 is a semiconductor chip whereas component 1310 is a display screen, but any other components can be used. Of course, although only two additional components are depicted in Fig. 26 for clarity of illustration, the system may include any number of such components. The structure 1306 as described above may be, for example, a microelectronic assembly 100 as discussed above in connection with Fig. 1, 2, 4, 20, and 21. In a further variant, both may be provided, and any number of such structures may be used. Structure 1306 and components 1308 and 1310 are mounted in a common housing 1301, schematically depicted in broken lines, and are electrically interconnected with one another as necessary to form the desired circuit. In the exemplary system shown, the system includes a circuit panel 1302 such as a flexible printed circuit board, and the circuit panel includes numerous conductors 1304, of which only

one is depicted in Fig. 26, interconnecting the components with one another. However, this is merely exemplary; any suitable structure for making electrical connections can be used. The housing 1301 is depicted as a portable housing of the type usable, for example, in a cellular telephone or personal digital assistant, and screen 1310 is exposed at the surface of the housing. Where structure 1306 includes a light-sensitive element such as an imaging chip, a lens 1311 or other optical device also may be provided for routing light to the structure. Again, the simplified system shown in Fig. 26 is merely exemplary; other systems, including systems commonly regarded as fixed structures, such as desktop computers, routers and the like can be made using the structures discussed above.

[0082] As these and other variations and combinations of the features discussed above can be utilized without departing from the present invention, the foregoing description of the preferred embodiments should be taken by way of illustration rather than by way of limitation of the invention.

[0083] While the above description makes reference to illustrative embodiments for particular applications, it should be understood that the claimed invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope of the appended claims.

CLAIMS:

1. A microelectronic assembly, comprising:

a first microelectronic element having a front surface and a first electrically conductive pad exposed at the front surface;

a second microelectronic element having a front surface and a second electrically conductive pad exposed thereat, the front surfaces of the first and second microelectronic elements facing one another, and the first and second pads being juxtaposed, each of the microelectronic elements embodying active semiconductor devices; and

an electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the front surface thereof, within a second opening extending from the first opening towards the front surface of the first microelectronic element, and within a third opening extending through at least one of the first and second pads, wherein interior surfaces of the first and second openings extend in first and second directions relative to the front surface of the first microelectronic element, respectively, to define a substantial angle, the electrically conductive element contacting the first and second pads.

2. The microelectronic assembly as claimed in claim 1, wherein the third opening extends from the second opening through at least the first pad of the first microelectronic element.

3. The microelectronic assembly as claimed in claim 2, wherein the third opening extends through each of the first and second pads.

4. The microelectronic assembly as claimed in claim 1, wherein the third opening extends from a second surface of the second microelectronic element through at least the second pad of the second microelectronic element.

5. A microelectronic assembly as claimed in claim 2 or 4, wherein the electrically conductive element includes at least one of a metal or a conductive compound of a metal between juxtaposed surfaces of the first and second pads.

6. The microelectronic assembly as claimed in claim 1, wherein the electrically conductive element conforms to a contour of at least a portion of the interior surface of at least one of the first or second openings.

7. The microelectronic assembly as claimed in claim 1, wherein the electrically conductive element does not conform to a contour of at least a portion of the interior surface of at least one of the first or second openings.

8. The microelectronic assembly as claimed in claim 4, wherein the electrically conductive element conforms to a contour of at least a portion of an interior surface the third opening.

9. The microelectronic assembly as claimed in claim 4, wherein the electrically conductive element does not conform to a contour of at least a portion of the interior surface of the third opening.

10. The microelectronic assembly as claimed in claim 4, wherein the first opening in the first microelectronic element and the opening in the second microelectronic element are tapered, becoming smaller in opposite directions from one another.

11. A microelectronic assembly, comprising:

a first microelectronic element having a first surface and an electrically conductive pad exposed at the first surface;

a second microelectronic element having a first surface facing the first surface of the first microelectronic element and an electrically conductive pad exposed at the first surface and juxtaposed with the conductive pad of the first

microelectronic element, each of the microelectronic elements embodying active semiconductor devices; and

an electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the first surface thereof, and within a second opening extending through at least one of the juxtaposed electrically conductive pads, wherein the electrically conductive element includes at least one of a metal or a conductive compound of a metal between juxtaposed surfaces of the pads.

12. The microelectronic assembly as claimed in claim 11, wherein the first opening includes a third opening extending from the rear surface of the first microelectronic element towards the first surface thereof and a fourth opening extending from the third opening in a direction towards the first surface of the first microelectronic element, wherein interior surfaces of the third and fourth openings extend in first and second directions relative to the first surface, respectively, to define a substantial angle.

13. The microelectronic assembly as claimed in claim 12, wherein the second opening extends through the pad of the first microelectronic element.

14. The microelectronic assembly as claimed in claim 11, wherein the second opening includes a third opening extending from the rear surface of the second microelectronic element towards the first surface of the second microelectronic element, wherein the second opening extends through the pad of the second microelectronic element.

15. A microelectronic assembly, comprising:

a first microelectronic element having a front surface and an electrically conductive pad exposed at the front surface;

a second microelectronic element having a front surface facing the front surface of the first microelectronic element

and an electrically conductive pad exposed at the front surface and juxtaposed with the conductive pad of the first microelectronic element, each of the microelectronic elements embodying active semiconductor devices; and

an electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the front surface thereof, within a second opening extending from a rear surface of the second microelectronic element towards the front surface thereof, wherein interior surfaces of the first and second openings extend in first and second directions relative to the front surface, respectively, to define a substantial angle, the electrically conductive element extending through at least one of the juxtaposed pads, and contacting the pads.

16. A microelectronic assembly, comprising:

a first microelectronic element having a front surface and a first electrically conductive pad exposed at the front surface, and a first electrically conductive element extending along the front surface away therefrom;

a second microelectronic element having a front surface facing the front surface of the first microelectronic element, and a second electrically conductive pad exposed at the front surface thereof and juxtaposed with a portion of the first electrically conductive element, the first and second microelectronic elements embodying active semiconductor devices;

a second electrically conductive element extending within an opening extending from a rear surface of the first microelectronic element towards the front surface thereof, the second conductive element contacting the first conductive pad; and

a third electrically conductive element extending within an opening extending from a rear surface of the second microelectronic element towards the front surface thereof, the

third conductive element extending through an opening in the second conductive pad and contacting the second conductive pad and the first conductive element.

17. A microelectronic assembly as claimed in claim 16, wherein the opening in the first microelectronic element includes a first opening extending from a rear surface of the first microelectronic element towards the front surface thereof, and a second opening extending from the first opening towards the front surface of the first microelectronic element, wherein interior surfaces of the first and second openings extend in first and second directions relative to the front surface, respectively, to define a substantial angle, the second conductive element contacting the first and second pads.

18. A microelectronic assembly as claimed in claim 17, wherein the opening in the second microelectronic element includes a first opening extending from a rear surface of the second microelectronic element towards the front surface thereof, and a second opening extending from the first opening towards the front surface of the second microelectronic element, wherein interior surfaces of the first and second openings extend in first and second directions relative to the front surface, respectively, to define a substantial angle, the second conductive element contacting the first and second pads.

19. A microelectronic assembly as claimed in claim 17 or 18, wherein the second and third conductive elements are spaced apart from one another in a direction along the front surfaces of the microelectronic elements.

20. A microelectronic assembly as claimed in claims 11, 17 or 18, wherein the first conductive element has an upper surface exposed at the front surface of the second microelectronic element and the second conductive element contacts at least a portion of the upper surface.

21. A microelectronic assembly as claimed in claim 16, wherein at least a portion of the first conductive element is an electrically conductive trace.

22. A microelectronic assembly as claimed in claims 16 or 17, further comprising a third microelectronic element having a front surface facing the rear surface of the second microelectronic element, and a fourth electrically conductive element extending within an opening extending from the rear surface of the third microelectronic element, the third conductive element extending through the conductive pad of the third microelectronic element and contacting the second conductive element.

23. A microelectronic assembly as claimed in claim 22, further comprising one or more fourth microelectronic elements each stacked to overlie the rear surface of the third microelectronic element and being electrically coupled with the third conductive element thereof, each fourth microelectronic element having a front surface facing the rear surface of the third or fourth microelectronic element adjacent thereto, and having a fifth electrically conductive element extending within at least an opening extending from the rear surface of the fourth microelectronic element and extending through the conductive pad of such fourth microelectronic element and contacting the conductive element extending through the microelectronic element adjacent thereto.

24. A system comprising a structure according to claims 1, 11, 15, or 16 and one or more other electronic components electrically connected to the structure.

25. A system as claimed in claim 24 further comprising a housing, said structure and said other electronic components being mounted to said housing.

26. A method of fabricating a microelectronic assembly, comprising:

(a) assembling a first microelectronic element with a second microelectronic element such that a first surface of the first microelectronic element faces a first surface of the second microelectronic element, each of the microelectronic elements embodying active semiconductor devices, such that electrically conductive pads exposed at the first surfaces of the microelectronic elements are juxtaposed with each other; and

(b) then forming an electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the first surface thereof, within a second opening extending from the first opening towards the first surface of the first microelectronic element, and within a third opening extending through at least one of the juxtaposed electrically conductive pads, wherein interior surfaces of the first and second openings extend in first and second directions relative to the first surface respectively defining a substantial angle, the electrically conductive element contacting the juxtaposed electrically conductive pads.

27. A method as claimed in claim 26, wherein the step of forming the electrically conductive element includes depositing at least one of metal or a conductive compound of a metal onto juxtaposed surfaces of the pads.

28. The method as claimed in claim 27, wherein the step of forming the electrically conductive element includes forming an undercut between the juxtaposed surfaces of the pads, wherein the step of depositing deposits the at least one of a metal or a conductive compound of metal within the undercut.

29. A method as claimed in claim 26, wherein the third opening extends from a second surface of the second

microelectronic element through at least the juxtaposed pad of the first microelectronic element.

30. A method as claimed in claim 26, wherein the third opening extends through at least the juxtaposed pad of the second microelectronic element.

31. A method as claimed in claim 29 or claim 30, wherein the step of forming the electrically conductive element includes forming the first opening and then forming the third opening by different processes.

32. The method as claimed in claim 26, wherein the electrically conductive element conforms to a contour of an interior surface of at least one of the first and second openings.

33. The method as claimed in claim 26, wherein the electrically conductive element does not conform to a contour of an interior surface of at least one of the first and second openings.

34. A method of fabricating a microelectronic assembly, comprising:

(a) assembling a first microelectronic element with a second microelectronic element such that a first surface of the first microelectronic element faces a first surface of the second microelectronic element, each of the microelectronic elements embodying active semiconductor devices, such that electrically conductive pads exposed at the first surfaces of the microelectronic elements are juxtaposed with each other; and

(b) then forming an electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the first surface thereof and within a second opening extending through at least one of the juxtaposed electrically conductive pads, the forming of the electrically conductive element including

depositing at least one of a metal or a conductive compound of a metal onto juxtaposed surfaces of the pads.

35. The method as claimed in claim 34, wherein the step of forming the electrically conductive element includes forming an undercut between the juxtaposed surfaces of the pads, wherein the step of depositing deposits the at least one of a metal or a conductive compound of metal within the undercut.

36. The method as claimed in claim 35, wherein the first opening includes a third opening extending from the rear surface of the first microelectronic element towards the first surface thereof and a fourth opening extending from the opening to the second opening, wherein interior surfaces of the first and second openings extend in first and second directions relative to the first surface respectively defining a substantial angle, and the second opening extends through the pad of the first microelectronic element.

37. The method as claimed in claim 35, wherein the second opening includes a third opening extending from the rear surface towards the first surface of the first microelectronic element and a fourth opening extending from the third opening through the pad of the second microelectronic element.

38. A method of fabricating a microelectronic assembly, comprising:

(a) assembling a first microelectronic element with a second microelectronic element such that a first surface of the first microelectronic element faces a first surface of the second microelectronic element, each of the microelectronic elements embodying active semiconductor devices, such that electrically conductive pads exposed at the first surfaces of the microelectronic elements are juxtaposed with each other; and

(b) then forming an electrically conductive element extending within a first opening extending from a second

surface of the first microelectronic element towards the first surface thereof, within a second opening extending from a second surface of the second microelectronic element towards the first surface thereof, wherein interior surfaces of the first and second openings extend in first and second directions relative to the first surface respectively defining a substantial angle, the electrically conductive element extending through at least one of the juxtaposed pads and contacting the pads.

39. A method of fabricating a microelectronic assembly, comprising:

(a) assembling a first microelectronic element with a second microelectronic element such that a first surface of the first microelectronic element faces a first surface of the second microelectronic element, each of the microelectronic elements embodying active semiconductor devices, such that an electrically conductive pad exposed at the first surface of one of the microelectronic elements is juxtaposed with a first conductive element exposed at the first surface of another of the microelectronic elements; and

(b) then forming a second electrically conductive element extending within a first opening extending from a rear surface of the first microelectronic element towards the first surface thereof, within a second opening extending from the first opening towards the first surface of the first microelectronic element, and within a third opening extending through at least one of the pad or the first electrically conductive element, wherein interior surfaces of the first and second openings extend in first and second directions relative to the first surface respectively defining a substantial angle, the second conductive element contacting the pad and the first electrically conductive element.

40. A method as claimed in claim 39, wherein the pad is a first pad exposed at the first surface of the first

microelectronic element and the second microelectronic element includes a second electrically conductive pad spaced in a direction along the first surface of the second microelectronic element from the first pad, and the first conductive element extends along the first surface of the second microelectronic element and is electrically coupled with the second pad.

41. A method as claimed in claim 39, wherein the pad is a first pad exposed at the first surface of the second microelectronic element and the first microelectronic element includes a second electrically conductive pad spaced in a direction along the first surface of the first microelectronic element from the first pad, and the first conductive element extends along the first surface of the first microelectronic element and is electrically coupled with the second pad.

42. A method as claimed in claims 40 or 41, wherein the second conductive element extends through the first pad.

43. A method as claimed in claims 40 or 41, wherein the second pad has an upper surface facing in a direction away from the second microelectronic element and the first conductive element contacts at least a portion of the upper surface of the second pad.

44. A method as claimed in claim 43, further comprising forming the first conductive element in contact with at least a portion of the upper surface of the second pad before step (a).

45. A method as claimed in claim 44, wherein at least a portion of the first conductive element is an electrically conductive trace extending along the surface of the first microelectronic element in a direction between the second pad and a location of the first microelectronic element juxtaposed with the first pad.

46. A method as claimed in claim 40, wherein the third opening extends through the first pad and a portion of the

second conductive element further extends within the third opening and contacts the first pad.

47. A method as claimed in claim 41, wherein a portion of the second conductive element further extends within an opening extending from a rear surface of the second microelectronic element through the second pad.

48. A method as claimed in claim 39, further comprising assembling a third microelectronic element with the first and second microelectronic elements such that a first surface of the third microelectronic element faces the second surface of the second microelectronic element, and then forming a third electrically conductive element extending within at least an opening extending from the second surface of the third microelectronic element, the third conductive element extending through the conductive pad of the third microelectronic element and contacting the second conductive element.

FIG. 1

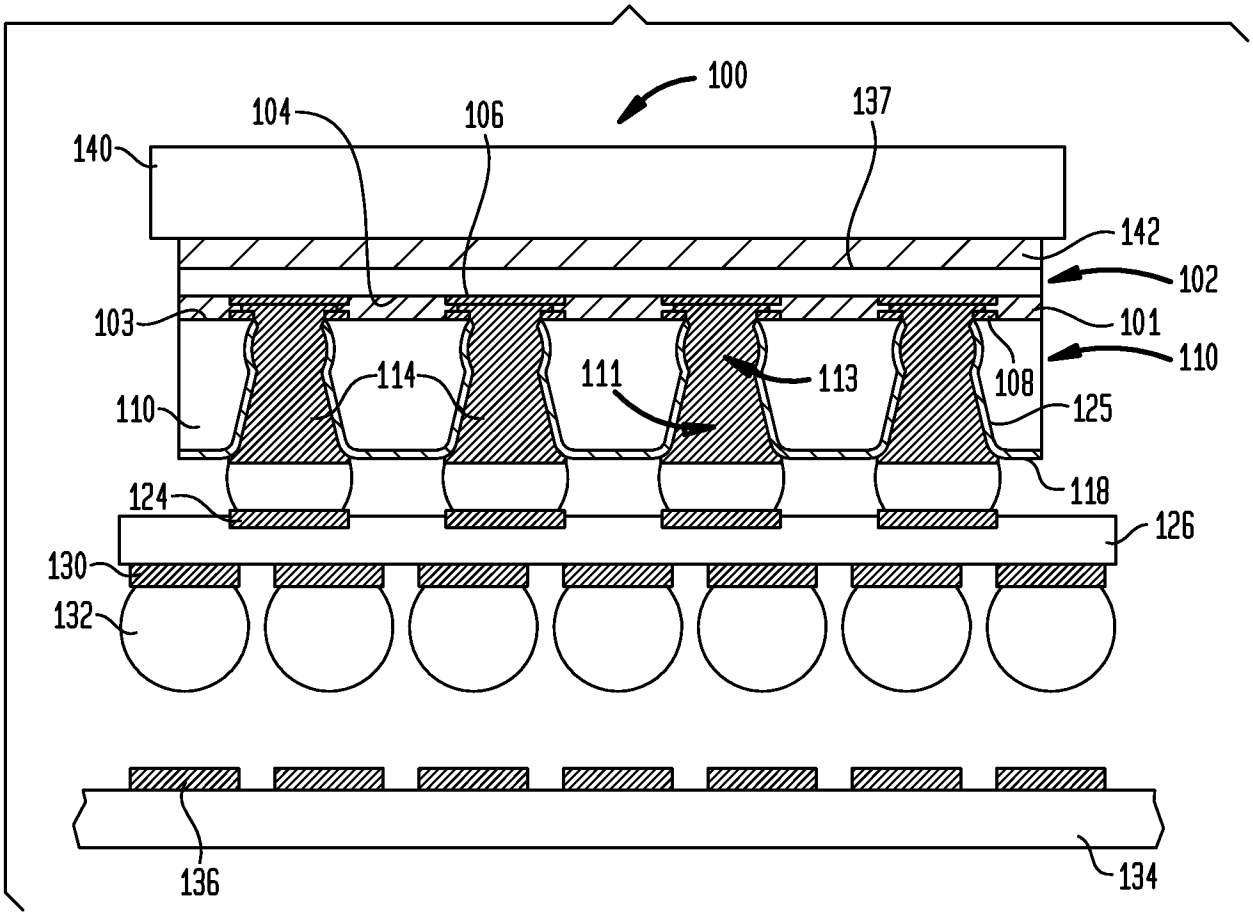
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FIG. 1A

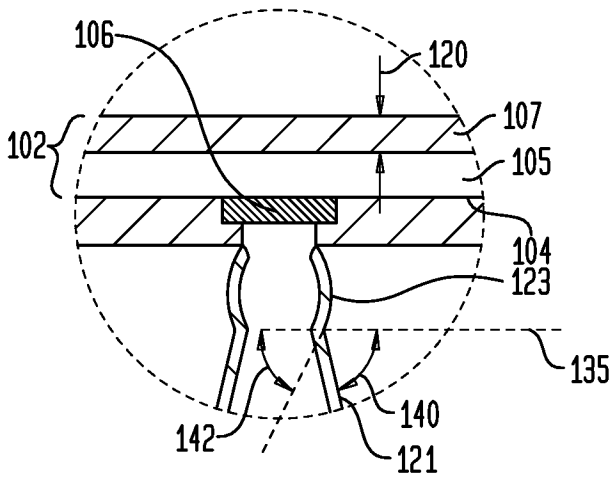
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FIG. 2

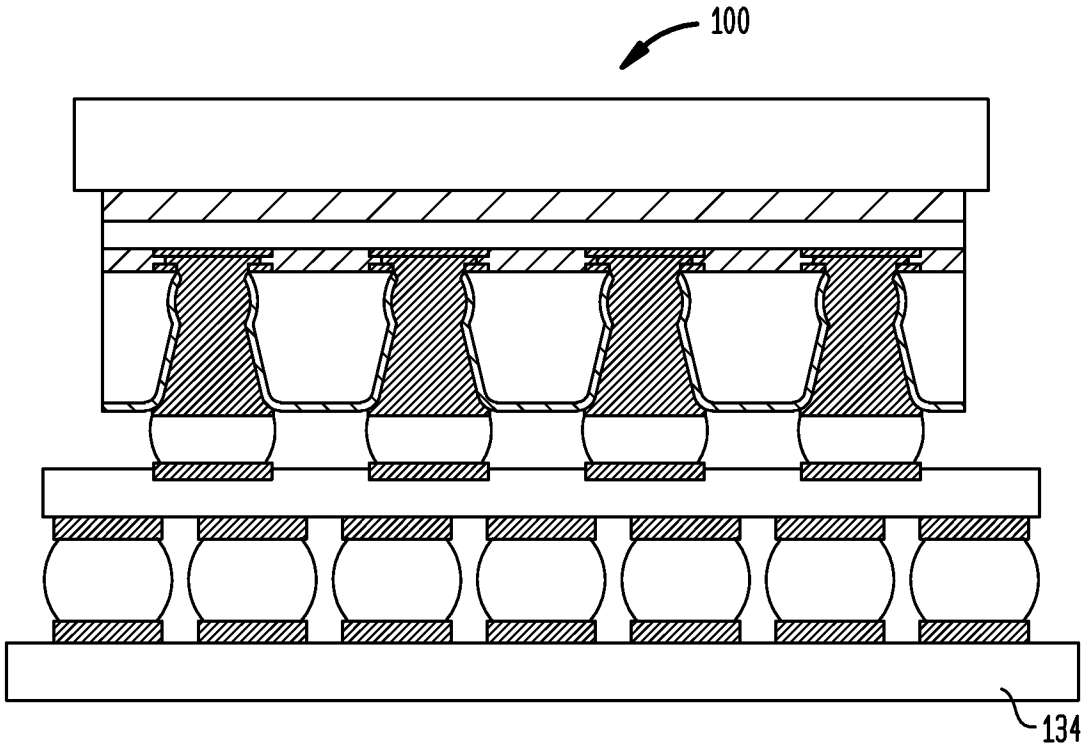

FIG. 3

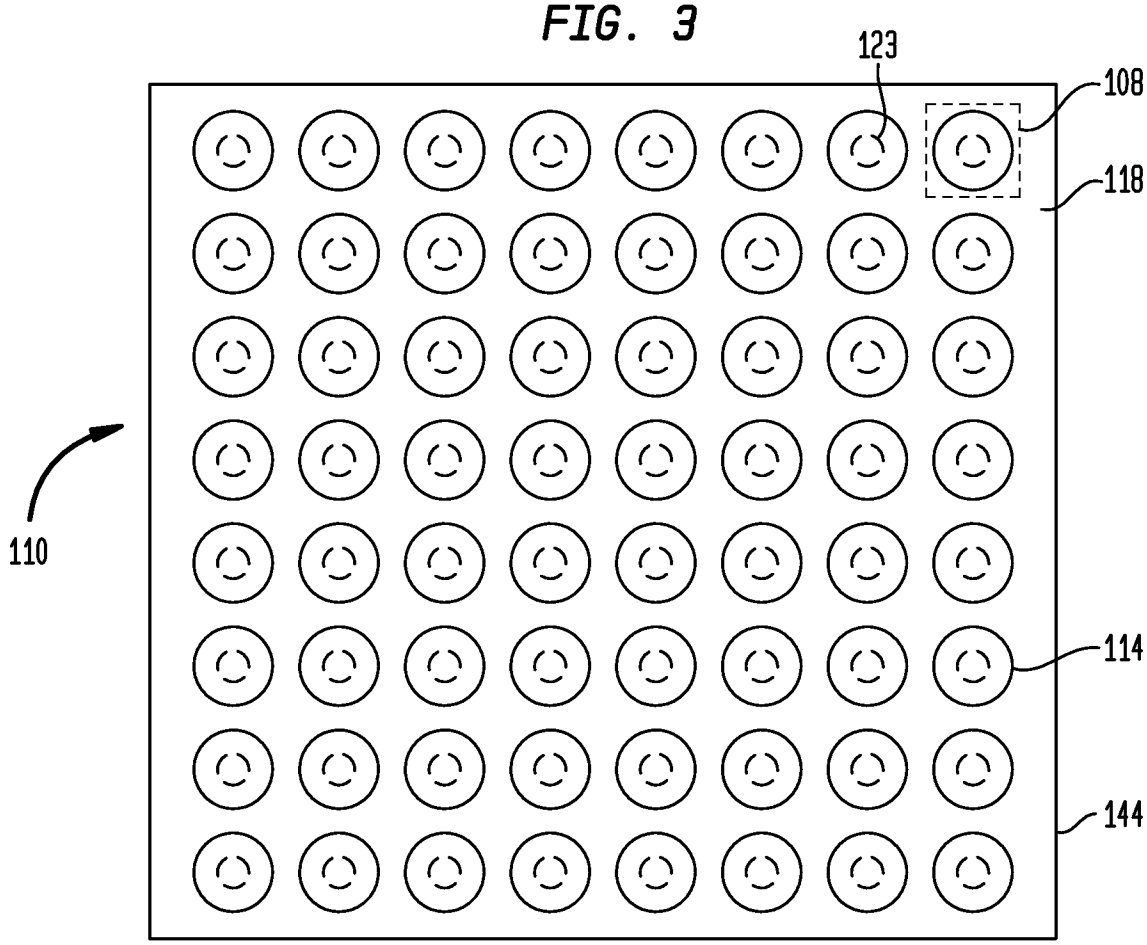

FIG. 4

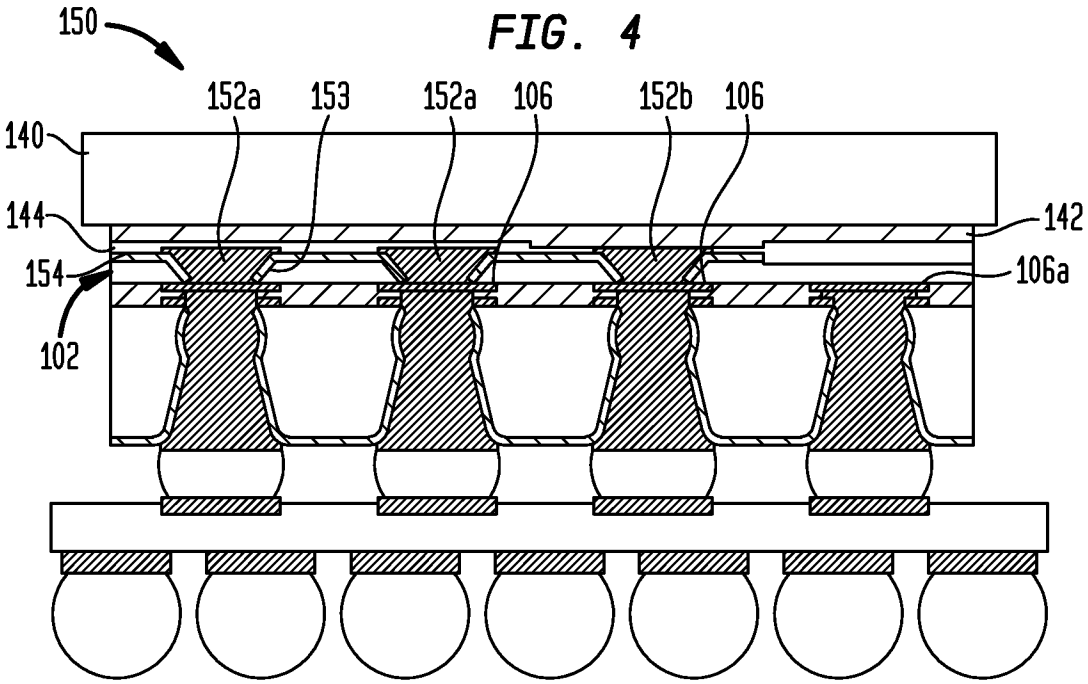

FIG. 5

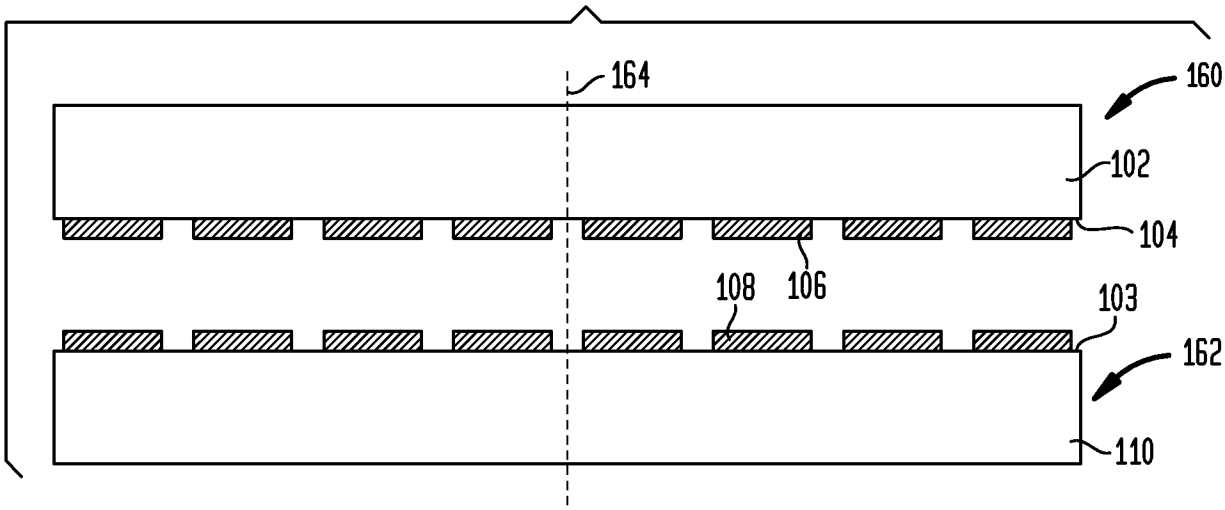

FIG. 6

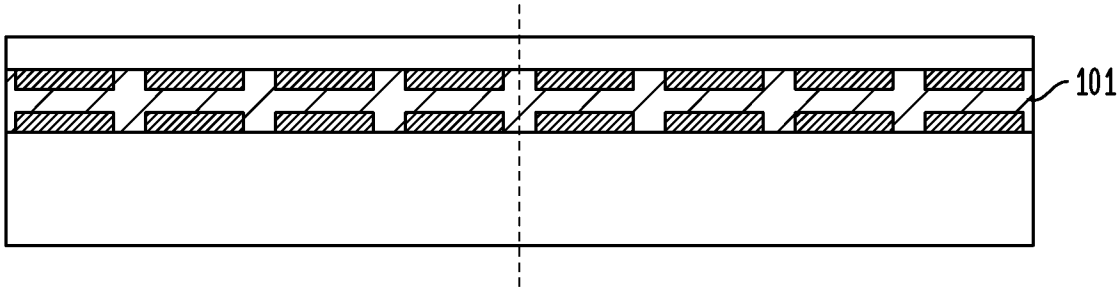

FIG. 7

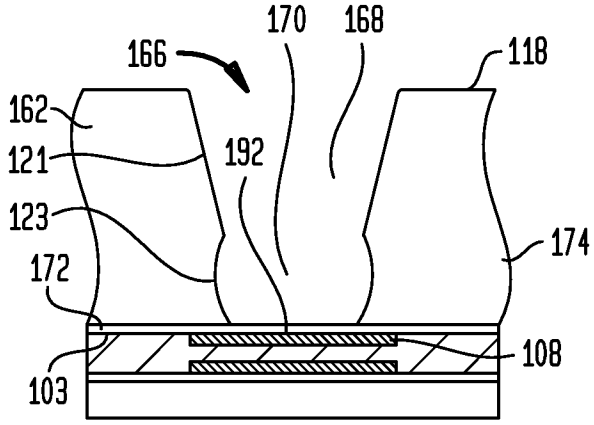

FIG. 8

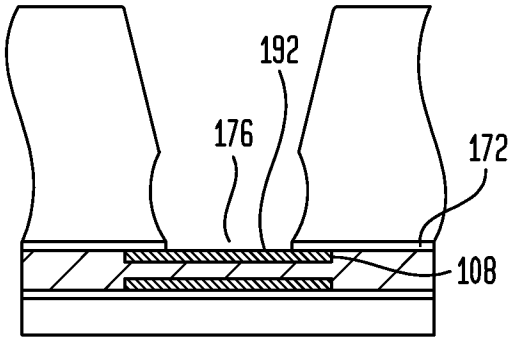

FIG. 9

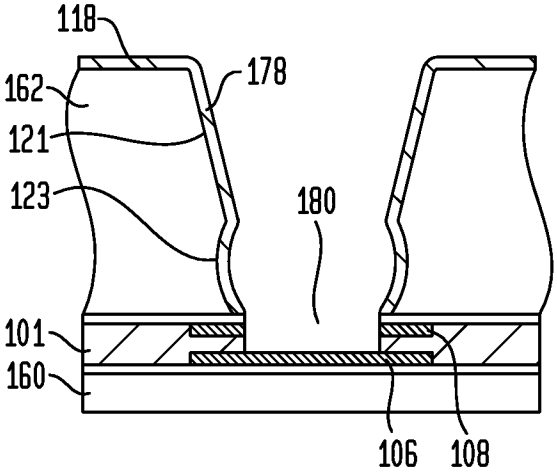

FIG. 10

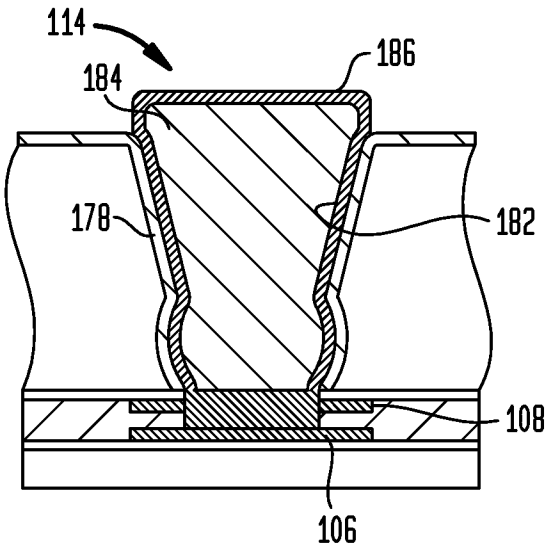

FIG. 11

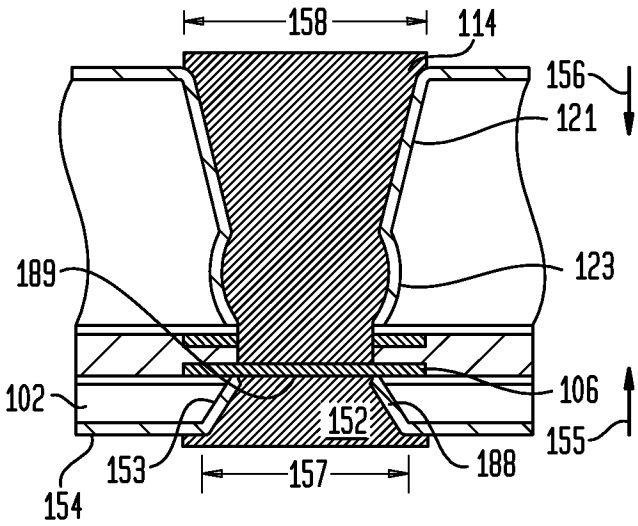

FIG. 12

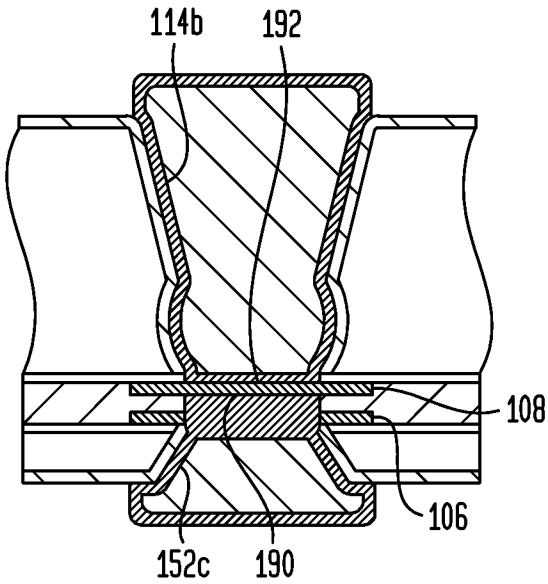

FIG. 13

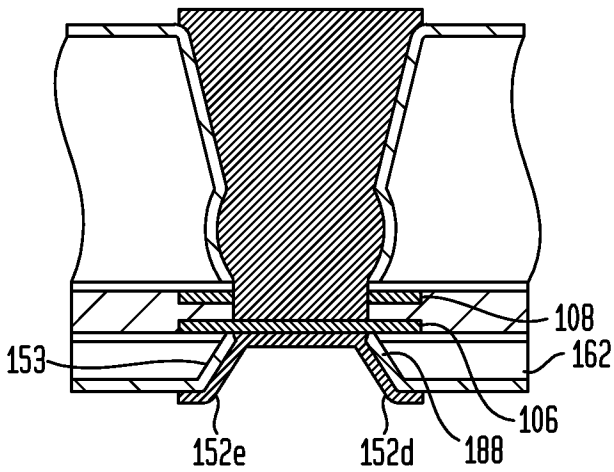

FIG. 14

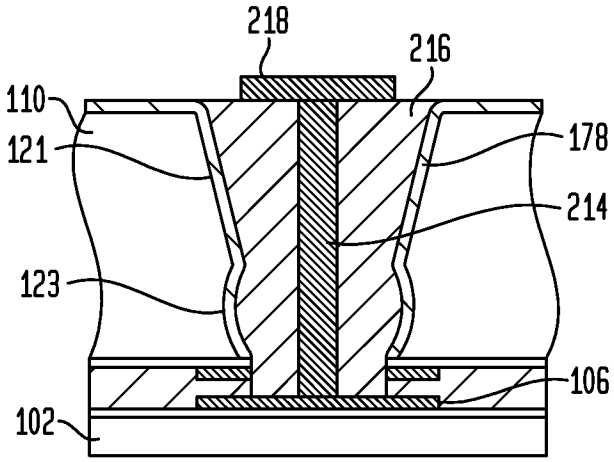

FIG. 15

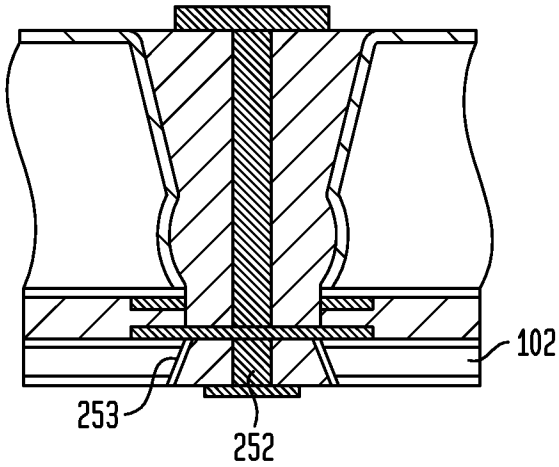

FIG. 16

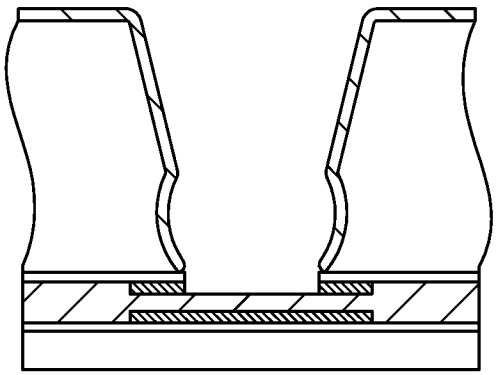

FIG. 17

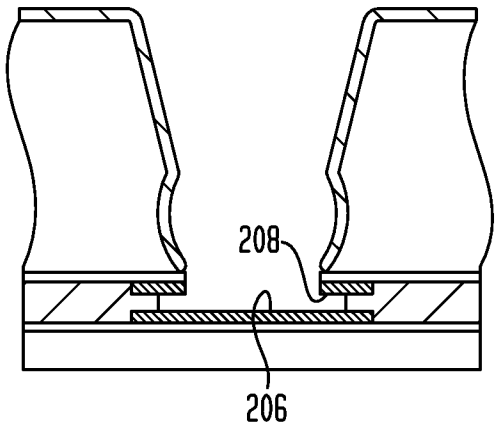

FIG. 18

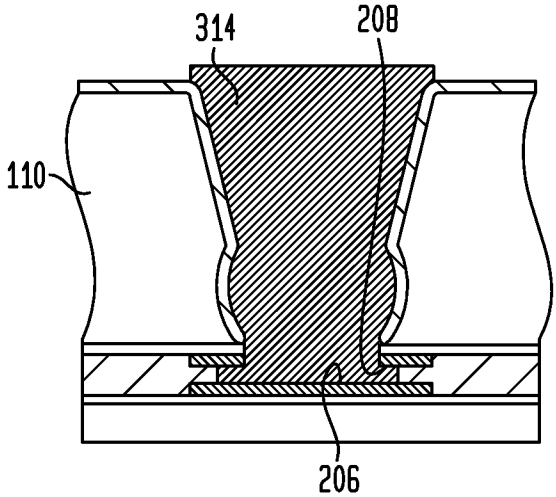

FIG. 19

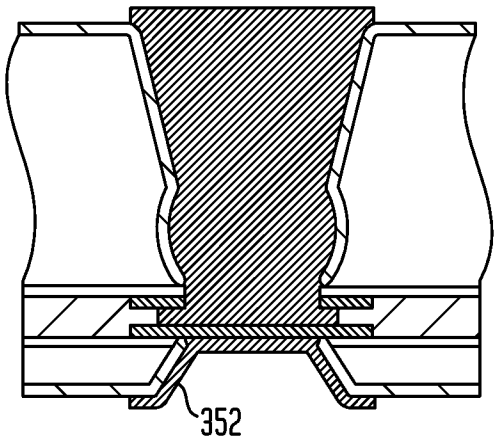

FIG. 20

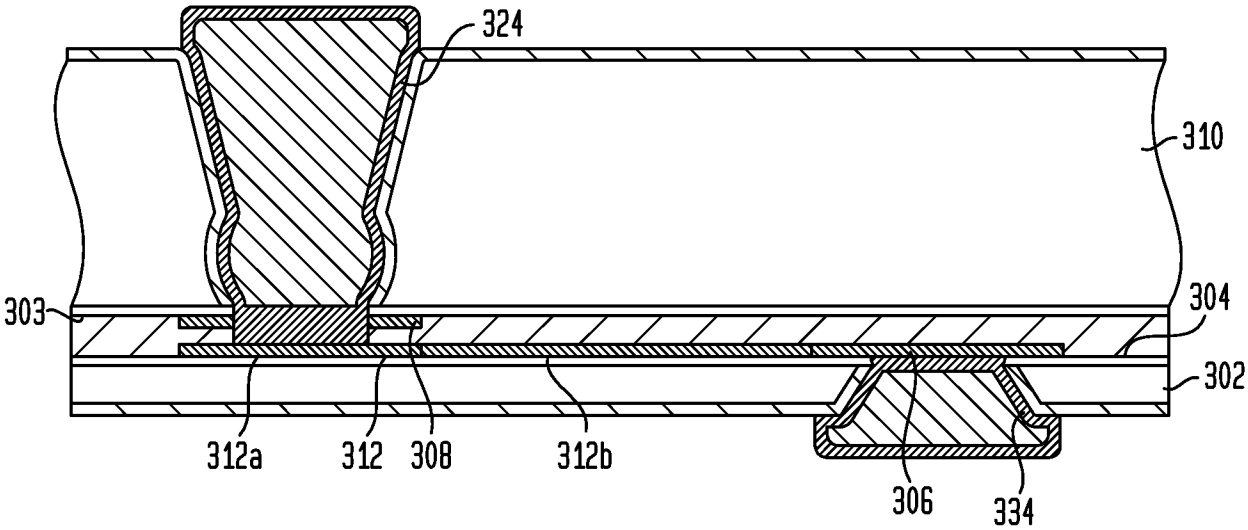
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FIG. 21

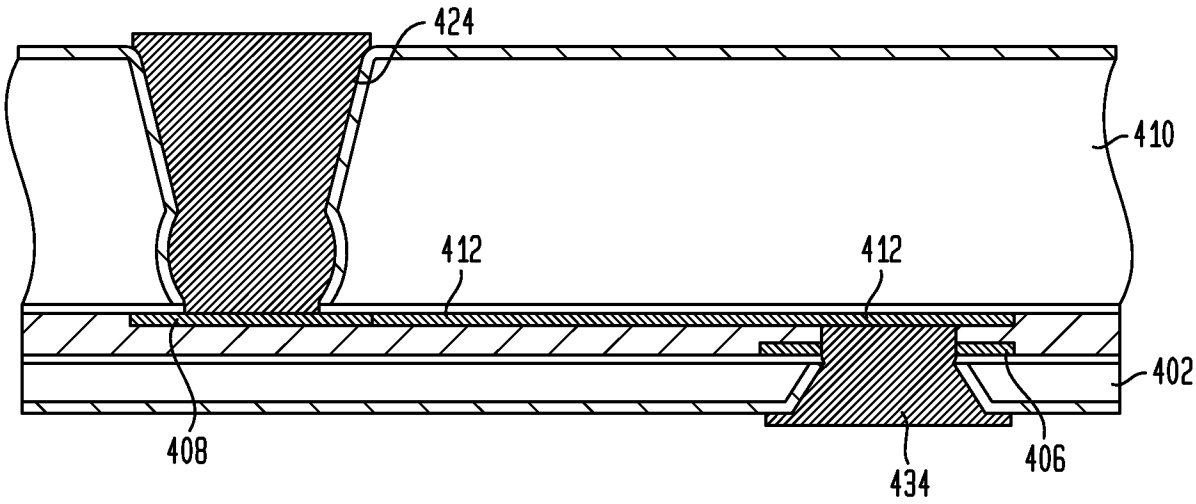
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FIG. 22

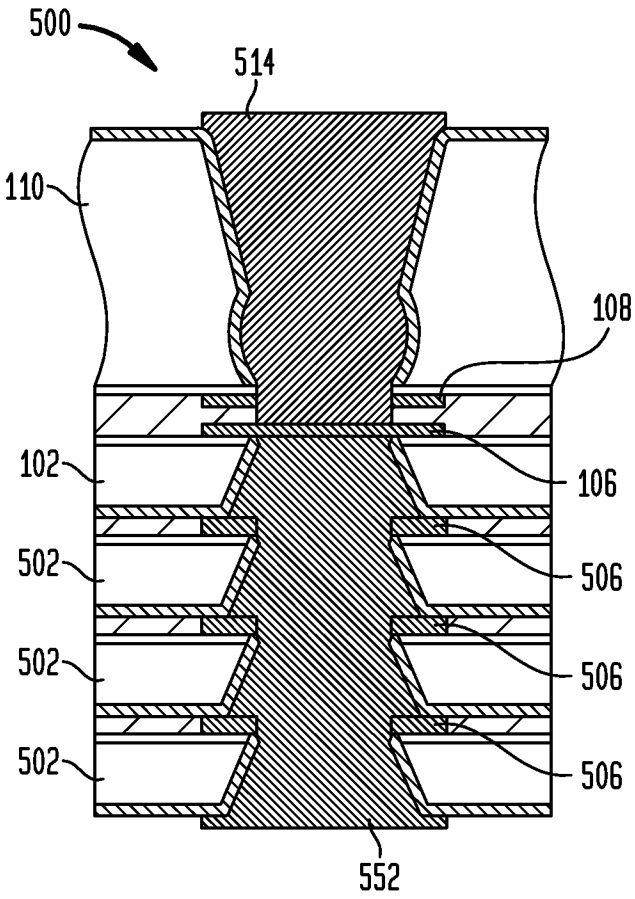


FIG. 23

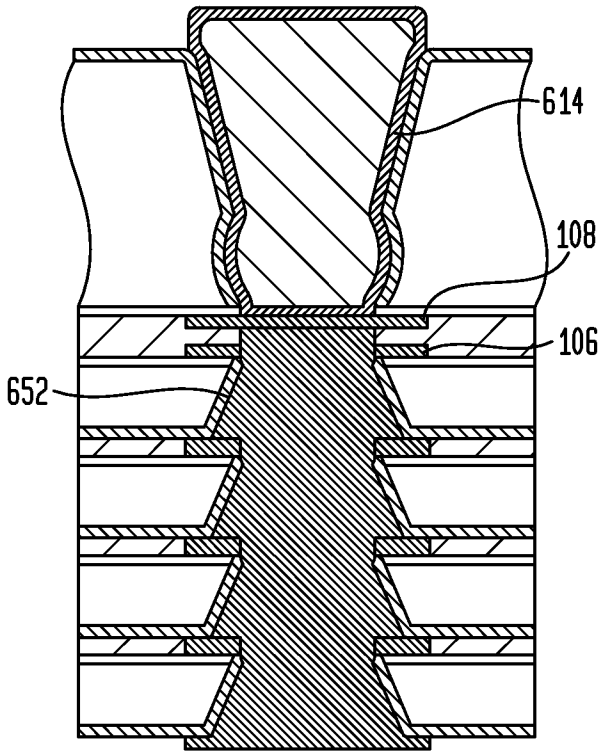


FIG. 24

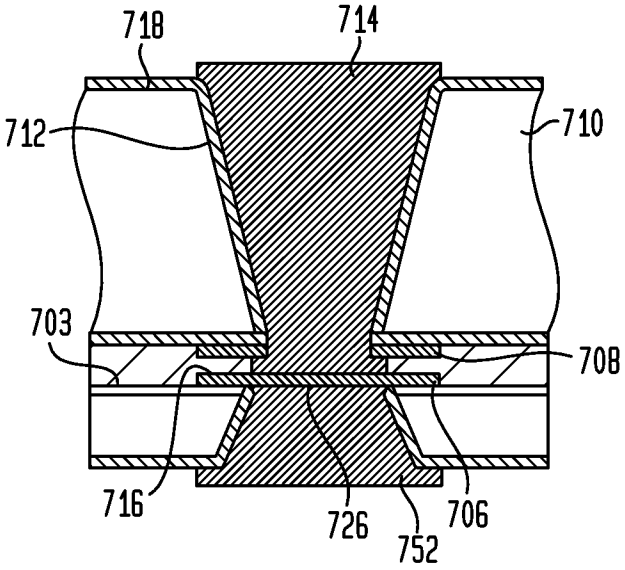


FIG. 25

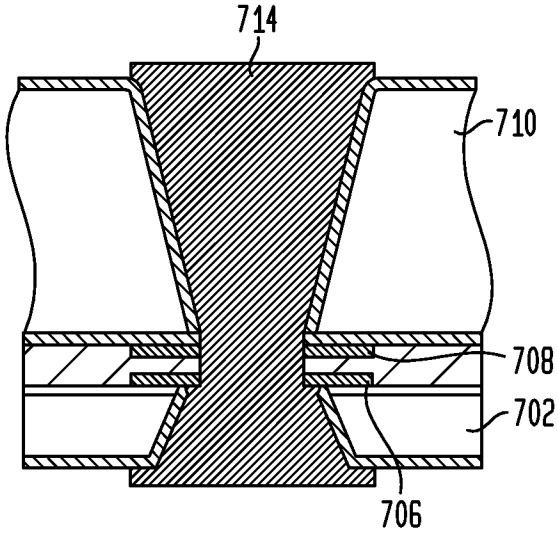
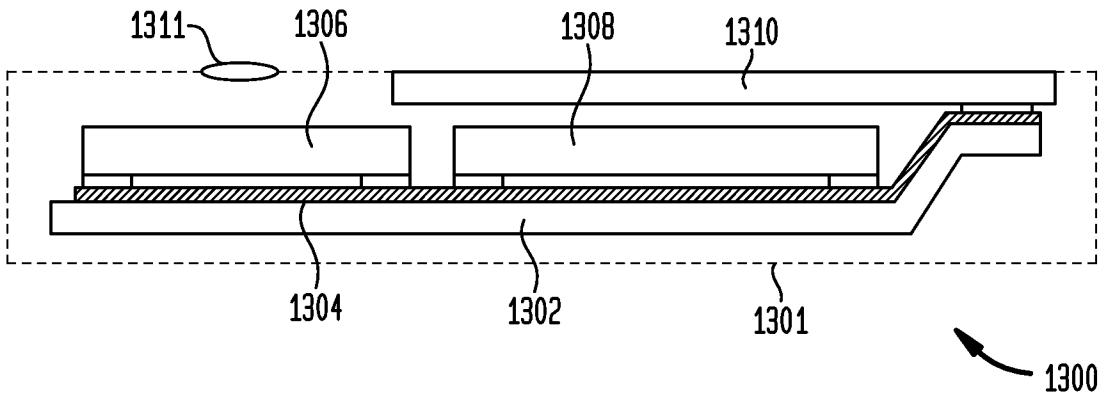


FIG. 26



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/029568

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/48 H01L25/065
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/155354 A1 (HANAOKA TERUNAO [JP] ET AL) 12 August 2004 (2004-08-12)	1-6,8, 10-18, 20-25
Y	paragraphs [0165] - [0169], [0185]; figures 10, 11	7,9
Y	US 2006/154446 A1 (WOOD ALAN G [US] ET AL) 13 July 2006 (2006-07-13) paragraphs [0051], [0055]; figures 2D-2F	7,9
X	US 2004/016942 A1 (MIYAZAWA IKUYA [JP] ET AL) 29 January 2004 (2004-01-29) paragraph [0063]; figure 5	1,2,5,6, 11-13, 24,25

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 October 2011	21/10/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ploner, Guido

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/029568

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/230923 A1 (JO CHA-JEA [KR] ET AL) 25 September 2008 (2008-09-25) paragraphs [0048] - [0065]; figures 3A-E, 4	16-25
X	US 2009/032966 A1 (LEE JONG HO [KR] ET AL) 5 February 2009 (2009-02-05) paragraphs [0036] - [0044], [0067], [0068], [0071]; figures 1A-E, 10, 11, 14	16,20-24
A	US 2010/193964 A1 (FAROOQ MUKTA G [US] ET AL) 5 August 2010 (2010-08-05) paragraph [0046]; figure 12	1-15,24, 25
A	US 2009/045504 A1 (SUH MIN SUK [KR]) 19 February 2009 (2009-02-19) figures 3, 5, 7, 9-11	1-10,12, 15,24,25
A	US 2007/035020 A1 (UMEMOTO MITSUO [JP]) 15 February 2007 (2007-02-15) figures 8-10	1,12,15, 17,18
A	US 2003/178714 A1 (SAKODA HIDEHARU [JP] ET AL) 25 September 2003 (2003-09-25) the whole document	16-25

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/029568

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☒ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

1-25

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-15, 24, 25

   Microelectronic assembly having through-chip vias with varying diameter and corresponding system

   ---

2. claims: 16-25

   Microelectronic assembly having through-chip vias and a redistribution trace and corresponding system

   ---

3. claims: 26-48

   Methods of forming a microelectronic assembly having through-chip vias

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2011/029568

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004155354 A1	12-08-2004	US 2004155355 A1	12-08-2004
US 2006154446 A1	13-07-2006	NONE	
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