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- (71) **Applicant:** QUALCOMM INCORPORATED [US/US];
ATTN: International IP Administration, 5775 Morehouse
Drive, San Diego, California 92121-1714 (US).
- (72) **Inventors:** GU, Shiqun; 5775 Morehouse Drive, San
Diego, California 92121 (US). RADOJCIC, Ratibor;
5775 Morehouse Drive, San Diego, California 92121 (US).
KIM, Dong Wook; 5775 Morehouse Drive, San Diego,
California 92121 (US).
- (74) **Agent:** HALLMAN, Jonathan W.; Haynes and Boone,
LLP, 2323 Victory Avenue, Suite 700, Dallas, Texas
75219 (US).
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(54) **Title:** BOTTOM PACKAGE WITH METAL POST INTERCONNECTIONS

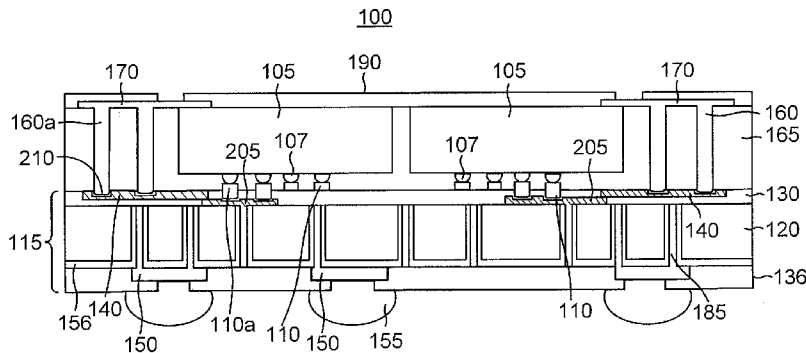


FIG. 1A

(57) **Abstract:** A bottom package substrate is provided that includes a plurality of metal posts that electrically couple through a die redistribution layer to a plurality of die interconnects. The metal posts and the die interconnects are plated onto a seed layer on the bottom package substrate.

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Bottom Package with Metal Post Interconnections

Sam Gu, Riko Radojicic, & Dong Wook Kim

Cross-Reference to Related Applications

[0001] This application claims priority to the filing date of U.S. Provisional Patent Application Serial No. 61/941,345, filed February 18, 2014, which claims priority to the filing date of U.S. Patent Application Serial No. 14/254,494, filed April 16, 2014, both of which are hereby incorporated by reference in their entirety.

Technical Field

[0002] This application relates to integrated circuit packaging, and more particularly to a bottom package having metal post interconnections.

Background

[0003] Organic substrates are commonly used in package-on-package architectures because of their low cost. For example, a flip-chip die such as a micro-processor may be coupled to a first surface of an organic substrate for a bottom package through a plurality of solder bumps or copper pillars. To support a coupling or interconnection to a top package substrate, the bottom package substrate has a footprint large enough such that there is perimeter about the bottom package die on the first surface of the bottom package substrate. That perimeter may then support solder ball interconnections to the top package. Although the resulting package-on-package architecture is quite popular due to its low cost, organic substrates are often not suitable for modern fine-pitch dies because an organic substrate accommodates only a relatively coarse interconnect pitch. The interconnect pitch is the separation between the

substrate-to-die interconnections such as micro-bumps or copper pillars as well as the bottom-package-to-top-package interconnections such as solder balls.

[0004] Because of the interconnect pitch limitations for organic substrates, the bottom package substrate for modern fine-pitch dies typically comprises a glass or semiconductor interposer. In contrast to an organic substrate, a glass or semiconductor interposer supports fine-pitch interconnections. It is thus conventional to mount fine-pitch dies onto an interposer because a glass or silicon interposer enables the necessary fine-pitch interconnections. Multiple fine-pitch dies such as a first processor die and a second processor die may be mounted on the same interposer. The interposer receives the fine-pitch interconnects such as micro-bumps or copper pillars from each die through a redistribution layer (RDL) that enables each die to communicate with the other die(s) through the RDL. Although the resulting interposer package is thus advantageous in that it accommodates the necessary fine-pitch interconnections, it is conventional to interface processors with associated external memories such as a DRAM die using a package-on-package (PoP) construction. But the footprint of the interposer is already somewhat large as it must have the necessary surface area to support the fine-pitch dies.

[0005] If such an interposer also includes a perimeter around the fine-pitch dies to provide space for conventional PoP solder ball interconnections to an upper memory package substrate, the interposer footprint becomes excessive. For example, it is conventional to encase the dies on the interposer and the solder ball interconnections with mold compound during manufacture of the bottom package. The encased solder balls must then be exposed such as through the use of laser drilling of the mold compound. The heat from the laser requires a certain keep-out distance between the solder balls and the dies. The resulting interposer for the bottom package thus requires

a relatively large footprint to support not only the dies and the solder balls but also the keep out distance between the solder balls and the dies. In addition, the solder balls must be relatively large to couple to the upper package. Such a relatively large interconnect size requires a correspondingly large interconnect pitch. The interposer footprint thus must be large enough to support both the solder balls with their requisite pitch as well as the associated keep-out area between the solder balls and the die, which decreases density and is expensive. As an alternative, the interposer may include a perimeter that supports an interconnect bar such as a printed circuit bar or a silicon or glass interconnect bar. The interconnect bar includes a number of plated vias as opposed to solder balls. But the manufacture of the plated vias in the interconnect bar also require a certain distance or keep out area with regard to the interconnect bar outer perimeter. Thus, regardless of whether a conventional interposer includes solder balls or interconnect bars, the interposer footprint must be relatively large.

[0006] Accordingly, there is a need in the art for bottom package substrates such as interposers with reduced footprints.

Summary

[0007] A bottom package is provided with plated metal posts for forming interconnects to a top package. The plated metal posts enable a reduced footprint for the bottom package as compared to conventional bottom packages that use solder balls or interconnect bars to form the interconnections to an upper package or additional die. The bottom package includes a bottom package substrate supporting one or more dies. In some embodiments, the bottom package substrate may comprise a glass, silicon, or laminated organic interposer that supports a plurality of dies. In alternative embodiments, the bottom package substrate may comprise a glass substrate, a semiconductor substrate, or a laminated organic substrate that supports a single die.

[0008] To provide the reduced footprint, the bottom package substrate includes a plurality of plated metal posts coupled to die interconnects through a redistribution layer (RDL). The die(s) supported by the bottom package substrate couple through the die interconnects to the RDL, from the RDL to the metal posts, and from the metal posts to a top package substrate. In contrast to conventional bar interconnect embodiments, both the metal posts and the die interconnects are plated onto a seed layer overlaying the RDL. The die interconnects and metal posts may be plated onto the seed layer prior to attachment of the die (or dies) to the bottom package substrate. The metal posts may thus be deposited without any need for a keep out area in contrast to conventional bar interconnect or solder ball embodiments. The resulting bottom package substrates disclosed herein thus have advantageously enhanced density as compared to conventional architectures.

Brief Description of the Drawings

[0009] Figure 1A is a cross-sectional view of a bottom package including metal posts in accordance with an embodiment of the disclosure.

[0010] Figure 1B is a cross-sectional view of the bottom package of Figure 1A as it receives a top package to form a package-on-package (PoP) construction.

[0011] Figure 2A is a cross-sectional view of an interposer used to form the bottom package of Figure 1A prior to deposition of die interconnects and the metal posts.

[0012] Figure 2B is a cross-sectional view of the interposer of Figure 2A after deposition of the seed layer.

[0013] Figure 2C is a cross-sectional view of the interposer of Figure 2B after deposition and patterning of a first mask layer for forming the die interconnects.

[0014] Figure 2D is a cross-sectional view of the interposer of Figure 2C after deposition of the die interconnects and removal of the first mask layer.

[0015] Figure 2E is a cross-section view of the interposer of Figure 2D after deposition and patterning of a second mask layer for forming the metal posts.

[0016] Figure 2F is a cross-section view of the interposer of Figure 2E after deposition of the metal posts and removal of the second mask layer.

[0017] Figure 2G is a cross-sectional view of the interposer of Figure 2F after attachment of a pair of dies.

[0018] Figure 2H is a cross-sectional view of the interposer of Figure 2G after deposition of mold compound to encase the dies and after attachment of solder balls.

[0019] Figure 2I is a cross-sectional view of the interposer of Figure 2H after back-side grinding and formation of a board-facing redistribution layer and solder balls.

[0020] Figure 2I is a cross-sectional view of the interposer of Figure 2I after dicing to complete construction of the bottom package.

[0021] Figure 3 is a plan view of the bottom package of Figure 2J showing the arrangement of the metal posts with respect to the dies.

[0022] Figure 4 is a flowchart summarizing a method of manufacture for a bottom package in accordance with an embodiment of the disclosure.

[0023] Figure 5 illustrates some example electronic systems incorporating a bottom package in accordance with an embodiment of the disclosure.

[0024] Embodiments of the present disclosure and their advantages are best understood by referring to the detailed description that follows. It should be appreciated that like reference numerals are used to identify like elements illustrated in one or more of the figures.

Detailed Description

[0025] To avoid the excessive footprint demands from the conventional use of solder balls or bar interconnects to electrically couple a bottom package to a top package, a bottom package is provided with plated metal posts for forming the interconnects to the top package. The plated metal posts enable a reduced footprint for the bottom package as compared to the conventional bottom packages that use solder balls or interconnect bars to form the interconnections to an upper package or additional die. The bottom package includes a bottom package substrate supporting one or more dies. In some embodiments, the bottom package substrate may comprise a glass, silicon, or laminated organic interposer that supports a plurality of dies. In alternative embodiments, the bottom package substrate may comprise a glass, semiconductor, or laminated organic substrate that supports a single die.

[0026] Since the metal posts disclosed herein are plated on the bottom package substrate, manufacturing costs are considerably reduced as compared to the conventional use of interconnect bars, which requires the extra process steps of embedding the interconnect bar in the bottom package substrate. Moreover, the interconnect bar manufacture typically requires laser drilling of the vias that are then plated to form the metal posts in the interconnect bar. The interconnect bar thus requires a relatively large keep out area around its entire perimeter. In contrast, the plating of the metal posts for the bottom package disclosed herein requires no laser drilling. The plated metal posts thus require a reduced keep out area as compared to the use of interconnect bars not only with respect to the die(s) but also with respect to the perimeter of the bottom package substrate. Accordingly, the disclosed bottom package offers increased density and reduced manufacturing costs.

[0027] To provide a reduced footprint and to increase density, the plated metal posts electrically couple to die interconnects through a redistribution layer (RDL) in the bottom package. In one embodiment, the die interconnects comprise metal pillars. In that regard, a conventional interposer may also have a redistribution layer that electrically couples die interconnects such as metal pillars to metal posts in a bar interconnect. But a conventional bar interconnect is manufactured separately from the bottom package substrate. In this conventional manufacturing process, the substrate forming the bar interconnect is drilled such as through laser or mechanical drilling to form a plurality of vias that are subsequently plated to complete the bar interconnect posts. Due to the drilling or machining process to form the vias in the bar interconnect substrate, the vias (and thus the metal posts that will eventually fill the vias) must be spaced a certain keep out distance from the bar interconnect substrate perimeter. As discussed earlier, the resulting keep out distance in bar-interconnect-containing bottom package substrates limits density and thus increases costs.

[0028] In sharp contrast, the metal posts disclosed herein are not manufactured separately in a bar interconnect. Instead, the disclosed metal posts are manufactured in situ on the bottom package substrate. To enable this in situ formation, a seed layer covers the redistribution layer. A dielectric layer then covers the seed layer. Windows are opened up in the dielectric layer to form die interconnect openings and also metal post openings. Metal may then be plated onto the seed layer portions exposed in the die interconnect openings and the metal post openings to form the die interconnects and the metal posts.

[0029] Since it is the same seed layer that is exposed in the die interconnect openings as is exposed in the metal post openings, this seed layer is also denoted herein as a single seed layer. The die interconnects and metal posts may be deposited onto the

seed layer prior to attachment of the die (or dies) to the bottom package substrate. As compared to the use of an interconnect bar, the metal posts may thus be formed without a reduced keep out area both with respect to the edge of the substrate and with respect to the dies(s). In contrast, an interconnect bar is diced from a wafer of such bars and thus requires a larger keep out area. The resulting bottom package substrates disclosed herein thus have advantageously enhanced density and lower fabrication cost as compared to conventional architectures. These advantageous features may be better appreciated with regard to the following example embodiments.

Example Embodiments

[0030] Turning now to the drawings, **Figure 1A** illustrates a metal-post-enhanced bottom package 100 including a semiconductor or glass interposer 115. Alternatively, interposer 115 may comprise a laminated organic interposer. In alternative embodiments, interposer 115 may instead comprise a substrate that supports only a single die 105. Analogous to the interposer embodiments, the substrate for bottom package single-die embodiments may comprise glass, semiconductor, or laminated organic polymers.

[0031] Each die 105 electrically couples through a plurality of interconnects such as solder bumps 107 to a corresponding plurality of die interconnects 110 on substrate 115. Die interconnects 110 also electrically couple to a die-side redistribution layer that in turn electrically couples to a plurality of metal posts 160. In bottom package 100, the die-side redistribution layer comprises an upper or first die-side RDL 140 and a lower or second die-side RDL 205. Alternative embodiments may have just a single metal layer for the die-side redistribution layer or may have more than two metal layers. In bottom package 100, interconnects 110 electrically couple to lower die-side RDL 205. In turn, lower die-side RDL 205 electrically couples to upper die-side RDL

140, which then electrically couples to metal posts 160. In one embodiment, die interconnects 110 may be deemed to comprise a means for electrically coupling dies 105 to a die-side redistribution layer such as lower die-side RDL 205. Die interconnects 110 and metal posts 160 may comprise any suitable plated metal such as copper or nickel. Similarly, the various redistribution layers disclosed herein such as upper and lower die-side redistribution layers 140 and 205 may comprise copper, nickel, or other conducting metals. Upper and lower die-side redistribution layers 140 and 205 form conductors or interconnects within a dielectric layer 130 to electrically couple die interconnects 110 to corresponding ones of metal posts 160. For example, a particular die interconnect 110 such as a die interconnect 110a may need to electrically couple to a particular metal post 160 such as a metal post 160a. Upper die-side RDL 140 and lower die-side RDL 205 thus electrically couple together these structures. In addition, upper and lower die-side RDLs 140 and 205 include conductors (not illustrated) to electrically couple die-to-die signals between dies 105. Similarly, lower die-side RDL 205 electrically couple dies 105 to a plurality of through-substrate vias 185.

[0032] Through-substrate vias 185 extend from lower die-side RDL 205 through a core layer 120 of substrate 115 to a board-facing redistribution layer (RDL) 150 that in turn electrically couples to board-facing solder balls 155. The composition of core layer 120 depends upon the substrate used in bottom package 100. For example, in a glass interposer embodiment, core layer 120 would comprise glass. Similarly, in a semiconductor interposer embodiment, core layer 120 would comprise semiconductor. Board-facing redistribution layer 150 may be insulated from core layer 120 by a dielectric layer 156. For example, dielectric layer 156 may be laminated onto core layer 120 to also line through-substrate vias 185. A board-side solder resist or passivation layer 136 includes openings so that exposed pad portions of board-facing redistribution

layer 150 may receive solder balls 155. Solder balls 155 electrically couple to a circuit board (not illustrated) or an underlying package.

[0033] A mold compound 165 partially encases dies 105 and metal posts 160. Metal posts 160 may also electrically couple to a top-side redistribution layer 170 on mold compound 165 and dies 105. A top-side solder resistor or passivation layer 190 covers top-side redistribution layer 170. In alternative embodiments, top-side redistribution layer 170 may be insulated from dies 105 by passivation layer 190, which includes openings to expose pads in top-side redistribution layer 170. These openings may receive interconnects 206 such as solder bumps or copper pillars from a top package 200 as shown in **Figure 1B**. Upper package 200 is shown in Figure 1B just prior to it being mounted onto bottom package 100. Thus bumps 206 do not yet make contact to top-side redistribution layer 170 in Figure 1B. Top-side redistribution layer 170 allows for a fan-out between pillars 160 and interconnects 206 from top package 200. An example manufacturing method will now be discussed.

Example Method of Manufacture

[0034] Manufacture of bottom package 100 shown in Figures 1A and 1B may be performed in wafer-level process (WLP) embodiments or individually. In a WLP embodiment, interposer core 120 would initially be part of a wafer or panel (not illustrated) that would be processed as a whole. The panel or wafer would include a plurality of interposer cores 120 that are processed with die interconnects 110 and metal posts 160 prior to dicing interposer cores 120 from the panel or wafer. Alternatively, each interposer core 120 may be processed individually after it is diced from a panel or wafer.

[0035] Interposer core 120 may be configured with through-substrate vias 185 in a variety of methods. For example, interposer core 120 may be laser drilled and plated

to form vias 185. Alternatively, a number of blind vias may be formed using, for example, laser drilling or machining and then plated in interposer core 120 prior to a grinding step that exposes the blind ends of the blind vias and thus forms through-substrate vias 185. For example, **Figure 2A** illustrates a cross-section of an interposer core 120 including a plurality of conductive blind vias 200. In this embodiment, interposer core 120 is part of a wafer or panel 215 such that a WLP manufacturing technique is being implemented. To form conductive blind vias 200, a die-facing surface of interposer core 120 is laser drilled, etched, or mechanically drilled to form a plurality of blind vias that are then plated to form conductive blind vias 200. Prior to plating, the blind vias may be lined with a dielectric layer (not illustrated) such as dielectric layer 156 shown in Figure 1A.

[0036] As shown in Figure 2A, a board-facing surface 202 of interposer core 120 has not yet been ground to expose the ends of conductive blind vias 200 so as to form through-substrate vias 185 discussed with regard to Figures 1A and 1B. Since Figure 2A is illustrating an initial manufacture step, through-substrate vias 185 shown in Figures 1A and 1B are not yet formed. After formation of conductive blind vias 200, a dielectric layer 135 is deposited on a die-facing surface 203 of interposer core 120 supports dielectric layer 135. For example, dielectric layer 135 may be laminated onto die-facing surface 203. In such embodiments, dielectric layer 135 may comprise polyimide, Ajinomoto build-up film, benzocyclobutene-based polymer, or other suitable dielectric materials. Alternatively, dielectric layer 135 may be spun onto die-facing surface 203 or deposited using chemical vapor deposition techniques. Dielectric layer 135 may be deposited in stages to allow for masking steps so a die-side redistribution layer such as upper die-side redistribution layer 140 may be formed within dielectric layer 135. For example, a metal such as copper or nickel may be deposited using

plating or electroless techniques to form upper die-side RDL 140. As discussed above, multiple metal layers may be used in the various redistribution layers disclosed herein. Thus dielectric layer 135 may include an additional die-side redistribution layer such as lower die-side RDL 205 formed analogously as discussed with regard to upper die-side RDL 140. In some embodiments, interposer core 120 may comprise a semiconductor such as silicon that has some conductivity. To prevent shorting to such conductive substrates, lower die-side RDL 205 may be insulated from interposer core 120 by dielectric layer 135 as shown in Figure 2B. Alternatively, if interposer core 120 comprises a glass or organic material, lower die-side RDL 205 may contact interposer core 120 as shown in Figure 1A.

[0037] After its deposition, dielectric layer 135 may be processed such as through etching to form openings for the subsequent formation of metal posts 160 and die interconnects 110 discussed with regard to Figures 1A and 1B. For example, dielectric layer 135 may be patterned to include die interconnect openings 201 that expose corresponding portions of lower die-side RDL 205. Similarly, dielectric layer 135 may be patterned to include metal post openings 225 that also expose corresponding portions of upper die-side RDL 140.

[0038] After the formation of die interconnect openings 201 and metal post openings 225, dielectric layer 135 may then be covered with a metal seed layer 210 to as shown in **Figure 2B**. For example, metal seed layer 210 may comprise TiCu, TiW, or copper deposited using, for example, a physical vapor technique. Note that single seed layer 210 lines both die interconnect openings 201 and metal post openings 225.

[0039] As shown in **Figure 2C**, a first mask layer 215 such as a wet or dry etch mask layer may then be deposited over seed layer 210 and patterned to re-expose die interconnect openings 201. In some embodiments, the re-expose may enlarge die

interconnect openings 201 as compared to their dimensions in Figure 2A. First mask layer 215 is thus deposited in a thickness that matches a desired height for the die interconnects (not yet formed) that will fill die interconnect openings 201. In this fashion, die interconnects 110 may then be plated into die interconnect openings 201 as shown in **Figure 2D**. For example, a suitable metal such as copper or nickel may be electroplated to form die interconnects 110. First mask layer 215 of Figure 2C may then be stripped or removed from panel or wafer 215 at this time.

[0040] Metal posts 160 of Figure 1A and 1B have a greater height or length as compared to die interconnects 110. Thus, in some embodiments metal posts 160 are not plated at the time of plating die interconnects 110 since first mask layer 215 has a height to match a desired height for die interconnects 110 and not for metal posts 160. The formation of metal posts 160 may then begin with a deposition of a second mask layer 220 over seed layer 210 as shown in **Figure 2E**. As compared to first mask layer 215 (Figure 2C), second mask layer 220 has a greater thickness or height so as to accommodate the greater height of metal posts 160 as compared to die interconnects 110. Analogous to first mask layer 215, second mask layer 220 is patterned to re-expose and enlarge metal post openings 225.

[0041] Metal posts 160 may then be plated into metal post openings 225 and second mask layer 220 stripped or otherwise removed as shown in **Figure 2F**. Similarly, the exposed portions of seed layer 210 are also etched away at this time. However, there will remain those portions of seed layer 210 (not illustrated) onto which die interconnects 110 and metal posts 160 were plated. The etching of seed layer 210 may produce the same amount of undercut (not illustrated) on those portions remaining under die interconnects 110 and metal posts 160.

[0042] The attachment of dies 105 is illustrated in **Figure 2G**. Interconnects on dies 105 such as solder bumps 107 or copper pillars electrically couple to corresponding die interconnects 110 on panel or wafer 215. An underfill 240 may also be applied at this time to assist in securing dies 105 to panel or wafer 215.

[0043] After dies 105 have been attached, a mold compound 245 may then be applied to at least partially encapsulate dies 105 as shown in **Figure 2H**. Mold compound also partially encapsulates metal posts 160. An upper surface for both metal posts and dies 105 may be left exposed after application of mold compound 245. Alternatively, a grinding process may be used to expose metal posts 160.

[0044] Through-substrate vias 185 may then be exposed on the bottom or board-facing surface of interposer core 120. For example, a manufacturer may grind board-facing side 202 of wafer or panel 215 to expose what had been the blind ends of conductive blind vias 200 (shown, for example in **Figure 2H**) to form through substrate-vias 185. A board-facing redistribution layer 150 may then be deposited on board-facing surface 202 along with a solder resist or passivation layer 136 that is patterned for form openings for solder balls 155 as shown in **Figure 2I**.

[0045] Since the manufacturing steps discussed above with regard to **Figures 2A** through **2I** were directed to a WLP embodiment, these steps may all be performed on intact wafer or panel 215. Dicing from panel 215 thus provides a completed bottom package 250 as shown in **Figure 2J**.

[0046] To provide a better appreciation of the density advantages for bottom package 250, its die-facing surface is shown in plan view in **Figure 3**. Metal posts 160 are arranged on a periphery of bottom package 250 with regard to dies 105. Mold compound 245 fills the spaces between metal posts 160 and dies 105. But such an arrangement need not include the keep-out area between metal posts 160 and dies 105

as in conventional interconnect bar packages. As discussed previously, the manufacture of an interconnect bar requires a certain keep-out area with regard to its perimeter in that the interconnect bar substrate is typically laser drilled to form vias for the subsequent plating of metal posts. Such drilling cannot be performed too closely to the interconnect bar substrate perimeter. In sharp contrast, metal posts 160 are deposited on the same seed layer 210 on which die interconnects 110 are deposited as discussed with regard to, for example, Figure 2F. Density becomes even worse for conventional bottom packages that use solder balls for the interconnects to the top package. Thus, bottom package 250 has advantageously increased density as compared to conventional approaches. A flowchart summarizing the manufacturing process will now be discussed.

Example Method of Manufacture Summary

[0047] The method of manufacture may be summarized as shown in the flowchart of **Figure 4**. A step 400 comprises exposing a redistribution layer through a plurality of die interconnect openings and a plurality of metal post openings within a dielectric layer on a substrate surface. The formation of die interconnect openings 201 shown in Figure 4C as well as the formation of metal post openings 235 shown in Figure 2E are examples of step 400. A step 405 comprises forming die interconnects in the die interconnect openings. The formation of die interconnects 110 shown in Figure 2D provides an example of step 405. Finally, a step 410 comprises forming metal posts in the metal post openings. The formation of metal posts 160 shown in Figure 2F provides an example of step 410.

Example Electronic Systems

[0048] Integrated circuit packages including a bottom package with metal posts as disclosed herein may be incorporated into a wide variety of electronic systems. For

example, as shown in **Figure 5**, a cell phone 500, a laptop 505, and a tablet PC 510 may all include an integrated circuit package incorporating a metal-post-containing bottom package constructed in accordance with the disclosure. Other exemplary electronic systems such as a music player, a video player, a communication device, and a personal computer may also be configured with integrated circuit packages constructed in accordance with the disclosure.

[0049] As those of some skill in this art will by now appreciate and depending on the particular application at hand, many modifications, substitutions and variations can be made in and to the materials, apparatus, configurations and methods of use of the devices of the present disclosure without departing from the spirit and scope thereof. In light of this, the scope of the present disclosure should not be limited to that of the particular embodiments illustrated and described herein, as they are merely by way of some examples thereof, but rather, should be fully commensurate with that of the claims appended hereafter and their functional equivalents.

Claims

We claim:

1. A package, comprising:
 - a substrate;
 - a die-side redistribution layer;
 - a seed layer on the die-side redistribution layer;
 - a plurality of die interconnects electrically coupled to the die-side redistribution layer through the seed layer; and
 - a plurality of metal posts electrically coupled to the die-side redistribution layer through the seed layer.
2. The package of claim 1, further comprising at least one die electrically coupled to at least a subset of the plurality of die interconnects.
3. The package of claim 2, wherein the substrate comprises a glass interposer, and wherein the at least one die comprises a plurality of dies, each die being electrically coupled to a corresponding subset of the die interconnects.
4. The package of claim 3, further comprising a mold compound at least partially encapsulating the plurality of dies, and wherein both the die interconnects and the metal posts comprise a metal selected from the group consisting of copper and nickel.
5. The package of claim 2, further comprising a top package electrically coupled to the plurality of metal posts.

6. The package of claim 1, wherein the die interconnects comprise a plurality of solder bumps.
7. The package of claim 1, wherein the die interconnects comprise a plurality of solder pillars.
8. The package of claim 1, further comprising:
 - a plurality of through-substrate vias extending through the substrate;
 - a board-facing redistribution layer adjacent a board-facing surface of the substrate, wherein at least a subset of the through-substrate vias electrically couple the die-facing redistribution layer to the board-facing redistribution layer.
9. The package of claim 8, further comprising a plurality of solder balls adjacent the board-facing surface of the substrate, wherein the plurality of solder balls are electrically coupled to the board-facing redistribution layer.
10. The package of claim 8, wherein the die-facing redistribution layer and the board-facing redistribution layer each comprises a patterned copper metal layer.
11. A method, comprising:
 - forming a plurality of die interconnect openings through a dielectric layer adjacent a redistribution layer on a substrate;
 - forming a plurality of metal post openings through the dielectric layer;
 - forming die interconnects in the die interconnect openings; and
 - forming metal posts in the metal post openings.

12. The method of claim 11, further comprising:
depositing a seed layer on the redistribution layer, wherein forming the die interconnects comprises plating the die interconnects onto portions of the seed layer exposed within the die interconnect openings, and wherein forming the metal posts comprises plating the metal posts onto portions of the seed layer exposed within the metal post openings.
13. The method of claim 12, wherein plating the die interconnects and the metal posts comprises plating a metal selected from the group consisting of copper and nickel.
14. The method of claim 11, further comprising attaching at least one die to at least a subset of the die interconnects.
15. The method of claim 14, wherein attaching the at least one die comprises attaching a plurality of dies to the plurality of die interconnects.
16. The method of claim 15, further comprising at least partially encapsulating dies with mold compound.
17. The method of claim 11, further comprising:
forming the redistribution layer as a die-facing redistribution layer adjacent a die-facing surface of the substrate; and
forming a board-facing redistribution layer on a board-facing surface of the substrate.

18. The method of claim 17, further comprising:
forming a plurality of through-substrate vias extending through the substrate such that the through-substrate vias electrically couple between the die-facing redistribution layer and the board-facing redistribution layer.
19. The method of claim 13, wherein plating the die interconnects comprises depositing a first mask layer on the dielectric layer, patterning the first mask layer to expose the die interconnect openings, and plating the die interconnects into the exposed die interconnect openings.
20. The method of claim 19, wherein plating the metal posts comprises depositing a second mask layer on the dielectric layer, patterning the second mask layer to expose the metal post openings, and plating the metal posts into the exposed metal post openings.
21. A package, comprising:
an interposer;
a plurality of die;
a die-side redistribution layer;
a seed layer on the die-side redistribution layer;
means for electrically coupling the plurality of die to the die-side redistribution layer through the seed layer; and
a plurality of metal posts electrically coupled to the die-side redistribution layer.
22. The package of claim 21, wherein the interposer comprises a glass interposer.

23. The package of claim 21, wherein the interposer comprises semiconductor interposer.
24. The package of claim 21, further comprising a plurality of through-substrate vias extending through the interposer, wherein the plurality of through-substrate vias are electrically coupled to the die-side redistribution layer.
25. The package of claim 21, wherein the package is incorporated into at least one of a cellphone, a laptop, a tablet, a music player, a communication device, a computer, and a video player.
26. The package of claim 21, wherein the metal posts comprise plated copper metal posts.
27. A method, comprising:
plating metal posts and die interconnects onto an interposer; and
mounting a plurality of dies onto the die interconnects.
28. The method of claim 27, wherein plating the metal posts and the die interconnects comprises plating the metal posts and the die interconnects onto a seed layer.
29. The method of claim 28, further comprising depositing the seed layer through atomic layer deposition.
30. The method of claim 28, further comprising partially encasing the die and the metal posts with mold compound.

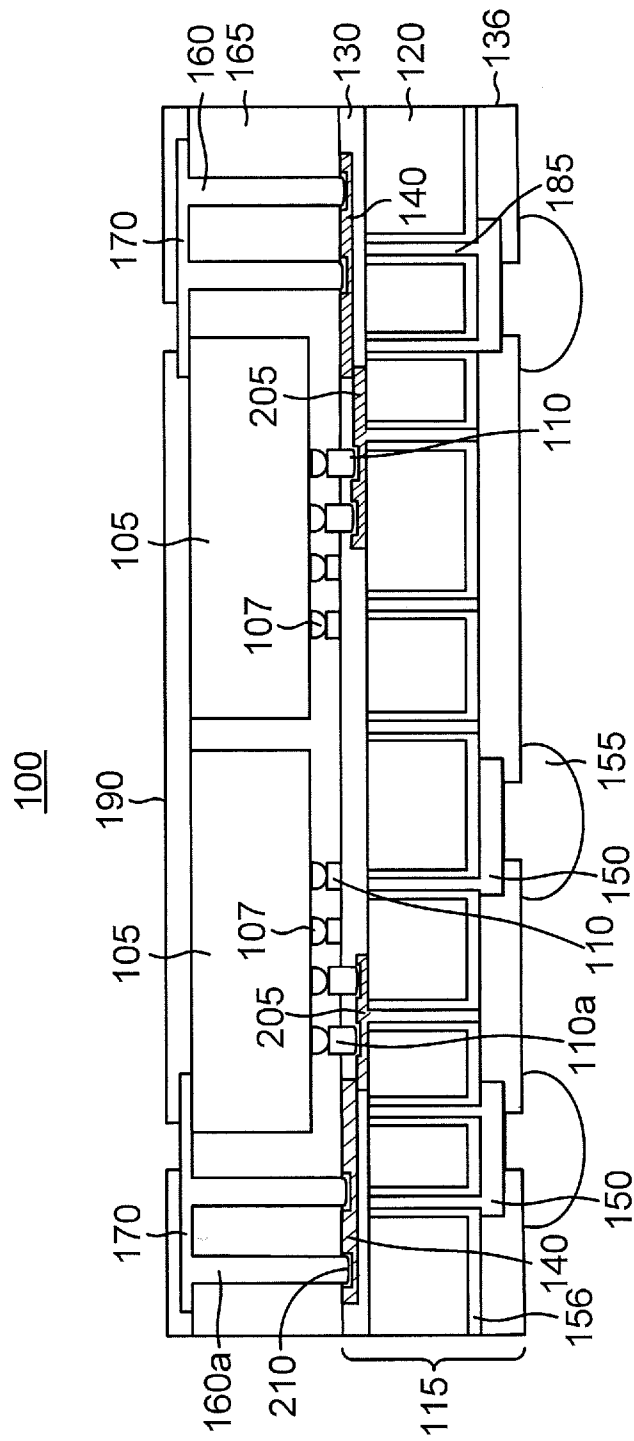


FIG. 1A

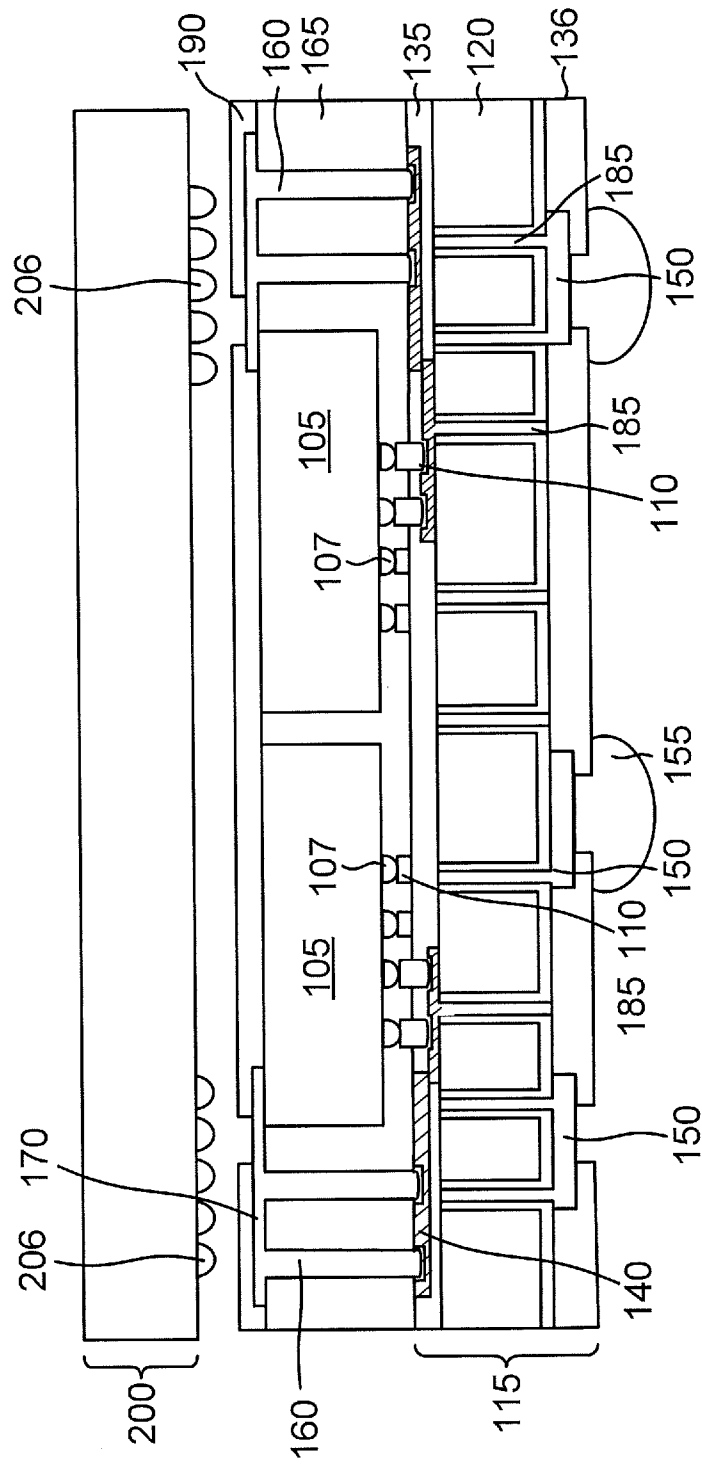
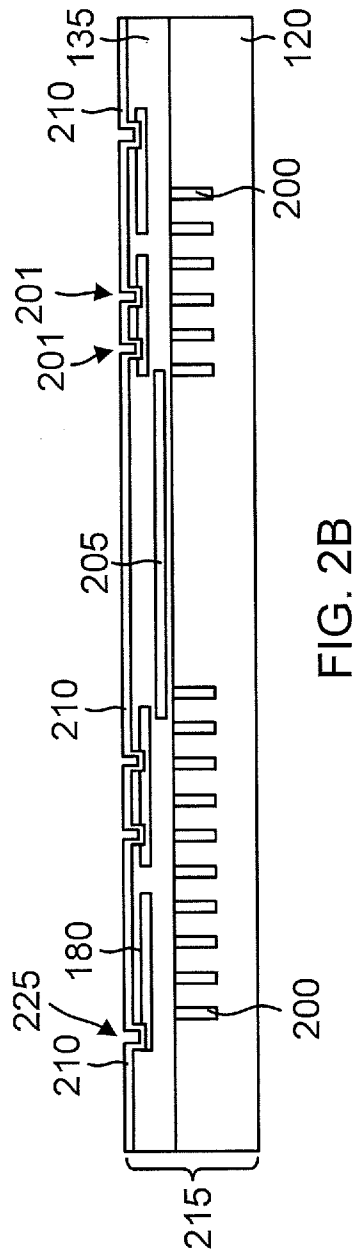
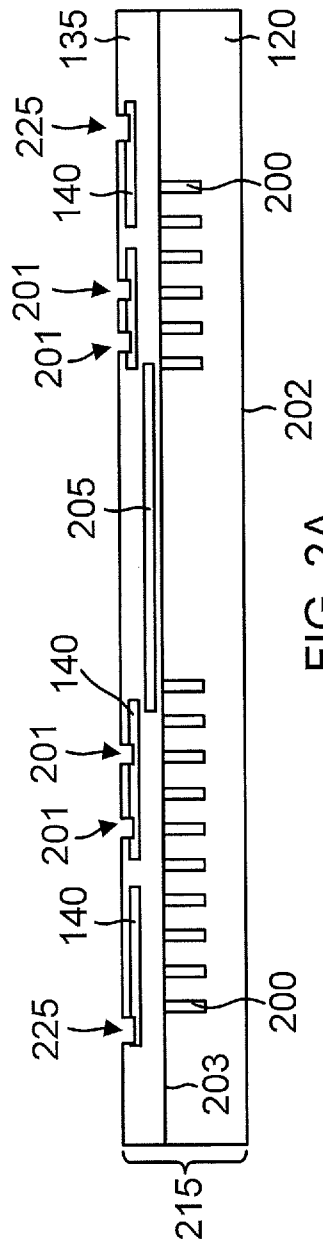


FIG. 1B



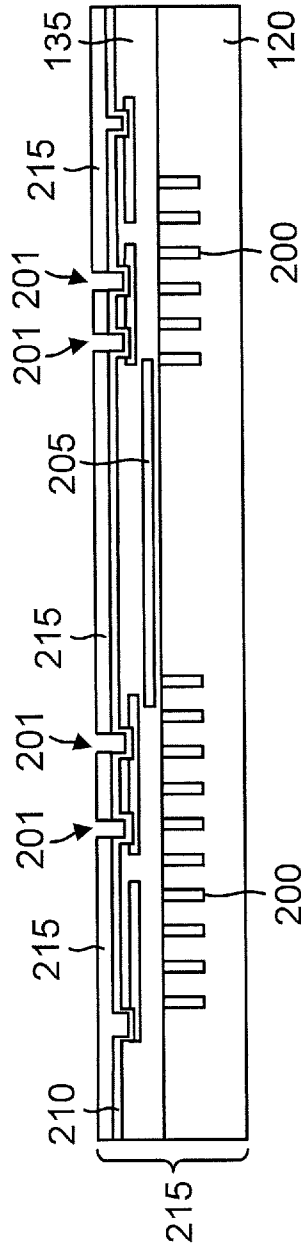


FIG. 2C

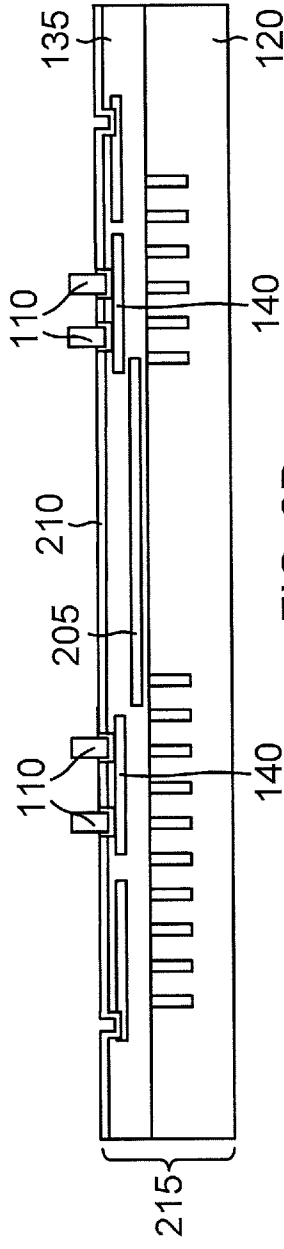


FIG. 2D

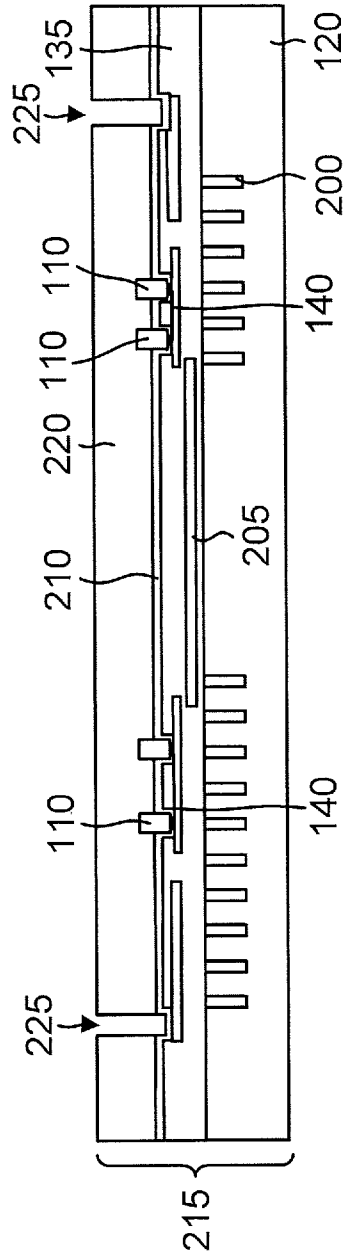


FIG. 2E

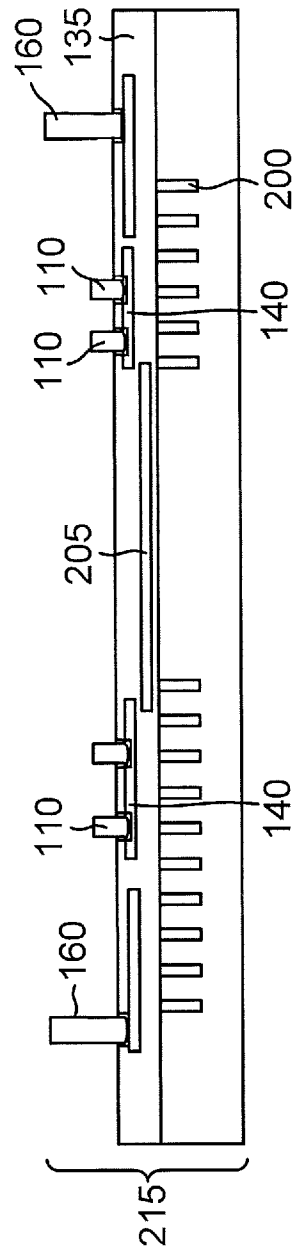
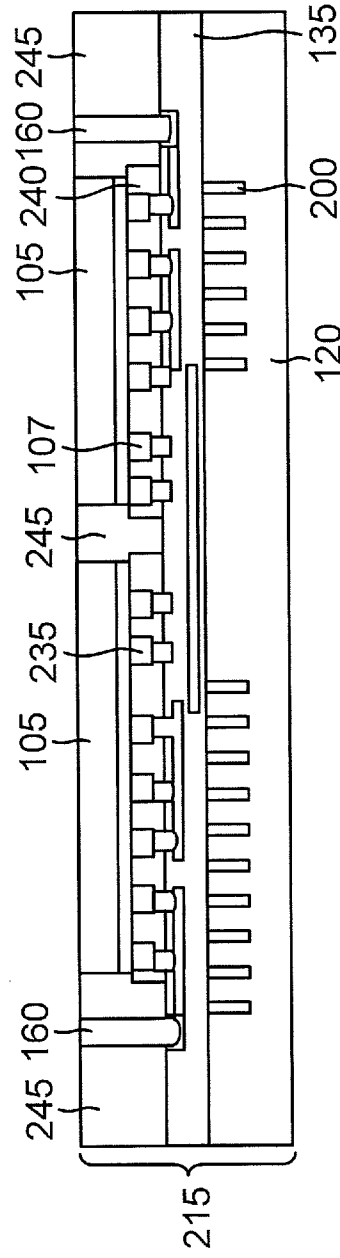
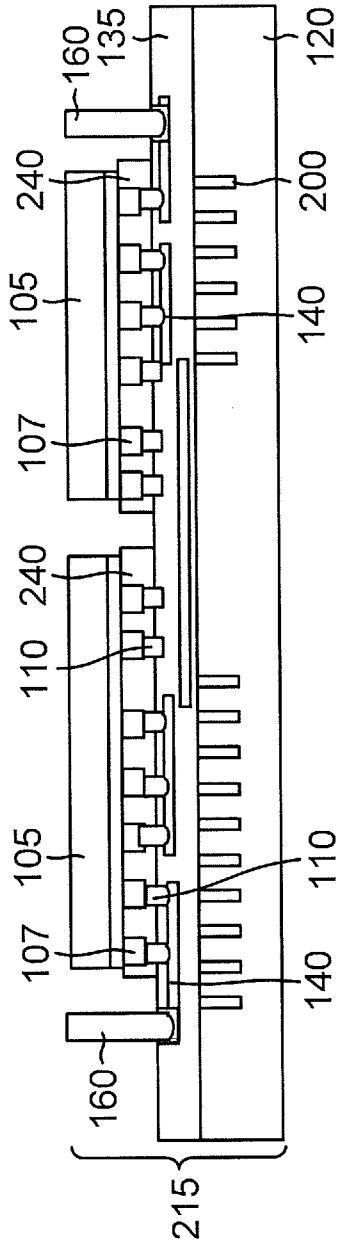


FIG. 2F



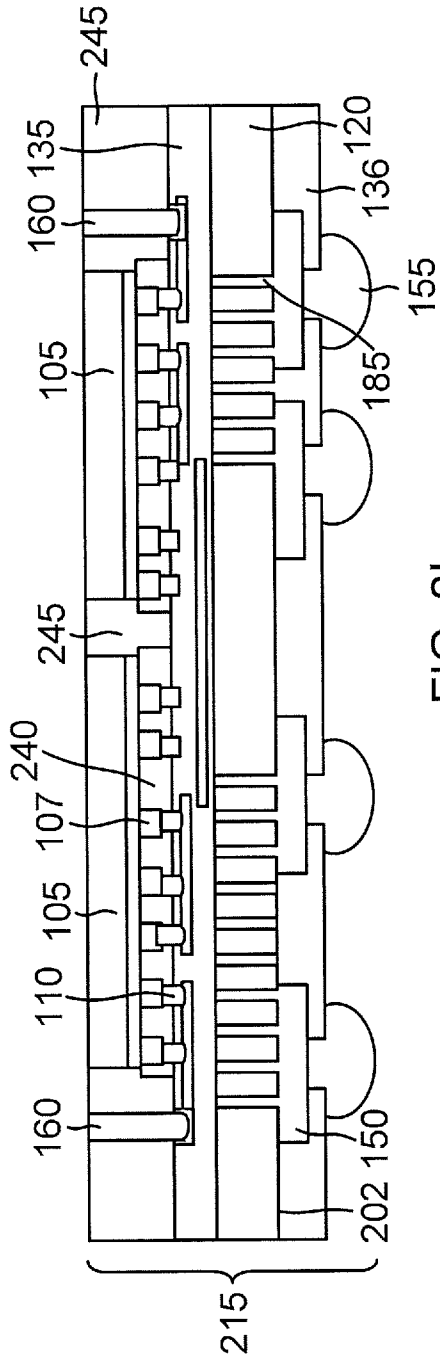


FIG. 2I

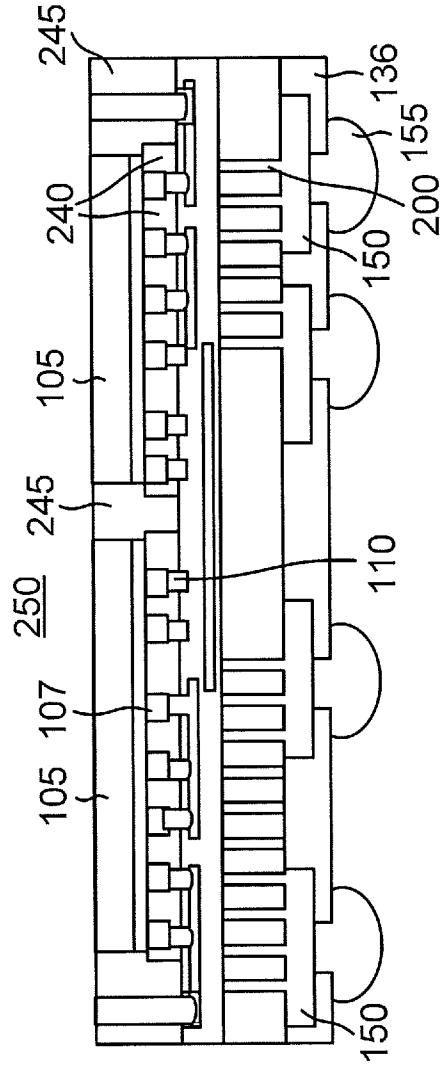


FIG. 2J

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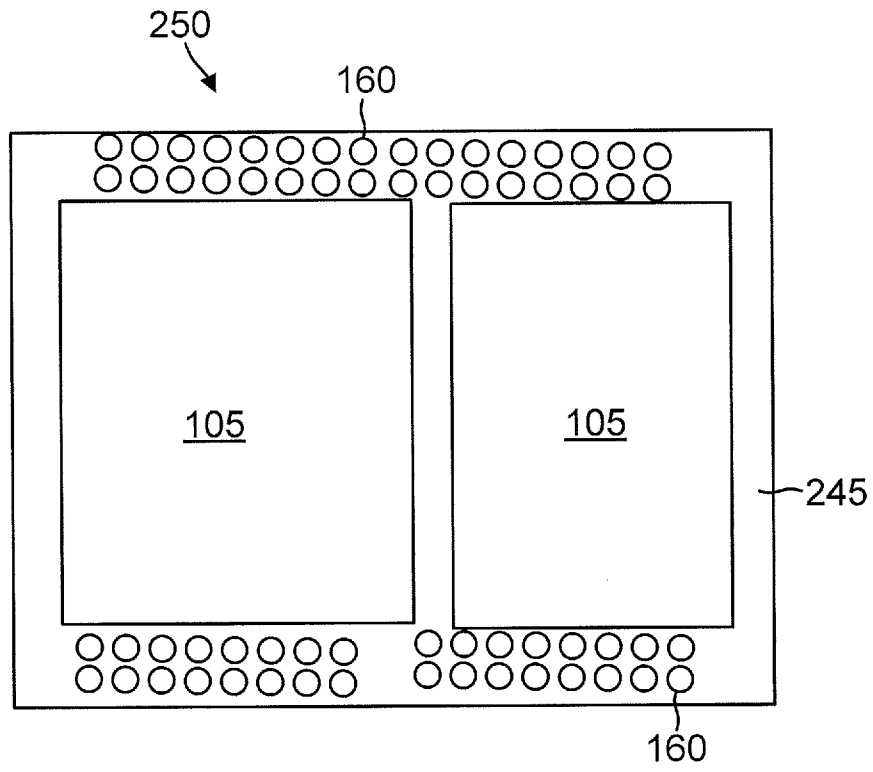


FIG. 3

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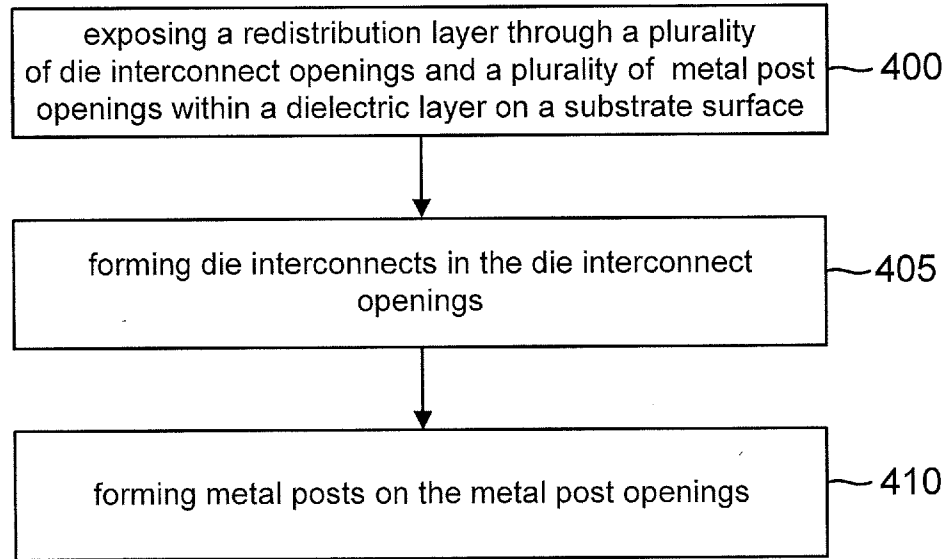


FIG. 4

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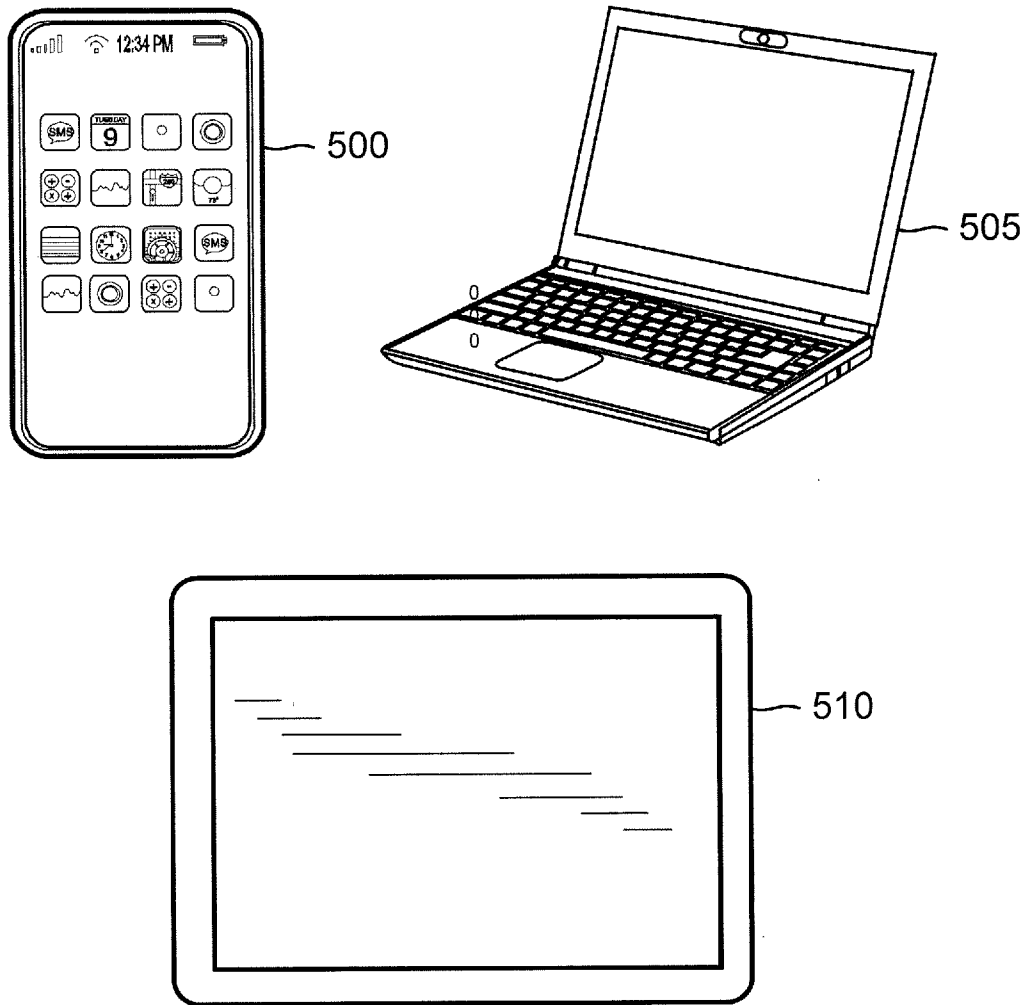


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/014870

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/48 H01L23/498 H01L25/10
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 744 362 A2 (SHINKO ELECTRIC IND CO [JP]) 17 January 2007 (2007-01-17)	1,2,5, 11-15, 19-21, 23,25-29
Y	paragraph [0053] - paragraph [0068]; figures 10-16 paragraph [0031] - paragraph [0037] paragraph [0075]	3,4,6,7, 16,22,30
Y	EP 1 418 617 A2 (SHINKO ELECTRIC CO LTD [JP] SHINKO ELECTRIC IND CO [JP]) 12 May 2004 (2004-05-12) paragraphs [0027], [0028], [0088]	3,22
Y	WO 2009/147148 A1 (COMMISSARIAT ENERGIE ATOMIQUE [FR]; BRUN JEAN [FR]) 10 December 2009 (2009-12-10) the whole document	4,16,30
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Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search 6 May 2015	Date of mailing of the international search report 15/07/2015
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Le Gallo, Thomas
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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/014870

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 1 909 323 A2 (SHINKO ELECTRIC IND CO [JP]) 9 April 2008 (2008-04-09) paragraph [0055]; figures 4K,4M -----	6,7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/014870

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-7, 11-16, 19-23, 25-30

Remark on Protest

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-7, 11-16, 19-23, 25-30

Package with a substrate and corresponding method

1.1. claims: 3, 22

package with a substrate/interposer which comprises a glass interposer

1.2. claims: 4, 16, 30

package with mold compound for at least encapsulating the dies on a substrate and corresponding method

1.3. claims: 6, 7

package with die interconnects made of solder material on a substrate

2. claims: 8-10, 17, 18, 24

package with a substrate with through-substrate vias and a redistribution layer on both surfaces and corresponding method

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2015/014870

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EP 1909323	A2	09-04-2008	CN 101159261 A	09-04-2008
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