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(54) **CELL FOR TRANSMIT ARRAY OR REFLECT ARRAY, TRANSMIT ARRAY OR REFLECT ARRAY, AND SYSTEM**

(57) A cell for a transmit array or a reflect array, the cell comprising an antenna which is a patch antenna or a ring resonator antenna, and at least one memristor (13, 13a, 13b) which is electrically connected in series with a respective conductive region (11, 111, 211, 311, 411, 418, 840P, 840N) of the antenna. A transmit array or a reflect array comprising a plurality of cells. A system comprising the array and further comprising a digital controller and, connectable to the digital controller, a corresponding interface circuit for each cell of the plurality of cells, wherein the digital controller in combination with the corresponding interface circuit are configured to controllably set the at least one memristor (13, 13a, 13b) of each cell to any of a first resistivity state and a second resistivity state.

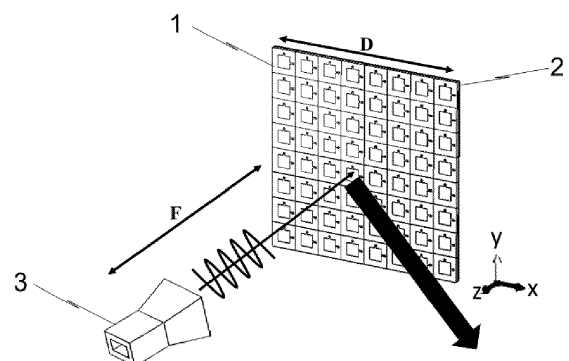


Fig. 1

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Description

TECHNICAL FIELD

[0001] The present invention relates to a cell for a transmit array or a reflect array. The present invention further relates to a transmit array or reflect array comprising a plurality of cells. Also, the present invention relates to a system comprising a transmit array or a reflect array.

STATE OF THE ART

[0002] There are known transmit arrays or reflect arrays comprising a plurality of cells. A particular important category of said arrays are the ones which comprise cells which are at a surface of the array and are actively controlled and tunable via a digital control such that the electric and magnetic properties of the surface, and hence, the reflection or transmission, respectively, of the electromagnetic waves by the surface is respectively actively controlled. Hence, the surfaces comprising said reconfigurable cells are also reconfigurable and are often called Reconfigurable Intelligent Surfaces (RISs). RISs are being developed for wireless communication systems, particularly towards 6G technology for communications, localization and sensing applications.

[0003] Over the past few decades, various techniques have been employed to achieve reconfigurability in RISs, including PIN diodes, MEMS, liquid crystals, and varactor diodes. These elements exhibit volatile switching behavior, necessitating a continuous power spending to maintain the desired switch states, which results in an energy demand that may be critical for the future scaling up of this technology to large areas in building surfaces and furniture.

[0004] A major disadvantage with the previously known arrays comprising the known conventional reconfigurable cells is that they do not address the static energy consumption problem because as mentioned further above the cells in the known arrays comprise elements which for maintaining their desired switch states require continuous power spending. Although RF MEMS devices achieve low power consumption, they face challenges due to their high switching voltages (typically in the range of 10-100 V) and complexities in fabrication and packaging. Therefore, it can be understood that the known conventional types of cells for transmit or reflect arrays and RISs, do not allow for solving the problem of achieving low or zero static energy consumption without requiring high switching voltages. Solving this problem is particularly important in the search for greener 6G technologies, i.e. environmentally sustainable in terms of energy and materials lifecycle.

DESCRIPTION OF THE INVENTION

[0005] The present invention overcomes the drawbacks of the conventional cells for transmit or reflect

arrays because it allows for solving the problem of achieving low or zero static energy consumption without requiring high switching voltages. Moreover, advantageously the present invention allows for solving said problem without imposing significant complications in the fabrication or packaging of the cells. In addition, advantageously the present invention may allow for solving said problem and, at the same time, for achieving fast switching time e.g. in the range of 1 microsecond. Also, the present invention may advantageously also allow for achieving reconfigurability of the cells at higher frequencies compared to many conventional types of cells and RISs.

[0006] In a first aspect of the invention, a cell for a transmit array or a reflect array is provided. The cell comprises an antenna which is a patch antenna or a ring resonator antenna. The cell also comprises at least one memristor which is electrically connected in series with a respective conductive region of the antenna.

[0007] Compared to conventional cells, the memristor of the cell of the present invention addresses the static energy problem and allows for achieving a low power consumption because the memristor typically can act as a non-volatile switch that requires no hold voltage for operation. Moreover, in preferred embodiments, the memristor of the present invention may advantageously allow for achieving fast switching times e.g. switching time in the range of 1 microsecond and low resistance, e.g. 4 ohms, in the ON state. Additionally, memristors may be of small size, e.g. $1 \mu\text{m} \times 1 \mu\text{m}$, and low capacitance e.g. $\sim 28 \text{ fF}/\mu\text{m}^2$, which makes them suitable for advantageously achieving reconfigurability at higher frequencies, e.g. up to 480 GHz, compared to conventional cells or conventional RISs.

[0008] In the cell of the present aspect of the invention, the memristor by being electrically connected in series with the respective conduction region of the antenna, it can allow for controlling the resistivity of the combination of the conduction of the region and the memristor, and hence, for controlling the electrical and magnetic properties of the antenna that comprises said conduction region.

[0009] It is noted that optionally the cell of the first aspect of the invention may comprise more than one memristor i.e. two or more memristors. In that case, each of the memristors may be connected to a respective conduction region of the antenna. Hence, optionally the antenna of the cell may optionally comprise more than one conductive regions, and at least one of said conduction regions may be connected to one, two or more memristors.

[0010] Preferably any or each of the at least one memristor comprises two conducting layers separated via (i.e. by) an insulating sheet. This preferred configuration of the memristor may advantageously allow the implementation of a non-volatile switching technique, as is explained further below.

[0011] In a first preferred exemplary embodiment of the

invention, the cell further comprises a first dielectric substrate, wherein the at least one memristor and the respective conductive region of the antenna are attached to a first surface of the first dielectric substrate. Some non-limiting examples of said dielectric substrate are fused silica, PTFE-based materials, ceramic- and hydro-carbon-based circuit laminates, which may advantageously contribute to the durability and the manufacturability of the cells. Preferably, the conduction region of the antenna may be formed on said first dielectric substrate via a metallization fabrication step.

[0012] In a preferred embodiment of the invention that is according to the first exemplary embodiment, the cell further comprises at least one first conductive channel which passes through the first dielectric substrate, and the cell also comprises a first ground plane that is electrically conductive, and wherein preferably a corresponding first terminal of the at least one memristor is connected to the first ground plane via the at least one first conductive channel. In the latter case, more preferably the first ground plane is attached to a second surface of the first dielectric substrate, the second surface being opposite to the first surface. In the latter embodiment, the configuration that involves the first conductive channel passing through the first dielectric substrate, advantageously allows for achieving a vertical structuring of the cell. In the optional case that said ground plane is at the aforementioned second surface of the first dielectric substrate, further optionally, said ground plane may have been formed on said second surface via a respective metallization step.

[0013] In a preferred embodiment of the invention that is according to the first exemplary embodiment, the cell further comprises a second dielectric substrate attached at a second surface of the first dielectric substrate oppositely the first surface of the first dielectric substrate. Preferably said second dielectric substrate is glued to the first dielectric substrate via an intermediate layer. It may be understood that said intermediate layer may be a layer of glue or another material that is configured to keep the second dielectric substrate glued or firmly attached to the first dielectric substrate. The use of the second dielectric layer may advantageously further contribute to the durability of the cell, and allow for the making of multilayer cell configurations, i.e. cells that comprise stacks of two or more layers.

[0014] In a preferred embodiment that is according to the previous preferred embodiment and, hence, comprises the second dielectric substrate and the at least one first conductive channel, moreover, the first ground plane is attached to a surface of the second dielectric substrate, and the at least one first conductive channel passes through (i.e. crosses) the second dielectric substrate.

[0015] In a second exemplary embodiment of the invention, the cell further comprises an electrical configuration which is electrically connected to the antenna and to the memristor. Said electrical configuration is suitable, this is to say the electrical configuration is configured, for

an application via the same of two or more different voltage difference values across the at least one memristor for respectively setting the at least one memristor to a first resistivity state, a second resistivity state and/or intermediate resistivity states. Preferably the electrical configuration comprises transistors, radio frequency decoupling elements or stubs, one or more H-bridges or microcontrollers, two or more conductive or biasing lines, or combinations thereof. Hence, preferably the electrical configuration may be an assembly of electrically electrical or electronic elements that is configured for the application via the same of the of two or more different voltage difference values across the at least one memristor. It may be understood in said second exemplary embodiment, said electrical configuration is electrically connected to the at least one memristor. It may also be understood that two or more voltage different values may refer to the corresponding values of the voltage difference between a first terminal of the memristor, and a second terminal of the memristor. Also, the aforementioned first resistivity state may be a high resistivity state (HRS) of the memristor, and the second resistivity state may be a low resistivity state (LRS) of the memristor, wherein the terms "high" and "low" are comparative for indicating that in the HRS the resistivity of the memristor is higher compared to the resistivity in the LRS. The HRS may also be called high resistance state, and the LRS may also be called low resistance state. Likewise, it may be understood that in the optional case that the cell comprises said electrical configuration, and at least one memristor is such that it can be set to one or more intermediate resistivity states by said electrical configuration, then the memristor's resistivity (or resistance) values at said one or more intermediate resistivity (or resistance) states would be between the value at the HRS and the value at the LRS. The HRS and LRS may respectively be, or be called, "OFF state" and "ON state".

[0016] In preferred embodiments, the at least one memristor is being configured to selectively exhibit an HRS (i.e. a first resistance state), an LRS (i.e. a second resistance state) and one or more intermediate states. It is noted that in the present disclosure the terms "resistance" and "resistivity" may be used interchangeably. More preferably, the at least one memristor is configured to exhibit a change in its resistivity between the HRS, the LRS and any possible intermediate state it may exhibit, without the resistivity change between the one or more intermediate states being accompanied by a change in a capacity of the memristor. This is to say, the at least one memristor may be configured to exhibit substantially the same capacitance when it exhibits and is at one or more intermediate states. In the latter case, the at least one memristor may advantageously allow the control of the reflection or transmission range of the antenna.

[0017] In some preferred embodiments that are according to the first and the second exemplary embodiments, at least a part of the electrical configuration is at the first surface of the first dielectric substrate, or at a

second surface of the first dielectric substrate, said second surface being opposite to the first surface. Optionally having at least part of the electrical configuration at the first or the second surface of the substrate, may advantageously contribute to improving the compactness of the cell.

[0018] In some preferred embodiments which are according to the second exemplary embodiment, and wherein the cell comprises the second dielectric substrate that is mentioned further above, at least part of the electrical configuration is attached to a first or a second surface of the second dielectric substrate. This may contribute to the efficient manufacturability of the cell, because it may facilitate the fabrication of the cell in a modular manner. Said fabrication may comprise forming or assembling the at least one memristor and the respective conductive part of the antenna at the first dielectric substrate, and separately forming and/or assembling part of the electrical configuration on the second dielectric substrate, and subsequently attaching to each other the first and the second dielectric substrates.

[0019] In a preferred embodiment which is according to the previous preferred embodiment, the cell further comprises at least one second conductive channel which passes (i.e. crosses) through the second dielectric substrate, and the cell also comprises a second ground plane that is electrically conductive and is at a second surface of the second dielectric substrate that is opposite the first surface of the second dielectric substrate, and a first member of the part of the electrical configuration attached to the first surface of the second dielectric substrate is connected to the second ground plane via the second conductive channel. It can be understood that the aforementioned optional configuration that involves the second conductive channel may advantageously allow the fabrication of cells that exhibit multilayer structure, are compact and exhibit optimized performance and properties. Moreover, in said optional configuration the first ground plane may preferably be an RF ground plane such as a plane that is configured to provide a direct path to ground potential for electrical currents of right frequency, for thereby advantageously improving and optimizing the performance of the cell. Likewise, in said configuration the second ground plane may be a DC ground plane such as a plane that is configured to provide a direct path to ground potential for DC-type electrical currents.

[0020] In a preferred embodiment that is according to the previous embodiment, the at least one first conductive channel also passes through the second dielectric substrate and electrically contacts a second member of the part of the electrical configuration attached to the first surface of the second dielectric substrate. In the latter case, preferably said at least one first conductive channel also passes through a corresponding opening of the second ground plane such that the at least one first conductive channel does not contact directly the second ground plane. Hence, said corresponding opening may

have a diameter that is larger than a cross section of the first conductive channel so that the latter does not directly contact, and hence is electrically isolated from, the second ground plane when passing through the latter's corresponding opening.

[0021] In a preferred embodiment of the invention the antenna is a patch antenna. In another preferred embodiment of the invention the antenna is a ring resonator antenna. In the optional case that the antenna is a patch antenna, advantageously the patch antenna may exhibit a low profile, so the antenna may be mounted or formed on a surface, and may be fabricated on a printed circuit board in a way that is not complex, thereby facilitating the potential use in a portable wireless device application. Advantageously, a ring resonator antenna may also exhibit a small size and be particularly suitable for potential portable wireless device applications of the cell.

[0022] In a preferred embodiment of the invention, the antenna is a patch antenna which comprises a first conductive region, a second conductive region and a third conductive region, wherein the second and the third conductive regions are separated from each other and from the first conductive region and are located on opposite positions with respect to the first conductive region, and the cell comprises two memristors of which one electrically connects to each other the first and the second conductive regions of the antenna, and the other one of the two memristors electrically connects to each other the first and the third conductive regions of the antenna. The latter preferred embodiment may advantageously allow for controllably switching the patch antenna between two phase states substantially equal to 0° and 180° , respectively. Said 0° and 180° phase states may respectively correspond to the case where the first of the two memristors is off (i.e. at an OFF state) while the second memristor is on (i.e. at an ON state), and to the case where the first resistor is on while the second memristor is off.

[0023] In a preferred embodiment of the invention, the antenna is a ring resonator antenna which comprises a first conductive region, a second conductive region, a third conductive region and a fourth conductive region which are separated from each other, wherein the first and the second conductive regions are arranged around an area in which the third and the fourth conductive regions are located, and the cell comprises two memristors of which one electrically connects to each other the first and the third conductive regions of the antenna, and the other one of the two memristors electrically connects to each other the third and the fourth conductive regions of the antenna.

[0024] The use of a ring resonator antenna in the cell may advantageously enable the use of the cell in a reflect or transmit array that may be electronically controlled via the element rotation approach which corresponds to the use of an electronically controlled element arrangement that can mimic a physical element rotation with a controlled phase shift. This is typically applied for circularly

polarized waves. In particular, the element rotation approach may be used to create a 180° phase shift in a linearly polarized wave.

[0025] In a preferred embodiment of the invention, the cell comprises two memristors and an interface circuit connected to the two memristors. Said interface circuit is connectable to an external circuit and is configured to control the two memristors in opposition such that the interface circuit can set any of the two memristors to a first or a second resistivity state. When the interface circuit sets a first one of the two memristors to a first resistivity state, it also sets a second one of the two memristors to a second resistivity state. Also, when the interface circuit sets the first memristor to the second resistivity state, it also sets the second memristor to the first resistivity state. As mentioned further above, the first resistivity state of the memristor may be the HRS of the memristor, and the second resistivity state of the memristor may be the LRS of the memristor. The interface circuit by being configured to control the two memristors in opposition such that when the first memristor is ON the other memristor is OFF, it may allow the switching the corresponding antenna of the cell between two phase states, substantially equal to 0° and to 180°. Preferably the interface circuit comprises any of an H-bridge or a microcontroller which are electronic elements that may enable controlling the two memristors in opposition.

[0026] In a second aspect of the invention, a transmit array or a reflect array is provided, said array comprising a plurality of cells of the first aspect of the invention. Preferably said array comprises a reconfigurable intelligent surface at which there are at least some of said cells of the array.

[0027] In a third aspect of the invention, a system is provided, wherein the system comprising an array of the second aspect of the invention, and further comprises a digital controller and also, connectable to the digital controller, a corresponding interface circuit for each cell of the plurality of cells, wherein the digital controller in combination with the corresponding interface circuit are configured to controllably set the at least one memristor of each cell to any of a first resistivity state and a second resistivity state. In a preferred embodiment the digital controller in combination with the corresponding interface circuit are also configured to controllably set the at least one memristor of each cell to one or more intermediate states.

[0028] In a preferred embodiment of the system of the third aspect of the invention, the system further comprises computing equipment that is configured to provide to the digital controller an encoding to achieve desired transmission/reflection amplitude and phase distribution and beamforming characteristics.

[0029] In a preferred embodiment of the third aspect of the invention, the digital controller in combination with the interface circuit is configured to enable a 1-bit phase control (180 degrees of phase tuneability), through the switching between two states of each memristor: a high

resistance state (e.g. >1000 ohm) to a low resistance state (e.g. <10 ohm).

[0030] In a preferred embodiment of the third aspect of the invention, the digital controller in combination with the interface circuit is configured to enable a 2-bit control of the transmission/reflection amplitude, by considering a multi-level cell operation regime of each memristor with 4 distinct resistive states levels. In the latter preferred embodiment, the memristor is correspondingly configured to exhibit said 4 distinct resistive states.

[0031] In a preferred embodiment of the third aspect of the invention, the digital controller in combination with the interface circuit is configured to enable an N-bit control of the transmission/reflection amplitude, by considering the multi-level cell operation regime of each memristor with 2^N distinct resistive states levels. In the latter embodiment, the memristor is correspondingly configured to exhibit said 2^N distinct resistive states.

[0032] In a preferred embodiment of the third aspect of the invention, the digital controller in combination with the interface circuit is configured to enable an N-bit phase control ($360/(2^N)$ degrees of transmission/reflection phase tuneability), by considering the integration of N memristors with 2 states control in each antenna element.

[0033] In a preferred embodiment of the third aspect of the invention, the digital controller in combination with the interface circuit is configured to enable an N-bit phase control ($360/(2^N)$ degrees of transmission/reflection phase tuneability), by considering the integration of N memristors with 2 states control in each antenna element, and M-bit control of the transmission/reflection amplitude by considering the multi-level cell operation regime of each memristor with 2^M distinct resistive states levels. In the latter embodiment, the memristor is preferably correspondingly configured to exhibit said 2^M distinct resistive states.

[0034] In a further aspect of the invention, a reconfigurable intelligent surface (RIS) is provided, wherein the RIS comprises a plurality of cells of the first aspect of the invention.

[0035] Additional advantages and features of the invention will become apparent from the detailed description that follows and will be particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] To complete the description and in order to provide for a better understanding of the invention, a set of drawings is provided. Said drawings form an integral part of the description and illustrate embodiments of the invention, which should not be interpreted as restricting the scope of the invention, but just as examples of how the invention can be carried out. The drawings comprise the following figures:

Fig. 1 illustrates a preferred embodiment of an array

according to the invention.

Fig. 2A illustrates an exploded view of parts of a preferred embodiment of a cell according to the invention.

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Fig. 2B illustrates a view of the part of the embodiment of Fig. 2B.

Fig. 2C illustrates part of the embodiment of Fig. 2A, and two equivalent circuits for said part.

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Fig. 2D illustrates part of the embodiment of Fig. 2A.

Fig. 2E illustrates part of the embodiment of Fig. 2A.

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Fig. 3A illustrates an example I-V curve for a switching mechanism operation of bi-polar memristors.

Fig. 3B illustrates an H-bridge biasing circuit for the memristor of the cell of Fig. 2A.

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Fig. 4 illustrates a control system for the embodiment of Fig. 1.

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Fig. 5A illustrates an exploded view of parts of a preferred embodiment of a cell according to the invention.

Fig. 5B illustrates a side view of parts of the embodiment of Fig. 5A.

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Fig. 5C illustrates a view of a part of the embodiment of Fig. 5A.

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Fig. 5D illustrates a view of a part of the embodiment of Fig. 5A.

Fig. 5E illustrates a view of a part of the embodiment of Fig. 5A.

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Fig. 5F illustrates a view of a part of the embodiment of Fig. 5A.

Fig. 6A illustrates an exploded view of parts of a preferred embodiment of a cell according to the invention.

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Fig. 6B illustrates a side view of parts of the embodiment of Fig. 6A.

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Fig. 6C illustrates a view of a part of the embodiment of Fig. 6A.

Fig. 6D illustrates a view of a part of the embodiment of Fig. 6A.

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Fig. 6E illustrates a view of a part of the embodiment

of Fig. 6A.

Fig. 6F illustrates a view of a part of the embodiment of Fig. 6A.

Fig. 7A illustrates an exploded view of parts of a preferred embodiment of a cell according to the invention.

Fig. 7B illustrates a side view of parts of the embodiment of Fig. 7A.

Fig. 7C illustrates a view of a part of the embodiment of Fig. 7A.

Fig. 7D illustrates a view of a part of the embodiment of Fig. 7A.

Fig. 8A illustrates an exploded side view of parts of a preferred embodiment of a cell according to the invention.

Fig. 8B illustrates a view of a part of the embodiment of Fig. 8A.

Fig. 8C illustrates a view of a part of the embodiment of Fig. 8A.

Fig. 8D illustrates a view of a part of the embodiment of Fig. 8A.

Fig. 8E illustrates a view of a part of the embodiment of Fig. 8A.

Fig. 8F illustrates a preferred embodiment of an array according to the invention.

Fig. 9A illustrates a preferred embodiment of an array according to the invention.

Fig. 9B illustrates an exploded side view of parts of a cell of the embodiment of Fig. 9A, wherein said cell is also a preferred embodiment according to the invention.

Fig. 9C illustrates a view of part of the embodiment of Fig. 9B.

Fig. 9D illustrates a view of part of the embodiment of Fig. 9B.

Fig. 9E illustrates a view of part of the embodiment of Fig. 9B.

Fig. 9F illustrates a view of part of the embodiment of Fig. 9B.

Fig. 9G illustrates a view of part of the embodiment of

Fig. 9B.

Fig. 10A illustrates a simulation set up of the unit cell of Fig. 2A.

Fig. 10B illustrates the simulated current distribution over the unit cell of Fig. 2A, when (a) the cell is at the ON state, and (b) the cell is at the OFF state.

Fig. 11 illustrates simulation results of the unit cell of Fig. 2A, specifically (a) Reflection loss, (b) Reflection phase, and (c) reflection phase difference.

Fig. 12 illustrates a preferred embodiment of a RIS according to the invention, illuminated by a 10-dBi horn antenna showing a reflected beam steered to an angle of 30° , and also shows patch and ground layers of 2×2 elements in the array of the RIS.

Fig. 13 illustrates a realized gain of an embodiment of a 8×8 RIS according to the invention, at a central frequency of 26.7 GHz in the plane $\Phi=0^\circ$ for steering angles 0° , 30° , and 60° and the corresponding phase distribution.

DESCRIPTION OF A WAY OF CARRYING OUT THE INVENTION

[0037] The following description is not to be taken in a limiting sense but is given solely for the purpose of describing the broad principles of the invention. Next embodiments of the invention will be described by way of example, with reference to the above-mentioned drawings, showing cells, arrays, RISs and systems according to the invention.

[0038] A preferred embodiment of a reflective array according to the second aspect of the invention is illustrated in Fig. 1. The array 1 of Fig. 1 comprises a plurality of cells 2 which are arranged at a surface of the array 2. Said surface can be considered as being a reconfigurable intelligent surface (RIS). The array configuration (i.e. the array 1) has a side length of D , is illuminated by a horn antenna 3 at a focal length of F . Each element, known as a unit cell 2, is equipped with a reconfigurable component that controls the phase distribution of the RIS, enabling, for example, precise control of beam steering characteristics. Said reconfigurable component is at least one memristor connected in series with a respective conductive region of the antenna of the cell. Given the pressing need for high-gain antennas in the 6G wireless communications technology, RISs are of high technological importance because they may offer high performance, lightweight design, compact size, and lower loss when compared to other types of devices such as parabolic reflectors. RISs may advantageously offer considerable benefits, particularly in beamforming radiation capabilities, making them of high interest for single user and multi-user communication applications in 6G networks. There-

fore, RISs may play a vital role in customizing the coverage area by adapting radiation patterns and enhancing energy efficiency for various applications, including satellite communications, sensing, localization, and network security improvement.

[0039] It is noted that a unit cell of a reflect array according to an aspect of the invention may preferably be electronically controlled via one of the following three main approaches: the tunable resonator approach, the guided wave approach, and the element rotation approach.

[0040] The tunable resonator approach corresponds to manipulating the phase of the scattered field from the elements by changing the resonance characteristics of the elements. This may for example be made in an element (i.e. a cell) that comprises a main patch and a secondary/parasitic patch connected to the main patch, by electronically controlling the connection of a main patch to the secondary/parasitic patch, therefore creating a change in the resonance characteristics of the element.

[0041] The guided wave approach comprises transitioning the space-waves received by the element to guided-waves, then imposing a phase-shift to the guided-waves using a guided-wave electronically controlled circuit ended with a short or open circuited transmission line stub, and then re-radiating the resulting wave.

[0042] The element rotation approach corresponds to the use of an electronically controlled element arrangement that can mimic a physical element rotation with a controlled phase shift. This is typically applied for circularly polarized waves.

[0043] It should be noted that combinations of the above-mentioned approaches can also enable the control of a unit cell installed in a reflect array, as well as in a transmit array. In particular, the element rotation approach may also be used to create a 180° phase shift in a linearly polarized wave. The at least one memristor when it is being controlled between an HRS and LRS may be used for realizing any of the aforementioned three control approaches. A transition between the HRS and the LRS may be considered as corresponding to a 1-bit control (manipulation of the reflection or transmission phase with a granularity of 180°). A higher resolution phase granularity (better than 180°) may preferably be achieved by combining multiple memristor devices (i.e. memristors) in a unit cell. Since a memristor in some cases may enable resistance control through the multi-level cell operation mode, this may be used to provide control of the reflection or transmission wave magnitude, which can be useful as an additional degree of freedom when computing a phase/amplitude profile of the reflector or transmit-array.

[0044] A preferred embodiment of a cell according to the first aspect of the invention is described next with reference to Fig. 2A-2E which illustrate the structure of each cell 2 of the array 1 of Fig. 1. The cell 2 comprises a

patch antenna and one memristor 13 which is electrically connected in series with a conductive region 11 of the antenna. Said conductive region 11 is a metallic square formed on a first surface of a first dielectric layer 51 of the cell 2. The memristor 13 is found in region A of said surface 51, and electrically connects said conductive region 11 to a second conductive region 17 of the antenna. The second conductive region 17 is connected via a first conductive channel 14 to a second biasing line 44 and to a first ground plane 21 of the cell. The first conductive channel 14 crosses the first dielectric substrate 51 and also crosses the first ground plane 21 and a second dielectric substrate 52 of the cell. The first ground plane 21 is located between the first dielectric substrate 51 and the second dielectric substrate 52. The conductive region 11 of the antenna is also connected to a first biasing line 41 of the cell via a second conductive channel 15 which contacts the first conductive region 11 and crosses and is substantially normal to the first dielectric substrate 51, the second dielectric substrate 52 and the first ground plane 21. The first ground plane 21 comprises an opening 22 the diameter of which is larger than a diameter of a cross section of the second conductive channel 15 such that the latter crosses the first ground plane 21 through said opening 22 such that it does not directly contact the first ground plane 21. Integrated at the first biasing line 41 there is also a radial stub 43 that serves for avoiding RF signal losses through this conduction path/line.

[0045] Also, it is noted that in the embodiment of Fig. 2A-2E the cell has a side size of $p = 0.4\lambda_0 = 4.5$ mm (considering a central frequency of 26.7 GHz). Also the first dielectric substrate 51 that is made of Fused Silica ($\epsilon_r = 3.81$, $\tan\delta = 0.0004$, thickness $t_1 = 0.5$ mm) and the second dielectric substrate 52 that is made of Taconic TLY-5 ($\epsilon_r = 2.2$, $\tan\delta = 0.0009$, thickness $t_2 = 0.25$ mm), are separated by the ground plane 21 that is a copper ground plane (dimensions: 4.45 mm $\times$ 4.45 mm). Fused Silica has been selected as the first substrate material due to its low surface roughness, advantageously offering favorable characteristics for fabricating directly memristors and benefiting their good performance. In the embodiment of Fig. 2A-2F, the first conductive region 11 that is a square patch with side length of $X = 2.5$ mm is printed on the top of the Fused Silica substrate layer and connected to one of the two biasing lines 41, 44 on the bottom of the Taconic substrate layer through the radial stub 43 that has with a size of $\lambda_0/4$, in order to avoid RF signal losses through this path. The memristor element may preferably be fabricated directly in the RIS unit cell, in a $10\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ empty space between two tapering sections as shown in Fig. 2C. The two biasing lines 41, 44 are designed (i.e. are configured or are suitable) to be connected to an FPGA-based digital controller through an H-bridge comprising four transistors to control the memristor switching mechanism. So, the memristor's HRS and LRS modes may be achieved by setting a single digital controller pin to either 'high' or 'low' voltage state to

initiate either the SET or RESET state of the memristor. In a simulation model, the memristor element may be replaced by its equivalent circuit as a lumped element in either the High Resistance State (HRS) or the Low Resistance State (LRS). In the HRS, it is represented by an OFF-Resistance (ROFF) in parallel with a Capacitor (COFF), while a low ON-Resistance (RON) represents the LRS, as illustrated in Fig. 2C. For the embodiment of Fig. 2A-2F, it may be considered that the principle of operation from an electromagnetic point of view comprises the following: the incident electromagnetic wave on the unit cell is converted into a surface current, and the square patch reradiates it based on the distributed current density. The reflection phase of the unit cell is electronically controlled by routing the current along different paths. When the memristor element is switched to an HRS state the current is distributed over the patch and reradiated directly, while when the memristor element is switched to an LRS state the current distribution is subject to an additional path to the ground plane, leading to re-radiation with a 180° phase shift. Consequently, a difference in the reflection phase is achieved using both switching states of the memristor. The geometrical dimensions of the unit cell may preferably be optimized through a parametric study, and in the particular embodiment of Fig. 2A-2F, said dimensions are the following: $p = 4.5$ mm, $x = 2.5$ mm, $w = 0.2$ mm, $l = 0.4$ mm, $v = 0.2$ mm, $t_1 = 0.5$ mm and $t_2 = 0.25$ mm.

[0046] The unit cell of Fig. 2A-2F achieves reconfigurability through a non-volatile switching technique, where no continuous power is needed to maintain the reconfiguration state; a voltage pulse is sufficient to change the state of the switch. Said non-volatile switching technique for the embodiment of Fig. 2A-2F is explained next with reference to the I-V curve of Fig. 3A which shows the schematic diagram of the complete memristor switching cycle, including the transition from HRS to LRS (curves 1+2) and the reverse transition from LRS to HRS (curves 3+4) in four steps. The memristor of the preferred embodiment of Fig. 2A-2F comprises two conducting layers separated with an insulating sheet resulting in the high-resistance state (HRS). The SET state is attained by applying a positive voltage difference between the two terminals of the memristor (V_1), leading to the formation of a metallic filament between its conducting layers (step 1). Once the filament is formed, the applied voltage can be removed, and the memristor memorizes its resistance state (LRS) (step 2). On the other hand, when a reverse voltage is applied to the memristor ($-V_2$), the conducting filament begins to break, preventing the transfer of electrons between terminals (step 3). As a result, the metallic filament is totally broken, and the memorized resistance state returns to HRS (step 4). The fact that both positive and negative voltages are required to switch between states implies that it may be possible, depending on the used circuit configuration, that the ground planes of different unit cells cannot be connected, as will be further explained further below. Yet, although in the embodiment

of Fig. 2A-2F a bipolar memristor is used, it may be possible to use bipolar memristors that could in principle circumvent this restriction.

[0047] Hence, the memristor of the cell may preferably be configured to exhibit a bipolar switching behavior, where positive and negative voltages are used to achieve set and reset functions, respectively. However, depending on the type of the memristor, and particularly of the materials used for fabricating the memristor, it may be possible to achieve also unipolar resistive switching, where the amplitude of current/voltage is responsible to set and reset the device rather than the polarity of the voltage bias.

[0048] Also, the memristor of the cell may preferably be configured to exhibit a multilevel cell (MLC) operation mode. The multilevel cell (MLC) operation mode allows one to achieve intermediate resistance levels. Through this method, at the set side, one may advantageously achieve a resistance higher than the typical value at the LRS, while on the reset side, one can achieve a resistance lower than the typical value at the HRS. This effect may be achieved either by the application of different current compliance (CC) on the set side to control the achieved LRS, or via reset-stop voltage on the reset side to control the final achieved LRS.

[0049] Preferably, the switching between the two states of the memristor, HRS and LRS, may be controlled by a digital controller through an H-bridge interface circuit comprising four transistors, providing two alternative conductive paths to the DC ground, as shown in Fig. 3B. The circuit generates a positive voltage difference for the SET operation (V_1), a negative voltage difference ($-V_2$) for the RESET operation, and passes through zero Volt during transitions. Both SET and RESET operations are associated with the logic levels of the digital controller (e.g., 'Logic high' for SET and 'Logic low' for RESET). Fig. 4 illustrates the control circuit for the entire RIS configuration of Fig. 1, wherein said RIS configuration comprises a plurality of cells as the one of Fig. 2A-2F. Fig. 4 may also be considered as illustrating the control of a preferred embodiment of a system according to an aspect of the invention, wherein said system comprises the RIS configuration, a digital controller and also, connectable to the digital controller, a corresponding interface circuit for each cell of the plurality of cells, wherein the digital controller in combination with the corresponding interface circuit are configured to controllably set the at least one memristor of each cell to any of the first resistivity state (i.e. the HRS) and the second resistivity state (i.e. the LRS). Each unit cell in the RIS contains an individual memristor controlled independently by the digital controller pins, s_1 to s_M (with M being the total number of memristors/unit cells) through an H-bridge circuit. Finally, the digital controller may preferably be connected to a computer for providing an encoding to achieve the desired amplitude/phase distribution and beamforming characteristics. Hence, the system according to the invention, very preferably further comprises

computing equipment (e.g. a computer) that is configured (e.g. is programmed) to provide to the digital controller an encoding to achieve desired amplitude/phase distribution and beamforming characteristics.

[0050] Another embodiment of a cell that is according to first aspect of the invention is explained next with reference to Fig. 5A-5F. The cell is suitable for implementing the guided wave approach, has a multilayered structure and comprises a square-shaped conductive region 111 that is the square patch of a patch antenna and is located attached to a first surface 110 of a first dielectric substrate 151. A second surface 120, opposite the first surface 110, of the first dielectric substrate 151 is attached via an adhesive layer 153 to a first surface 130 of a second dielectric substrate 152 which also comprises a second surface 140 that is opposite the first surface 130 of the second dielectric substrate 152. The conductive region 111 is electrically connected in series to a first terminal of a memristor 13, and a second terminal of the memristor is connected via a respective conductive line 112 to a first conductive channel 114. Said first conductive channel 114 is normal to and crosses the first and the second dielectric substrates 151, 152, as well as a first ground plane 121 and a second ground plane 131 of the cell. In the embodiment of Fig. 5A-5F the first ground plane 121 is an RF ground and is attached to the second surface 120 of the first dielectric substrate 151, and the second ground plane 131 is an DC ground and is attached to the first surface 130 of the second dielectric substrate 152. On the second surface 140 of the second dielectric substrate 152 there is an interface circuit that comprises two parts which are respectively connectable to a first external biasing line and a second external biasing line. Voltages V_1 and V_2 may be applied to the first and second external biasing lines, respectively. The first of the two parts of the interface circuit comprises two transistors 42 which are connected to each other via a line 141 that also integrates a radial stub 43 and is connected, via a third conductive channel 115 and a line 112 which is the first surface 110 of the first dielectric substrate 151, to the conductive region 111 of the antenna. Also, one of the two transistors 41 of the first part is connectable to the first external biasing line, and the other of the two transistors 41 is also connected via a respective line 141a and a fourth conductive channel 132 to the second ground plane 131. The two transistors 42 of the second part of the interface circuit are also connected to each other via a respective line 141b that is further connected to the first conduction channel 141. One of the two transistors of said second section is connected to the second external biasing line, and the other one of the two transistors is connected via a second conduction channel 134 to the second ground plane 131. The first 114 and the third 115 conduction channels are substantially normal and cross the first 151 and second 152 dielectric substrates and the adhesive layer 153. The first conduction channel 114 contacts the first ground plane 121, and does not contact directly the second

ground plane 131 which comprises a respective opening 135 through which the first conduction channel 114 passes without contacting directly the second ground plane 131. Also, the second conductive channel 115 does not contact directly the first ground plane 121 which comprises a respective opening 122 through which the second conduction channel 115 passes without contacting directly the first ground plane 121. Similarly, the second conductive channel 115 does not contact directly the second ground plane 131 which comprises a respective opening 133 through which the second conduction channel 115 passes without contacting directly the second ground plane 131.

[0051] Another embodiment of a cell that is according to first aspect of the invention is explained next with reference to Fig. 6A-6F. The cell is suitable for implementing the tunable resonator approach, has a multi-layered structure and comprises a ring resonator antenna that comprises a conductive region 211 that is shaped as a square ring and attached to a first surface 210 of a first dielectric substrate 251. A second surface 220, opposite the first surface 210, of the first dielectric substrate 251 is attached via an adhesive layer 253 to a first surface 230 of a second dielectric substrate 252 which also comprises a second surface 240 that is opposite the first surface 230 of the second dielectric substrate 252. The cell also comprises a first ground plane 221 that is attached to the second surface 220 of the first dielectric substrate 251, and a second ground plane 231 that is attached to the first surface 230 of the second dielectric substrate 252. The ring-shaped conductive region 211 is electrically connected in series to a first terminal of a memristor 13, and a second terminal of the memristor is connected to another conductive region 216 that is square-shaped and is also attached to the first surface 210 of the first dielectric substrate and is surrounded by the ring-shaped conductive region 211. The square-shaped conductive region 216 and the ring-shaped conduction region 211 of the ring-resonator antenna of the cell do not directly contact each other. The square-shaped conductive region 216 of the antenna is connected via a first conductive channel 214 to a first part of an interface circuit that is at the second surface 240 of the second dielectric substrate 252. Said first part of the interface circuit is connectable to a first external biasing line and comprises two transistors 42 that are connected to each via a respective line 241a that is also connected to said first conductive channel 214, and one of said two transistors 42 is connectable to said external biasing line whereas the other of the two transistors is connected via a second conduction channel 232 to the second ground plane 231 of the cell. Also, the ring-shaped conductive region 211 of the antenna is connected via two third conduction channels 215a, 215b to a second part of the interface circuit. The second part of the interface circuit is connectable to a second external biasing line, and also comprises two transistors 42 which are connectable to each other via a line 241b that is connected to

each of the third conduction channels 215a, 245b. Voltages V1 and V2 may be applied to the first and second external biasing lines, respectively. Also, said second part of the interface circuit comprises two radial stubs 43 each of which is integrated in said line 241b close to a respective one of the third conductive channels 215a, 215b. One of the two transistors 42 of the second part of the interface circuit is connectable to the second external biasing line whereas the other one is connected via a fourth conduction channel 234 to the second ground plane 231. The second 232 and the fourth 234 conduction channels pass through (i.e. cross) and are substantially normal to the second dielectric substrate 252. The first 214 and the third 215a, 215b conduction channels pass through (i.e. cross) and are substantially normal to the first dielectric substrate 251, the first ground plane 221, the second ground plane 231 and the second dielectric substrate 252. The first conduction channel 214 contacts, and hence is directly connected to, the first ground plane 221, but does not contact directly the second ground plane 231 which comprises a respective first opening 235 through which the first conductive channel 214 passes without contacting directly the second dielectric substrate 231. Each of the third conduction channels 215a, 215b does not contact directly nor the first ground plane 221 nor the second ground plane 231, and for this purpose, the first ground plane comprises respective openings 222a, 222b through which a respective one of the third conduction channels 215a, 215b passes. Likewise, the second ground plane 231 comprises second openings 233a, 233b through which passes a respective one of the third conduction channels 215a, 215b. For this purpose, each of the second openings 233a, 233b has a diameter that is larger than the diameter of the respective third conduction channel 215a, 215b that passes therethrough. It is noted that the first ground plane 221 may be considered as being an RF ground, and the second ground plane 231 may be considered as being a DC ground. It is also noted, that the four transistors 42 advantageously enable achieving the a bipolar memristor control.

[0052] Another embodiment of a cell that is according to first aspect of the invention is explained next with reference to Fig. 7A-7D. The cell is suitable for implementing the tunable resonator approach, and comprises a main patch antenna which comprises a square shaped conductive region 311, and a parasitic patch antenna that comprises a rectangle-shaped conductive region 316, whereas said conductive regions 311, 316 are attached to a first surface 310 of a first dielectric substrate 351. The square shaped conductive region 311 is connected to a first terminal of the memristor 13, and the rectangle-shaped conductive region 316 is connected to a second terminal of the memristor 13. The cell also comprises an interface circuit that comprises two parts for respectively connecting the square-shaped conductive region 311 and the rectangle shaped conductive region 316 to two biasing lines to which voltages V1 and V2 may be applied

respectively. The first and the second parts of said interface circuit are also on the first surface 310 of the dielectric substrate 351. The first part comprises two transistors 42 which are connected to each other via line 341a that also integrates a radial stub 43 and is connected to the square-shaped conductive region 311 of the main antenna, whereas the one of the two transistors is connectable to the first biasing line, and the other of the two transistors of the first part is connectable via one first conductive channel 332 to a ground plane 321 of the cell. Said ground plane 231 is attached to a second surface 320 of the first dielectric substrate 351, said second surface 320 being opposite the first surface 310. The second part of the interface circuit also comprises two more transistors 42 which are connected to each other via line 341b that also integrates a respective radial stub 43 and is connected to the rectangle-shaped conductive region 316 of the parasitic antenna, whereas the one of the two transistors is connectable to the second biasing line, and the other of the two transistors of the second part is connectable via another first conductive channel 334 to the ground plane 321 of the cell. The first conductive channels 332, 334 cross (i.e. pass through) the dielectric substrate 351. It is noted that advantageously the radial stubs 43 enable avoiding the RF signal from escaping through the DC, and the four transistors 42 advantageously enable achieving a bipolar memristor control. The ground plane 320 of the cell may also be considered as being an RF ground.

[0053] Another embodiment of a cell that is according to first aspect of the invention is explained next with reference to Fig. 8A-6E. The cell is suitable for implementing the element rotation approach, has a multi-layered structure and comprises a ring resonator that comprises a first 411, a second 417, a third 416 and a fourth 418 conductive regions which are on a first surface 410 of a first dielectric substrate 451. Each of the first conductive region 411 and the second conductive region 417 is shaped as a half square-ring, and said first and second conductive regions are separated from each other and are arranged around a region of said first surface 410 at which there are the third 416 and the fourth 418 conductive regions each of which is square shaped and separated from the rest of the four conductive regions. The cell comprises two memristors 13a, 13b which are also on said first surface 410 of the first dielectric substrate 451. The first conductive region 411 is connected to a first terminal of the first memristor 13a, and the third conductive region 416 is connected to a second terminal of the first memristor 13a. The third conductive region 416 is also connected to a first terminal of the second memristor 13b, and the fourth conductive region 418 is connected to a second terminal of the second memristor 13b. The first dielectric substrate 451 also comprises a second surface 420 which is opposite to the first surface 410 and is attached via an adhesive layer 453 to a first surface 430 of a second dielectric substrate 452 which also comprises a second

surface 440 that is opposite the first surface 430 of the second dielectric substrate 452. The cell also comprises a first ground plane 431 that is attached to the second surface 440 of the second dielectric substrate 452. The third conductive region 416 of the ring resonator antenna is connected via a first conductive channel 414 to the first ground plane 431 of the cell. On the first surface 430 of the second dielectric substrate the first conductive channel 414 is also connected via lines 436, 437 to additional conduction lines 432, 434 which cross the second dielectric substrate 452, extending from the first 430 to the second 440 surface of the second dielectric substrate 452 and also contact and, hence, are connected to the ground plane 431. The cell further comprises two biasing lines 441a, 441b which are on the second surface 420 of the first dielectric substrate 451. The first biasing line 441a is connectable to a first external biasing line, and the second biasing line 441b is connectable to a second external biasing line. Voltages V1 and V2 may be applied to the first and second external biasing lines, respectively. Also, the first biasing line 441a integrates two radial stubs 43 and is connected via two second conductive lines 415a, 415b to two respective opposite ends of the first ring-shaped conductive region 411 of the ring resonator antenna. The second biasing line 441b also integrates two respective radial stubs 43 and is connected via two third conductive lines 433a, 433b to two respective opposite ends of the second ring-shaped conductive region 417 of the ring resonator antenna. The fourth conductive region 418 of the antenna is also connected to a fourth conductive channel 419, and the second conductive region is also connected to a fifth conductive channel 433c. At the second surface 420 of the first dielectric substrate 451 the fourth 419 and the fifth 433c conductive channels are connected via a respective conductive line. The second 415b, 415a, the third 433a, 433b, the fourth 419 and the fifth conduction channels extend from the first surface 410 to the second surface 420 of the first dielectric substrate 451, passing through the latter. The first conduction channel 414 passes through (i.e. crosses) the first 451 and the second 452 dielectric substrates, and the adhesive layer 453 that in the particular embodiment is a layer of glue. It is noted that the embodiment of Fig. 8A-8E may be used in a reflect array, and Fig. 8F illustrates such a reflect array 403 which comprises a plurality of cells 405 which are according to the embodiment of Fig. 8A-8E. The antenna 400 of Fig. 8F comprises a source 43, but it may alternatively comprise a plurality of sources 43. The source(s) irradiates, i.e. emits radiation towards, the cells 405 of the array 403. Each cell 405 comprises a first antenna element 205a that is the layer that faces the source 43 and is on the first surface 410 of the first dielectric substrate 451 and comprises the aforementioned conductive regions 411, 417, 416, 418. The cell 405 further comprises reflector element 405b that is the ground plane 431. The first surface 410 of the first dielectric substrate 451 can be considered as being the first surface of the array 403, and the second

surface 440 of the second dielectric substrate 452 can be considered as being the second surface of the array 403. Each cell 405 of the embodiment of Fig. 8F is preferably capable, in reflection mode, to receive the radiation emitted by source 43 on its antenna element 405a. Also, in said reflection mode, each of said cells 405 is capable to retransmit said radiation from its antenna element 405a, after reflection of said radiation by the reflector element 405b, for example by introducing a phase shift φ which may be known. Moreover, in reflection mode, each cell 405 of the embodiment of Fig. 8F, is preferably capable to receive the radiation on its antenna element 405b and to retransmit with the same phase shift φ this radiation from its antenna element 405a towards source 201, after reflection by reflector element 405b. The radiation reemitted by antenna element 405a may for example be focused on source 43, or on any other desired target. It is contemplated that the characteristics of a beam generated by antenna 400, and particularly its shape or profile and its maximum transmission direction or pointing direction, may depend on the values of the phase shifts respectively introduced by the cells 405 of the array 403.

[0054] A further embodiment of the invention is explained next with reference to Fig. 9A-9F. According to this embodiment, a first antenna element 805a of elementary cell 805 comprises a patch antenna which is adapted to capturing an electromagnetic radiation 800 emitted by a source 83, and a second antenna element 805b which comprises another patch antenna adapted to transmitting towards the outside of the antenna 805, a phase-shifted signal. Hence, Fig. 9A-9F illustrate an embodiment of a cell 805 that can be used as part of a transmit array 803 according to the first aspect of the invention. Said cell 805 comprises a first dielectric substrate 851 and a second dielectric substrate 852 which are attached together via an intermediate layer 853 that is prepreg adhesive layer. The second dielectric substrate 852 comprises a first surface 814, and also comprises a second surface on which there is deposited the first antenna element 805a, wherein the first surface 814 is opposite the second surface of the second dielectric substrate 852. The first dielectric substrate 851 comprises a first surface, and also comprises a second surface 850 which is attached via the prepreg layer 853 to the first surface 814 of the second substrate 852. The first surface of the first dielectric substrate 851 is opposite to the latter's second surface 850 and has attached on it the second antenna element 805b. The first antenna element 805a comprises a conductive region 820 a perimeter of which is square and inside which there is a U-turn slot which is substantially centered with respect to the conductive region 820 of the antenna and is arranged around a central region of said conductive region 820. Said central region is connected via a first conductive channel 816 to the center of a central square conductive region 840C of the second antenna element 805b. The cell further comprises a first ground plane 830 that is attached

to the first surface 814 of the second dielectric substrate 852 and is connected to the conductive region 820 via two second conductive channels 818 which respectively contact the first conductive region 820 at positions which are opposite to each and are aligned with the position where the first conductive channel 816 contacts the square conductive region 820 at about the latter's center. The second conductive channels 818 cross the second dielectric substrate 852 extending from the first surface 814 to the second surface of the said second substrate 852. The first conductive channel 816 crosses the second dielectric substrate 852, the ground plane 830 and the first substrate 851, and extend from the first antenna element 805a to the second antenna element 805b. The ground plane 830 comprises an orifice (i.e. an opening) 832 through which passes the first conductive channel 816 without directly contacting the ground plane 830. For this purpose, a diameter of the said orifice 832 is larger than a diameter of a cross section of the first conductive channel 816. On the second surface 850 of the first dielectric substrate 851 the cell further comprises an interface circuit that comprise a first biasing line 845 that is connectable to a first external biasing line, and a second biasing line that is connectable to a second external biasing line. Voltages V1 and V2 may be applied to the first and second external biasing lines, respectively. Each of the biasing lines 845, 846 of the interface circuit integrates two respective radial stubs 41. Each of the radial stubs 41 of the first biasing line 845 is positioned between the point of contact of the line 845 with the first external biasing circuit and a respective one of two third conductive channels 843 via which the biasing line 845 is respectively connected to a respective one of two ends of a second conductive region 840P of the second antenna element 805b. Similarly, each of the radial stubs 43 of the second biasing line 846 is positioned between the point of contact of the second biasing line 846 with the second external biasing circuit and a respective one of two fourth conductive channels 844 via which the second biasing line 846 is respectively connected to a respective one of two ends of a third conductive region 840N of the second antenna element 805b. Each of the second 840P and the third 840N conductive regions of the second antenna element 805b is U-shaped, and said second 840P and third 840N conductive regions are separated from each other (i.e. do not contact directly each other) via respective gaps located in between the respective ends at which the second 843 and the third conductive channels 844 conduct said second 840P and third 840N conductive regions. The second 840P and third 840N conductive regions are also separated from the central square-shaped region 840C which can be considered as being a first conductive region of the second antenna element 805b. Said first conductive region 840C is substantially surrounded by the second 840P, the third conductive region 840N and the gaps in between the second 840P and the third 840N conductive regions. The cell 803 further comprises a first memristor 13a and a second

memristor 13b which may be controlled via the biasing lines 845, 846 in opposite. The second conductive region 840P is connected to a first terminal of the first memristor 13a, and the first conductive region 840C is connected to a second terminal of the first memristor 13a. Similarly, the third conductive region 840N is connected to a first terminal of the second memristor 13b, and the first conductive region 840C is connected to a second terminal of the second memristor 13b. At the vicinity of the respective memristor 13a, 13b a respective portion of each of the first, second and third conductive region may preferably have a substantially triangular shape with characteristic dimensions D3, D6 and D7 as illustrate in Fig. 9G. Preferably, the first antenna element 805a, the second antenna element 805b, the ground plane 830 and the first and second biasing lines 845, 846 may be formed on the respective surface of the corresponding dielectric substrate by a respective metallization step.

[0055] From all the above it can be understood that in the embodiments of Fig. 2A-2E, Fig. 5A-5F, Fig. 6A-6F, Fig. 7A-7D, Fig. 8A-8F, Fig. 9A-9D, the cell comprises an antenna which is a patch antenna or a ring resonator antenna, and at least one memristor 13, 13a, 13b which is electrically connected in series with a respective conductive region 11, 111, 211, 311, 411, 418, 840P, 840N of the antenna.

[0056] Also, it can be understood that in the embodiments of Fig. 2A-2E, Fig. 5A-5F, Fig. 6A-6F, Fig. 7A-7D, Fig. 8A-8F, Fig. 9A-9D, the cell further comprises a first dielectric substrate 51, 151, 251, 351, 451, 851, wherein the at least one memristor 13, 13a, 13b and the respective conductive region 11, 111, 211, 311, 411, 418, 840P, 840N of the antenna are attached to a first surface 110, 210, 310, 410 of the first dielectric substrate 51, 151, 251, 351, 451, 851.

[0057] Also, it can be understood that in the embodiments of Fig. 2A-2E, Fig. 5A-5F, Fig. 6A-6F, Fig. 7A-7D, Fig. 8A-8F, Fig. 9A-9D, the cell further comprises at least one first conductive channel 14, 114, 214, 334, 332, 414, 816, 843, 844 which passes through the first dielectric substrate 51, 151, 251, 351, 451, 851, and the cell also comprises a first ground plane 21, 121, 221, 321, 431, 830 that is electrically conductive. Also, it can be understood that in some of the aforementioned embodiments, a corresponding first terminal of the at least one memristor 13, 13a, 13b is connected to the first ground plane 21, 121, 221, 431 via the at least one first conductive channel 14, 114, 214, 414. Also, in some of the aforementioned embodiments, the first ground plane 21, 121, 221, 321 is attached to a second surface of the first dielectric substrate 51, 151, 251, 351, the second surface being opposite to the first surface 110, 210, 310.

[0058] Also, it can be understood that in some of the aforementioned embodiments, the cell further comprises a second dielectric substrate 52, 152, 252, 452, 852 attached at a second surface of the first dielectric substrate 51, 151, 251, 451, 851 oppositely the first surface 110, 210, 410 of the first dielectric substrate 51, 151, 251,

451, 851, the second dielectric substrate 52, 152, 252, 452, 852 being glued to the first dielectric substrate 51, 151, 251, 451, 851 via a an intermediate layer 153, 253, 453, 853.

[0059] Also, it can be understood that in the embodiments of Fig. 2A-2E, Fig. 5A-5F, Fig. 6A-6F, Fig. 7A-7D, Fig. 8A-8F, Fig. 9A-9D, the cell further comprises an electrical configuration which is electrically connected to the antenna and the memristor 13, 13a, 13b and is suitable for an application via the same of two or more different voltage difference values across the at least one memristor 13, 13a, 13b for respectively setting the at least one memristor 13, 13a, 13b to a first resistivity state (e.g. the LRS), a second resistivity state (e.g. the HRS) or intermediate resistivity states. Preferably the electrical configuration comprises transistors 42, radio frequency decoupling elements or stubs 43, one or more H-bridges or microcontrollers, biasing (conductive) lines or combinations thereof.

[0060] Also, it can be understood that in some of the aforementioned embodiments, at least a part of the electrical configuration is at the first surface 310 of the first dielectric substrate 351, or at a second surface 420, 850 of the first dielectric substrate 451, 851, the second surface 420 being opposite to the first surface 410.

[0061] Also, it can be understood that in some of the aforementioned embodiments, at least part of the electrical configuration is attached to a second surface 140, 240 of the second dielectric substrate 152, 252.

[0062] Also, it can be understood that in some of the aforementioned embodiments, the cell further comprises at least one second conductive channel 134, 234, 232 passing through the second dielectric substrate 152, 252, and the cell also comprises a second ground plane 131, 231 that is electrically conductive and is at a first surface 130, 230 of the second dielectric substrate 152, 252 that is opposite the second surface 140, 240 of the second dielectric substrate 152, 252, and a first member of the part of the electrical configuration attached to the second surface 140, 240 of the second dielectric substrate 152, 252 is connected to the second ground plane 131, 231 via the second conductive channel 134, 234, 232.

[0063] Also, it can be understood that in some of the aforementioned embodiments, the at least one first conductive channel 114, 214 also passes through the second dielectric substrate 152, 252 and electrically contacts a second member of the part of the electrical configuration attached to the second surface 140, 240 of the second dielectric substrate 152, 252, the at least one first conductive channel 114, 214 also passing through a corresponding opening 135, 235 of the second ground plane 131, 231 such that the at least one first conductive channel 114, 214 does not contact directly the second ground plane 131, 231.

[0064] Also, it can be understood that in some of the aforementioned embodiments, the first ground plane 431, 830 is attached to a surface 440, 814 of the second dielectric substrate 452, 852, and the at least one first

conductive channel 414, 816 passes through the second dielectric substrate 452, 852.

[0065] Also, it can be understood that in the embodiments of Fig. 9A-9D, the antenna is a patch antenna which comprises a first conductive region 840C, a second conductive region 840P and a third conductive region 840N, wherein the second and the third conductive regions 840P, 840N are separated from each other and from the first conductive region 840C and are located on opposite positions with respect to the first conductive region 840C, and the cell comprises two memristors 13a, 13b of which one 13a electrically connects to each other the first and the second conductive regions of the antenna, and the other one 13b of the two memristors electrically connects to each other the first and the third conductive regions of the antenna.

[0066] Also, it can be understood that in the embodiments of Fig. 8A-8F, the antenna is a ring resonator antenna which comprises a first conductive region 411, a second conductive region 417, a third conductive region 416 and a fourth conductive region 418 which are separated from each other, wherein the first 411 and the second 417 conductive regions are arranged around an area in which the third 416 and the fourth conductive regions 418 are located, and the cell comprises two memristors 13a, 13b of which one 13a electrically connects to each other the first 411 and the third 416 conductive regions of the antenna, and the other one 13b of the two memristors electrically connects to each other the third 416 and the fourth 418 conductive regions of the antenna.

[0067] Also, it can be understood that a preferred embodiment, the cell comprises two memristors 13a, 13b and an interface circuit connected to the two memristors, wherein the interface circuit is connectable to an external circuit and is configured to control the two memristors 13a, 13b in opposition such that the interface circuit can set any of the two memristors to a first or a second resistivity state, and when it sets a first one of the two memristors to a first resistivity state, it also sets a second one of the two memristors to a second resistivity state, and when the external circuit sets the first memristor to the second resistivity state, it also sets the second memristor to the first resistivity state, preferably the interface circuit comprising any of an H-bridge or a microcontroller.

[0068] An operation of the cell illustrated by Fig. 2A-2E was performed, and particular findings from the performed simulations are explained below. The unit cell simulation model was excited using a Floquet port with normal incidence and analyzed with the full-wave EM simulator ANSYS HFSS under a periodic boundary condition, as depicted in Fig. 10A. The simulation results for the optimized structure were also confirmed using a CST simulation platform. Controlling the current distribution over the radiating element between the two states, State OFF and State ON, results in the reflection phase difference of 180° , as shown in the resultant current distribu-

tion illustrated in Fig. 10B. In Fig. 10B (a), a positive voltage difference has been applied to the memristor device through logic level 'high' in the digital controller resulting in a LRS state. Consequently, the current is shorted to the ground plane, minimizing the current value on the square patch element. On the other hand, when logic level 'low' is applied, a negative voltage difference is achieved across the memristor, resulting in HRS and high current distribution on the unit cell surface, as shown in Fig. 10B (b). The simulation of the proposed unit cell has been performed using two 3D electromagnetic simulator platforms, HFSS and CST. This validation and verification process using both platforms ensures confidence in the accuracy of the simulation results. The performance of the unit cell, in terms of reflection loss and reflection phase difference, is presented in Fig. 11, where it is shown that both HFSS and CST results are in perfect alignment, with only a slight shift in the reflection phase difference, as shown in graph (c) of Fig. 11. The reflection loss is less than 1 dB across the frequency band of 25-28.3 GHz. Additionally, the unit cell achieves a 180° phase difference at the central frequency of 26.7 GHz with an operation bandwidth of approximately 1 GHz (26.3-27.3 GHz), considering a phase difference between the two states of the RIS element of $|\Delta\Phi| = 180^\circ \pm 20^\circ$, as shown in graph (c) of Fig. 11.

[0069] To demonstrate and validate the simulated unit cell's capability when integrated into an array configuration, a simple 8×8 array with overall dimensions of $36 \times 36 \times 0.855 \text{ mm}^3$ and total number of 64 reflective elements has been designed and illuminated using a standard 10-dBi horn antenna. For simplicity, the horn antenna is positioned perpendicularly to the RIS at a height corresponding to the focal distance F. As represented in Fig. 12, the focal distance is set to achieve a ratio of $F/D = 0.8$, where D represents the aperture size of the RIS, ensuring a good compromise between both illumination loss and spill-over loss. In the concerned simulated embodiment, the ground planes of all memristors in the array configuration cannot be connected to each other to allow for independent positive and negative voltage application to each memristor. Consequently, in the simulated unit cell structure, the ground plane 21 is smaller than the substrate 51 by 0.05 mm in all directions, resulting in a 0.1 mm separation between all ground planes in the array configuration as depicted in Fig. 12.

[0070] Three scenarios were considered for beam-forming the antenna electromagnetic radiation towards different reflection angles: 0° , 30° , and 60° . The phase distribution of the unit cells has been configured using MATLAB. For instance, as shown in Fig. 12, the 3D visualization demonstrates the incident beam from the horn antenna being reflected towards an angle $\theta = 30^\circ$. These scenarios, with the phase distribution over the RIS configuration for each desired reflection angle, were considered in the EM simulator CST. In Fig. 13, the RIS gain has been plotted versus the beam steering angle (θ) in the $\Phi = 0^\circ$ plane for the discussed

scenarios in addition to the RIS phase distribution of each scenario. The 8x8 RIS successfully achieves the targeted beamforming characteristics such that the main beam angle could be controlled with a maximum gain of 13.2 dBi, 13.6 dBi, and 11.5 dBi at steering angles of 0°, 30°, and 60°, respectively. The relatively large side lobes may be explained by the small size of the modelled RIS.

[0071] Hence, the simulation study showed that the concerned unit cell of Fig. 2A-2F, achieved 1-bit phase reconfigurability at 26.7 GHz with an operational bandwidth of around 1 GHz. Additionally, the simulations showed that reflection loss over this frequency range was less than 0.6 dB. The simulation also showed that the aforementioned exemplary designed 8x8 RIS configuration has the ability to achieve beam steering. Also, preferred embodiments of the invention may comprise memristors which are configured to provide intermediate resistance levels between HRS and LRS through an effect known as multilevel cell programming. This may for example be achieved by preferably applying different current compliance levels in the memristor, thereby advantageously enabling additional flexibility in the control over the RIS's performance.

[0072] In this text, the term "comprises" and its derivations (such as "comprising", etc.) should not be understood in an excluding sense, that is, these terms should not be interpreted as excluding the possibility that what is described and defined may include further elements, steps, etc.

[0073] The invention is obviously not limited to the specific embodiment(s) described herein, but also encompasses any variations that may be considered by any person skilled in the art (for example, as regards the choice of materials, dimensions, components, configuration, etc.), within the general scope of the invention as defined in the claims.

Claims

1. A cell for a transmit array or a reflect array, the cell comprising an antenna which is a patch antenna or a ring resonator antenna, and at least one memristor (13, 13a, 13b) which is electrically connected in series with a respective conductive region (11, 111, 211, 311, 411, 418, 840P, 840N) of the antenna.
2. A cell according to claim 1, further comprising a first dielectric substrate (51, 151, 251, 351, 451, 851), wherein the at least one memristor (13, 13a, 13b) and the respective conductive region (11, 111, 211, 311, 411, 418, 840P, 840N) of the antenna are attached to a first surface (110, 210, 310, 410) of the first dielectric substrate (51, 151, 251, 351, 451, 851).
3. A cell according to claim 2, further comprising at least one first conductive channel (14, 114, 214, 334, 332,
- 414, 816, 843, 844) which passes through the first dielectric substrate (51, 151, 251, 351, 451, 851), and the cell also comprises a first ground plane (21, 121, 221, 321, 431, 830) that is electrically conductive, and wherein preferably a corresponding first terminal of the at least one memristor (13, 13a, 13b) is connected to the first ground plane (21, 121, 221, 431) via the at least one first conductive channel (14, 114, 214, 414), more preferably the first ground plane (21, 121, 221, 321) being attached to a second surface of the first dielectric substrate (51, 151, 251, 351), the second surface being opposite to the first surface (110, 210, 310).
4. A cell according to any of claims 2-3, further comprising a second dielectric substrate (52, 152, 252, 452, 852) attached at a second surface of the first dielectric substrate (51, 151, 251, 451, 851) oppositely the first surface (110, 210, 410) of the first dielectric substrate (51, 151, 251, 451, 851), preferably the second dielectric substrate (52, 152, 252, 452, 852) being glued to the first dielectric substrate (51, 151, 251, 451, 851) via an intermediate layer (153, 253, 453, 853).
5. A cell according to any of the previous claims, further comprising an electrical configuration which is electrically connected to the antenna and the memristor (13, 13a, 13b) and is suitable for an application via the same of two or more different voltage difference values across the at least one memristor (13, 13a, 13b) for respectively setting the at least one memristor (13, 13a, 13b) to a first resistivity state, a second resistivity state or intermediate resistivity states, preferably the electrical configuration comprising any of transistors (42), radio frequency decoupling elements or stubs (43), one or more H-bridges or microcontrollers, biasing lines or combinations thereof.
6. A cell according to claim 2 and 5, wherein at least a part of the electrical configuration is at the first surface (310) of the first dielectric substrate (351), or at a second surface (420, 850) of the first dielectric substrate (451, 851), the second surface (420, 850) being opposite to the first surface (410).
7. A cell according to claims 4 and 5, wherein at least part of the electrical configuration is attached to a second surface (140, 240) of the second dielectric substrate (152, 252).
8. A cell according to claim 7, further comprising at least one second conductive channel (134, 234, 232) passing through the second dielectric substrate (152, 252), and the cell also comprises a second ground plane (131, 231) that is electrically conductive and is at a first surface (130, 230) of the second

dielectric substrate (152, 252) that is opposite the second surface (140, 240) of the second dielectric substrate (152, 252), and a first member of the part of the electrical configuration attached to the second surface (140, 240) of the second dielectric substrate (152, 252) is connected to the second ground plane (131, 231) via the second conductive channel (134, 234, 232).

9. A cell according to claims 3 and 8, wherein the at least one first conductive channel (114, 214) also passes through the second dielectric substrate (152, 252) and electrically contacts a second member of the part of the electrical configuration attached to the second surface (140, 240) of the second dielectric substrate (152, 252), preferably the at least one first conductive channel (114, 214) also passing through a corresponding opening (135, 235) of the second ground plane (131, 231) such that the at least one first conductive channel (114, 214) does not contact directly the second ground plane (131, 231).
10. A cell according to claims 2 and 4, wherein the first ground plane (431, 830) is attached to a surface (440, 814) of the second dielectric substrate (452, 852), and the at least one first conductive channel (414, 816) passes through the second dielectric substrate (452, 852).
11. A cell according to any one of the previous claims, wherein the antenna is a patch antenna which comprises a first conductive region (840C), a second conductive region (840P) and a third conductive region (840N), wherein the second and the third conductive regions (840P, 840N) are separated from each other and from the first conductive region (840C) and are located on opposite positions with respect to the first conductive region (840C), and the cell comprises two memristors (13a, 13b) of which one (13a) electrically connects to each other the first and the second conductive regions of the antenna, and the other one (13b) of the two memristors electrically connects to each other the first and the third conductive regions of the antenna.
12. A cell according to any one of claim 1-10, wherein the antenna is a ring resonator antenna which comprises a first conductive region (411), a second conductive region (417), a third conductive region (416) and a fourth conductive region (418) which are separated from each other, wherein the first (411) and the second (417) conductive regions are arranged around an area in which the third (416) and the fourth conductive regions (418) are located, and the cell comprises two memristors (13a, 13b) of which one (13a) electrically connects to each other the first (411) and the third (416) conductive regions of the antenna, and the other one (13b) of the two memris-

tors electrically connects to each other the third (416) and the fourth (418) conductive regions of the antenna.

13. A cell according to any of the previous claims, comprising two memristors (13a, 13b) and an interface circuit connected to the two memristors, wherein the interface circuit is connectable to an external circuit and is configured to control the two memristors (13a, 13b) in opposition such that the interface circuit can set any of the two memristors to a first or a second resistivity state, and when it sets a first one of the two memristors to a first resistivity state, it also sets a second one of the two memristors to a second resistivity state, and when the external circuit sets the first memristor to the second resistivity state, it also sets the second memristor to the first resistivity state, preferably the interface circuit comprising any of an H-bridge or a microcontroller.
14. A transmit array or a reflect array comprising a plurality of cells which are according to any of the previous claims.
15. A system comprising an array according to claim 14, further comprising a digital controller and, connectable to the digital controller, a corresponding interface circuit for each cell of the plurality of cells, wherein the digital controller in combination with the corresponding interface circuit are configured to controllably set the at least one memristor (13, 13a, 13b) of each cell to any of a first resistivity state and a second resistivity state.

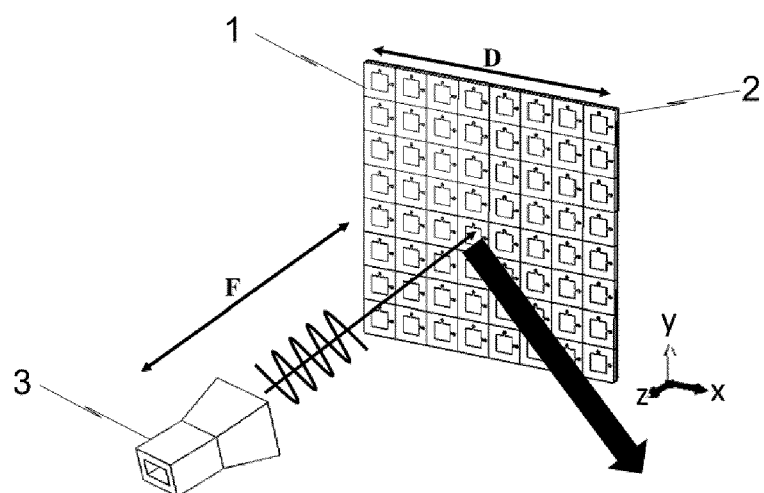


Fig. 1

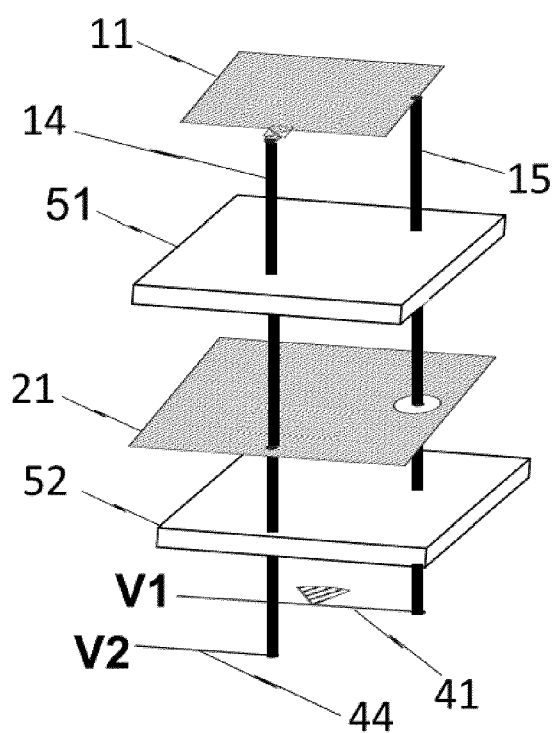


Fig. 2A

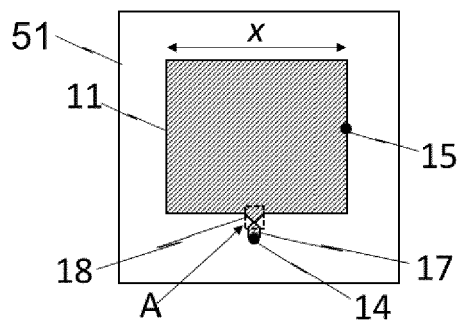


Fig. 2B

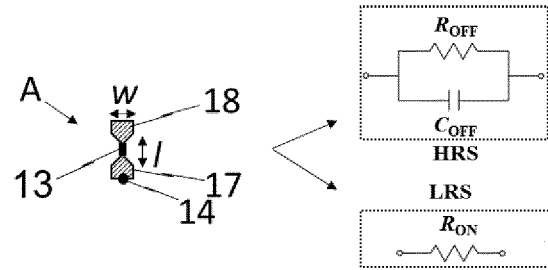


Fig. 2C

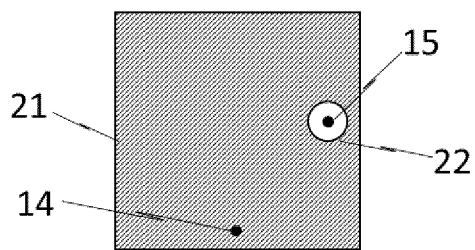


Fig. 2D

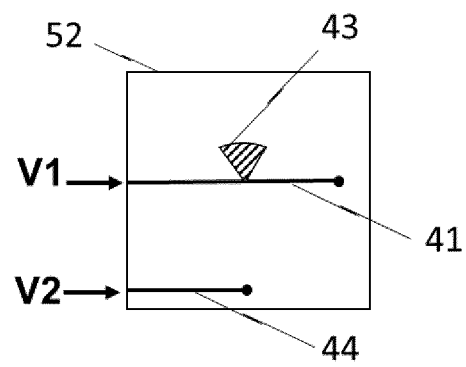


Fig. 2E

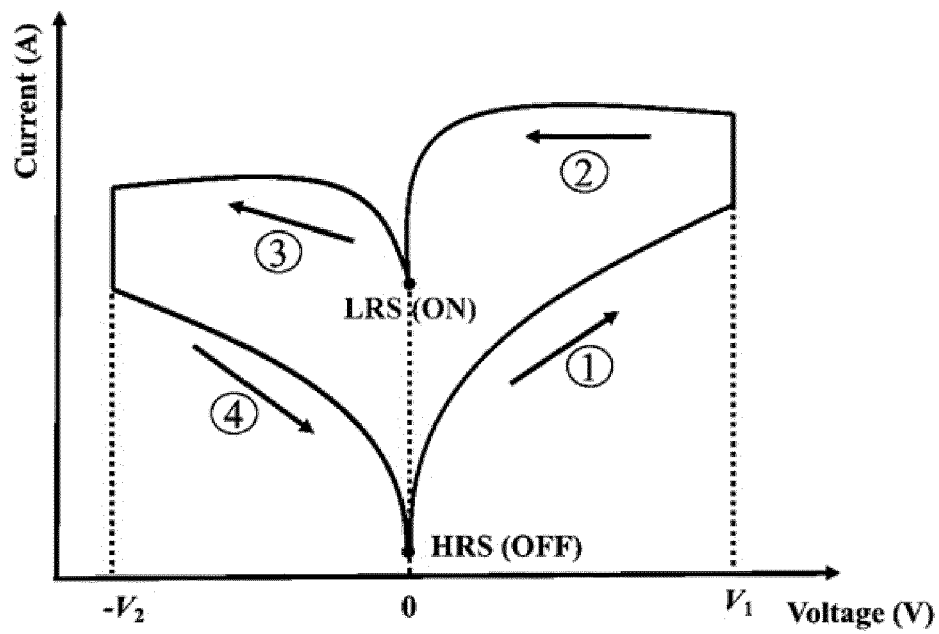


Fig.3A

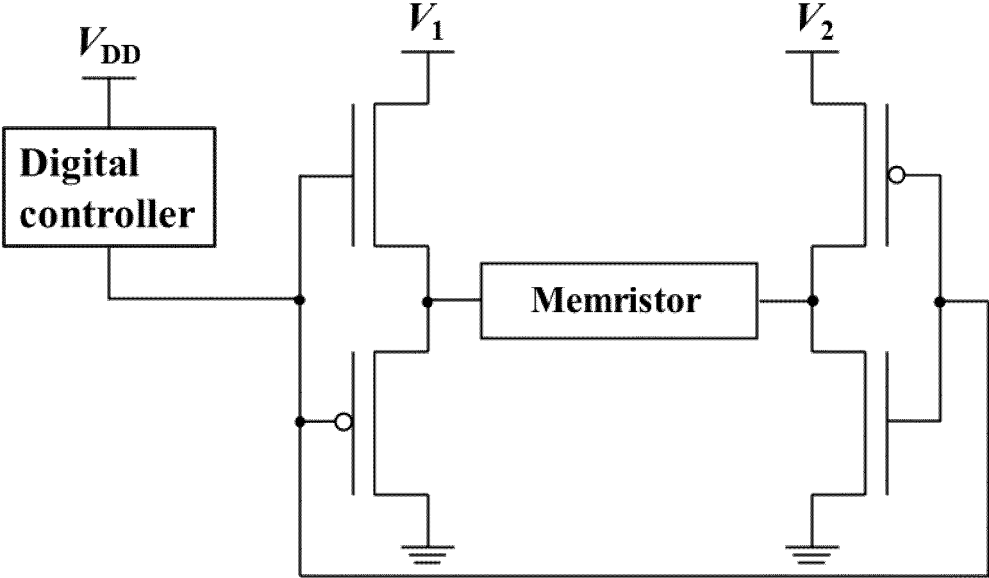


Fig.3B

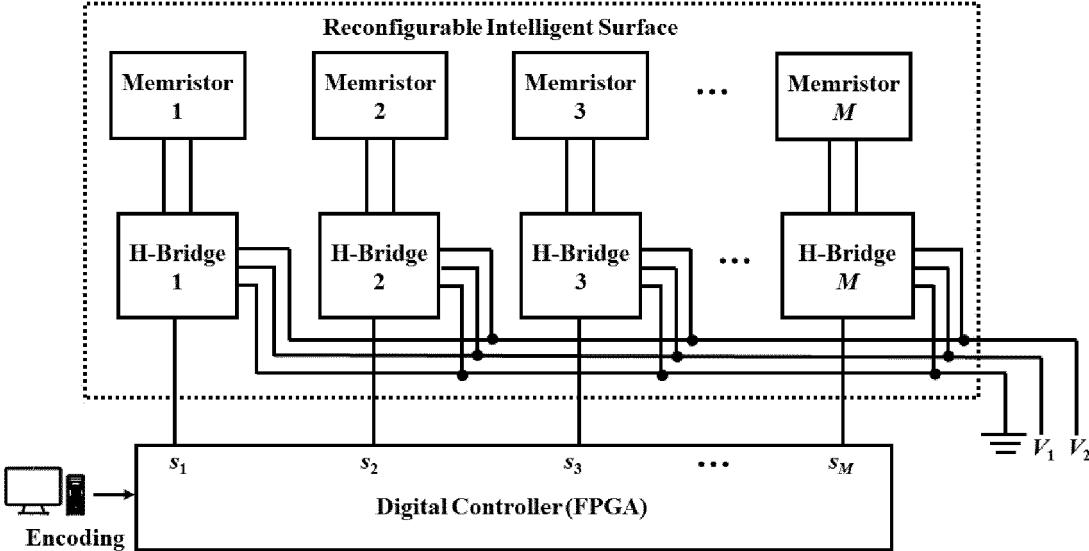


Fig. 4

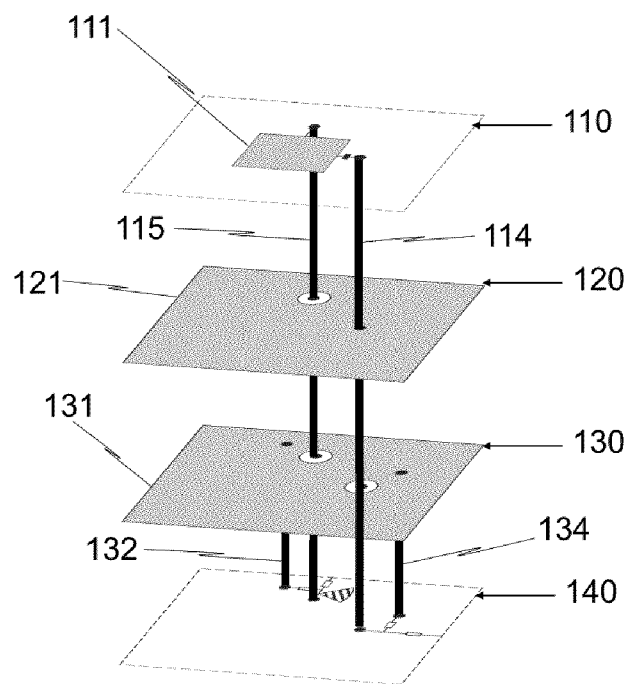


FIG. 5A

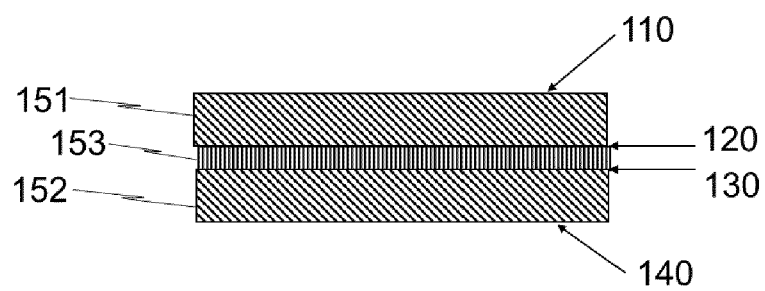


FIG. 5B

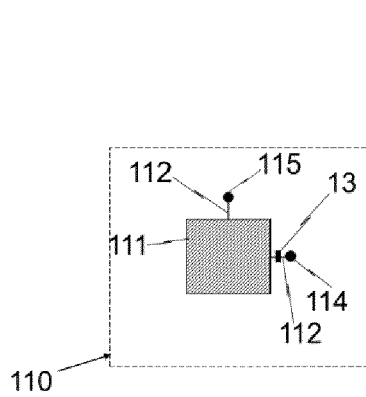


FIG. 5C

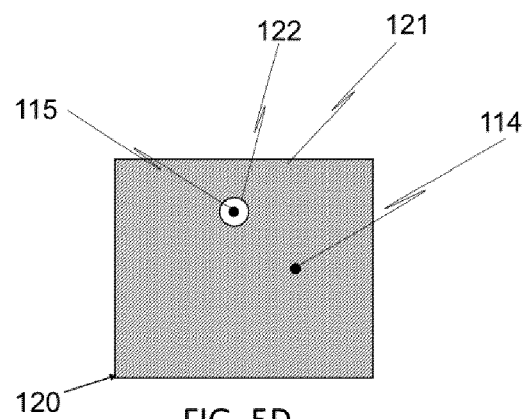


FIG. 5D

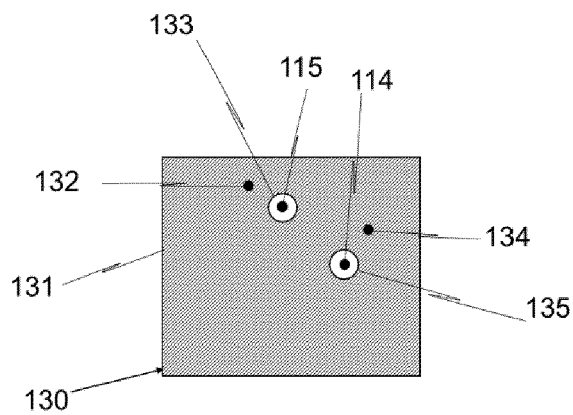


FIG. 5E

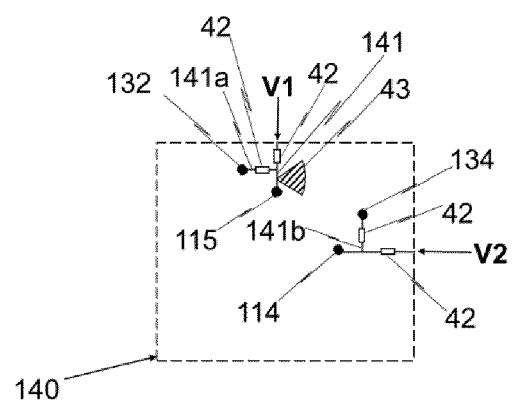


FIG. 5F

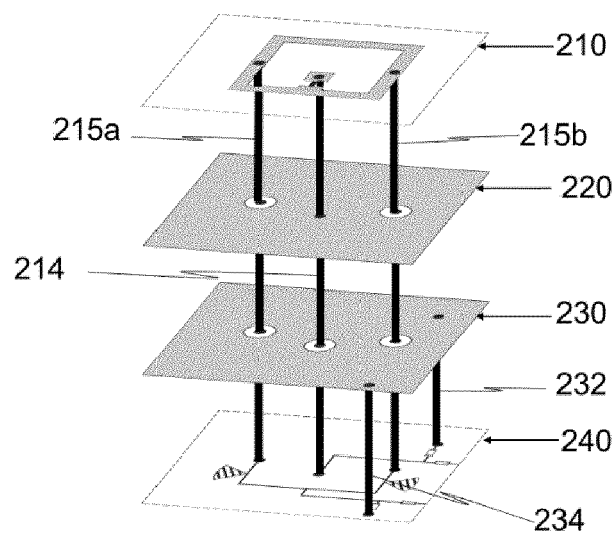


FIG. 6A

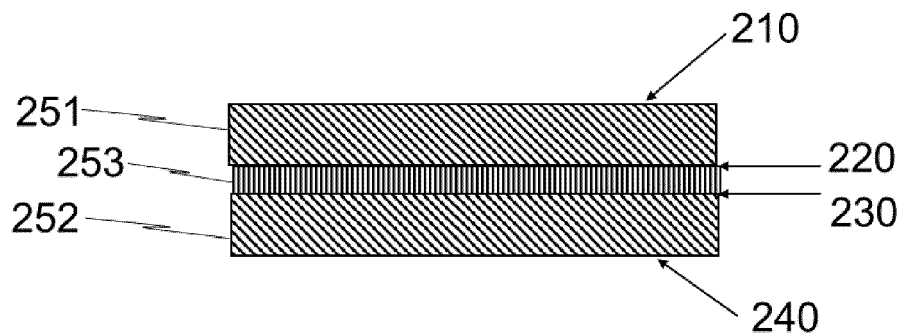


FIG. 6B

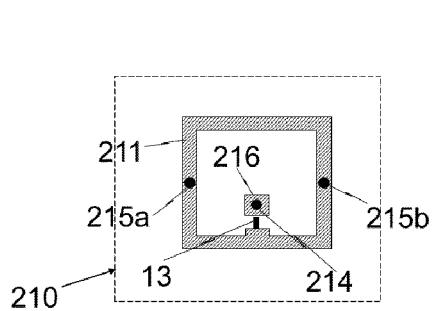


FIG. 6C

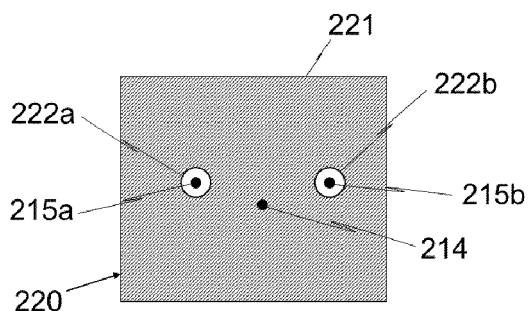


FIG. 6D

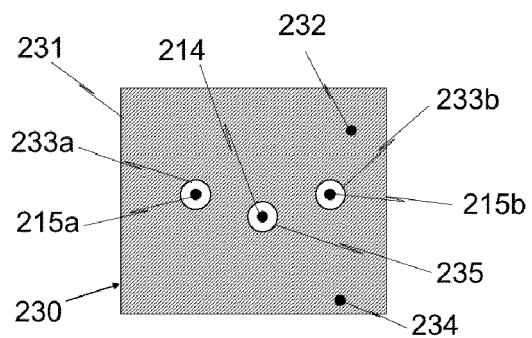


FIG. 6E

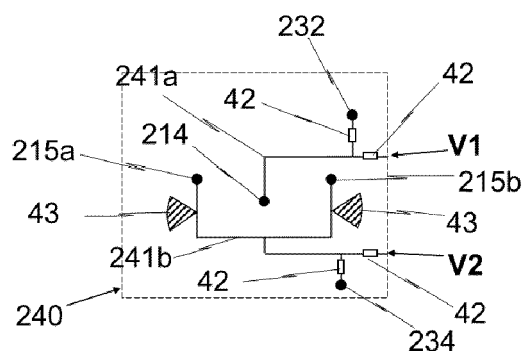


FIG. 6F

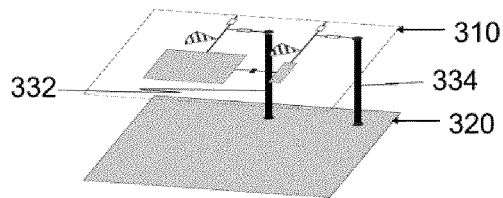


FIG. 7A

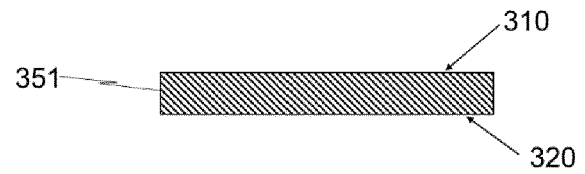


FIG. 7B

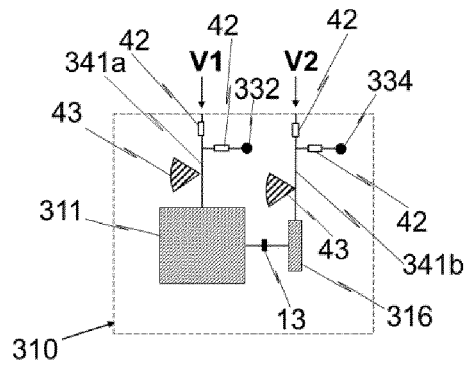


FIG. 7C

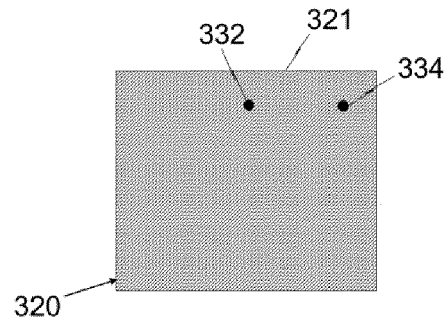


FIG. 7D

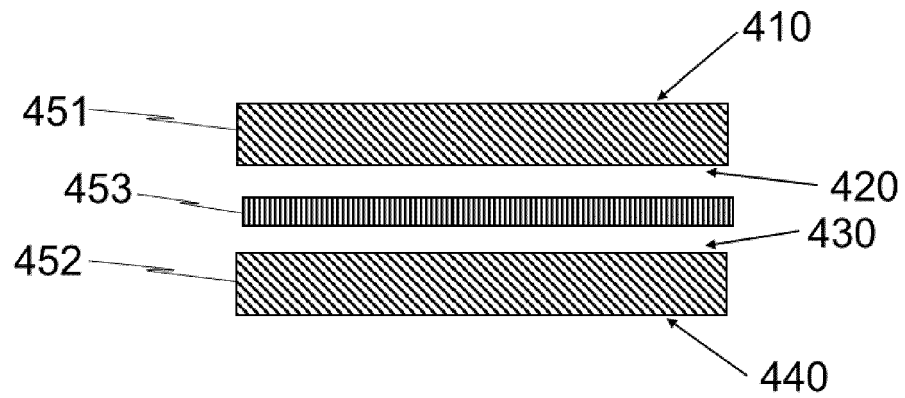


FIG. 8A

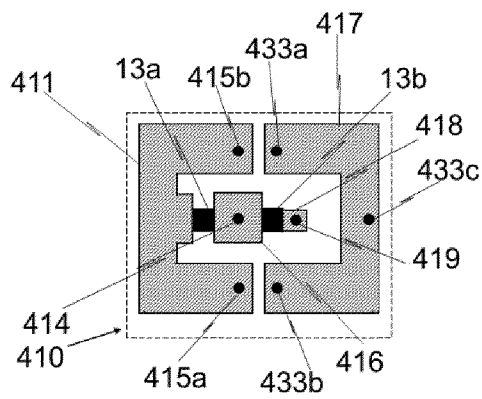


FIG. 8B

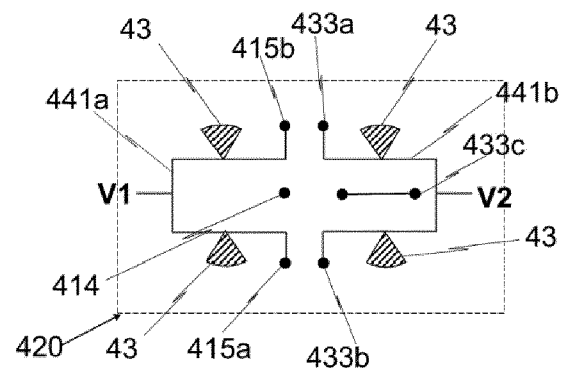


FIG. 8C

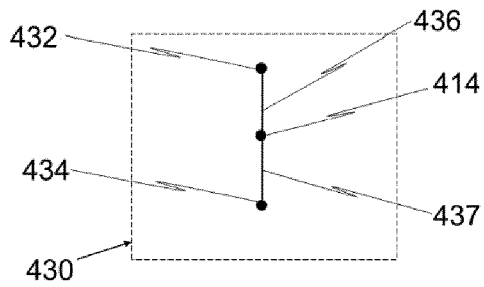


FIG. 8D

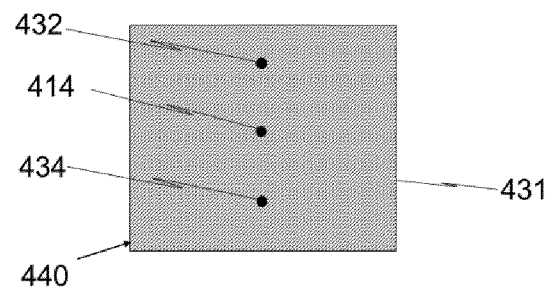


FIG. 8E

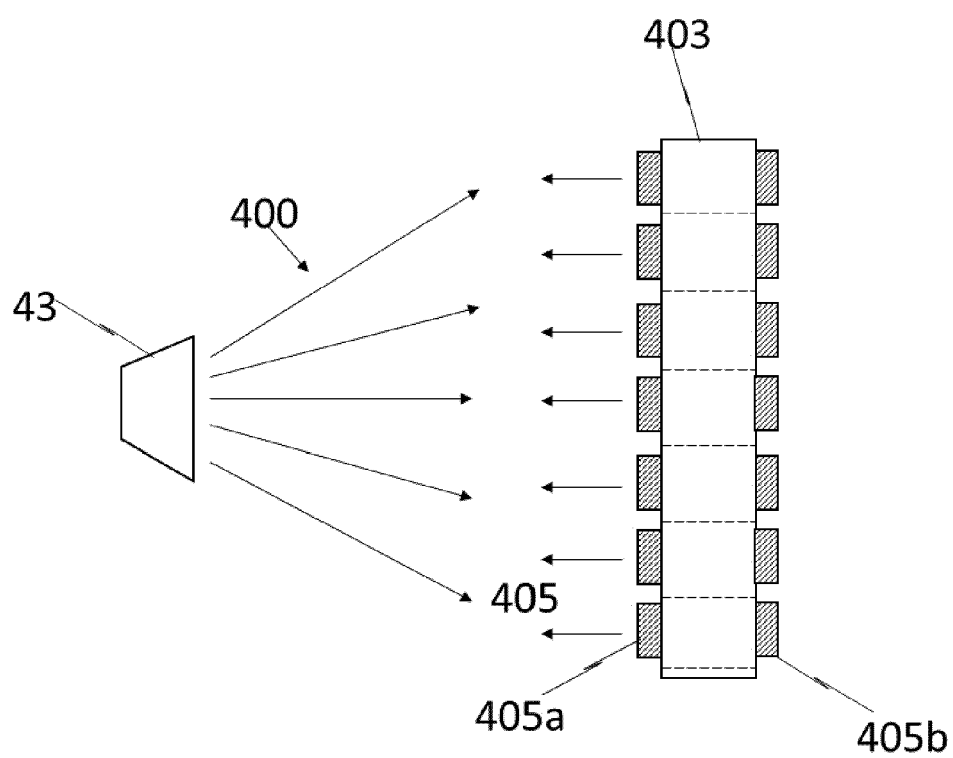


FIG. 8F

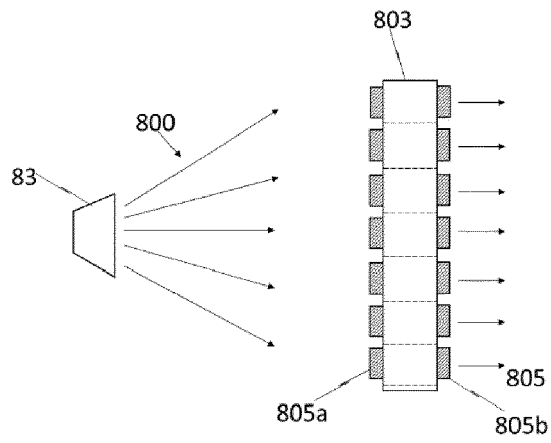


FIG. 9A

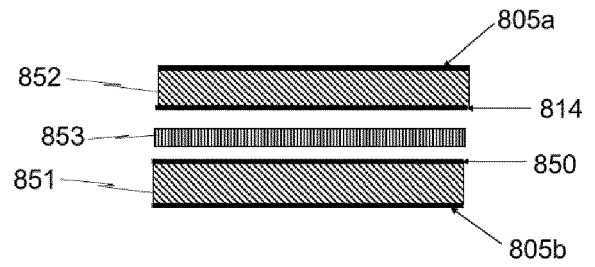


FIG. 9B

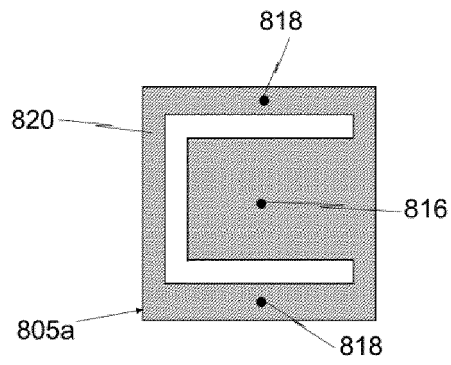


FIG. 9C

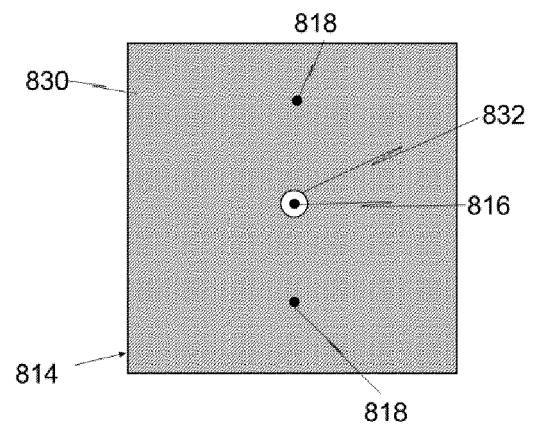


FIG. 9D

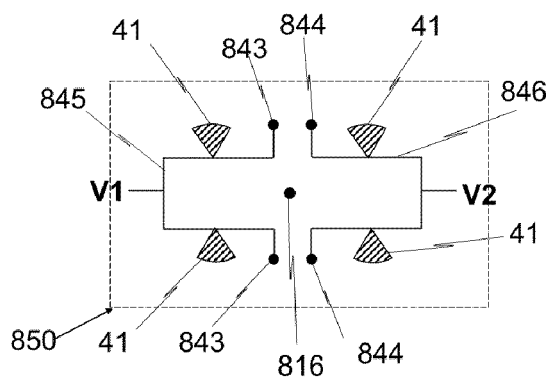


FIG. 9E

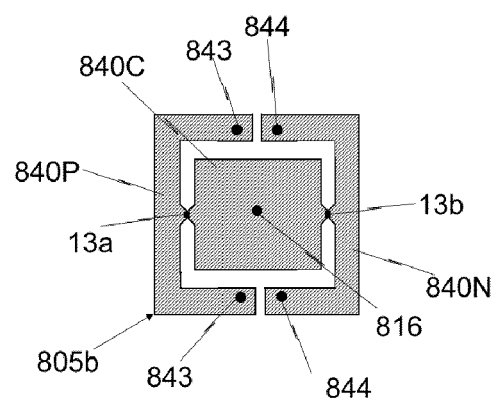


FIG. 9F

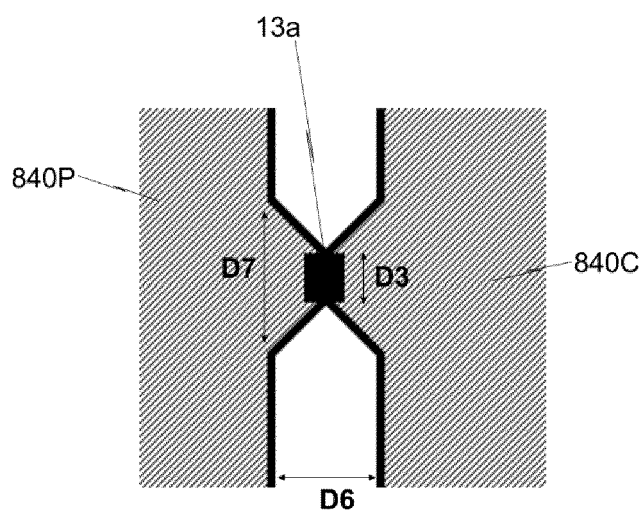


FIG. 9G

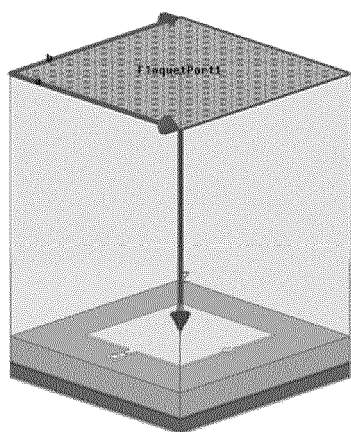


FIG. 10A

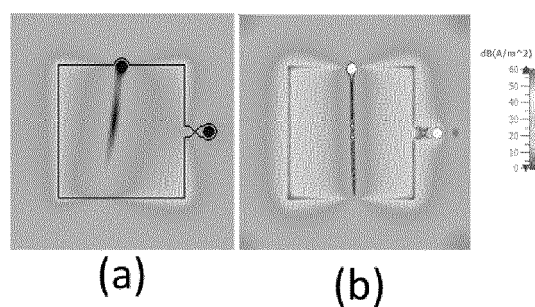


FIG. 10B

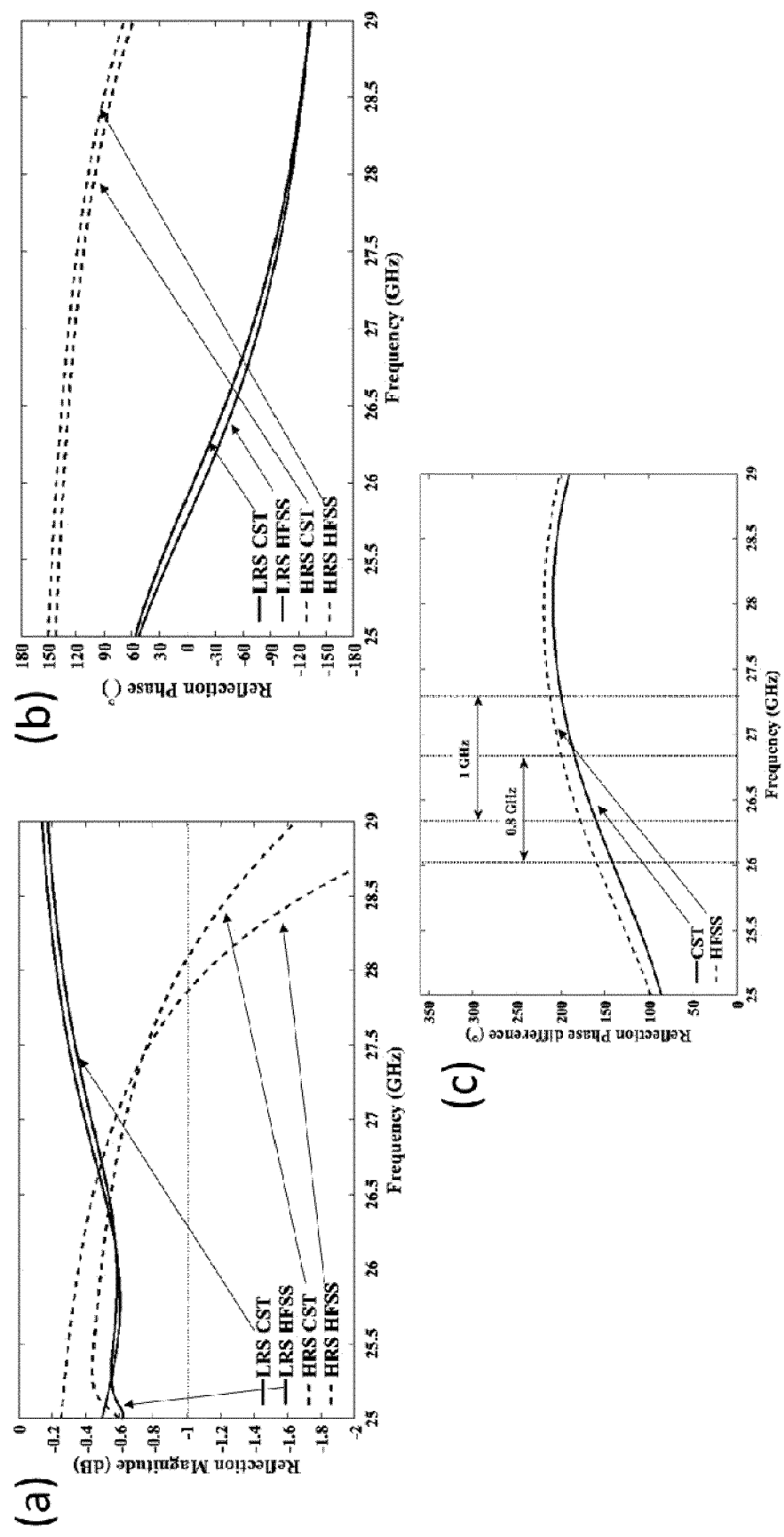


FIG. 11

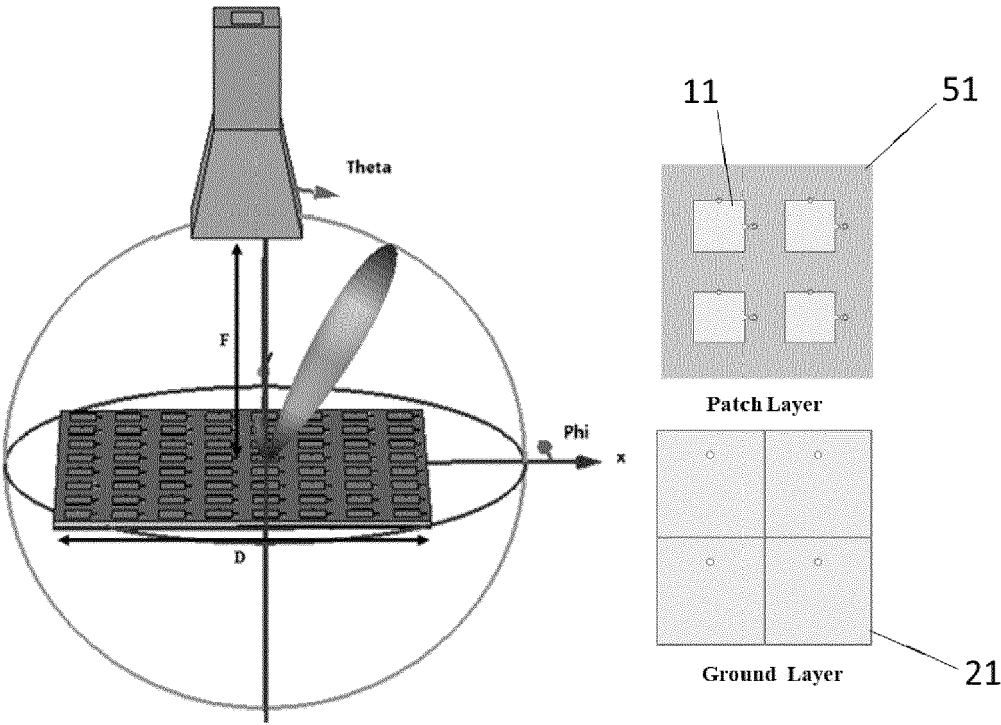


FIG. 12

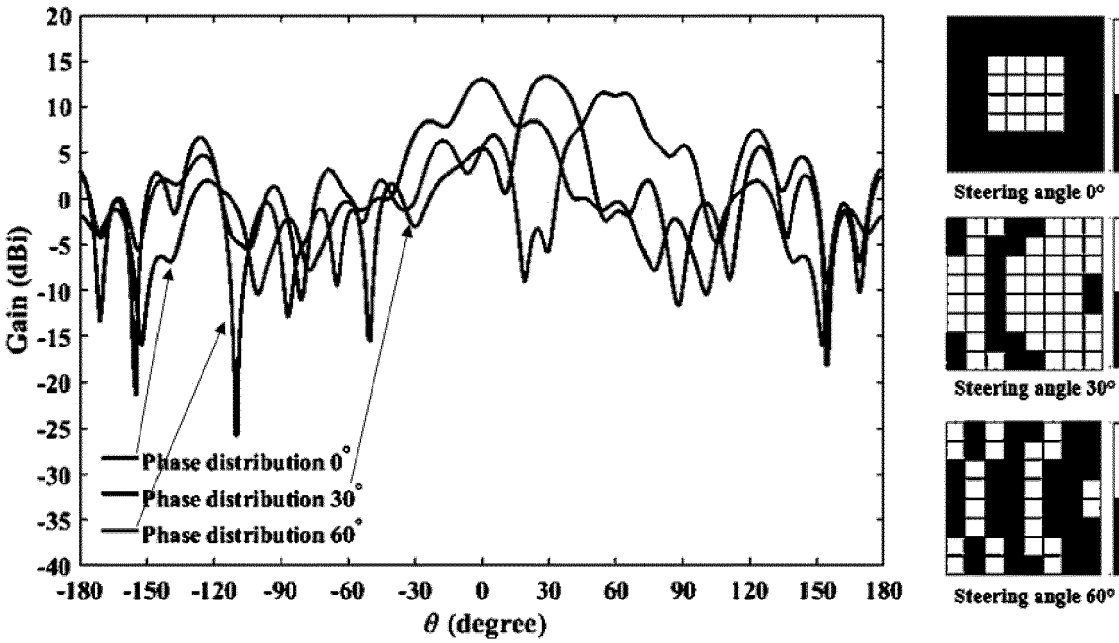


FIG. 13



EUROPEAN SEARCH REPORT

Application Number

EP 24 15 4002

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	WO 2023/207721 A1 (ZTE CORP [CN]) 2 November 2023 (2023-11-02) * figures 2,5,6 *	1-3,5,6, 13-15 7-12	INV. H01Q3/46 H01Q15/14
A	* paragraphs [0027], [0035] * * paragraphs [0039] - [0040] * * paragraphs [0047] - [0048] * * paragraphs [0050] - [0052] *		
X	CN 116 093 630 A (SHAANXI GEXIN GUOWEI SEMICONDUCTOR TECH CO LTD) 9 May 2023 (2023-05-09) * figures 1,2 * * paragraphs [0018] - [0031] *	1,2,4,5, 13-15	
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