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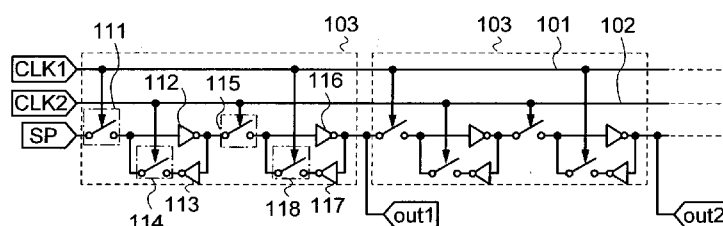
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FIG. 1B



(57) Abstract: An object of the present invention is to provide a driver circuit including a normally-on thin film transistor, which driver circuit ensures a small malfunction and highly reliable operation. The driver circuit includes a static shift register including an inverter circuit having a first transistor and a second transistor, and a switch including a third transistor. The first to third transistors each include a semiconductor layer of an oxide semiconductor and are depletion-mode transistors. An amplitude voltage of clock signals for driving the third transistor is higher than a power supply voltage for driving the inverter circuit.

DESCRIPTION

DRIVER CIRCUIT, DISPLAY DEVICE INCLUDING THE DRIVER CIRCUIT, AND
ELECTRONIC APPLIANCE INCLUDING THE DISPLAY DEVICE

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TECHNICAL FIELD

[0001]

This invention relates to a driver circuit (also referred to as a shift register circuit), a display device including a driver circuit formed over the same substrate as a pixel area, or an electronic appliance including the display device.

10

BACKGROUND ART

[0002]

Along with the widespread use of large display devices such as liquid crystal televisions, higher-value-added products are required and thus development is being carried out. In particular, a technique to form a driver circuit, such as a scan line driver circuit, over the same substrate as a pixel area with the use of a thin film transistor (TFT) having a channel region of an amorphous semiconductor, specifically an oxide semiconductor, is under active development.

15

[0003]

Examples of the structure of the driver circuit include a static shift register circuit which is disclosed in Patent Document 1 (see FIG. 2 and the like).

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[Reference]

[0004]

[Patent Document 1] Japanese Published Patent Application No. S64-89810

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DISCLOSURE OF INVENTION

[0005]

A static shift register circuit includes a thin film transistor which functions as a switch, and an inverter circuit. The use of an oxide semiconductor for a semiconductor layer of transistors serving as the thin film transistor and the inverter circuit offers a substantial merit: good electrical characteristics such as high field-effect mobility. The threshold voltage of an oxide semiconductor, however, fluctuates because of a defect of

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void by lack of oxygen even without the addition of an extrinsic impurity to the oxide semiconductor and thus the thin film transistor having a semiconductor layer of an oxide semiconductor is depletion mode (also referred to as normally on) in some cases.

[0006]

5 In view of this, an object of one embodiment of the present invention is to provide a driver circuit with a small malfunction even when the driver circuit is provided using thin film transistors, all of which are of the same conductivity type and which are normally on because of, for example, their channels including an oxide semiconductor.

10 [0007]

One embodiment of the present invention is a driver circuit including a static shift register including an inverter circuit including a first transistor and a second transistor, and a switch including a third transistor. The first to third transistors each include a semiconductor layer including an oxide semiconductor and are

15 depletion-mode transistors. An amplitude voltage of clock signals for driving the third transistor is higher than a power supply voltage for driving the inverter circuit.

[0008]

One embodiment of the present invention is a driver circuit including a static shift register including an inverter circuit including a first transistor and a second

20 transistor, and a switch including a third transistor; and a demultiplexer circuit connected to an output terminal of the shift register. The first to third transistors each include a semiconductor layer including an oxide semiconductor and are depletion-mode transistors. An amplitude voltage of clock signals for driving the first transistor is higher than a power supply voltage for driving the inverter circuit. Output

25 terminals of the demultiplexer circuit are each connected to a fourth transistor for holding a potential of the output terminal.

[0009]

One embodiment of the present invention can be a driver circuit in which the clock signals are a first clock signal and a second clock signal, and the second clock

30 signal is an inverted signal of the first clock signal.

[0010]

One embodiment of the present invention can be a driver circuit in which an

L/W ratio of the first transistor is higher than an L/W ratio of the second transistor.

[0011]

One embodiment of the present invention can be a driver circuit in which a film thickness of a semiconductor layer of the first transistor is larger than a film thickness of a semiconductor layer of the second transistor.

[0012]

One embodiment of the present invention can be a driver circuit in which an L/W ratio of a fifth transistor in the demultiplexer circuit is lower than an L/W ratio of the fourth transistor.

10 [0013]

One embodiment of the present invention can be a driver circuit in which a gate of the fourth transistor is electrically connected to a line through which a positive power supply voltage is supplied; a first terminal of the fourth transistor is electrically connected to a line through which a negative power supply voltage is supplied; and a second terminal of the fourth transistor is electrically connected to an output terminal of the demultiplexer circuit.

[0014]

One embodiment of the present invention can be a driver circuit in which the first to fourth transistors are n-channel transistors.

20 [0015]

One embodiment of the present invention can provide a driver circuit with a small malfunction even when the driver circuit is provided using thin film transistors, all of which are of the same conductivity type and which are normally on because of, for example, their channels including an oxide semiconductor.

25

BRIEF DESCRIPTION OF DRAWINGS

[0016]

FIGS. 1A and 1B show an example of a driver circuit.

FIGS. 2A and 2B show an inverter circuit, FIG. 2C shows a switch, and FIGS.

30 2D and 2E each show an example of the waveform of signals.

FIG. 3 shows an example of the top view of the inverter circuit.

FIG. 4 shows an example of a driver circuit.

FIG. 5 shows an example of the driver circuit.

FIG. 6 shows an example of the timing chart of the driver circuit.

FIG. 7 shows an example of the top view of an inverter circuit.

FIG. 8 shows an example of the cross-sectional view of the inverter circuit.

5 FIGS. 9A and 9B show an example of a display device.

FIGS. 10A to 10C each show an example of an electronic appliance.

FIG. 11 shows an example of the driver circuit.

FIG. 12 shows an example of the timing chart of the driver circuit.

10 BEST MODE FOR CARRYING OUT THE INVENTION

[0017]

Hereinafter, embodiments of the present invention will be described with reference to the accompanying drawings. However, the present invention can be carried out in many different modes, and it is easily understood by those skilled in the art that modes and details of the present invention can be modified in various ways without departing from the purpose and the scope of the present invention. Therefore, this invention is not interpreted as being limited to the description of the embodiments below. Note that identical portions or portions having the same function in all drawings illustrating the structure of the invention that are described below are denoted by the same reference numerals.

[0018]

Note that the size, the thickness of a layer, or a region of each structure illustrated in drawings or the like of embodiments is exaggerated for simplicity in some cases. Therefore, embodiments of the present invention are not limited to such scales.

25 [0019]

Note that terms such as first, second, third to N th (N is a natural number of two or more) employed in this specification are used in order to avoid confusion between components and do not set a limitation on number.

[0020]

30 (Embodiment 1)

In this embodiment, first, the structure of a driver circuit which is a static shift register circuit including pulse output circuits of a plurality of stages will be described

with reference to drawings. A driver circuit according to this embodiment is formed using a thin film transistor serving as a switch, and an inverter circuit.

[0021]

A driver circuit 100 in this embodiment includes a line 101 through which a first clock signal (CLK1) is supplied, a line 102 through which a second clock signal (CLK2) is supplied, pulse output circuits 103 of a plurality of stages, and a line 104 through which a start pulse (also referred to as SP, a signal from the previous stage, or an input signal) is supplied. In addition, the driver circuit according to this embodiment outputs pulse signals out1 to outN. Note that a structure is also acceptable in which a scan direction switching signal, which shifts a scan direction, or the like is input. In addition, although this embodiment shows an example in which the driver circuit is driven by a two-phase clock signal including a first clock signal (CLK1) and a second clock signal (CLK2), it is also acceptable that the driver circuit is driven by a clock signal other than a two-phase clock signal.

[0022]

If the driver circuit in FIG. 1A is a driver circuit which drives gate lines, a buffer circuit or the like is connected to each output terminal of a pulse output circuit. Alternatively, if the driver circuit in FIG. 1A is a driver circuit which drives signal lines, a sampling switch which samples an image signal, a latch circuit, or the like is connected to each output terminal of a pulse output circuit.

[0023]

Note that an oxide semiconductor is preferably used for the semiconductor layer of each transistor in the driver circuit 100. The use of an oxide semiconductor for the semiconductor layer of a transistor provides higher field-effect mobility than that of a silicon-base semiconductor material such as amorphous silicon. Note that the oxide semiconductor can be zinc oxide (ZnO), tin oxide (SnO₂), or the like. In addition, In or Ga can be added to ZnO.

[0024]

The oxide semiconductor can use a thin film expressed by $\text{InMO}_3(\text{ZnO})_x$ ($x > 0$). Note that M denotes one or more of the metal elements selected from gallium (Ga), iron (Fe), nickel (Ni), manganese (Mn), and cobalt (Co). For example, M denotes Ga in some cases and M denotes the above metal element such as Ni or Fe in addition to Ga

(Ga and Ni or Ga and Fe) in other cases. Moreover, the above oxide semiconductor may contain Fe or Ni, another transitional metal element, or an oxide of the transitional metal as an impurity element in addition to the metal element contained as M. For example, the oxide semiconductor can use an In-Ga-Zn-O-based non-single-crystal film.

[0025]

Instead of the oxide semiconductor layer ($\text{InMO}_3(\text{ZnO})_x$ ($x > 0$) film) which is the In-Ga-Zn-O-based non-single-crystal film, an $\text{InMO}_3(\text{ZnO})_x$ ($x > 0$) film in which M is another metal element can be used. In addition, the oxide semiconductor can use, in addition to the above, any of the following oxide semiconductors: an In-Sn-Zn-O-based oxide semiconductor; an In-Al-Zn-O-based oxide semiconductor; a Sn-Ga-Zn-O-based oxide semiconductor; an Al-Ga-Zn-O-based oxide semiconductor; a Sn-Al-Zn-O-based oxide semiconductor; an In-Zn-O-based oxide semiconductor; a Sn-Zn-O-based oxide semiconductor; an Al-Zn-O-based oxide semiconductor; an In-O-based oxide semiconductor; a Sn-O-based oxide semiconductor; and a Zn-O-based oxide semiconductor.

[0026]

Note that a thin film transistor is an element having at least three terminals: a gate terminal, a drain terminal, and a source terminal, and has a channel region between a drain region and a source region. Current can be fed through the drain region, the channel region, and the source region. In this specification, a terminal connected to a line through which a positive power supply voltage V_{dd} is supplied is a drain terminal, and a terminal connected to a line through which a negative power supply voltage V_{ss} is supplied is a source terminal. Note that a source terminal and a drain terminal are referred to as a first terminal and a second terminal in some cases.

[0027]

Note that the structure of a thin film transistor can employ various modes without being limited to a specific structure. For example, the structure of a thin film transistor can employ a multi-gate structure having two or more gate electrodes.

[0028]

Moreover, the structure of a thin film transistor can employ a structure where

gate electrodes are formed above and below a channel region. Note that the structure where gate electrodes are formed above and below a channel region can lead to a structure where a plurality of thin film transistors is connected in parallel.

[0029]

5 Note that an explicit description "A is connected to B," indicates cases including the case where A is electrically connected to B, the case where A is functionally connected to B, and the case where A is directly connected to B. Here, A and B each denote an object (e.g., a device, an element, a circuit, a line, an electrode, a terminal, a conductive film, or a layer). Therefore, the meaning of such a description
10 is not limited to a predetermined connection relation, e.g. connection relation shown in a drawing or text; the meaning of such a description includes connection relation other than connection relation shown in a drawing or text.

[0030]

Next, the structure of a pulse output circuit 103 will be described with
15 reference to FIG. 1B. A pulse output circuit 103 includes, for example, a first switch 111 connected to a terminal to which the start pulse SP is input, a first inverter circuit 112 which inverts and outputs a signal which is input to the first inverter circuit 112 through the first switch 111, a second inverter circuit 113 which inverts and outputs the signal inverted by the first inverter circuit 112, a second switch 114 connected to a
20 terminal to which the signal inverted by the second inverter circuit 113 is input, a third switch 115 connected a terminal from which the signal inverted by the first inverter circuit 112 is output, a third inverter circuit 116 which inverts and outputs the signal which is input to the third inverter circuit 116 through the third switch 115, a fourth inverter circuit 117 which inverts and outputs the signal inverted by the third inverter
25 circuit 116, and a fourth switch 118 connected to a terminal to which the signal inverted by the fourth inverter circuit 117 is input. In the circuit diagram shown in FIG. 1B, a block indicated by a dotted line corresponds to a pulse output circuit 103 that outputs a pulse signal from single stage. The shift register in FIG. 1A includes pulse output circuits of N -stages (N is a natural number of two or more). The pulse output circuits
30 of N -stages output the output signals out1 to out N through output terminals of their third inverter circuits 116.

[0031]

Note that the first switch 111 and the fourth switch 118 described above are connected to the line 101 so that their on (conducting state) or off (non-conducting state) is controlled by the first clock signal CLK1, and the second switch 114 and the third switch 115 are connected to the line 102 so that their on or off is controlled by the second clock signal CLK2.

[0032]

Next, an example of the circuit configuration of the first to fourth inverter circuits 112 to 117 shown in FIG. 1B will be described with reference to FIGS. 2A to 2E. The inverter circuits are each formed using thin film transistors, all of which are of the same conductivity type as shown in FIGS. 2A and 2B because semiconductor layers of the thin film transistors are made of an oxide semiconductor. An inverter circuit 120 in FIG. 2A includes a first transistor 121 and a second transistor 123. A first terminal (a drain terminal here) of the first transistor 121 is connected to a line 122 through which the positive power supply voltage Vdd is supplied, a second terminal (a source terminal here) of the first transistor 121 is connected to a gate of the first transistor 121, and the second terminal of the first transistor 121 is an output terminal of the inverter circuit 120. A first terminal (a drain terminal here) of the second transistor 123 is connected to the second terminal and a gate of the first transistor 121, a second terminal (a source terminal here) of the second transistor 123 is connected to a line 124 through which the negative power supply voltage Vss is supplied, and a gate of the second transistor 123 is an input terminal of the inverter circuit 120.

[0033]

In addition, an inverter circuit having a different structure from in FIG. 2A is shown in FIG. 2B. An inverter circuit 130 in FIG. 2B includes a first transistor 131 and a second transistor 132. A first terminal (a drain terminal here) of the first transistor 131 is connected to a line 122 through which the positive power supply voltage Vdd is supplied and to a gate of the first transistor 131, and a second terminal (a source terminal here) of the first transistor 131 is an output terminal of the inverter circuit 130. A first terminal (a drain terminal here) of the second transistor 132 is connected to a second terminal of the first transistor 131, a second terminal (a source terminal here) of the second transistor 132 is connected to a line 124 through which the negative power supply voltage Vss is supplied, and a gate of the second transistor 132 is an input

terminal of the inverter circuit 130.

[0034]

Note that a positive power supply voltage is a higher than a reference potential, and a negative power supply voltage is lower than a reference potential. Note that preferably, both a positive power supply voltage and a negative power supply voltage is such that a transistor operates, i.e. a supply of a positive power supply voltage to a gate allows a desired transistor (whose threshold voltage is 0 V) to be turned on, and a supply of a negative power supply voltage to a gate allows a desired transistor to be turned off.

[0035]

Note that a voltage means a potential difference between a potential and a reference potential in many cases. Therefore, a voltage, a potential and a potential difference can be referred to as a potential, a voltage, and a voltage difference, respectively.

[0036]

Next, an example of the circuit configuration of the first to fourth switches 111 to 118 in FIG. 1B will be described. The switches are each formed using a transistor 140 (also referred to as a third transistor) which has a semiconductor layer of an oxide semiconductor, as shown in FIG. 2C. A first terminal (one of a source terminal and drain terminal) of the transistor 140 shown in FIG. 2C which functions as a switch is an input terminal IN of the switch, a second terminal (the other one of the source terminal and drain terminal) of the transistor 140 is an output terminal OUT of the switch, and a gate of the transistor 140 is supplied with the first clock signal CLK1 or the second clock signal CLK2 (FIG. 2C shows the first clock signal CLK1 as an example) from the line 101 or the line 102, which controls on or off of the transistor.

[0037]

Next, a schematic view of the voltage amplitude of the positive power supply voltage Vdd, the negative power supply voltage Vss, and the first clock signal CLK1 which are input to each circuit shown in FIG. 2A to 2C is shown in FIG. 2D. In FIG. 2D, the vertical axis denotes the potential, a wave form 141 denotes the first clock signal CLK1, a wave form 142 denotes the positive power supply voltage Vdd, a wave form 143 denotes the negative power supply voltage Vss, and a wave form 144 denotes

the start pulse SP.

[0038]

FIG. 2E shows the voltage amplitude of the second clock signal CLK2 instead of the voltage amplitude of the first clock signal CLK1. In FIG. 2E, as in FIG. 2D, the vertical axis denotes the potential, a wave form 145 denotes the second clock signal CLK2, the wave form 142 denotes the positive power supply voltage Vdd, the wave form 143 denotes the negative power supply voltage Vss, and the wave form 144 denotes the start pulse SP. Note that the second clock signal CLK2 is an inverted signal of the first clock signal CLK1.

[0039]

The voltage amplitude of the first clock signal CLK1 and the second clock signal CLK2 ranges from a high level signal VH to a low level signal VL as shown in FIG. 2D and 2E. In addition, the potential of the positive power supply voltage Vdd, the potential of the negative power supply voltage Vss, and the voltage amplitude of the start pulse SP ranges from Vss, which is higher than the low level signal VL, to Vdd, which is lower than the high level signal VH.

[0040]

If the first to fourth inverter circuits 112 to 117, which have a semiconductor layer of an oxide semiconductor, have normally-on transistors, flow-through current is increased, which leads to an increase in the power consumption. Therefore, the power consumption can be reduced by setting the amplitude voltage of the positive power supply voltage Vdd, the negative power supply voltage Vss, and the start pulse SP low in advance. In addition, the first to fourth switches 111 to 118 needs to reliably hold an on state or off state in order to prevent malfunction of a driver circuit. The voltage amplitude of the first clock signal CLK and second clock signal CLK2 is thus set higher than that of the power supply voltage of the inverter circuit, allowing the first to fourth switches 111 to 118 to hold an on state or off state more reliably.

[0041]

Note that in the case where the first transistor 121 and the second transistor 123 included in the first to fourth inverter circuits 112 to 117 shown in FIG. 2A are normally on, the power consumption is increased even if the voltage of a power supply voltage supplied to the line 122 and the line 124 is lowered. Thus, when an inverter circuit is

formed using a transistor which has a semiconductor layer of an oxide semiconductor, the resistance of the second transistor 123 is preferably higher than that of the first transistor 121, i.e. the L/W ratio of the second transistor 123 is preferably higher than that of the first transistor 121.

5 [0042]

A top view of the inverter circuit 120 in which the L/W ratio of the second transistor 123 is higher than that of the first transistor 121 is shown in FIG. 3 for specific description. In the inverter circuit 120 shown in FIG. 3, the line 122 through which the positive power supply voltage V_{dd} is supplied, the line 124 through which the negative power supply voltage V_{ss} is supplied, the first transistor 121, the second transistor 123, a gate line 201 of the first transistor 121, a gate line 202 of the second transistor 123, a semiconductor layer 203 of the first transistor 121, a semiconductor layer 204 of the second transistor 123, and a line 205 which is the source terminal of the first transistor 121 and the drain terminal of the second transistor 123 are shown. Connections of the lines is the same as in FIG. 2A. For example, the gate line 201 and the line 205 are connected to each other through a contact hole. Note that the gate line 202 is an input terminal IN of the inverter circuit 120, and the line 205 is an output terminal of the inverter circuit 120.

[0043]

20 Note that the film thickness of the semiconductor layer of the second transistor 123 can be smaller than that of the semiconductor layer of the first transistor 121. This configuration is preferable because it can differentiate the above mentioned resistance. Note that a gate length L is a length of a portion between a source and a drain which portion is in a region where a gate and semiconductor layer of a transistor overlap with each other; and a gate width W is a width of a portion between a source and a drain which portion is in a region where a gate and semiconductor layer of a transistor overlap with each other. Thus, an L/W ratio is a ratio of a gate length to a gate width.

[0044]

30 Note that although in this embodiment an example of the thin film transistor which has a semiconductor layer of an oxide semiconductor is described, the configuration disclosed in this embodiment allows a thin film transistor in a driver circuit to operate even when the thin film transistor is normally on. Therefore, the

configuration can be applied to, for example, a transistor which is normally on because an impurity giving n-type conductivity is intentionally or unintentionally added to its semiconductor layer of amorphous silicon. Moreover, the configuration can be applied to a transistor which is normally-on because of a parasitic channel formed by accumulation of charge that occurs in the opposite side of a semiconductor layer, which forms a channel region, from a gate insulating film (on the back channel side).

[0045]

The configuration of this embodiment can control on or off of a transistor in a driver circuit, all of the transistors of which are of the same conductivity type, even when the transistor is normally on. Therefore, a driver circuit with higher accuracy and a small malfunction can be provided despite the normally-on transistor in the driver circuit.

[0046]

This embodiment can be implemented in appropriate combination with the structures described in the other embodiments.

[0047]

(Embodiment 2)

In this embodiment, in addition to the configuration of the driver circuit described above, the configuration of the driver circuit which has a pulse output circuit whose output terminals are each connected to a demultiplexer circuit will be described with reference to drawings. Adding a component described in this embodiment to a driver circuit including an inverter circuit and a thin film transistor serving as a switch which are the components of the driver circuit according to Embodiment 1, is preferable because it can further reduce the power consumption.

[0048]

A driver circuit 400 according to this embodiment shown in FIG. 4 includes a line 401 through which the first clock signal (CLK1) is supplied, a line 402 through which the second clock signal (CLK2) is supplied, pulse output circuits 403 of a plurality of stages, and a line 404 through which the start pulse (also referred to as SP or input signal) is supplied. The driver circuit according to this embodiment has output terminals, which output pulse signals out1 to outN, each connected to a demultiplexer circuit 405. The demultiplexer circuit 405 generates M (a natural number of two or

more) signals rising at different timings, and outputs pulse signals of $N \times M$ through lines 406 which are the output terminals of the demultiplexer circuit 405.

[0049]

In other words, the number of the stages of the pulse output circuit described in Embodiment 1 can be reduced to N/M . This results in a reduction in the frequency of clock signals for driving the driver circuit. Therefore, significant reduction in power consumption can be achieved even with a normally-on transistor.

[0050]

The demultiplexer circuit 405 is a circuit which generates a plurality of pulse signals each formed of a high-level signal VH and a low-level signal VL passing through the lines 406, by ORing each of the output signals out1 to outN of the static shift register and a control signal of the demultiplexer circuit together. By the demultiplexer circuit 405, the lines are made to be short circuited to a line through which a high-level signal is supplied, short circuited to a line through which a low-level signal is supplied, or electrically floating. This provides a circuit with a small malfunction even if transistors in the demultiplexer circuit 405 are also normally on.

[0051]

The configuration of the demultiplexer circuit will be specifically described with reference to FIG. 5. Note that the demultiplexer circuit 405 shown in FIG. 5 generates a plurality of signals rising at different timings (four signals here) by using single input signal and a plurality of control signals.

[0052]

A specific example of the demultiplexer circuit 405 includes a first transistor 501, a second transistor 502, a third transistor 503, a fourth transistor 504, a fifth transistor 505, a sixth transistor 506, a seventh transistor 507, an eighth transistor 508, a ninth transistor 509, a tenth transistor 510, an eleventh transistor 511, a twelfth transistor 512, a thirteenth transistor 513, a fourteenth transistor 514, a line 515 and a line 517 through which a high-level signal is supplied, and a line 516 and a line 518 through which a low-level signal is supplied. On or off of the third transistor 503 is controlled by the application of a first control signal MUX1 to the gate of the third transistor 503. On or off of the fourth transistor 504 is controlled by the application of a second control signal MUX2 to the gate of the fourth transistor 504. On or off of the

fifth transistor 505 is controlled by the application of a third control signal MUX3 to the gate of the fifth transistor 505. On or off of the sixth transistor 506 is controlled by the application of a fourth control signal MUX4 to the gate of the sixth transistor 506. On or off of the seventh transistor 507 is controlled by the application of a first inversion control signal MUX1B to the gate of the seventh transistor 507. On or off of the eighth transistor 508 is controlled by the application of a second inversion control signal MUX2B to the gate of the eighth transistor 508. On or off of the ninth transistor 509 is controlled by the application of a third inversion control signal MUX3B to the gate of the ninth transistor 509. On or off of the tenth transistor 510 is controlled by the application of a fourth inversion control signal MUX4B to the gate of the tenth transistor 510. A first terminal of the first transistor 501 is connected to the line 515, and a gate of the first transistor 501 is connected to an output terminal of the driver circuit 400. A first terminal of the second transistor 502 is connected to the line 516, and a gate of the second transistor 502 is connected to an output terminal of the driver circuit 400 as the first transistor 501. A first terminal of the third transistor 503 is connected to the second terminal of the first transistor 501, and a second terminal of the third transistor 503 is connected to a line G1. A first terminal of the fourth transistor 504 is connected to the second terminal of the first transistor 501, and a second terminal of the fourth transistor 504 is connected to a line G2. A first terminal of the fifth transistor 505 is connected to the second terminal of the first transistor 501, and a second terminal of the fifth transistor 505 is connected to a line G3. A first terminal of the sixth transistor 506 is connected to the second terminal of the first transistor 501, and a second terminal of the sixth transistor 506 is connected to a line G4. A first terminal of the seventh transistor 507 is connected to the second terminal of the second transistor 502, and a second terminal of the seventh transistor 507 is connected to the line G1. A first terminal of the eighth transistor 508 is connected to the second terminal of the second transistor 502, and a second terminal of the eighth transistor 508 is connected to the line G2. A first terminal of the ninth transistor 509 is connected to the second terminal of the second transistor 502, and a second terminal of the ninth transistor 509 is connected to the line G3. A first terminal of the tenth transistor 510 is connected to the second terminal of the second transistor 502, and a second terminal of the tenth transistor 510 is connected to the line G4. A first terminal of the eleventh

transistor 511 is connected to the line G1, a gate of the eleventh transistor 511 is connected to a line 517, and a second terminal of the eleventh transistor 511 is connected to a line 518. A first terminal of the twelfth transistor 512 is connected to the line G2, a gate of the twelfth transistor 512 is connected to the line 517, and a
5 second terminal of the twelfth transistor 512 is connected to the line 518. A first terminal of the thirteenth transistor 513 is connected to the line G3, a gate of the thirteenth transistor 513 is connected to the line 517, and a second terminal of the thirteenth transistor 513 is connected to the line 518. A first terminal of the fourteenth transistor 514 is connected to the line G4, a gate of the fourteenth transistor 514 is
10 connected to the line 517, and a second terminal of the fourteenth transistor 514 is connected to the line 518.

[0053]

Note that in the demultiplexer circuit 405 shown in FIG. 5, the first to tenth transistors 501 to 510 are designed to have lower L/W ratio than the eleventh to
15 fourteenth transistors 511 to 514. In other words, the first to tenth transistors 501 to 510 are designed to have higher current supply capability than the eleventh to fourteenth transistors 511 to 514.

[0054]

Specifically, in the case where a demultiplexer circuit is configured using
20 transistors which have a semiconductor layer of an oxide semiconductor, the eleventh to fourteenth transistors 511 to 514 are preferably designed to have higher capacitance than the first to tenth transistors 501 to 510. In other words, the eleventh to fourteenth transistors 511 to 514 are preferably designed to have higher L/W ratio than the first to tenth transistors 501 to 510. Note that the eleventh to fourteenth transistors 511 to 514
25 can have a semiconductor layer, a thickness of which is smaller than that of the first to tenth transistors 501 to 510. This configuration is preferable because it can differentiate the above mentioned capacitance.

[0055]

In FIG. 5, when the lines G1 to G4 have the high-level signal VH given by the
30 first to tenth transistors 501 to 510, the lines G1 to G4 have the high-level signal VH since the first to tenth transistors 501 to 510 have higher current supply capability than the eleventh to fourteenth transistors 511 to 514. Further, in a period where the lines

G1 to G4 are floating, the high-level signal VH is supplied to the gate of the eleventh to fourteenth transistors 511 to 514, whereby the eleventh to fourteenth transistors 511 to 514 can make the lines G1 to G4 maintain the low-level signal VL. In other words, the eleventh to fourteenth transistors 511 to 514 have a function of holding the potential of the low-level signal except when the lines G1 to G4 have the potential of the high-level signal VH. Note that the eleventh to fourteenth transistors 511 to 514 are each called a fourth transistor in some cases, according to the first transistor and the second transistor which are included in an inverter circuit of the driver circuit 400, and the third transistor which is a switch of the driver circuit 400. In addition, the first to tenth transistors 501 to 510 are each called a fifth transistor in some cases, according to the first transistor and the second transistor which are included in an inverter circuit of the driver circuit 400, the third transistor which is a switch of the driver circuit 400, and the fourth transistor.

[0056]

As described above, if the transistors included in the demultiplexer circuit 405 are also normally on, it is possible that the potential of the low-level signal VL may be not held because of a leakage current or the like which occurs in a period where the lines are floating. The circuit configuration shown in FIG. 5 allows the potential of the low-level signal VL to be held even when a leakage current occurs in the lines G1 to G4, whereby a malfunction can be small.

[0057]

Next, the operation shown in FIG. 5 will be described with reference to a timing chart in FIG. 6. Signals shown in FIG. 6 are the first clock signal CLK1 and the second clock signal CLK2 which are supplied to the driver circuit 400; the output signal out1, the output signal out2, the output signal out3, and the output signal out4 which are output from the driver circuit 400; the first control signal MUX1, the second control signal MUX2, the third control signal MUX3, the fourth control signal MUX4, the first inversion control signal MUX1B, the second inversion control signal MUX2B, the third inversion control signal MUX3B, the fourth inversion control signal MUX4B, which are shown in FIG. 5; and output signals GOUT1, GOUT2, and GOUT3 which are output from the demultiplexer circuit 405.

[0058]

The output signals out1 to out4 are sequentially output as pulse signals in response to the first clock signal CLK1 and the second clock signal CLK2 as shown in FIG. 6. The pulse signal of out1 is ORed with the first control signal MUX1, the second control signal MUX2, the third control signal MUX3, or the fourth control signal MUX4, so that the signals GOUT1, GOUT2, and GOUT3 are output through the lines G1 to G3. Note that the first inversion control signal MUX1B, the second inversion control signal MUX2B, the third inversion control signal MUX3B, and the fourth inversion control signal MUX4B are in opposite phase to the first control signal MUX1, the second control signal MUX2, the third control signal MUX3, and the fourth control signal MUX4, respectively.

[0059]

In addition, even if an inversion output signal out1B which is an inverted signal of the output signal out1 is used instead of the first inversion control signal MUX1B, the second inversion control signal MUX2B, the third inversion control signal MUX3B, and the fourth inversion control signal MUX4B, the similar output signal can be output through the lines G1 to G4. FIG. 11 shows a circuit configuration as a specific example. Note that a demultiplexer circuit 450 shown in FIG. 11 generates a plurality of signals arising at different timings (four signals here) by using single input signal and a plurality of control signals as in FIG. 5.

[0060]

Specifically, the demultiplexer circuit 450 includes a line 459 through which the low-level signal VL is supplied to a first transistor 451, a second transistor 452, a third transistor 453, a fourth transistor 454, a fifth transistor 455, a sixth transistor 456, a seventh transistor 457, an eighth transistor 458; and an inverter circuit 460 which outputs the inversion output signal OUT1B, for example. Further, the demultiplexer circuit 450 includes a line 461 through which the first control signal MUX1 is supplied, a line 462 through which the second control signal MUX2 is supplied, a line 463 through which the third control signal MUX3 is supplied, and a line 464 through which the fourth control signal MUX4 is supplied. A first terminal of the first transistor 451 is connected to the line 461, a gate of the first transistor 451 is connected to an output terminal of the driver circuit 400, and a second terminal of the first transistor 451 is connected to the line G1. A first terminal of the second transistor 452 is connected to

the line 462, a gate of the second transistor 452 is connected to the output terminal of the driver circuit 400, and a second terminal of the second transistor 452 is connected to the line G2. A first terminal of the third transistor 453 is connected to the line 463, a gate of the third transistor 453 is connected to the output terminal of the driver circuit 400, and a second terminal of the third transistor 453 is connected to the line G3. A first terminal of the fourth transistor 454 is connected to the line 464, a gate of the fourth transistor 454 is connected to the output terminal of the driver circuit 400, and a second terminal of the fourth transistor 454 is connected to the line G4. Further, an input terminal of the inverter circuit 460 is connected to the output terminal of the driver circuit 400. Further, a first terminal of the fifth transistor 455 is connected to the line 459, a gate of the fifth transistor 455 is connected to an output terminal of the inverter circuit 460, and a second terminal of the fifth transistor 455 is connected to the line G1. A first terminal of the sixth transistor 456 is connected to the line 459, a gate of the sixth transistor 456 is connected to an output terminal of the inverter circuit 460, and a second terminal of the sixth transistor 456 is connected to the line G2. A first terminal of the seventh transistor 457 is connected to the line 459, a gate of the seventh transistor 457 is connected to an output terminal of the inverter circuit 460, and a second terminal of the seventh transistor 457 is connected to the line G3. A first terminal of the eighth transistor 458 is connected to the line 459, a gate of the eighth transistor 458 is connected to an output terminal of the inverter circuit 460, and a second terminal of the eighth transistor 458 is connected to the line G4.

[0061]

A timing chart of the signals shown in FIG. 11 is shown in FIG. 12 according to FIG. 6. FIG. 12 shows that the same output signals as those in FIG. 6 can be obtained.

[0062]

Note that in the demultiplexer circuit 450 shown in FIG. 11, the first to fourth transistors 451 to 454 are designed to have lower L/W ratio than the fifth to eighth transistors 455 to 458. In other words, the first to fourth transistors 451 to 454 are designed to have higher current supply capability than the fifth to eighth transistors 455 to 458.

[0063]

Specifically, in the case where a demultiplexer circuit is configured using

transistors which have a semiconductor layer of an oxide semiconductor, the fifth to eighth transistors 455 to 458 are preferably designed to have higher capacitance than the first to fourth transistors 451 to 454. In other words, the fifth to eighth transistors 455 to 458 are preferably designed to have higher L/W ratio than the first to fourth transistors 451 to 454. Note that the fifth to eighth transistors 455 to 458 can have a semiconductor layer, a thickness of which is smaller than that of the first to fourth transistors 451 to 454. This configuration is preferable because it can differentiate the above mentioned capacitance. Note that the fifth to eighth transistors 455 to 458 are each called a fourth transistor in some cases, according to the first transistor and the second transistor which are included in an inverter circuit of the driver circuit 400, and the third transistor which is a switch of the driver circuit 400. In addition, the first to fourth transistors 451 to 454 are each called a fifth transistor in some cases, according to the first transistor and the second transistor which are included in an inverter circuit of the driver circuit 400, the third transistor which is a switch of the driver circuit 400, and the fourth transistor.

[0064]

The number of input signals is reduced by applying the inversion output signal out1B to the demultiplexer circuit 405. Further, space savings can be achieved by a reduction in the area for routing wiring, which reduction is accompanied by a reduction in the number of signals, thereby downsizing the driver circuit and reducing the power consumption.

[0065]

The configuration according to this embodiment can control on or off of a transistor in a driver circuit, all of the transistors of which are of the same conductivity type, even when the transistor is normally on. Therefore, a driver circuit with higher accuracy and a small malfunction can be provided despite a normally-on transistor in the driver circuit.

[0066]

This embodiment can be implemented in appropriate combination with the structures described in the other embodiments.

[0067]

(Embodiment 3)

In this embodiment, the manufacturing process of the driver circuit described in the above embodiments, specifically a top view and cross-sectional view of the thin film transistor which has a semiconductor layer of an oxide semiconductor will be described. Note that a display device including a driver circuit in this embodiment can be applied to a liquid crystal display device and a display device including a light-emitting element such as an organic EL. The driver circuit described in the above embodiments can be applied to a driver circuit of an electronic paper including an electrophoresis element. Note that the driver circuit described in the above embodiments can be applied to not only a driver circuit of a display device but other devices such as a driver circuit for a photosensor.

[0068]

FIG. 7 is a top view of the inverter circuit 120 including the first transistor 121 and the second transistor 123 described in Embodiment 1 with reference to FIG. 3. FIG. 8 is a cross-sectional view of the first transistor 121 and the second transistor 123. In addition, the cross-sectional view of the first transistor 121 and the second transistor 123 corresponds to sections A-A', B-B', and C-C' in the top view of the inverter circuit 120 shown in FIG. 7. Note that in this embodiment, an example of the method of forming a thin film transistor which has a semiconductor layer of an oxide semiconductor, in particular, will be described.

[0069]

First, a base film 902 is deposited on a substrate 901. Next, a conductive film is formed over the base film 902, and then gate electrode layers 903A and 903B are formed by a photolithography process.

[0070]

Note that a resist mask can be formed by an inkjet method. A photomask is not used when the resist mask is formed by an inkjet method, which results in reducing manufacturing cost.

[0071]

Examples of the material for the conductive film used for the gate electrode layers 903A and 903B include an element selected from Al, Cr, Ta, Ti, Mo, and W, an alloy containing any of these elements as its component, and an alloy film containing any of these elements in combination.

[0072]

In the case where a glass substrate is used as the substrate 901, a glass substrate having a strain point of 730 °C or higher is preferably used if the temperature of heat treatment performed later is high. For the glass substrate, a glass material such as
5 aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example.

[0073]

The base film 902 has a function of preventing diffusion of an impurity element from the substrate 901, and can be formed to have a single-layer or multilayer
10 structure of one or more of a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0074]

Next, a gate insulating layer 904 is formed over the gate electrode layers 903A and 903B.

15 [0075]

The gate insulating layer 904 can be formed using a single-layer or multilayer structure of any of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, and a silicon nitride oxide layer by plasma CVD, sputtering, or the like. For example, a silicon oxynitride layer can be formed using a deposition gas containing SiH₄, oxygen,
20 and nitrogen by plasma CVD.

[0076]

Next, the gate insulating layer 904 is selectively etched by a photolithography process, so that a contact hole reaching the gate electrode layer 903B is formed.

[0077]

25 Next, an oxide semiconductor film is formed over the gate insulating layer 904. The preferable thickness is 50 nm or less, so that the oxide semiconductor film can have an amorphous structure even when heat treatment for dehydration or dehydrogenation is performed after formation of the oxide semiconductor film.

[0078]

30 Any of the following is used as the oxide semiconductor film: an In-Ga-Zn-O-based non-single-crystal film, an In-Sn-Zn-O-based oxide semiconductor

film, an In-Al-Zn-O-based oxide semiconductor film, a Sn-Ga-Zn-O-based oxide semiconductor film, an Al-Ga-Zn-O-based oxide semiconductor film, a Sn-Al-Zn-O-based oxide semiconductor film, an In-Zn-O-based oxide semiconductor film, a Sn-Zn-O-based oxide semiconductor film, an Al-Zn-O-based oxide semiconductor film, an In-O-based oxide semiconductor film, an Sn-O-based oxide semiconductor film, and a Zn-O-based oxide semiconductor film. The oxide semiconductor film can be formed by sputtering in a rare gas (typically argon) atmosphere, an oxygen atmosphere, or an atmosphere of a rare gas (typically argon) and oxygen.

10 [0079]

Here, deposition is performed using an oxide semiconductor target containing In, Ga, and Zn ($\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3:\text{ZnO} = 1:1:1$ [mol%], $\text{In}:\text{Ga}:\text{Zn} = 1:1:0.5$ [at%]) under the condition where the distance between the substrate and the target is 100 mm, the pressure is 0.6 Pa, the direct current (DC) power source is 0.5 kW, and the atmosphere is an oxygen atmosphere (of an oxygen flow rate of 100 %). Note that a pulse direct current (DC) power source is preferable because it reduces dust and makes the film thickness uniform.

[0080]

Examples of sputtering include RF sputtering in which a high-frequency power source is used as a sputtering power source, DC sputtering, and pulsed DC sputtering in which a bias is applied in a pulsed manner. RF sputtering is mainly used in the case of forming an insulating film, and DC sputtering is mainly used in the case of forming a metal conductive film.

[0081]

25 In addition, there is also a multi-source sputtering apparatus in which a plurality of targets of different materials can be set. The multi-source sputtering apparatus allows a multilayer film of different materials to be deposited in the same chamber, or allows plural kinds of materials to be deposited by electric discharge at the same time in the same chamber.

30 [0082]

In addition, there are a sputtering apparatus provided with a magnet system

inside the chamber and used for a magnetron sputtering, and a sputtering apparatus used for an ECR sputtering in which plasma generated with the use of microwaves is used without using glow discharge.

[0083]

5 Furthermore, as a deposition method by sputtering, there are also a reactive sputtering method in which a target substance and a sputtering gas component are chemically reacted with each other during deposition to form a thin compound film thereof, and a bias sputtering in which a voltage is also applied to a substrate during deposition.

10 [0084]

Note that before the oxide semiconductor film is formed by sputtering, dust on a surface of the gate insulating layer 904 is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. The reverse sputtering refers to a method in which, without application of a voltage to a target side, an RF
15 power source is used for application of voltage to a substrate side in an argon atmosphere and plasma is generated in the vicinity of the substrate to modify a surface. Note that instead of an argon atmosphere, nitrogen, helium, oxygen, or the like may be used.

[0085]

20 Next, the oxide semiconductor film is processed into island-shape oxide semiconductor layers 905A and 905B by a photolithography process. In addition, the resist mask for forming the island-shaped oxide semiconductor layers 905A and 905B may be formed by an inkjet method.

[0086]

25 Next, the oxide semiconductor layer is subjected to dehydration or dehydrogenation. The temperature of heat treatment for dehydration or dehydrogenation is greater than or equal to 400 °C and less than or equal to 750 °C, preferably greater than or equal to 425 °C and less than or equal to the strain point of the substrate. Note that in the case of the temperature that is 425 °C or higher, the heat
30 treatment time may be one hour or shorter, whereas in the case of the temperature lower than 425 °C, the heat treatment time is longer than one hour. Here, the substrate is

introduced into an electric furnace which is one of heat treatment apparatuses, and the heat treatment of the oxide semiconductor layer is performed in a nitrogen atmosphere. After that, the oxide semiconductor layer is not exposed to air, which prevents the oxide semiconductor layer from including water or hydrogen again; thus, an oxide semiconductor layer is obtained. In this embodiment, one furnace used in the heat treatment is continuously used up to the time when the temperature is lowered from the heat temperature T at which dehydration or dehydrogenation of the oxide semiconductor layer is performed to the temperature enough to prevent reincorporation of water. Specifically, slow cooling is performed in a nitrogen atmosphere up to the time when the temperature becomes less than the heat temperature T by 100 °C or more. The atmosphere in which dehydration or dehydrogenation is performed is not limited to a nitrogen atmosphere; dehydration or dehydrogenation is performed in a rare gas atmosphere (helium, neon, argon, or the like). The degree of crystallinity of an oxide semiconductor becomes 90 % or higher or 80 % or higher in some heat conditions.

[0087]

The heat treatment apparatus is not limited to an electric furnace and can be provided with a device that heats an object by thermal conduction or thermal radiation from a heater such as a resistance heater or the like. For example, an RTA (rapid thermal annealing) apparatus such as a GRTA (gas rapid thermal annealing) apparatus or an LRTA (lamp rapid thermal annealing) apparatus can be used. An LRTA apparatus is an apparatus for heating an object by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with a process object by heat treatment, such as nitrogen or a rare gas such as argon is used.

[0088]

Next, a conductive film is formed over the gate insulating layer 904 and the oxide semiconductor layers 905A and 905B. After that, a resist mask is formed through a photolithography process and then, the conductive film is selectively etched to form an electrode layer 906. As a material of the conductive film, an element

selected from Ti, Mo, W, Al, Cr, Cu, and Ta, an alloy containing any of these elements as a component, an alloy containing these elements in combination, or the like is used. The conductive film is not limited to a single-layer film containing the above element and can be a multi-layer film of two or more layers. Note that in FIG. 8, only the
5 conductive film on and in contact with the oxide semiconductor layer is selectively removed. Therefore, when an ammonia peroxide mixture (hydrogen peroxide : ammonia : water = 5:2:2) or the like as an alkaline etchant is used in order to selectively remove only the conductive layer, which is on and in contact with the oxide semiconductor layer, the conductive film can be selectively removed so that the oxide
10 semiconductor layer containing an In-Ga-Zn-O-based oxide semiconductor can be left.

[0089]

Next, an insulating layer 907 is formed over the gate insulating layer 904, the oxide semiconductor layers 905A and 905B, and the electrode layer 906. The insulating layer 907 can be formed to a thickness of at least 1 nm or more using a
15 method by which an impurity such as water and hydrogen is not included in the oxide insulating film, such as sputtering, as appropriate. As the insulating layer 907 which is formed so as to be in contact with the oxide semiconductor layers 905A and 905B, an inorganic insulating film which does not include an impurity such as moisture, a hydrogen ion, and OH⁻ and blocks entry of these from the outside is used. Specifically,
20 a silicon oxide film, a silicon nitride oxide film, an aluminum oxide film, or an aluminum oxynitride film is used.

[0090]

Through the above process, the first transistor 121 and the second transistor 123 can be formed.

25 [0091]

Note that the first transistor 121 and the second transistor 123 shown in FIG. 8 are bottom-gate TFTs which have a semiconductor layer of an oxide semiconductor. An embodiment of the present invention is, however, not limited to this; the first transistor 121 and the second transistor 123 can be top-gate TFTs.

30 [0092]

The configuration according to this embodiment can control on or off of a transistor in a driver circuit even if the transistor is normally on. Therefore, a driver

circuit with higher accuracy and a small malfunction can be provided despite a normally-on transistor in the driver circuit.

[0093]

5 This embodiment can be implemented in appropriate combination with the structures described in the other embodiments.

[0094]

(Embodiment 4)

10 In this embodiment, an example will be described below in which at least a part of a driver circuit and thin film transistors to be arranged in a pixel area are formed over the same substrate. The thin film transistors to be arranged in the pixel area are formed in a manner similar to those in Embodiment 3.

[0095]

15 FIG. 9A shows an example of the block diagram of an active matrix display device. Over a substrate 5300 in the display device, a pixel area 5301, a first scan line driver circuit 5302, a second scan line driver circuit 5303, and a signal line driver circuit 5304 are provided. In the pixel area 5301, a plurality of signal lines extended from the signal line driver circuit 5304 is arranged and a plurality of scan lines extended from the first scan line driver circuit 5302 and the second scan line driver circuit 5303 is arranged. Note that pixels which include display elements are provided in a matrix in respective
20 regions where the scan lines and the signal lines intersect with each other. Further, the substrate 5300 in the display device is connected to a timing control circuit 5305 (also referred to as a controller or a controller IC) through a connection portion such as a Flexible Printed Circuit (FPC).

[0096]

25 In FIG. 9A, the first scan line driver circuit 5302, the second scan line driver circuit 5303, and the signal line driver circuit 5304 are formed over the substrate 5300 over which the pixel area 5301 is formed. Thus, the number of components of a driver circuit and the like which is provided outside are reduced, so that a reduction in cost can be achieved. Further, if the driver circuit is provided outside the substrate 5300, wiring
30 would need to be extended and the number of wiring connections would be increased, but if the driver circuit is provided over the substrate 5300, the number of wiring connections can be reduced. Consequently, improvement in reliability and yield can

be achieved.

[0097]

Note that the timing control circuit 5305 supplies, for example, a first scan line driver circuit start signal (GSP1) and a scan line driver circuit clock signal (GCLK1) to the first scan line driver circuit 5302. Moreover, the timing control circuit 5305 supplies, for example, a second scan line driver circuit start signal (GSP2) (which is also referred to as a start pulse) and a scan line driver circuit clock signal (GCLK2) to the second scan line driver circuit 5303. The timing control circuit 5305 supplies a signal line driver circuit start signal (SSP), a signal line driver circuit clock signal (SCLK), a video signal data (DATA) (also simply referred to as a video signal), and a latch signal (LAT) to the signal line driver circuit 5304. Note that each clock signal can be a plurality of clock signals with different cycles or can be supplied together with a signal (CLKB) obtained by inverting the clock signal. Note that it is possible to omit one of the first scan line driver circuit 5302 and the second scan line driver circuit 5303.

[0098]

FIG. 9B shows a structure in which circuits with low driving frequency (e.g., the first scan line driver circuit 5302 and the second scan driver circuit 5303) are formed over the substrate 5300 over which the pixel area 5301, and the signal line driver circuit 5304 is formed over a substrate which is different from a substrate over which the pixel area 5301 is formed. With this structure, a driver circuit formed over the substrate 5300 can be constituted by using thin film transistors with lower field-effect mobility as compared to that of a transistor formed using a single crystal semiconductor. Thus, an increase in the size of the display device, a reduction in the number of steps, a reduction in cost, an improvement in yield, or the like can be achieved.

[0099]

This embodiment can be implemented in appropriate combination with the structures described in the other embodiments.

[0100]

(Embodiment 5)

In this embodiment, examples of electronic apparatuses whose display portion is provided with the display device shown in the above embodiments will be described.

[0101]

The contents (or part of the contents) described in each drawing of the above embodiments can be applied to various electronic devices, specifically to a display portion of an electronic device. Examples of such electronic device include a video camera, a digital camera, a goggle-type display, a navigation system, an audio reproducing device (e.g., a car audio component or an audio component), a computer, a game machine, a personal digital assistant (e.g., a mobile computer, a mobile phone, a portable game console, or an e-book reader), and an image reproducing device provided with a recording medium (specifically, a device which reproduces a recording medium such as a digital versatile disc (DVD) and has a display for displaying a reproduced image).

[0102]

FIG. 10A shows a display device which includes a housing 1211, a support 1212, and a display portion 1213. The display device shown in FIG. 10A has a function of displaying a variety of information (e.g., still images, moving images, and text images) on the display portion. Note that the function that the display device shown in FIG. 10A has is not limited to this; the display device shown in FIG. 10A can have various functions.

[0103]

FIG. 10B shows a camera which includes a main body 1231, a display portion 1232, an image receiving portion 1233, operation keys 1234, an external connection port 1235, and a shutter button 1236. The camera shown in FIG. 10B has a function of taking still images and a function of taking moving images. Note that the camera illustrated in FIG. 10B is not limited to having these functions. Note that the functions of the camera shown in FIG. 10B are not limited to these functions; the camera can have various functions.

[0104]

FIG. 10C shows a computer which includes a main body 1251, a housing 1252, a display portion 1253, a keyboard 1254, an external connection port 1255, and a pointing device 1256. The computer shown in FIG. 10C has a function of displaying various kinds of information (e.g., still images, moving images, and text images) on the display portion. Note that the functions of the computer illustrated in FIG. 10C are not limited to these functions; the computer can have various functions.

[0105]

Applying the display device described in the above embodiments to the display portion of this embodiment allows the transistor in the driver circuit shown in FIGS. 10A to 10C to be turned on or off even if the transistor is normally on. Thus, a driver
5 circuit with higher accuracy and a small malfunction can be provided despite a normally-on transistor in the driver circuit. In addition, it is possible to reduce the power consumption by reducing the frequency of clock signals of the driver circuit.

[0106]

This embodiment can be combined with any of the other embodiments as
10 appropriate.

This application is based on Japanese Patent Application serial no. 2009-219066 filed with Japan Patent Office on September 24, 2009, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A driver circuit comprising:

a static shift register comprising an inverter circuit and a switch,

wherein the inverter circuit comprises a first transistor and a second transistor,

5 wherein the switch comprises a third transistor,

wherein the first to third transistors each comprise an oxide semiconductor layer and are depletion-mode transistors, and

wherein an amplitude voltage of clock signals for driving the third transistor is higher than a power supply voltage for driving the inverter circuit.

10

2. The driver circuit according to claim 1,

wherein the clock signals are a first clock signal and a second clock signal, and

wherein the second clock signal is an inverted signal of the first clock signal.

15

3. The driver circuit according to claim 1, wherein an L/W ratio of the first transistor is higher than an L/W ratio of the second transistor.

4. The driver circuit according to claim 1, wherein a film thickness of a semiconductor layer of the first transistor is larger than a film thickness of a semiconductor layer of the second transistor.

20

5. The driver circuit according to claim 1, wherein the first to third transistor are n-channel transistors.

25

6. A display device comprising the driver circuit according to claim 1.

7. An electronic appliance comprising the display device according to claim 6.

8. A driver circuit comprising:

a static shift register comprising an inverter circuit and a switch; and

a demultiplexer circuit connected to an output terminal of the shift register,

wherein the inverter circuit comprises a first transistor and a second transistor,

30

wherein the switch comprises a third transistor,

wherein the first to third transistors each comprise an oxide semiconductor layer and are depletion-mode transistors,

5 wherein an amplitude voltage of clock signals for driving the first transistor is higher than a power supply voltage for driving the inverter circuit, and

wherein output terminals of the demultiplexer circuit are each connected to a fourth transistor for holding a potential of the output terminal.

9. The driver circuit according to claim 8,

10 wherein the clock signals are a first clock signal and a second clock signal, and wherein the second clock signal is an inverted signal of the first clock signal.

10. The driver circuit according to claim 8, wherein an L/W ratio of the first transistor is higher than an L/W ratio of the second transistor.

15

11. The driver circuit according to claim 8, wherein a film thickness of a semiconductor layer of the first transistor is larger than a film thickness of a semiconductor layer of the second transistor.

20 12. The driver circuit according to claim 8, wherein an L/W ratio of a fifth transistor in the demultiplexer circuit is lower than an L/W ratio of the fourth transistor.

13. The driver circuit according to claim 8,

25 wherein a gate of the fourth transistor is electrically connected to a line through which a positive power supply voltage is supplied,

wherein a first terminal of the fourth transistor is electrically connected to a line through which a negative power supply voltage is supplied, and

wherein a second terminal of the fourth transistor is electrically connected to an output terminal of the demultiplexer circuit.

30

14. The driver circuit according to claim 8, wherein the first to fourth transistor are n-channel transistors.

15. A display device comprising the driver circuit according to claim 8.

16. An electronic appliance comprising the display device according to claim

5 15.

17. A method for driving a driver circuit, the driver circuit including a static shift register comprising an inverter circuit and a switch,

wherein the inverter circuit comprises a first transistor and a second transistor,

10 wherein the switch comprises a third transistor, and

wherein the first to third transistors each comprise an oxide semiconductor layer and are depletion-mode transistors,

said method comprising the step of:

inputting clock signals to the switch,

15 wherein an amplitude voltage of the clock signals for driving the third transistor is higher than a power supply voltage for driving the inverter circuit.

18. The driver circuit according to claim 17,

wherein the clock signals are a first clock signal and a second clock signal, and

20 wherein the second clock signal is an inverted signal of the first clock signal.

19. The driver circuit according to claim 17, wherein an L/W ratio of the first transistor is higher than an L/W ratio of the second transistor.

25 20. The driver circuit according to claim 17, wherein a film thickness of a semiconductor layer of the first transistor is larger than a film thickness of a semiconductor layer of the second transistor.

21. The driver circuit according to claim 17, wherein the first to third transistor
30 are n-channel transistors.

22. A display device comprising the driver circuit according to claim 17.

23. An electronic appliance comprising the display device according to claim
22.

FIG. 1A

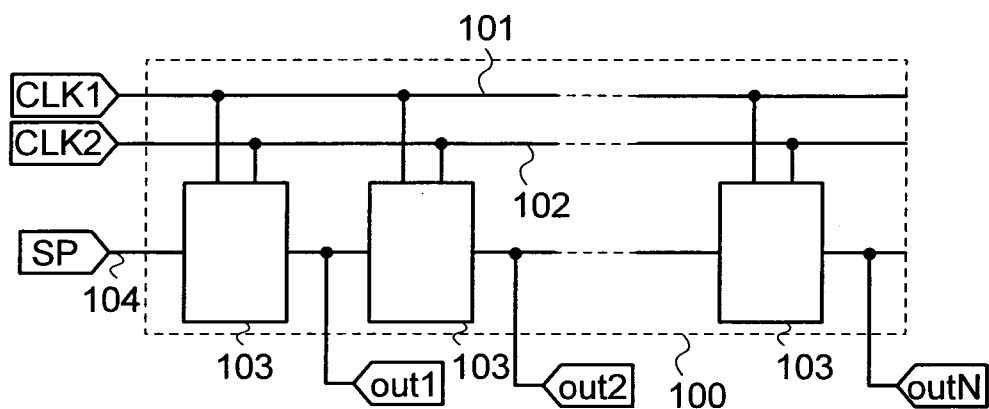


FIG. 1B

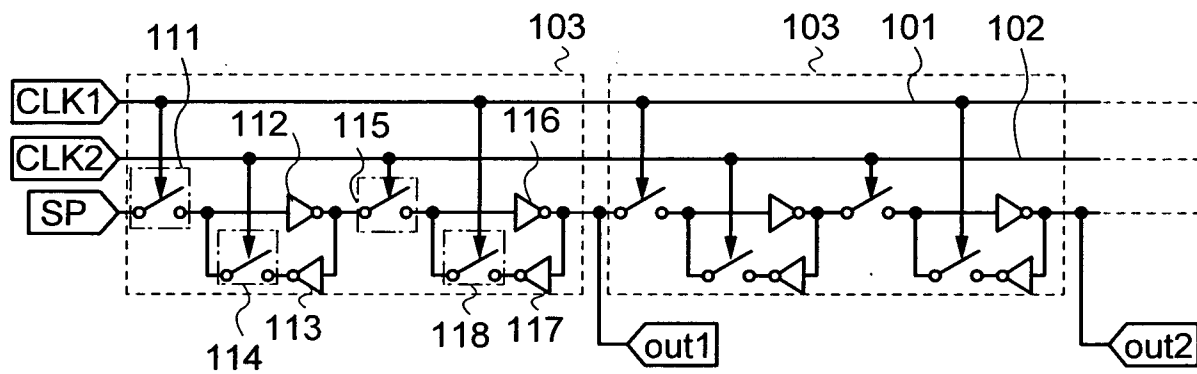


FIG. 2A

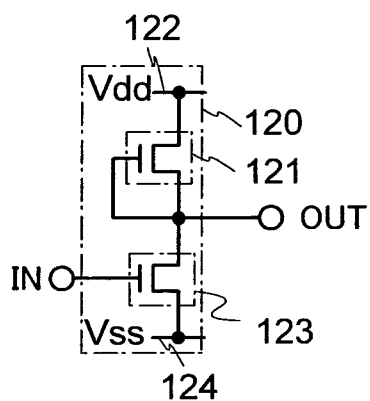


FIG. 2B

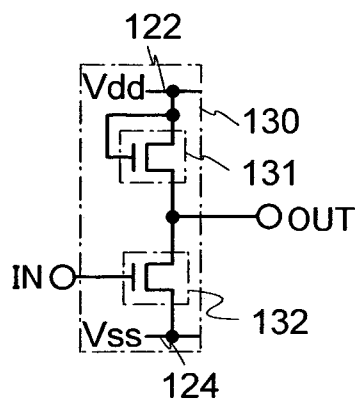


FIG. 2C

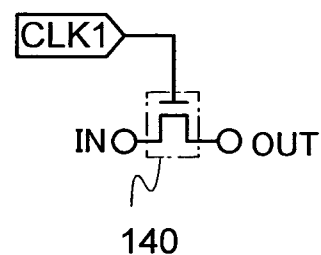


FIG. 2D

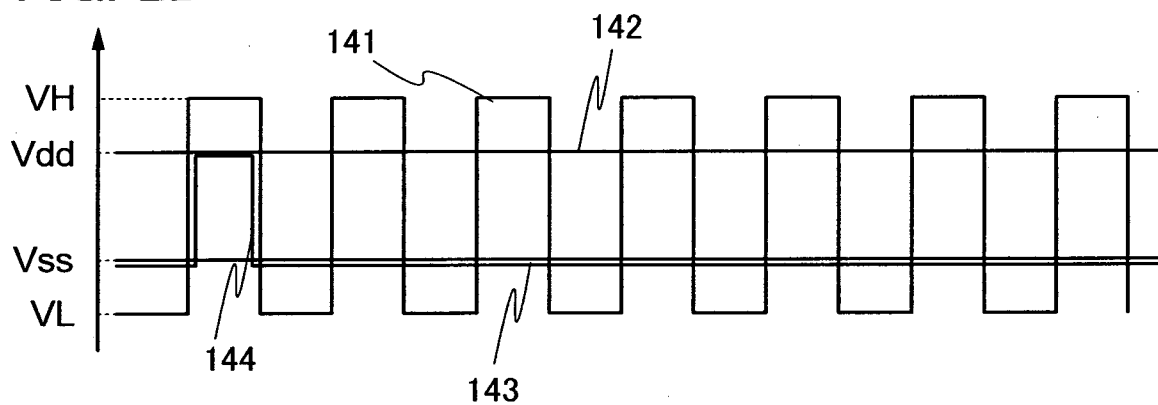


FIG. 2E

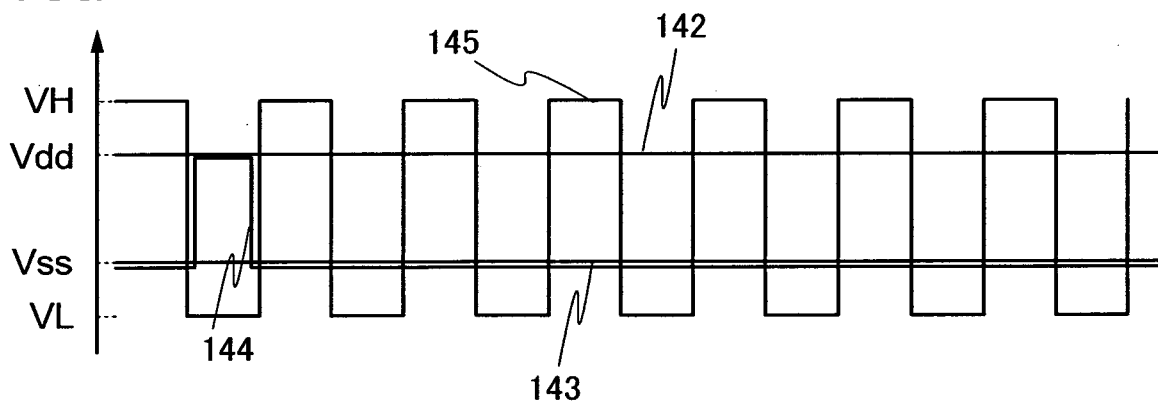


FIG. 3

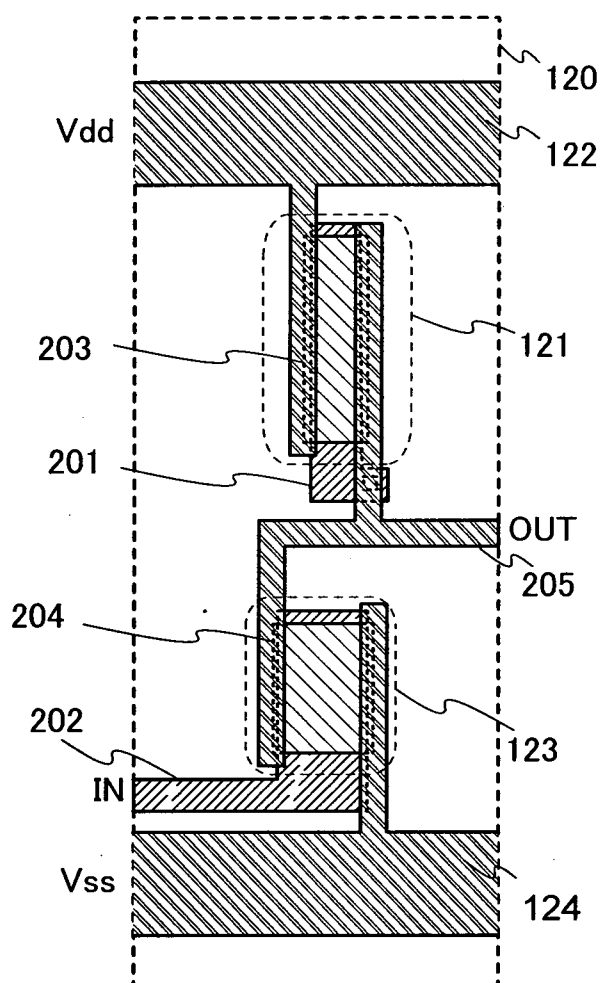
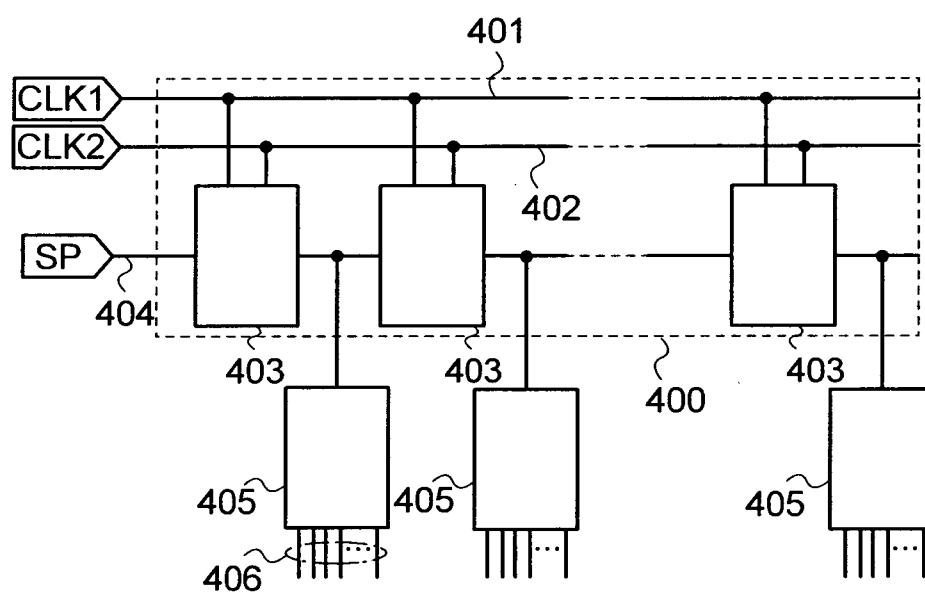


FIG. 4



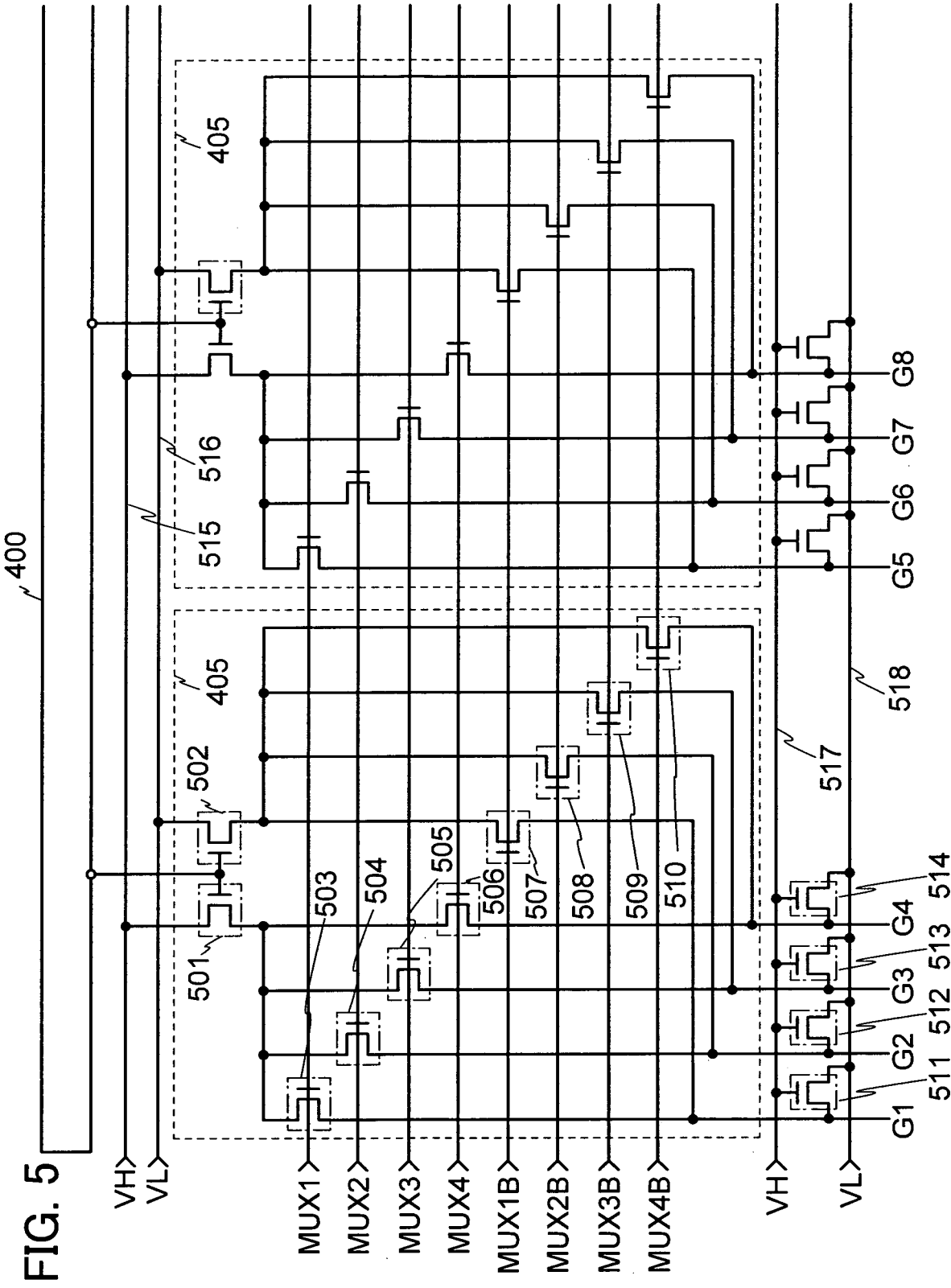


FIG. 6

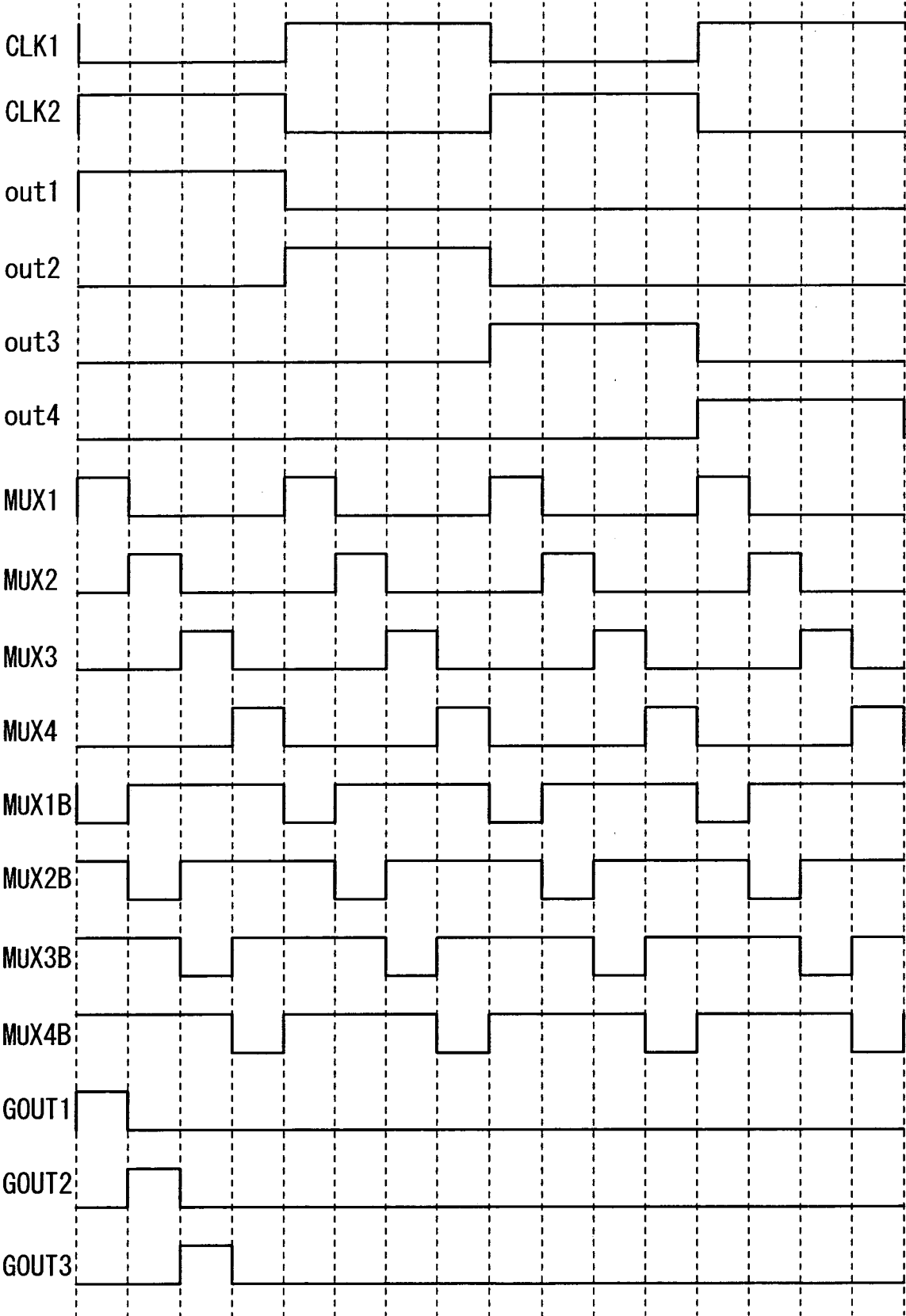


FIG. 8

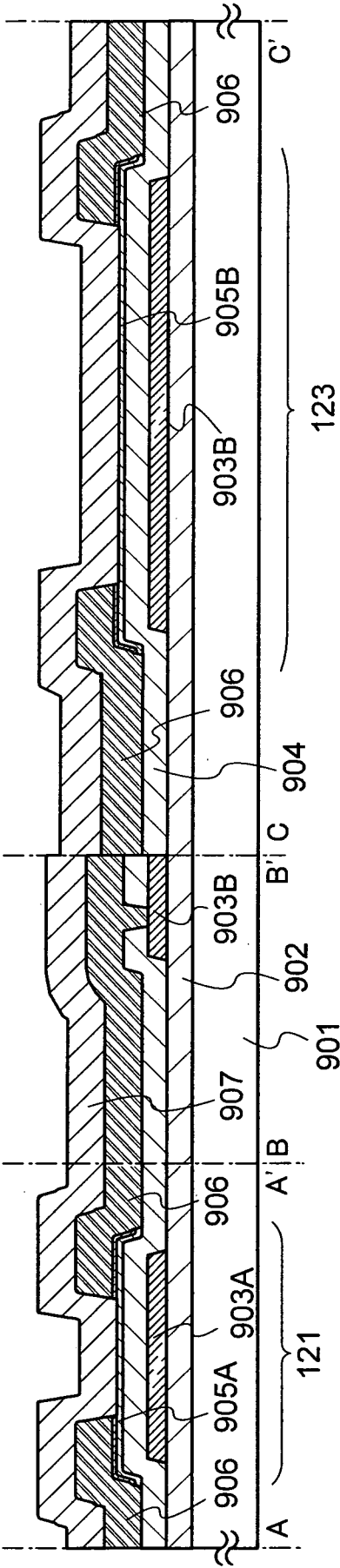


FIG. 9A

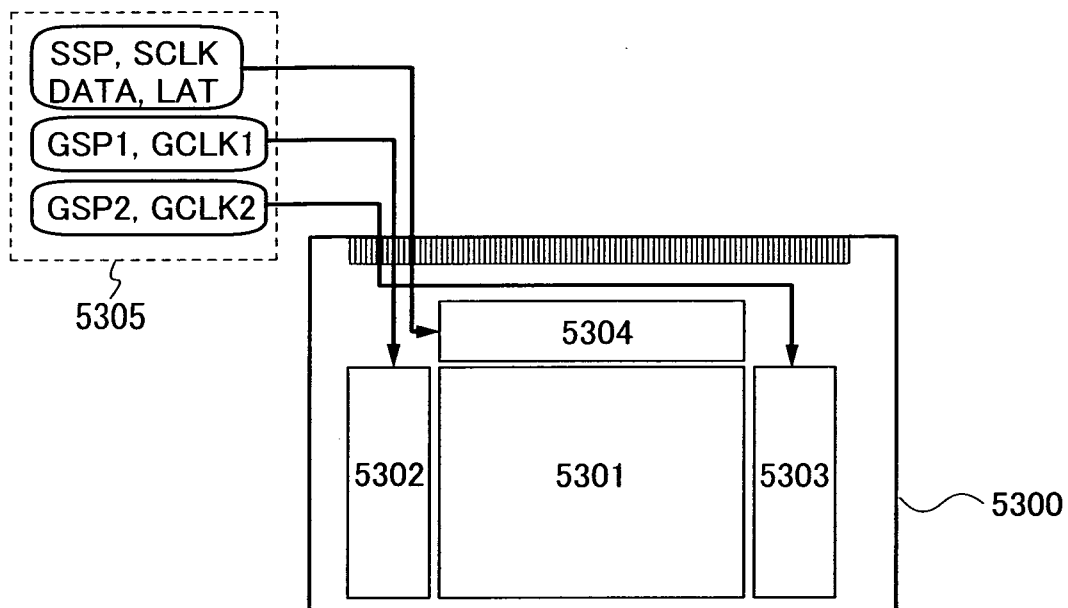


FIG. 9B

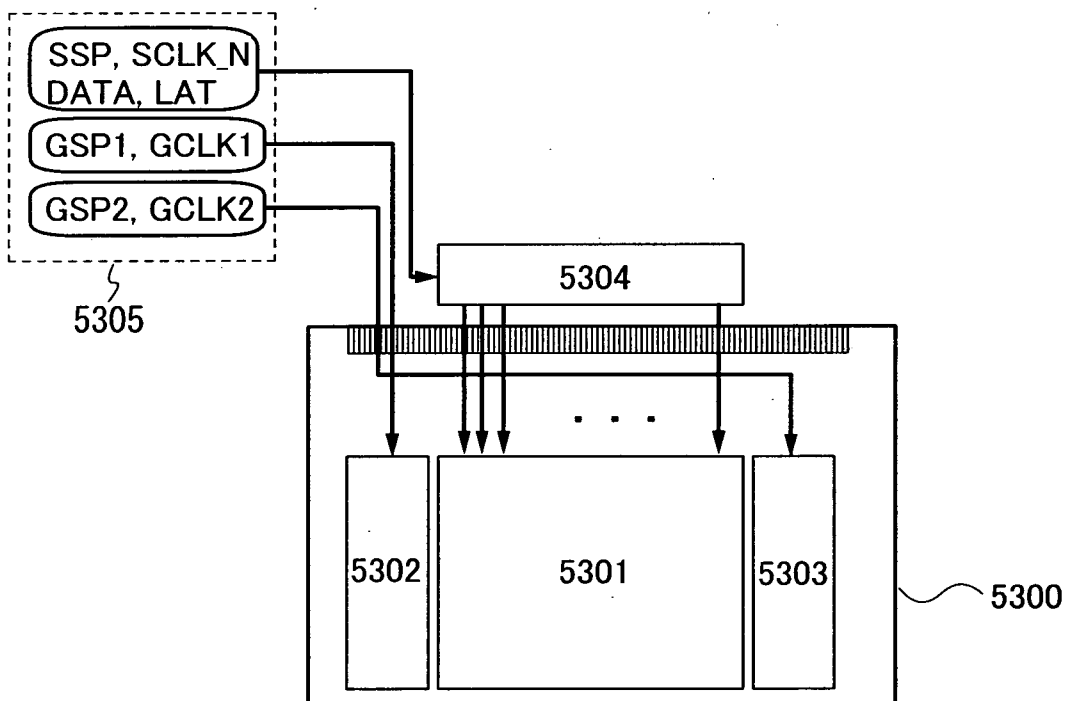


FIG. 10A

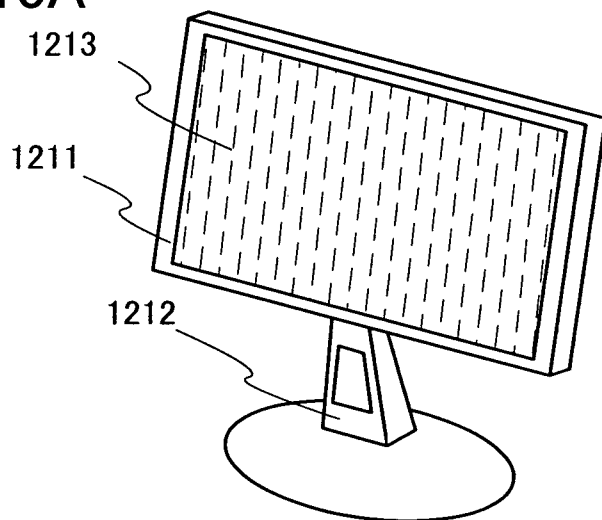


FIG. 10B

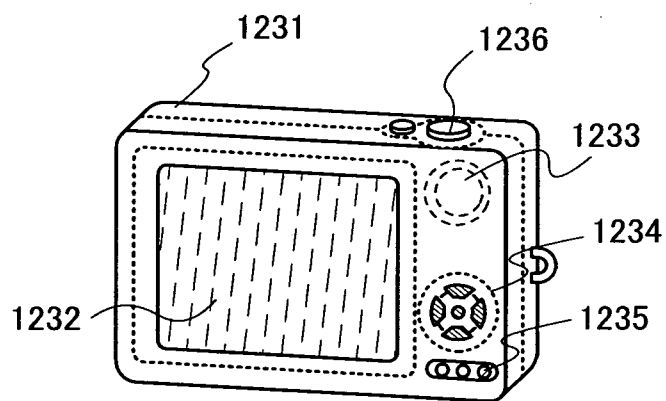


FIG. 10C

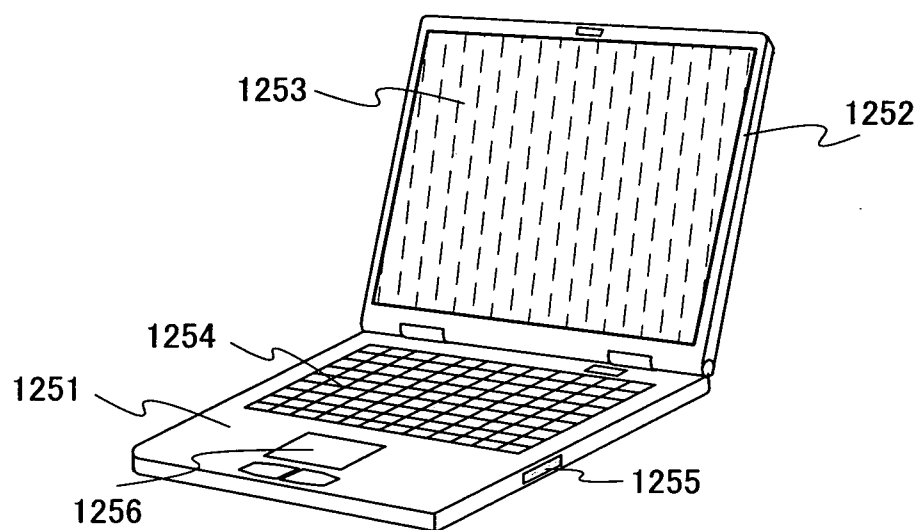


FIG. 11

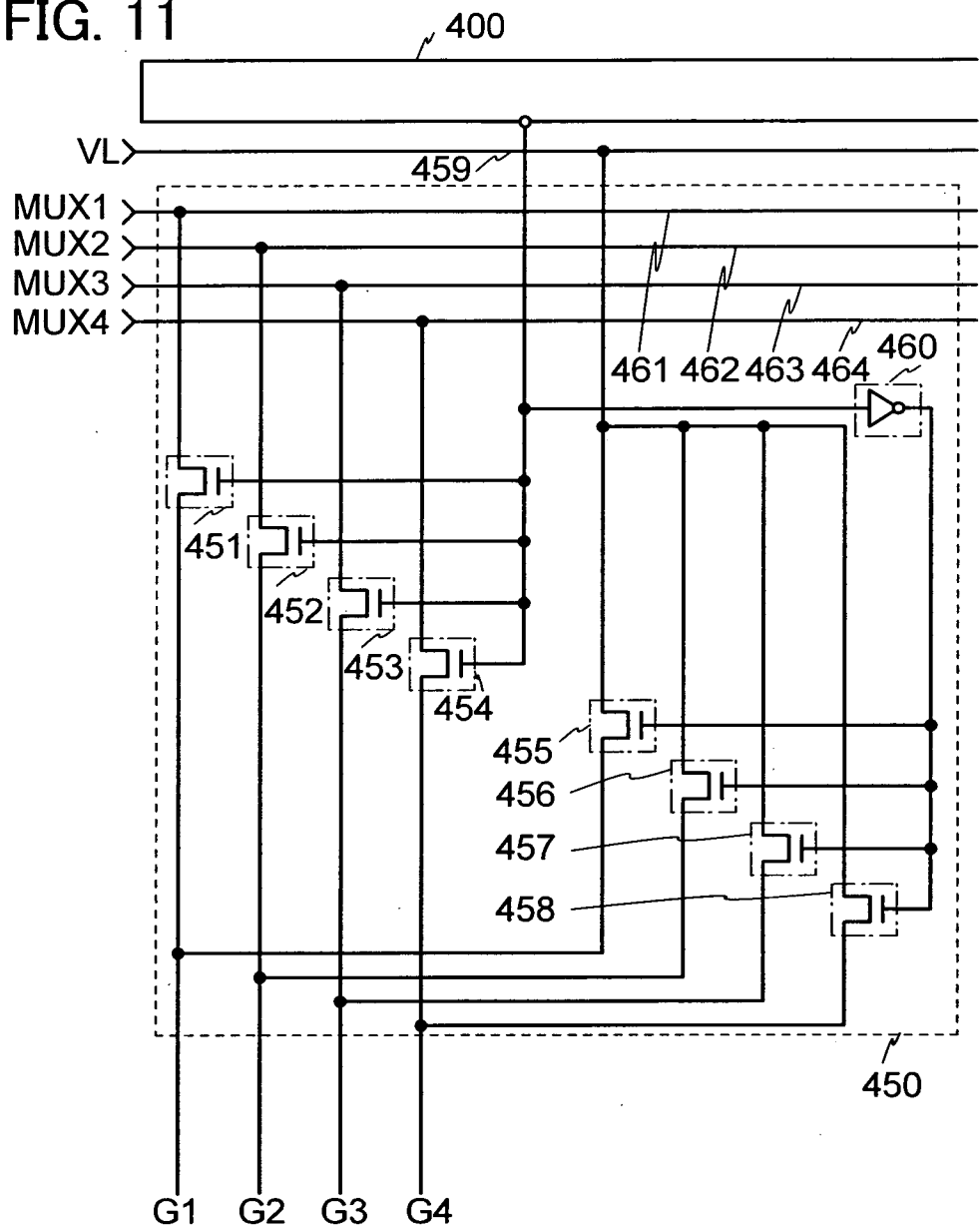
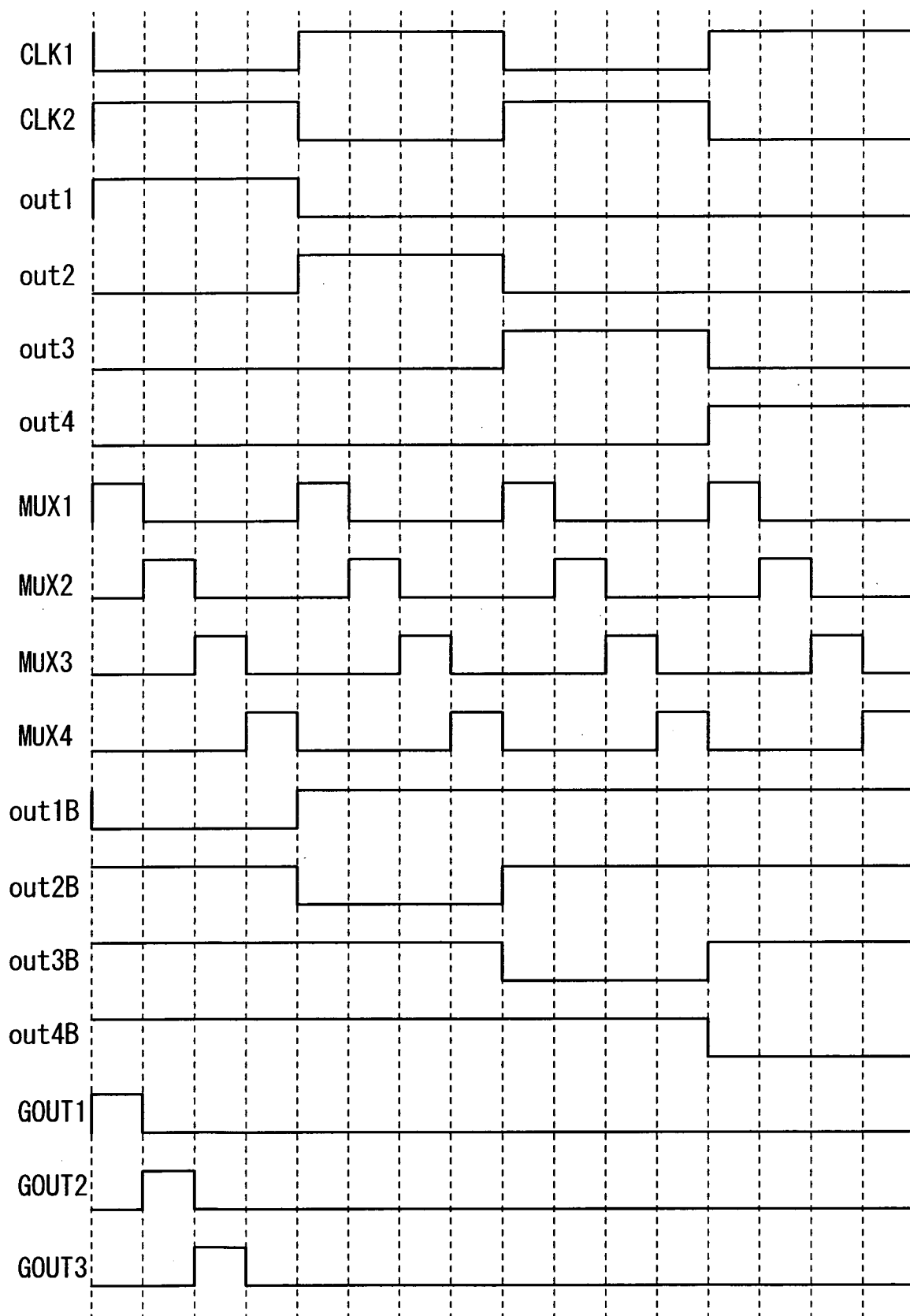


FIG. 12



EXPLANATION OF REFERENCE

100: driver circuit, 101: line, 102: line, 103: pulse output circuit, 104:
5 line, 111: first switch, 112: first inverter circuit, 113: second inverter
circuit, 114: second switch, 115: third switch, 116: third inverter circuit,
117: fourth inverter circuit, 118: fourth switch, 120: inverter circuit,
121: first transistor, 122: line, 123: second transistor, 124: line, 130:
inverter circuit, 131: first transistor, 132: second transistor, 140:
10 transistor, 141: wave form, 142: wave form, 143: wave form, 144:
wave form, 145: wave form, 201: gate line, 202: gate line, 203:
semiconductor layer, 204: semiconductor layer, 205: line, 400: driver
circuit, 401: line, 402: line, 403: pulse output circuit, 404: line, 405:
demultiplexer circuit, 406: line, 501: first transistor, 502: second
15 transistor, 503: third transistor, 504: fourth transistor, 505: fifth
transistor, 506: sixth transistor, 507: seventh transistor, 508: eighth
transistor, 509: ninth transistor, 510: tenth transistor, 511: eleventh
transistor, 512: twelfth transistor, 513: thirteenth transistor, 514:
fourteenth transistor, 515: line, 516: line, 517: line, 518: line, 901:
20 substrate, 902: base film, 904: gate insulating layer, 906: electrode
layer, 907: insulating layer, 1211: housing, 1212: support, 1213:
display portion, 1231: main body, 1232: display portion, 1233: image
receiver, 1234: control key, 1235: external connection port, 1236:
shutter button, 1251: main body, 1252: housing, 1253: display portion,
25 1254: keyboard, 1255: external connection port, 1256: pointing
device, 5300: substrate, 5301: pixel area, 5302: scan line driver
circuit, 5303: scan line driver circuit, 5304: signal line driver circuit,

5305: timing control circuit, 903A: gate electrode layer, 903B: gate electrode layer, 905A: oxide semiconductor layer, 450: demultiplexer circuit, 451: first transistor, 452: second transistor, 453: third transistor, 454: fourth transistor, 455: fifth transistor, 456: sixth transistor, 457: seventh transistor, 458: eighth transistor, 459: line, 460: inverter circuit, 461: line, 462: line, 463: line, 464: line

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2010/065089

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H03K19/0175 (2006.01) i, G09G3/20 (2006.01) i, G11C19/00 (2006.01) i,
G11C19/28 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H03K19/0175, G09G3/20, G11C19/00, G11C19/28

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2010
Registered utility model specifications of Japan 1996-2010
Published registered utility model applications of Japan 1994-2010

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2009-188749 A (SONY CORPORATION) 2009.08.20, 【0064】 - 【0068】, Fig.6 (Family : none)	1-23
A	JP 63-34798 A (MITSUBISHI Electric Corporation) 1988.02.15, the whole document (Family : none)	1-23
A	JP 64-89810 A (ROHM Co., Ltd.) 1989.04.05, the whole document (Family : none)	1-23

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

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national filing date“L” document which may throw doubts on priority claim(s) or which
is cited to establish the publication date of another citation or other
special reason (as specified)“O” document referring to an oral disclosure, use, exhibition or other
means“P” document published prior to the international filing date but later
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priority date and not in conflict with the application but cited to
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be considered novel or cannot be considered to involve an
inventive step when the document is taken alone“Y” document of particular relevance; the claimed invention cannot
be considered to involve an inventive step when the document is
combined with one or more other such documents, such
combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

06.10.2010

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