(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 February 2017 (09.02.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/021721 A1

(51) International Patent Classification:
H01L 45/00 (2006.01) *H03H 7/01* (2006.01)
G11C 13/00 (2006.01) *H03K 19/20* (2006.01)
H01L 49/00 (2006.01)

(21) International Application Number:
PCT/GB2016/052365

(22) International Filing Date:
1 August 2016 (01.08.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/815,054 31 July 2015 (31.07.2015) US

(71) Applicant: **ARM LTD** [GB/GB]; 110 Fulbourn Road, Cambridge CB1 9NJ (GB).

(72) Inventor: **SHIFREN, Lucian**; 150 Rose Orchard Way, San Jose, California 95134 (US).

(74) Agent: **TLIP LTD**; Leeds Innovation Centre, 103 Clarendon Road, Leeds Yorkshire LS2 9DF (GB).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

WO 2017/021721 A1

(54) Title: CORRELATED ELECTRON SWITCH



FIG. 1b

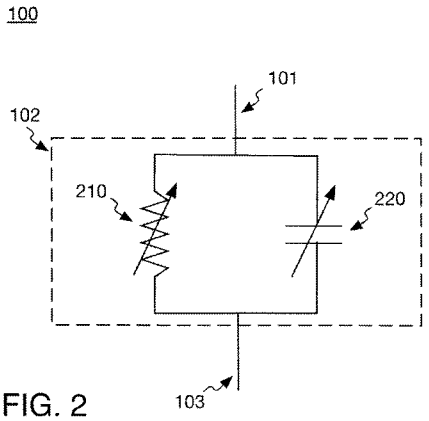


FIG. 2

(57) Abstract: Subject matter disclosed herein relates to correlated electron switches.

CORRELATED ELECTRON SWITCH

[0001] Subject matter disclosed herein may relate to a correlated electron switch device.

[0002] Integrated circuit devices, such as electronic switching devices, for example, may be found in a wide range of electronic device types. For example, memory and/or logic devices may incorporate electronic switches that may be used in computers, digital cameras, cellular telephones, tablet devices, personal digital assistants, etc. Factors related to electronic switching devices, such as may be incorporated in memory and/or logic devices, that may be of interest to a designer in considering suitability for any particular application may include physical size, storage density, operating voltages, and/or power consumption, for example. Other example factors that may be of interest to designers may include cost of manufacture, ease of manufacture, scalability, and/or reliability. Also, there appears to be an ever increasing need for memory and/or logic devices that exhibit characteristics of lower power and/or higher speed.

[0003] Claimed subject matter is particularly pointed out and distinctly claimed in the concluding portion of the specification. However, both as to organization and/or method of operation, together with objects, features, and/or advantages thereof, it may best be understood by reference to the following detailed description if read with the accompanying drawings in which:

[0004] FIG. 1a shows block diagram of an example embodiment of a correlated electron switch device comprising a correlated electron material, in accordance with an embodiment.

[0005] FIG. 1b depicts an example symbol for a correlated electron switch.

[0006] FIG. 2 is a schematic diagram of an equivalent circuit of a correlated electron switch, in accordance with an embodiment.

[0007] FIG. 3 shows a plot of current density versus voltage for a correlated electron switch, according to an embodiment.

[0008] FIG. 4 depicts a schematic diagram of an example compound device, in accordance with an embodiment.

[0009] FIG. 5 depicts a schematic diagram of an example compound device comprising a transistor, in accordance with an embodiment.

[0010] FIG. 6 shows an example plot depicting an example current vs. voltage curve for an example correlated electron switch device, in accordance with an embodiment.

[0011] FIG. 7 shows an example plot depicting example current vs. voltage curves for an example correlated electron switch device, in accordance with an embodiment.

[0012] FIG. 8 shows an example plot depicting example current vs. voltage curves representative of data collected for a set condition for an example correlated electron switch device, in accordance with an embodiment.

[0013] FIG. 9 shows an example plot depicting example current vs. voltage curves representative of data collected for a reset condition for an example correlated electron switch device, in accordance with an embodiment.

[0014] FIG. 10 depicts a schematic diagram of an example compound device comprising a diode, in accordance with an embodiment.

[0015] FIG. 11 shows an example plot depicting example current vs. voltage curves representative of data collected for an example compound device including a diode, in accordance with an embodiment.

[0016] FIG. 12 is a schematic diagram of an example memory cell including a correlated electron switch device, in accordance with an embodiment.

[0017] FIG. 13 is a schematic diagram of an example low-pass filter circuit including a correlated electron switch device, in accordance with an embodiment.

[0018] Reference is made in the following detailed description to accompanying drawings, which form a part hereof, wherein like numerals may designate like parts throughout to indicate corresponding and/or analogous components. It will be appreciated that components illustrated in the figures have not necessarily been drawn to scale, such as for simplicity and/or clarity of illustration. For example, dimensions of some components may

be exaggerated relative to other components. Further, it is to be understood that other embodiments may be utilized. Furthermore, structural and/or other changes may be made without departing from claimed subject matter. It should also be noted that directions and/or references, for example, such as up, down, top, bottom, and so on, may be used to facilitate discussion of drawings and/or are not intended to restrict application of claimed subject matter. Therefore, the following detailed description is not to be taken to limit claimed subject matter and/or equivalents.

[0019] References throughout this specification to one implementation, an implementation, one embodiment, an embodiment and/or the like means that a particular feature, structure, and/or characteristic described in connection with a particular implementation and/or embodiment is included in at least one implementation and/or embodiment of claimed subject matter. Thus, appearances of such phrases, for example, in various places throughout this specification are not necessarily intended to refer to the same implementation or to any one particular implementation described. Furthermore, it is to be understood that particular features, structures, and/or characteristics described are capable of being combined in various ways in one or more implementations and, therefore, are within intended claim scope, for example. In general, of course, these and other issues vary with context. Therefore, particular context of description and/or usage provides helpful guidance regarding inferences to be drawn.

[0020] As utilized herein, the terms "coupled", "connected," and/or similar terms are used generically. It should be understood that these terms are not intended as synonyms. Rather, "connected" is used generically to indicate that two or more components, for example, are in direct physical, including electrical, contact; while, “coupled" is used generically to mean that two or more components are potentially in direct physical, including electrical, contact; however, "coupled" is also used generically to also mean that two or more components are not necessarily in direct contact, but nonetheless are able to co-operate and/or interact. The term coupled is also understood generically to mean indirectly connected, for example, in an appropriate context.

[0021] The terms, “and”, “or”, “and/or” and/or similar terms, as used herein, include a variety of meanings that also are expected to depend at least in part upon the particular context in which such terms are used. Typically, “or” if used to associate a list, such as A, B or C, is intended to mean A, B, and C, here used in the inclusive sense, as well as A, B or C,

here used in the exclusive sense. In addition, the term "one or more" and/or similar terms is used to describe any feature, structure, and/or characteristic in the singular and/or is also used to describe a plurality and/or some other combination of features, structures and/or characteristics. Likewise, the term "based on" and/or similar terms are understood as not necessarily intending to convey an exclusive set of factors, but to allow for existence of additional factors not necessarily expressly described. Of course, for all of the foregoing, particular context of description and/or usage provides helpful guidance regarding inferences to be drawn. It should be noted that the following description merely provides one or more illustrative examples and claimed subject matter is not limited to these one or more illustrative examples; however, again, particular context of description and/or usage provides helpful guidance regarding inferences to be drawn.

[0022] Particular aspects of the present disclosure incorporate correlated electron material (CEM) to form a correlated electron switch (CES), such as, for example, in memory and/or logic devices. CES devices may also be utilized in other types of electronic circuits, such as, for example, filter circuits, as discussed more fully below. However, the scope of claimed subject matter is not limited in scope in these respects. In this context, a CES may exhibit a substantially abrupt conductor/insulator transition arising from electron correlations rather than solid state structural phase changes (e.g., crystalline/amorphous in phase change memory (PCM) devices or filamentary formation and conduction in resistive RAM devices). In one aspect, a substantially abrupt conductor/insulator transition in a CES may be responsive to a quantum mechanical phenomenon, in contrast to melting/solidification or filament formation, for example. Such a quantum mechanical transition between conductive and insulative states, and/or between first and second impedance states, in a CES may be understood in any one of several aspects. As used herein, the terms "conductive state", "lower impedance state", and/or "metal state" may be interchangeable, and/or may at times be referred to as a "conductive/lower impedance state." Similarly, the terms "insulative state" and "higher impedance state" may be used interchangeably herein, and/or may at times be referred to as an "insulative/higher impedance state."

[0023] In an aspect, a quantum mechanical transition of correlated electron switch material between an insulative/higher impedance state and a conductive/lower impedance state may be understood in terms of a Mott transition. In a Mott transition, a material may switch from an insulative/higher impedance state to a conductive/lower

impedance state if a Mott transition condition occurs. The Mott criteria is defined by $(n_C)1^{/3}\, a \approx 0.26$, where n_C is a concentration of electrons and "a" is the Bohr radius. When a critical carrier concentration is achieved such that the Mott criteria is met, the Mott transition will occur and the state of the CES will change from a higher resistance/higher capacitance state to a lower resistance/lower capacitance state.

[0024] In another aspect, the Mott transition is controlled by a localization of electrons. When carriers are localized, the strong coulomb interaction between the electrons splits the bands of the CEM to create an insulator. When electrons are no longer localized, the weak coulomb interaction dominates and the band splitting is removed, resulting in a metal (conductive) band. This is sometimes explained as a "crowded elevator" phenomenon. While an elevator has only a few people in it, the people can move around easily, which is analogous to a conductive/lower impedance state. While the elevator reaches a certain concentration of people, on the other hand, the people can no longer move, which is analogous to the insulative/higher impedance state. However, it should be understood that this classical explanation provided for illustrative purposes, like all classical explanations of quantum phenomenon, is only an incomplete analogy, and that claimed subject matter is not limited in this respect.

[0025] In a further aspect, switching from an insulative/higher impedance state to a conductive/lower impedance state may bring about a change in capacitance in addition to a change in resistance. That is, in an aspect, a CES may comprise the property of variable resistance together with the property of variable capacitance. For example, in a metal state, a CEM may have substantially zero electric field, and therefore substantially zero capacitance. Similarly, in an insulative/higher impedance state (in which electron screening may be very imperfect due to lower density of free electrons), an external electric field may be capable of penetrating the CEM and therefore the CEM will have capacitance due to a physical change in the dielectric function of the CEM. Thus, for example, a transition from an insulative/higher impedance state to a conductive/lower impedance state in a CES may result in changes in both resistance and capacitance, in an aspect.

[0026] In an embodiment, a CES device may switch impedance states responsive to a Mott-transition in a majority of the volume of the CEM of a CES device. In an embodiment, a CES device may comprise a “bulk switch.” As used herein, the term

"bulk switch" refers to at least a majority volume of a CEM of a CES device switching impedance states, such as responsive to a Mott-transition. For example, in an embodiment, substantially all of a CEM of a CES device may switch from an insulative/higher impedance state to a conductive/lower impedance state or from a conductive/lower impedance state to an insulative/higher impedance state responsive to a Mott-transition. In an aspect, a CEM may comprise one or more transition metal oxides, one or more rare earth oxides, one or more oxides of one or more f-block elements of the periodic table, one or more rare earth transitional metal oxide perovskites, yttrium, and/or ytterbium, although claimed subject matter is not limited in scope in this respect. In an embodiment, a device, such as CES device, may comprise CEM including one or more materials selected from a group comprising aluminum, cadmium, chromium, cobalt, copper, gold, iron, manganese, mercury, molybdenum, nickel, palladium, rhenium, ruthenium, silver, tin, titanium, vanadium, and zinc (which may be linked to a cation such as oxygen or other types of ligands), or combinations thereof, although claimed subject matter is not limited in scope in this respect.

[0027] FIG. 1a shows an example embodiment 100 of a CES device comprising CEM, such as material 102, sandwiched between conductive terminals, such as conductive terminals 101 and 103. In an embodiment, a CES device, such as CES device 100, may comprise a variable impeder device. As utilized herein, the terms "correlated electron switch" and "variable impeder" may be interchangeable. At least in part through application of a critical voltage and a critical current between the terminals, such as between conductive terminals 101 and 103, the CEM, such as material 102, may transition between the aforementioned conductive/lower impedance state and insulative/higher impedance state. As mentioned, CEM, such as material 102, in a variable impeder device, such as variable impeder 100, may transition between a first impedance state and a second impedance state due to a quantum mechanical transition of the correlated electron switch material as a result an applied critical voltage and an applied critical current, as described in more detail below. Also, as mentioned above, a variable impeder device, such as variable impeder device 100, may exhibit properties of both variable resistance and variable capacitance.

[0028] In a particular embodiment, a variable impeder device, such as variable impeder device 100, may comprise CEM that may transition between or among a plurality of detectable impedance states based, at least in part, on a transition of at least

a majority portion of the CEM between an insulative/higher impedance state and a conductive/lower impedance state due to a quantum mechanical transition of the correlated electron switch material. For example, in an embodiment, a variable impeder device may comprise a bulk switch, in that substantially all of a CEM of a variable impeder device may switch from an insulative/higher impedance state to a conductive/lower impedance state or from a conductive/lower impedance state to an insulative/higher impedance state responsive to a Mott-transition. In this context, an "impedance state" means a detectable state of a variable impeder device that is indicative of a value, symbol, parameter and/or condition, just to provide a few examples. In one particular embodiment, as described below, an impedance state of a variable impeder device may be detected based, at least in part, on a signal detected on terminals of the variable impeder device in a read and/or sense operation. In another particular embodiment, as described below, a variable impeder device may be placed in a particular impedance state to represent or store a particular value, symbol, and/or parameter, and/or to achieve a particular capacitance value for the variable impeder device by application of one or more signals across terminals of the variable impeder device in a "write" and/or "program" operation, for example. Of course, claimed subject matter is not limited in scope to the particular example embodiments described herein.

[0029] FIG. 1b depicts an example symbol 110 that may be utilized, for example, in electrical circuit schematic diagrams to notate a CES and/or a variable impeder device. Example symbol 110 is meant to remind the viewer of the variable resistance and variable capacitance properties of a CES and/or variable impeder device, such as variable impeder device 100. Example symbol 110 is not meant to represent an actual circuit diagram, but is merely meant as an electrical circuit diagram symbol. Of course, claimed subject matter is not limited in scope in these respects.

[0030] FIG. 2 depicts a schematic diagram of an equivalent circuit of an example variable impeder device, such as variable impeder device 100. As mentioned, a variable impeder device may comprise characteristics of both variable impedance and variable capacitance. For example, an equivalent circuit for a variable impeder device may, in an embodiment, comprise a variable resistor, such as variable resistor 210 in parallel with a variable capacitor, such as variable capacitor 220. Of course, although a variable resistor 210 and variable capacitor 220 are depicted in FIG. 2 as comprising discrete components, a variable impeder device, such as variable impeder device 100, may

comprise a substantially homogenous CEM, such as CEM 102, wherein the CEM comprises characteristics of variable capacitance and variable resistance.

[0031] Table 1 below depicts an example truth table for an example variable impeder device, such as variable impeder device 100.

Resistance	Capacitance
$R_{high}(V_{applied})$	$C_{high}(V_{applied})$
$R_{low}(V_{applied})$	$C_{low}(V_{applied})$~0

Table 1 – Correlated Electron Switch Truth Table

[0032] In an embodiment, example truth table 120 shows that a resistance of a variable impeder device, such as variable impeder device 100, may transition between a lower resistance state and a higher resistance state that is a function, at least in part, of a voltage applied across the CEM. In an embodiment, a resistance of a lower resistance state may be 10-100,000 times lower than a resistance of a higher impedance state, although claimed subject matter is not limited in scope in this respect. Similarly, example truth table 120 shows that a capacitance of a variable impeder device, such as variable impeder device 100, may transition between a lower capacitance state, which for an example embodiment may comprise approximately zero, or very little, capacitance, and a higher capacitance state that is a function, at least in part, of a voltage applied across the CEM. It should be noted that a variable impeder is not a resistor, but rather comprises a device having properties of both variable capacitance and variable resistance. In an embodiment, resistance and/or capacitance values depend, at least in part, on an applied voltage.

[0033] FIG. 3 shows a plot of current density versus voltage across electrically conductive terminals, such as electrically conductive terminals 101 and 103, for a variable impeder device, such as example variable impeder device 100, according to an embodiment. Based, at least in part, on a voltage applied to terminals of a variable impeder device (e.g., in a write operation), such as variable impeder device 100, a CEM, such as CEM 102, may be placed in a conductive/lower impedance state or an insulative/higher impedance state. For example, application of a voltage V_{reset} and current density J_{reset} may place the variable impeder device in an insulative/higher

impedance state, and application of a voltage V_{set} and a current density J_{set} may place the variable impeder device in a conductive/lower impedance state. That is, a "set" condition may place a variable impeder device, such as variable impeder device 100, into a conductive/lower impedance state, and a "reset" condition may place a variable impeder device, such as variable impeder device 100, into an insulative/higher impedance state, in an embodiment. Following placement of the variable impeder device in a lower impedance state or a higher impedance state, the particular state of the variable impeder device may be detected at least in part by application of a voltage V_{read} (e.g., in a read operation) and detection of a current or current density at terminals, such as electrically conductive terminals 101 and 103, of a variable impeder device, such as variable impeder device 100.

[0034] In an embodiment, a CEM of a variable impeder device may include, for example, any TMO, such as, for example, peroskovites, Mott insulators, charge exchange insulators, and/or Anderson disorder insulators. In a particular embodiment, a CES device may be formed from materials such as nickel oxide, cobalt oxide, iron oxide, yttrium oxide and peroskovites such as Cr doped strontium titanate, lanthanum titanate, and the manganite family including praesydium calcium manganite, and praesydium lanthanum manganite, to provide a few examples. In an embodiment, oxides incorporating elements with incomplete ***d*** and ***f*** orbital shells may exhibit sufficient impedance switching properties for use in a CES device. In an embodiment, a CES may be prepared without electroforming. Other embodiments may employ other transition metal compounds without deviating from claimed subject matter. For example, $\{M(chxn)_2Br\}Br_2$ where M may comprise Pt, Pd, or Ni, and chxn comprises 1R,2R-cyclohexanediamine, and other such metal complexes may be used without deviating from the scope of claimed subject matter.

[0035] In one aspect, the variable impeder device of FIG. 1 may comprise materials that comprise TMO metal oxide variable impedance materials, though it should be understood that these are exemplary only, and are not intended to limit the scope of claimed subject matter. Particular implementations may employ other variable impedance materials as well. Nickel oxide, NiO, is disclosed as one particular TMO. NiO materials discussed herein may be doped with extrinsic ligands, which may stabilize variable impedance properties by passivating the interfacing and allowing for adjustable voltages and impedances, in an embodiment. In a particular embodiment, NiO variable

impedance materials disclosed herein may include a carbon containing ligand, which may be indicated by $NiO(C_x)$. Here, one skilled in the art may determine a value of x for any specific carbon containing ligand and any specific combination of carbon containing ligand with NiO simply by balancing valences, in an embodiment. In another particular example embodiment, NiO doped with extrinsic ligands may be expressed as $NiO(L_x)$, where L_x is a ligand element or compound and x indicates a number of units of the ligand for one unit of NiO. One skilled in the art may determine a value of x for any specific ligand and any specific combination of ligand with NiO or any other transition metal simply by balancing valences, in an embodiment.

[0036] According to an embodiment, if sufficient bias is applied (e.g., exceeding a band-splitting potential) and the aforementioned Mott condition is met (injected electron holes = the electrons in the switching region), the variable impeder device may rapidly switch from a conductive/lower impedance state to an insulator state via the Mott transition. This may occur at point 308 of the plot in FIG. 3. At this point, electrons are no longer screened and become localized. This correlation splits the bands to form an insulator. While the CEM of the variable impeder device is still in the insulative/higher impedance state, current may generated by transportation of holes. If enough bias is applied across terminals of the variable impeder device, electrons may be injected into a metal-insulator-metal (MIM) diode over the potential barrier of the MIM device. If enough electrons have been injected and enough potential is applied across terminals to achieve a set condition, an increase in electrons may screen electrons and remove a localization of electrons, which may collapse the band-splitting potential forming a metal, thereby placing the variable impeder device in a conductive/lower impedance state.

[0037] According to an embodiment, current in a CEM of a variable impeder device may be controlled by an externally applied "compliance" condition determined based, at least in part, on the external current limited during a write operation to achieve a set condition to place the variable impeder device in a conductive/lower impedance state. This externally applied compliance current also sets the subsequent reset condition current density requirement. As shown in the particular implementation of FIG. 3, a current density J_{comp} applied during a write operation at point 316 to place the variable impeder device in a conductive/lower impedance state may determine a compliance condition for placing the variable impeder device in an insulative/higher impedance state in a subsequent write operation. As shown, the CEM of the variable impeder device

may be subsequently placed in an insulative/higher impedance state by application of a current density $J_{reset} \geq J_{comp}$ at a voltage V_{reset} at point 308, wherein J_{comp} may be externally applied, in an embodiment.

[0038] A compliance current, such as an externally applied compliance current, therefore may set a number of electrons in a CEM of a variable impeder device which are to be "captured" by holes for the Mott transition. In other words, a current applied in a write operation to place a variable impeder device in a conductive/lower impedance state may determine a number of holes to be injected to the CEM of the variable impeder device for subsequently transitioning the variable impeder device to an insulative/higher impedance state. As discussed more fully below, a compliance current may be applied dynamically.

[0039] As pointed out above, a transition to an insulative/higher impedance state may occur in response to a Mott transition at point 308. As pointed out above, such a Mott transition may occur at a condition in a CEM of a variable impeder device in which a concentration of electrons n equals a concentration of electron holes p. This condition occurs when the following Mott criteria is met, as represented by expression (1) as follows:

$$\lambda_{TF} n^{\frac{1}{3}} = C \sim 0.26$$
$$n = \left(\frac{C}{\lambda_{TF}} \right)^3 \qquad (1)$$

where:

λ_{TF} is a Thomas Fermi screening length; and

C is a constant which equals approximately 0.26 for the Mott transition.

[0040] According to an embodiment, a current or current density in a region 304 of the plot shown in FIG. 3 may exist in response to an injection of holes from a voltage signal applied across terminals, such as terminals 101 and 103, of a variable impeder device, such as variable impeder device 100. Here, injection of holes may meet a Mott transition criterion for the conductive to insulator transition at current I_{MI} as a critical

voltage V_{MI} is applied across terminals, such as terminal 101 and 103, of a variable impeder device, such as variable impeder device 100. This may be modeled according to expression (2) as follows:

$$I_{MI}(V_{MI}) = \frac{dQ(V_{MI})}{dt} \approx \frac{Q(V_{MI})}{t}$$
$$Q(V_{MI}) = qn(V_{MI}) \qquad (2)$$

Where $Q(V_{MI})$ is the charge injected (hole or electron) and is a function of the applied voltage. As used herein, the notation "MI" signifies a metal-to-insulator transition, and the notation "IM" signifies an insulator-metal transition. That is, "V_{MI}" refers to a critical voltage and "I_{MI}" refers to a critical current to transition a CEM from a conductive/lower impedance state to an insulative/higher impedance state. Similarly, "V_{IM}" refers to a critical voltage and "I_{IM}" refers to a critical current to transition a CEM from an insulative/higher impedance state to a conductive/lower impedance state.

[0041] Injection of holes to enable a Mott transition may occur between bands and in response to critical voltage V_{MI}. and critical current I_{MI}. By equating electron concentration n with the needed charge concentration to result in a Mott transition by holes injected by I_{MI} in expression (2) according to expression (1), a dependency of such a critical voltage V_{MI} on Thomas Fermi screening length λ_{TF} may be modeled according to expression (3) as follows:

$$I_{MI}(V_{MI}) = \frac{Q(V_{MI})}{t} = \frac{qn(V_{MI})}{t} = \frac{q}{t}\left(\frac{C}{\lambda_{TF}}\right)^3$$

$$J_{reset}(V_{MI}) = J_{MI}(V_{MI}) = \frac{I_{MI}(V_{MI})}{A_{CEM}} = \frac{q}{A_{CEM}t}\left(\frac{C}{\lambda_{TF}(V_{MI})}\right)^3 \qquad (3)$$

Wherein A_{CEM} is a cross-sectional area of a CEM, such as CEM 102, of a variable impeder device, such as variable impeder device 100, and wherein $J_{reset}(V_{MI})$, depicted at point 308 of example plot 300, is a current density through the CEM, such as CEM 102, to be applied to the CEM at a critical voltage V_{MI} to place the CEM of the variable impeder device in an insulative/higher impedance state. In an embodiment, a CEM may be switched between a conductive/lower impedance state and an insulative/higher impedance state at least in part by a disproportionation reaction.

[0042] According to an embodiment, a CEM, such as CEM 102, of a variable impeder device, such as variable impeder device 100, may be placed in a conductive/lower impedance state (e.g., by transitioning from an insulative/higher impedance state) by injection of a sufficient number of electrons to satisfy a Mott transition criteria.

[0043] In transitioning a CEM of a variable impeder device to a conductive/lower impedance state, as enough electrons have been injected and the potential across terminals of the variable impeder device overcomes a critical switching potential (e.g., V_{set}), injected electrons begin to screen and unlocalize double-occupied electrons to reverse a disproportion reaction and closing the bandgap. A current density $J_{set}(V_{MI})$, depicted at point 314 of FIG. 3, for transitioning the CEM of the variable impeder device to the conductive/lower impedance state in a metal-insulator Mott transition at a critical voltage V_{MI} enabling transition to the conductive/lower impedance state may be represented according to expressions (4) as follows:

$$I_{MI}(V_{MI}) = \frac{dQ(V_{MI})}{dt} \approx \frac{Q(V_{MI})}{t}$$

$$Q(V_{MI}) = qn(V_{MI})$$

$$I_{MI}(V_{MI}) = \frac{Q(V_{MI})}{t} = \frac{qn(V_{MI})}{t} = \frac{q}{t}\left(\frac{C}{a_B}\right)^3$$

$$J_{set}(V_{IM}) = J_{injection}(V_{IM}) = J_{IM}(V_{IM}) = \frac{I_{IM}(V_{IM})}{A_{CEM}} = \frac{q}{A_{CEM}t}\left(\frac{C}{a_B}\right)^3 \qquad (4)$$

where:

a_B is a Bohr radius.

[0044] According to an embodiment, a "read window" 302 for detecting a memory state of a variable impeder device in a read operation may be set out as a difference between a portion 306 the plot of FIG. 3 while the CEM of the variable impeder device is in an insulative/higher impedance state and a portion 304 of the plot FIG. 3 while the CEM of the variable impeder device is in a conductive/lower impedance state at a read voltage V_{read}. In a particular implementation, read window 302 may be used to determine the Thomas Fermi screening length λ_{TF} of a CEM, such as correlated electron

switch material 102, of a variable impeder device, such as variable impeder device 100. For example, at a voltage V_{reset}, current densities J_{reset} and J_{set} may be related to according to expression (5) as follows:

$$\lambda_{TF}(@V_{reset}) = a_B \left(\frac{J_{reset}}{J_{off}} \right)^{\frac{1}{3}} \quad (5)$$

wherein J_{off} represents a current density of a CEM in an insulative/higher impedance state at V_{reset}. See, for example, point 309 of FIG. 3.

[0045] In another embodiment, a "write window" 310 for placing a CEM of variable impeder device in an insulative/higher impedance or conductive/lower impedance state in a write operation may be set out as a difference between V_{reset} and V_{set}. Establishing $|V_{set}| > |V_{reset}|$ may enable a switch between the conductive/lower impedance and insulative/higher impedance state. V_{reset} may comprise approximately the band splitting potential caused by the correlation and V_{set} may comprise approximately twice the band splitting potential, such that the read window may comprise approximately the band-splitting potential. In particular implementations, a size of write window 310 may be determined, at least in part, by materials and doping of the CEM of the variable impeder device.

[0046] In an embodiment, a process for reading a value represented as an impedance state of a variable impeder device, such as variable impeder device 100, may comprise a voltage being applied to a CEM of a variable impeder device. At least one of a current and/or current density within a CEM of a variable impeder device may be measured, and an impedance state of a CEM of a variable impeder device may be determined, at least in part, on the measured current and/or current density, in an embodiment.

[0047] Additionally, in an embodiment, an impedance of an impedance state may depend at least in part on a combination of a capacitance and a resistance of a CEM of a variable impeder device. In an embodiment, the determined impedance state may comprise one of a plurality of impedance states. A first impedance state may comprise a lower resistance and lower capacitance, and a second impedance state may comprise a higher resistance and a higher capacitance, for example. Also, in an embodiment, a ratio

of the impedances of the plurality of impedance states may be proportional to a physical property of the CEM of the variable impeder device. In an embodiment, the physical property of the CEM of the variable impeder device may comprise at least one of a Thomas Fermi screening length and a Bohr radius. Further, in an embodiment, individual impedance states of the plurality of impedance states may be associated with a data value. Additionally, in an embodiment, a difference in current between a first impedance state and a second impedance state at a predetermined voltage provides an indication of a read window. However, claimed subject matter is not limited in scope in these respects.

[0048] In an embodiment, a plurality of electrons may be provided to a CEM of a variable impeder device such that the CEM enters a first impedance state. A plurality of holes may be provided to the CEM such that the CEM enters a second impedance state. Also, in an embodiment, the plurality of electrons may cause a voltage across the CEM to be greater than a set voltage threshold, and the plurality of holes may cause the voltage across the CEM to be equal to or greater than a reset voltage threshold. Further, in an embodiment, a voltage across the CEM may cause a current density in the CEM to be equal to or greater than a set current density and/or a set current, and a voltage across the CEM may cause a current density in the CEM to be equal to or greater than a reset current density and/or a reset current.

[0049] Also, in an embodiment, a set voltage across the CEM and a set current density through a CEM of a variable impeder device may be exceeded. Additionally, a reset voltage across a CEM and a reset current density through a CEM of a variable impeder device may be exceeded. Further, in an embodiment, individual impedance states of a plurality of impedance states may be associated with a data value.

[0050] In an embodiment, at least one of a reset voltage, a set voltage, and a difference between the set voltage and the reset voltage are proportional to a physical property of a CEM of a variable impeder device. A physical property of a CEM may include at least one of a strong electron potential due to localization, and/or a correlation of electrons, for example. Also, in an embodiment, a difference in the set voltage and the reset voltage may provide an indication of a size of at least one of a write/program window.

[0051] FIG. 4 depicts a schematic diagram of an embodiment 400 of an example compound device. As utilized herein, the term "compound device" refers to a CES, such as CES 420, coupled to a current and/or voltage source, such as current source 410. In an embodiment, compound device behavior may be defined, at least in part, by how a CES, such as CES 420, behaves when coupled to an external current and/or voltage source, such as current source 410. Example current sources may include, but are not limited to, a diode and/or a transistor, in an embodiment. As described above, a CES, such as CES 420, may require both critical voltage and critical current conditions to achieve a set condition and/or to achieve a reset condition. In an embodiment, set and reset conditions comprise unique physical actions. For example, set and/or reset conditions individually require particular carrier densities (i.e., to meet the Mott criteria) and an applied bias to inject holes and/or electrons into the CEM of a CES device. Therefore, a CES, such as CES 420, may exhibit different, distinct characteristics when coupled with different current and/or voltage sources, such as current source 410, in an embodiment. Thus, coupling a CES, such as CES 420, to different current and/or voltage sources, such as current source 410, may yield different compound devices exhibiting characteristics that depend, at least in part, on the particular current and/or voltage source. As a CES requires both a critical voltage and current (as opposed to a one or the other) to transition from one impedance state to another, compound device behavior can vary widely, depending at least in part on the characteristics of the current/voltage source. That compound device behavior may depend, at least in part, on the particular current and/or voltage source coupled to a CES may be understood through examination of the following Kirchhoff Current Law equations, represented by expressions (6) below:

$$J_{CEM}(V_{CEM}) = J_{critical}(V_{critical}) = J_{reset}(V_{reset}) \; or \; J_{set}(V_{set})$$

$$J_{CEM}(V_{CEM}) = \sigma E_{CEM}(V_{CEM}) = \frac{I_{source}(V_{source})}{A_{CEM}}$$

$$E_{CEM}(V_{CEM}) \sim \frac{(V_{CEM})}{d_{CEM}}$$

$$J_{CEM}(V_{CEM}) = \sigma \frac{(V_{CEM})}{d_{CEM}} = \frac{I_{source}(V_{source})}{A_{CEM}}$$

$$I_{source}(V_{source}) = J_{CEM}(V_{CEM})A_{CEM} = \frac{A_{CEM}}{d_{CEM}}\sigma V_{CEM} \quad (6)$$

wherein σ represents CEM conductivity, A_{CEM} represents an area of a CEM of a CES device, and d_{CEM} represents a depth or thickness of the CEM of the CES device.

[0052] From expressions (6) above, it may be seen that criteria for switching from a conductive/lower impedance state to an insulative/higher impedance state or from an insulative/higher impedance state to a conductive/lower impedance state for a CES may be determined at least in part by CEM design. In an embodiment, CEM material composition and/or dimensions may affect switching criteria. For example, an increase in CEM area may result in an increase in critical current ($I_{critical}$) and/or critical voltage ($V_{critical}$), in an embodiment. Similarly, current through a CES, such as CES 420, may depend at least in part on the particular characteristics of the current and/or voltage supply, such as current source 410, due at least in part to the duel dependency of critical voltage and critical current for switching. Also, in an embodiment, a Mott transition inside a CEM of a CES, such as CES 420, may be controlled and/or determined via one or more characteristics of a particular current and/or voltage source, such as current source 410.

[0053] FIG. 5 depicts a schematic diagram of an embodiment 500 of an example compound device comprising a transistor, such as transistor 510, as a current source coupled to a CES, such as CES 520. In an embodiment, a voltage source, such as voltage source (V_{DD}) 540, may be applied across a transistor, such as transistor 510, and a CES device, such as CES 520. An additional voltage source, such as voltage source (Vg) 530, may be applied to a transistor, such as transistor 510. For example, Vg 530 may be applied to a gate of an NMOS transistor, such as transistor 510, in an embodiment. The Kirchhoff Current Law equations represented by expressions (7) below may be utilized to consider one or more characteristics of example compound device 500 comprising example transistor 510 coupled to example CES 520.

$$I_{ds}(V_{gs,}\, V_{ds,}t) = \frac{A_{CEM}}{d_{CEM}}\sigma V_{CEM}$$

$$V_{CEM} = V_{DD} - V_{ds} = V_{DD} - I_{ds}R_{ds}$$

$$\sigma \sim \sigma(V_{gs})$$

$$I_{ds}(V_{gs,}\, V_{ds,}t) = \frac{A_{CEM}}{d_{CEM}}\sigma(V_{gs})(V_{DD} - V_{ds})$$

$$I_{ds}(V_{gs,}\, V_{ds,}t) = \frac{A_{CEM}}{d_{CEM}}\sigma(V_{gs})(V_{DD} - I_{ds}R_{ds})$$

$$I_{ds}(V_{gs,}\, V_{ds,}t) = \frac{\frac{A_{CEM}}{d_{CEM}}\sigma(V_{gs})V_{DD}}{1+\frac{A_{CEM}}{d_{CEM}}\sigma(V_{gs})R_{ds}} \qquad (7)$$

wherein I_{ds} represents a current through a transistor, such as transistor 510, wherein V_{ds} represents a voltage across a transistor, such as across source and drain terminals 511 and 512 of transistor 510, and wherein V_{gs} represents a voltage applied to a transistor, such as across gate and source terminals 513 and 511 of transistor 510, in an embodiment. Additionally, R_{ds} represents a resistance of a transistor, such as between drain and source terminals 512 and 511 of transistor 510.

[0054] As may be seen in expressions (7) above, a current through a CEM of a CES device, such as CES 520, may depend at least in part on a voltage, such as V_{DD} 540, applied across both a transistor, such as transistor 510, and a CES device, such as CES 520, and may also depend, at least in part, on a voltage, such as V_g 530, applied to a terminal of a transistor, such as gate terminal 513 of transistor 510. Therefore, a Mott transition inside a CEM of a CES device, such as CES 520, may be controlled and/or determined at least in part via voltages and/or characteristics of a transistor, such as transistor 510, in an embodiment. For example, a voltage drop across a transistor, such as V_{ds} of transistor 510, may be reduced and/or increased depending on a voltage, such as V_g 530, applied to a terminal, such as gate terminal 513, of a transistor, such a transistor 510. Similarly, a voltage, such as V_g 530, applied to a terminal, such as gate terminal 513, of a transistor, such a transistor 510, may control an injection of holes and/or electrons in a CEM of a CES device, such as CES 520. Additionally, in an embodiment, a critical voltage for a CEM of a CES device, such as CES 520, may be set at least in part by a voltage across a transistor, such as V_{ds} across source and drain terminals 511 and 512 of transistor 510, and/or by a voltage, such as V_{DD} 540, applied across both a transistor, such as transistor 510, and a CES device, such as CES 520. For example, a critical voltage for CES 520 may be determined, at least in part, by V_{ds} of transistor 510 and/or by V_{DD} 540. Similarly, for example, a critical current may be

determined, at least in part, by V_g 530 applied to gate terminal 513 of transistor 510, in an embodiment.

[0055] Expression (8) provided below represents a special case of expression (7) provided above when σ is relatively large, such as when a CEM is placed in a conductive/lower impedance state.

$$I_{ds}(V_{gs,} V_{ds,}t) \sim \frac{V_{DD}}{R_{ds}(V_{gs,} V_{ds,}t)} \quad (8)$$

[0056] For situations in which σ is relatively large, such as when a CEM of a CES device is placed in a conductive/lower impedance state, current may pass through a CES device, such as CES 520, with little voltage drop. Therefore, as can be seen from expression (8), current flowing through a CES device, such as CES 520, may depend, at least in part, on a voltage, such as V_{DD} 540, applied to a transistor, such as transistor 510, and on a resistance of the transistor, such as R_{ds} of transistor 510, in an embodiment. This situation where the resistance of a transistor, such as transistor 510, largely determines the amount of current flowing through a CES device, such as CES 520, may occur when the resistance of the transistor is significantly greater than the resistance of the CES device while the CES device is in a conductive/lower impedance state, for example.

[0057] Expression (9) provided below represents a special case of expression (7) above when σ is relatively small, such as when a CEM is placed in an insulative/higher impedance state.

$$I_{ds}(V_{gs,} V_{ds,}t) \sim \frac{A_{CEM}}{d_{CEM}} \sigma(V_{gs}) V_{ds} \quad (9)$$

[0058] For situations in which σ is relatively small, such as when a CEM of a CES device is placed in an insulative/higher impedance state, current through a transistor, such as transistor 510, may be substantially controlled and/or determined by a resistance of a CEM of a CES device, such as CES 520. In such a situation, V_{DD} 540 may approximate V_{ds} due at least in part to a larger voltage drop across CES 520, in an embodiment.

[0059] Continuing with an example embodiment of a compound device, such as compound device 500, comprising a transistor, such as transistor 510, coupled to a

CES, such as CES 520, FIG. 6 shows an example plot 600 depicting an example current vs. voltage curve for a CES device, such as CES device 520. For example plot 600, a critical current 621 corresponding to a particular area size of a CEM of a CES device, such as CES 520, is shown. A second critical current 622 corresponding to a second particular area size of a CEM of a CES device, such as CES 520, is also depicted. For example plot 600, a CEM area corresponding to critical current 622 is greater than a CEM area corresponding to critical current 621. Thus, example plot 600 shows that an increase in CEM area may result in an increase in critical current, thereby affecting switching behavior of a CES device, such as CES 520, and by extension the switching behavior of a compound device, such as compound device 500.

[0060] As previously discussed, for a Mott transition to occur, both a critical current and a critical voltage need to be achieved in a CEM of a CES device, such as CES 520. For the example depicted in plot 600, for the smaller CEM area corresponding to critical current 621, a critical current and critical voltage are achieved, and a Mott transition occurs, at point 601. For the larger CEM area corresponding to critical current 622, a critical current and critical voltage are achieved at point 602. Of course, claimed subject matter is not limited in scope to the specific examples described herein.

[0061] Continuing with an example embodiment of a compound device, such as compound device 500, comprising a transistor, such as transistor 510, coupled to a CES, such as CES 520, FIG. 7 shows an example plot 700 depicting example current vs. voltage curves, such as curves 701-704, for a CES device, such as CES device 520. The various example curves, such as curves 701-704, may represent current vs. voltage characteristics corresponding to different voltages, such as different values of V_g 530, that may be applied to a terminal, such as gate terminal 513, of a transistor, such a transistor 510, of a compound device, such as compound device 500, in an embodiment. For the example depicted in plot 700, curve 704 corresponds to a V_g 530 that may exceed a V_g 530 for curve 703. Similarly, curve 703 corresponds to a V_g 530 that may exceed a V_g 530 for curve 702, and curve 702 corresponds to a V_g 530 that may exceed a V_g 530 for curve 701. A critical current value 720 is depicted, along with a critical voltage value 710. As described previously, to trigger a set and/or reset condition, that is, to trigger a Mott transition, both the critical current and the critical voltage must be achieved within a CEM of a CES device, such as CES 520, for example.

[0062] For the example depicted in plot 700 of FIG. 7, a V_g 530 corresponding to example curve 701 would be insufficient to trigger a set and/or reset condition because critical current value 720 is never reached. However, a V_g 530 corresponding to example curves 702, 703, and/or 704 would be sufficient to cause a set and/or reset condition to occur. Further, as explained in more detail below, different values for V_g 530, for example, may result in different values for R_{sd} and I_{ds}. Additionally, there may also be relatively small changes in critical voltage for set and/or reset conditions if different compliance currents are utilized.

[0063] FIG. 8 is an example plot 800 depicting several example current vs. voltage curves representative of data collected for different example values of V_g 530 for a set condition, or, in other words, a transition from a higher impedance state to a lower impedance state for an example CES, such as CES 520 of a compound device, such as example compound device 500. As mentioned previously, a compliance current may be externally applied to a CES, such as CES 520. As depicted in example plot 800 of FIG. 8, V_g, such as V_g 530, may be utilized to dynamically change the compliance. Also, for the examples depicted in FIG. 8, a set condition for V_g=0.7V may not have been achieved because the critical criteria for a Mott transition was not reached.

[0064] FIG. 9 is an example plot 900 depicting several example current vs. voltage curves representative of data collected for different values of V_g 530 for a reset condition, or, in other words, a transition from a conductive/lower impedance state to an insulative/higher impedance state for an example CES, such as CES 520 of a compound device, such as example compound device 500. As also mentioned previously, and as depicted in example plot 800, a compliance current may set the number of electrons in a CEM of a CES device, such as CES 520, which may determine the amount of holes to be injected for a reset condition (i.e., a Mott transition from a conductive/lower impedance state to an insulative/higher impedance state). As may be seen in example plot 900 depicted in FIG. 9, different values for V_g applied during a set condition may yield different current vs. voltage curve characteristics for a reset condition, in an embodiment. Also note that there is no reset depicted for V_g=0.7V because the device result depicted in 800 did not set at 0.7V as it did not reach the critical criteria for the Mott transition, as mentioned above.

[0065] As discussed previously in connection with FIG. 3, a current and/or current density applied during a write operation to place a CES, such as CES 520, in a conductive/lower impedance state (i.e., a set condition) may determine a compliance condition for placing the CES, such as CES 520, in an insulative/higher impedance state (i.e, a reset condition) in a subsequent write operation. As depicted in FIG. 3, a CEM of a CES device, such as CES 520, may be subsequently placed in an insulative/higher impedance state (i.e., a reset condition) by application of a current density $J_{reset} \geq J_{comp}$ at a voltage V_{reset}, wherein J_{comp} may be externally applied, in an embodiment.

[0066] Therefore, a compliance current, such as may be externally applied via V_{gs} 530, may determine a number of electrons in a CEM of a CES device, such as CES 520, which are to be "captured" by electron holes for the Mott transition for a reset condition. In other words, a current applied in a write operation to place a CES device in a conductive/lower impedance state may determine a number of holes to be injected to the CEM of the CES device for subsequently transitioning the CEM of the CES to an insulative/higher impedance state. Also, for an embodiment, after reset, the system may lose memory of any previous compliance, and the compliance condition may need to be reapplied during a subsequent set condition. This behavior is depicted in FIGs. 8 and 9, described above.

[0067] FIG. 10 is a schematic diagram depicting an embodiment 1000 of an example compound device comprising a CES device, such as CES 1020, coupled to a diode, such as diode 1010. In an embodiment, diode 1010 may comprise a current and/or voltage source, along with a voltage, such as V_{DD} 1030, applied across both diode 1010 and CES 1020. Characteristics of behavior for a compound device, such as compound device 1000, comprising a diode, such as diode 1010, may be described by expression (10), below.

$$I_{diode}(V_{CE}, t) = I_O\,(e^{\frac{V_{CE}}{nV_t}} - 1)$$

$$I_{diode}(V_{CE}, t) = \frac{A_{CEM}}{d_{CEM}}\sigma V_{CEM}$$

$$V_{CEM} = V_{DD} - V_{ce} = V_{DD} - I_{diode}R_{diode} \qquad (10)$$

wherein V_{ce} represents a voltage across terminals, such as terminals 1011 and 1012, of a diode, such as diode 1010.

[0068] FIG. 11 depicts an example plot 1100 including an example current vs. voltage curve 1102 representative of data collected for an example set condition and an example curve 1103 representative of data collected for an example reset condition. Example curve 1101 depicts example current vs. voltage data for a diode-only, such as may be observed across terminals 1011 and 1012 of diode 1010 of example compound device 1000, for example. As depicted in example plot 1100, utilization of a diode, such as diode 1010, as a current and/or voltage source for a compound device, such as compound device 1000, results in a shifting of both Diode/CES – Reset 1103 (V_{reset}) and Diode/CES – Set (V_{set}) due to a voltage drop across the diode. For example, a diode, such as diode 1010, needs to turn on before a critical voltage can be developed across a CES device, such as CES 1020, and before a critical current can be developed so that switching can occur.

[0069] As mentioned previously, for a compound device, such as compound device 1000, a CES device, such as CES 1020, may adopt characteristic behavior of a current and/or voltage source, such as diode 1010, in an embodiment. In an embodiment, current through a CES device, such as CES 1020, may be dependent on a voltage, such as V_{ce}, across terminals, such as terminals 1011 and 1012, of a diode, such as diode 1010. In an embodiment, a voltage, such as V_{ce}, across terminals, such as terminals 1011 and 1012, of a diode, such as diode 1010, may set a critical voltage and critical current for a compound device, such as compound device 1000. Expression (11) below represents a special case of expression (10) when σ is relatively large, such as when a CEM is placed in a conductive/lower impedance state.

$$I_{diode}(V_{ce}) \sim \frac{V_{DD}}{R_{diode}(V_{ce})} \qquad (11)$$

[0070] Expression (12) below represents a special case of expression (10) when σ is relatively small, such as when a CEM is placed in an insulative/higher impedance state.

$$I_{diode}(V_{ce}) \sim \frac{A_{CEM}}{d_{CEM}} \sigma V_{DD} \qquad (12)$$

[0071] For situations in which σ is relatively large, such as when a CEM of a CES device is placed in a conductive/lower impedance state, a current through a CES device, such as CES 1020, may be dominated by the diode, such as diode 1010. For situations in which σ is relatively small, such as when a CEM of a CES device, such as CES 1020, is placed in an insulative/higher impedance state, the current through the CES device, such as CES 1020, may be determined mainly by the resistance of a diode, such as diode 1010. As compared with example compound device 500 comprising a transistor 510, the possible behavioral options for example compound device 1000, comprising diode 1010, are more limited. This is due mainly to the fact that V_{ce} is the only voltage that can be varied for a compound device implementing a diode as a current/voltage source, in an embodiment.

[0072] As mentioned above, a CES device, also referred to as a variable impeder device, such as variable impeder device 100, may be implemented in a wide range of electronic device types. For example, a variable impeder device, such as variable impeder device 100, may be utilized in logic circuits, memory circuits, filter circuits, etc. Generally speaking, a variable impeder device, such as variable impeder device 100, may be utilized in any circuit or device, presently existing or to exist in the future, that may benefit from the variable impeder device's variable resistance and/or variable capacitance characteristics.

[0073] For example, in an embodiment, a CES device, such as variable impeder device 100, may be implemented in a memory cell, for example. In one or more embodiments, a CES memory may comprise: a variable impeder memory cell including a CES; a write circuit for placing the variable impeder memory cell in a first impedance state or a second impedance state depending on signals provided to the memory device; and a read circuit for sensing an impedance state of the memory cell and providing an electrical signal corresponding to the sensed state of the memory cell. In one aspect, an impedance of a CES in the second memory cell state may be significantly greater than the impedance in the first memory cell state.

[0074] FIG. 12 is a schematic diagram of an example architecture for a CES memory cell 1200 according with an embodiment. In an embodiment, a CES memory cell may comprise one or more memory elements (e.g., non-volatile memory elements) comprising a CES device, such as CES 1210. In this context, a "memory cell" as

referred to herein comprises a circuit or portion of a circuit capable of representing a value, symbol or parameter as a state. For example, a memory cell may comprise one or more memory devices that capable of representing a value, symbol or parameter as an impedance state of the memory device. For example, a memory element, such as CES 1210, may be placed in a particular memory state (e.g., a lower impedance state or higher impedance state) by independently controlling voltage and current applied across terminals of the memory element in a "write operation." In an embodiment, such a write operation may be executed by application of a signal which is controlled to provide a critical current and voltage across terminals of CES 1210 to place CES 1210 in a particular impedance state. In another aspect, an impedance state of a memory element, such as CES 1210, may be detected or sensed in a "read operation" by applying a read enable voltage signal 1203 to close switch transistor 1230, and applying a wordline voltage signal 1202 to close transistor 1220 to connect a voltage at node 1205 to a bitline 1201. In an embodiment, a sense circuit (not shown) may detect an impedance state of CES 1210 based on a magnitude of current from bitline 1201 through transistor 1220 in a read operation. An output signal may have a voltage that is indicative of a current impedance state memory cell 1200 (e.g., as a "1," "0" or other symbol), in an embodiment. Of course, claimed subject matter is not limited in scope in these respects.

[0075] In one or more embodiments wherein a CES device is utilized, at least in part, as a memory cell and/or circuitry associated with a memory cell, advantages may be realized as compared to memory circuits incorporating conventional and/or prior memory technologies. For example, as a result of improved device reliability and/or improved endurance, needs for wear-leveling and/or error correcting circuitry may be reduced, and costs may also be reduced. Additionally, because a wide range of metal and/or conductive materials that may be used to form contacts in a CES device, ease of manufacture may be greatly improved. Further, in an embodiment, processing temperatures may relatively low, making CES devices easier to process. Also, performance for a CES device may be extremely quick as compared to prior and/or conventional memory technologies due to switch events occurring in distances less than a Thomas Fermi screening length, for example. Additionally, the lack of a filament such as may be formed in some resistive memory technologies may lead to improved performance and/or reliability. Of course, these are merely example advantages that a

CES device may have over prior and/or conventional memory technologies, and claimed subject matter is not limited in scope in these respects.

[0076] FIG. 13 is a schematic diagram depicting an example active low-pass filter 1300 comprising a variable impeder device 1310 in a feedback path of an operational amplifier 1320. In an embodiment, variable impeder device 1310 may be switched between two or more impedance states, thereby altering amplification characteristics of operational amplifier 1320 and/or frequency response characteristics of an output signal at node 1303 in reference to an input signal received at node 1301 through resistor 1330. In an embodiment, the variable capacitance characteristics of a variable impeder device, such as variable impeder device 1310, may provide a variable higher-frequency roll-off aspect to low-pass filter 1300. That is, by altering the capacitance characteristics of variable impeder device 1310 through switching between two or more distinct impedance states, the frequency response low-pass filter 1300 may be altered. Of course, claimed subject matter is not limited in scope in these respects.

[0077] Although variable impeder devices are described herein as being implemented in example memory and/or low-pass filter circuits, claimed subject matter is not limited in scope in this respect. Embodiments in accordance with claimed subject matter may implement variable impeder devices in any electronic circuit, whether currently existing or to exist in the future, for example that may benefit from the variable resistance and/or variable capacitance characteristics of a variable impeder device.

[0078] As described previously, in an embodiment, a voltage may be applied to a CEM of a CES device. Also, in an embodiment, at least one of a current density and/or a current within the CEM may be measured, and an impedance state of the CES dependent on the measured current and/or current density may be determined. In an embodiment, the impedance state may be dependent on a combination of a capacitance and a resistance of the CEM. Further, in an embodiment, the impedance state may comprise one of a plurality of impedance states, wherein a first of the plurality of impedance states has a lower impedance than a second of the plurality of impedance states. In an embodiment, the first impedance state may have a lower resistance and a lower capacitance, and the second impedance state may have a higher resistance and a higher capacitance. Additionally, in an embodiment, a ratio of impedances of the plurality of impedance states may be proportional to a physical property of the CEM. The physical property of the CEM may include, for

example, a Thomas Fermi screening length and/or a Bohr radius. Also, in an embodiment, individual impedance states of the plurality of impedance states may be associated with a data value. Further, a difference in current between the first impedance state and the second impedance state at a determined voltage may provide an indication of a read window, in an embodiment.

[0079] As also described previously, in an embodiment, a plurality of electrons may be provided to a CEM of a CES device such that the CES enters a first impedance state, and a plurality of holes may be provided to the CEM such that the CES enters a second impedance state. Also, in an embodiment, the plurality of electrons may cause a voltage across the CEM to be greater than a set voltage threshold, and the plurality of holes may cause the voltage across the CEM to be equal to or greater than a reset voltage threshold. Additionally, the voltage across the CEM may cause a current density in the CEM to be equal to or greater than a set current density and/or a set current, and the voltage across the CEM may cause the current density in the CEM to be equal to or greater than a reset current density and/or a reset current, in an embodiment. Further, in an embodiment, a set voltage across the CEM and a set current density through the CEM may be exceeded, and a reset voltage across the CEM and a reset current density through the CEM may be exceeded, in an embodiment. Also, in an embodiment, individual impedance states may be associated with a data value. Additionally, at least one of the reset voltage, the set voltage, and a difference between the set voltage and the reset voltage may be proportional to a physical property of the CEM, wherein the physical property of the CEM may include at least one of a strong electron potential due to localization and/or a correlation of the electrons, in an embodiment. Further, in an embodiment, the difference between the set voltage and the reset voltage may provide an indication of a size of at least one of a write window and/or a programming window.

[0080] In a further embodiment, as described previously, a plurality of electrons may be provided to a CEM of a CES device such that a current and/or current density within the CEM exceeds a first threshold and a voltage across the CEM exceeds a second threshold. Further, in an embodiment, switching from a first impedance state to a second impedance state may result from the current and/or current density exceeding the second threshold. The first impedance state may have a higher resistance and a higher capacitance, and the second impedance state has a lower resistance and a lower capacitance, in an embodiment. Additionally, the first threshold may be dependent on at least one of a current and/or current

density required to enable a Mott transition in the CEM, a voltage required to inject electrons over a metal insulator barrier within the CEM, and/or a voltage greater or equal to twice the band-splitting potential, in an embodiment.

[0081] An another embodiment, a plurality of electrons may be provided to a CEM of a CES device such that a concentration of electrons within the CEM exceeds a threshold, and a switching from a first impedance state to a second impedance state may occur as a result of the concentration of electrons exceeding the threshold for a Mott transition. Further, in an embodiment, at least one of the plurality of electrons may be recombined with at least one of a plurality of holes within the CEM to enable the switching from the first impedance state to the second impedance state. In an embodiment, the concentration of the plurality of electrons and/or holes may be dependent at least in part on at least one physical property associated with the CEM. The at least one physical property may include, for example the Bohr radius. Further, in an embodiment, the threshold may be dependent at least in part on a current and/or current density required to enable the Mott transition. Also, in an embodiment, a resistance and/or capacitance (or impedance) of the CEM may be substantially different, such as as a result of the Mott transition, for example. Additionally, a switching from the first impedance state to the second impedance state may be caused by a disproportionation reaction, in an embodiment.

[0082] As discussed above, a CEM of a CES device may be provided with a plurality of holes such that a concentration of holes within the CEM exceeds a threshold, and switching from a first impedance state to a second impedance state may occur as a result of the concentration of holes exceeding the threshold, in an embodiment. The first impedance state may comprise a lower resistance, lower capacitance state, and the second impedance state may comprise a higher resistance, higher capacitance state, for example. Also, in an embodiment, the threshold may depend, at least in part, on at least one of a current and/or current density required to enable a Mott-like transition within the CEM, and/or a voltage greater or equal to the band-splitting potential. Additionally, in an embodiment, the threshold may be dependent on a current and/or currently density required to enable a Mott-like transition. In an embodiment, at least one of the plurality of holes may be recombined with a respective at least one of a plurality of electrons within the CEM to enable switching from the first impedance state to the second impedance state. Also, a concentration of the plurality of electrons and/or holes may be dependent at least in part on at least one physical property associated with the CEM. The at least one physical property may include, for example, a

Thomas Fermi screening length. Further, in an embodiment, the switching from the first impedance state to the second impedance state may be caused by a disproportionation reaction. Also, in an embodiment, resistance and/or capacitance of the CEM may be substantially different, such as between the first impedance state and the second impedance state, for example.

[0083] As also discussed previously, a variable impeder device may comprise a CEM capable of operating in a first impedance state and a second impedance state. In an embodiment, the first impedance state may comprise a lower resistance, lower capacitance state, and the second impedance state may comprise a higher resistance, higher capacitance state. Also, in an embodiment, a change in the capacitance may be dependent on at least one material property associated with the CEM. In an embodiment, the CEM may comprises one or more of: one or more transition metal oxides, one or more rare earth oxides, one or more oxides of one or more f-block elements of the periodic table, one or more rare earth transitional metal oxide perovskites, yttrium, and/or ytterbium. Additionally, in an embodiment, a transition from the first impedance state to the second impedance state of the variable impeder device may depend at least in part on an applied critical bias and a critical current/current density.

[0084] In the preceding description, various aspects of claimed subject matter have been described. For purposes of explanation, specifics, such as amounts, systems and/or configurations, as examples, were set forth. In other instances, well-known features were omitted and/or simplified so as not to obscure claimed subject matter. While certain features have been illustrated and/or described herein, many modifications, substitutions, changes and/or equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all modifications and/or changes as fall within claimed subject matter.

CLAIMS

What is claimed is:

1. A method, comprising:

providing a plurality of electrons to a correlated electron material of a correlated electron switch device such that the correlated electron material enters a first impedance state; and

providing a plurality of holes to the correlated electron material such that the correlated electron material enters a second impedance state.

2. The method of claim 1, wherein the providing the plurality of electrons to the correlated electron material causes a voltage across the correlated electron material to be greater than a set voltage, and/or wherein the providing the plurality of holes to the correlated electron material causes the voltage across the correlated electron material to be equal to or greater than a reset voltage.

3. The method of claim 2, wherein the voltage across the correlated electron material produces a current density in the correlated electron material equal to or greater than a set current density and/or a set current threshold, and/or wherein the voltage across the correlated electron material produces the current density in the correlated electron material equal to or greater than a reset current density and/or a reset current threshold.

4. The method of claim 2 or claim 3, further comprising exceeding the set voltage across the correlated electron material and a set current density through the correlated electron material, and/or exceeding the reset voltage across the correlated electron material and a reset current density through the correlated electron material.

5. The method of any preceding claim, wherein the first impedance state represents a first data value and wherein the second impedance state represents a second data value.

6. The method of any of claims 2 to 5, wherein at least one of the reset voltage, the set voltage, and/or a difference between the set voltage and the reset voltage are proportional to one or more physical properties of the correlated electron material.

7. The method of claim 6, wherein the one or more physical properties of the correlated electron material comprise one or more of a strong electron potential due to localization and/or a correlation of electrons, and wherein a difference between the set voltage and the reset voltage indicates a size of at least one of a write window and/or a programming window.

8. The method of any preceding claim, further comprising switching between the first impedance state and the second impedance state at least in part by a disproportionation reaction.

9. The method of any preceding claim, further comprising controlling a current through the correlated electron material at least in part by dynamically applying an external compliance condition based, at least in part, on an external current limited during a write operation to place the correlated electron material in the first impedance state.

10. A method, comprising:

applying a voltage to a correlated electron material; and

determining an impedance state of the correlated electron material at least in part by measuring a current density and/or a current within the correlated electron material.

11. The method of claim 10, wherein the impedance state depends at least in part on a combination of resistance and capacitance of the correlated electron material.

12. The method of claim 11, wherein the determining the impedance state of the correlated electron material comprises determining one of a plurality of impedance states, wherein the plurality of impedance states comprises a first impedance state and a second impedance state, wherein the first impedance state comprises an impedance lower than an impedance for the second impedance state.

13. The method of claim 12, wherein the first impedance state comprises a lower resistance and a lower capacitance for the correlated electron material, and wherein the second impedance state comprises a higher resistance and a higher capacitance for the correlated electron material.

14. The method of claim 13, wherein a ratio of impedances for the first and second impedance states is proportional to a physical property of the correlated electron material.

15. The method of claim 14, wherein the physical property of the correlated electron material is one or more of a Thomas Fermi screening length and/or a Bohr radius.

16. The method of any of claims 10 to 15, wherein the first impedance state represents a first data value and the second impedance state represents a second data value, and wherein a difference in current between the first impedance state and the second impedance state at a determined voltage indicates a read window.

17. An apparatus, comprising:

a variable impeder device comprising a correlated electron material capable of operating in a first impedance state and a second impedance state.

18. The apparatus of claim 17, wherein the first impedance state comprises a lower resistance, lower capacitance state, and wherein the second impedance state comprises a higher resistance, higher capacitance state.

19. The apparatus of claim 18, wherein a change in capacitance of the variable impeder between the first impedance state and the second impedance state to depend at least in part on one or more material properties of the correlated electron material.

20. The apparatus of claim 18 or claim 19, wherein a transition from the first impedance state to the second impedance state of the variable impeder device to depend at least in part on an applied critical bias and a critical current/current density.

21. The apparatus of any of claims 18 to 20, further comprising one or more current and/or voltage sources, wherein to transition from the first impedance state to the second impedance state, the one or more current and/or voltage sources to provide the correlated electron material with a plurality of holes such that a concentration of holes within the correlated electron material exceeds a threshold.

22. The apparatus of claim 21, wherein to transition from the first impedance state to the second impedance state, at least one of the plurality of holes to recombine with a respective at least one of a plurality of electrons within the correlated electron material.

23. The apparatus of claim 22, wherein to transition from the second impedance state to the first impedance state of the variable impeder device, the one or more current and/or voltage sources to provide the correlated electron material with a plurality of electrons such that a current and/or current density within the correlated electron material exceeds a first threshold and/or a voltage across the correlated electron material exceeds a second threshold.

24. The apparatus of any of claims 17 to 23, wherein the correlated electron material comprises one or more of: one or more transition metal oxides, one or more rare earth oxides, one or more oxides of one or more f-block elements of the periodic table, one or more rare earth transitional metal oxide perovskites, yttrium, and/or ytterbium.

25. The apparatus of any of claims 17 to 24, wherein the variable impeder device comprises a memory cell.

26. The apparatus of any of claims 17 to 24, wherein the variable impeder device comprises at least a portion of a logic device.

27. The apparatus of any of claims 17 to 24, wherein the variable impeder device comprises at least a portion of a filter circuit.



FIG. 1b

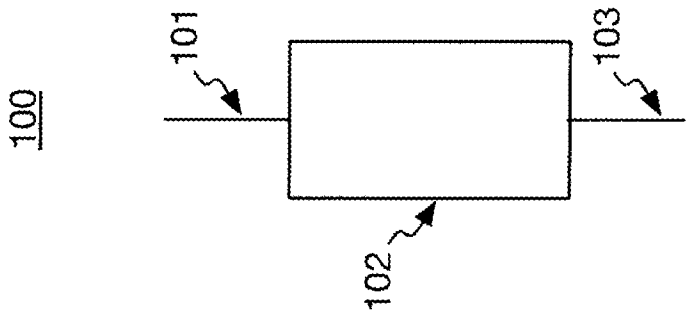


FIG. 1a

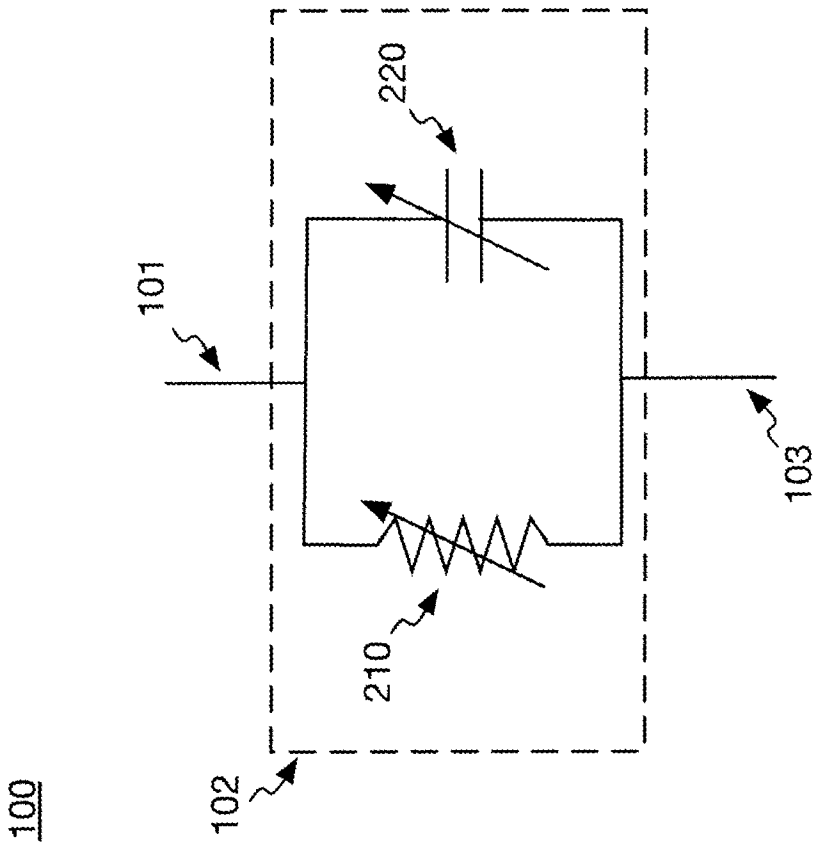


FIG. 2

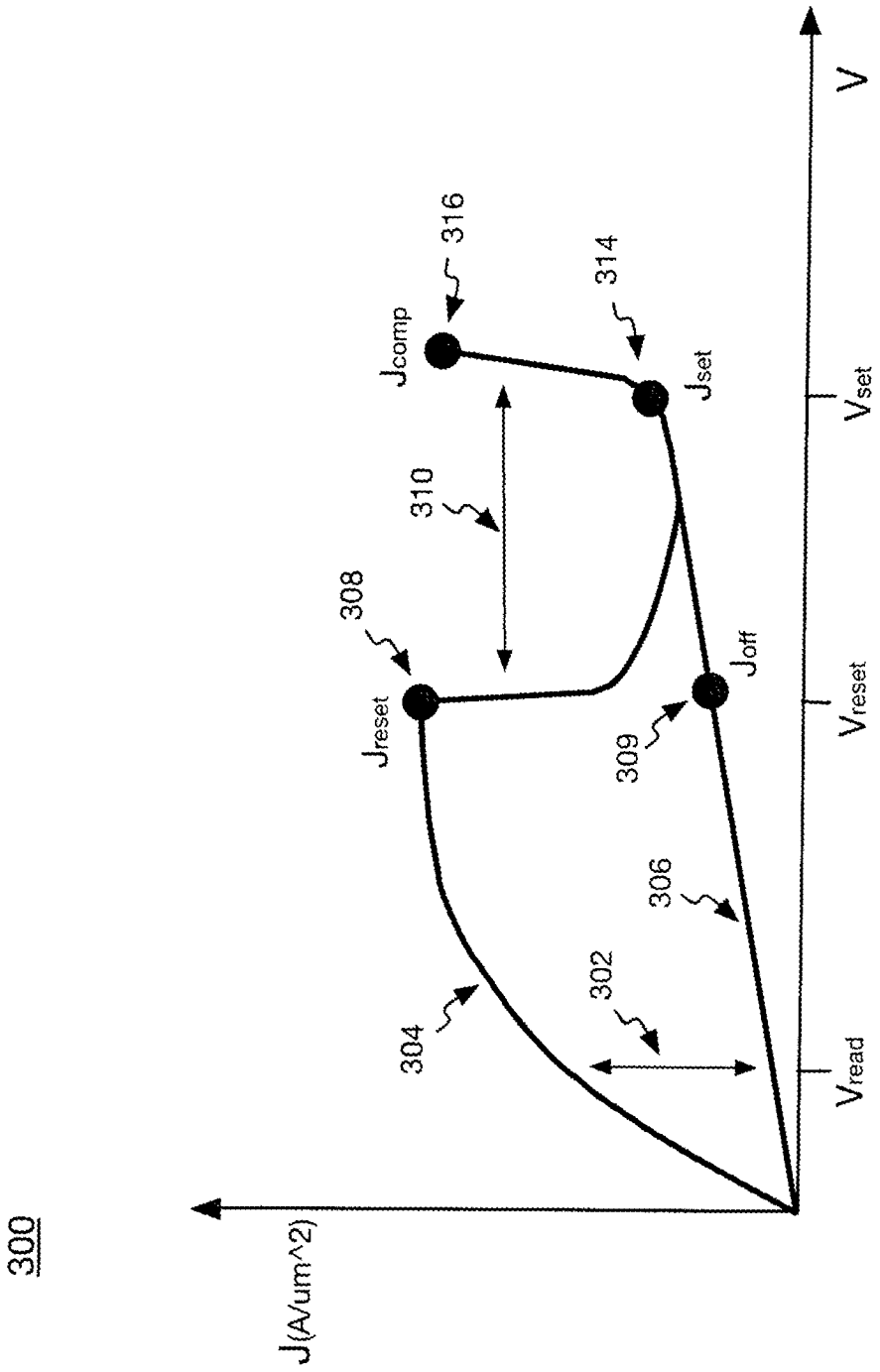
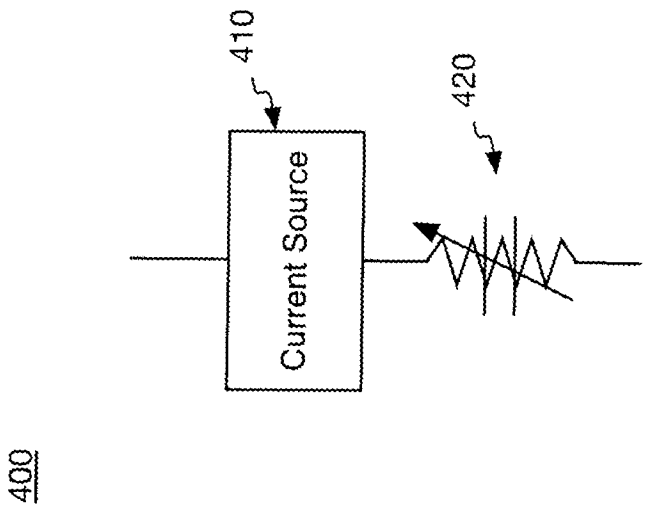

300
J(A/um^2)
V
Vread
Vreset
Vset
Jcomp
Jset
Jreset
Joff
302
304
306
308
309
310
314
316

FIG. 3

FIG. 4



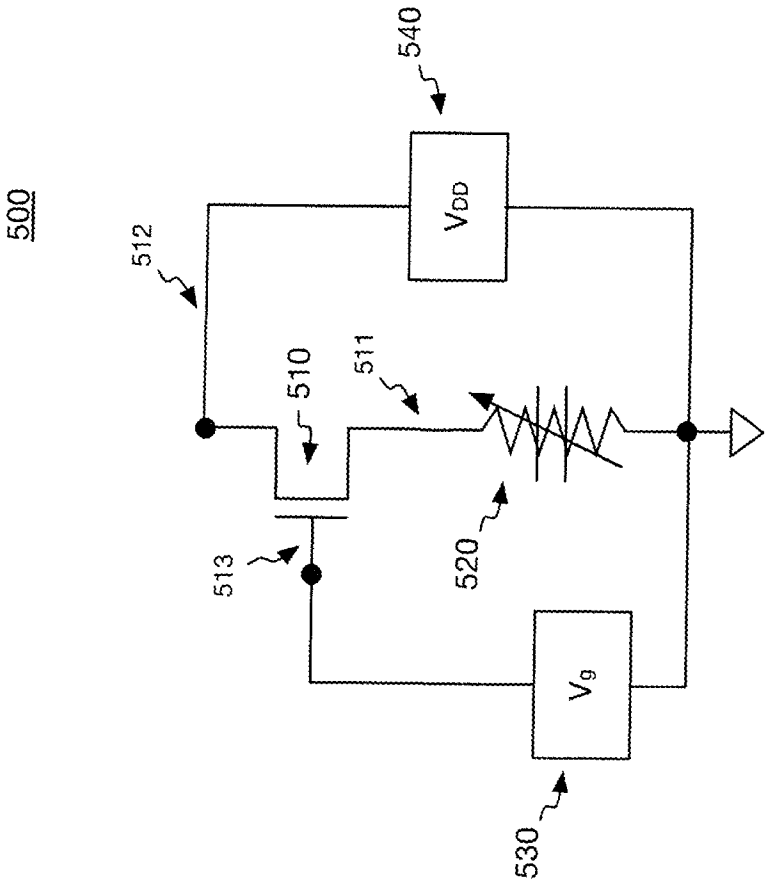


FIG. 5

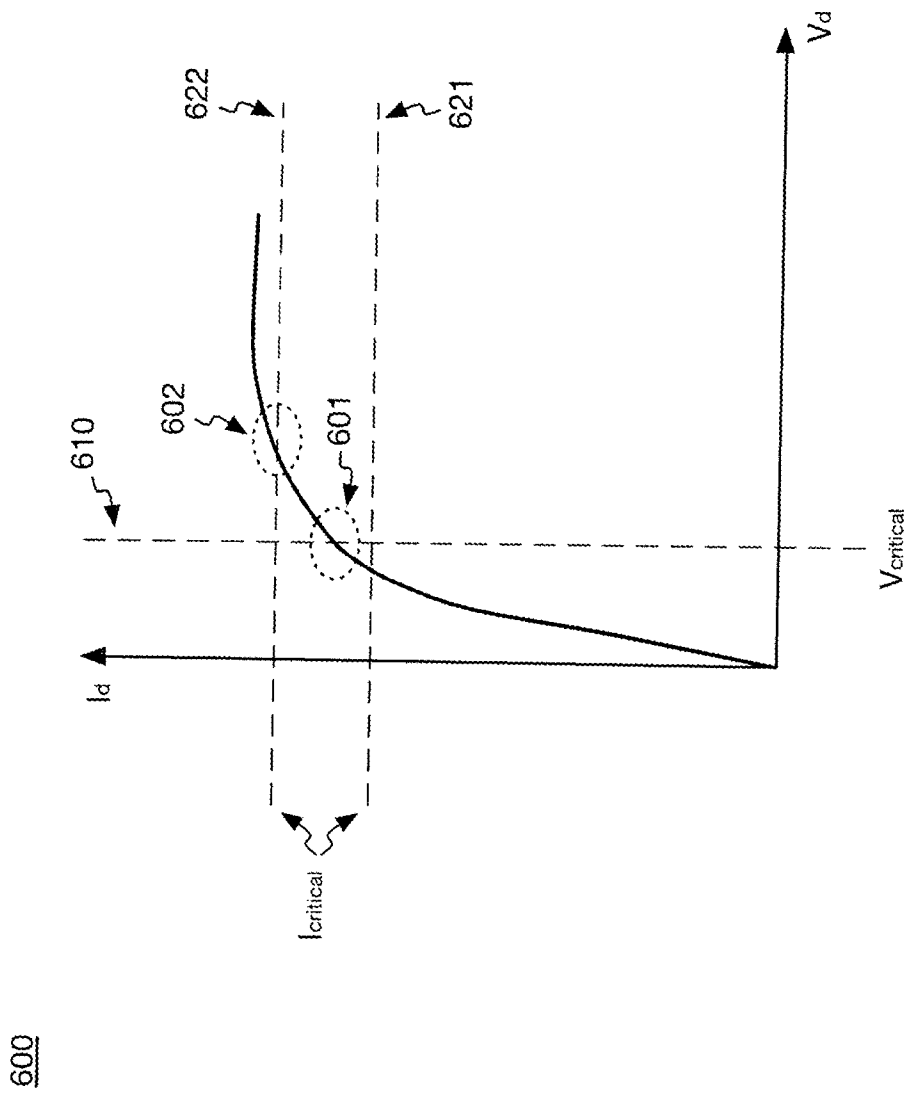


FIG. 6

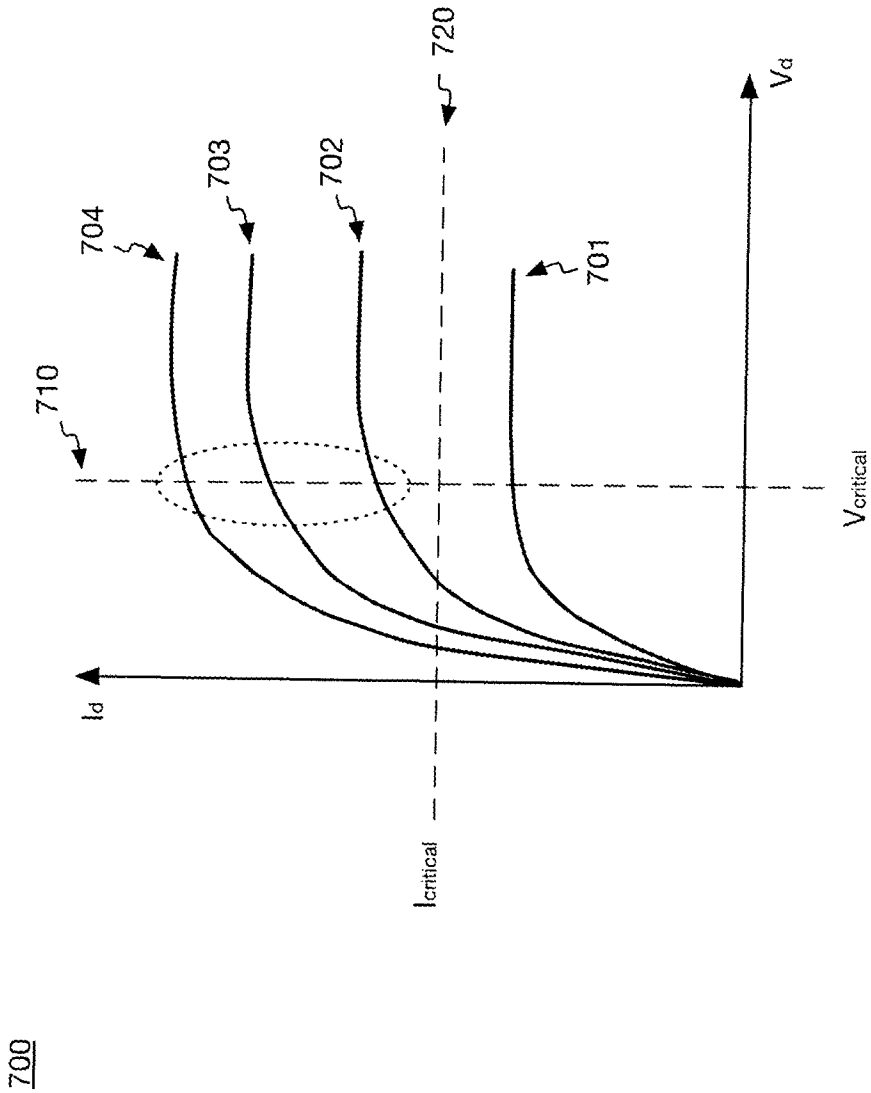


FIG. 7

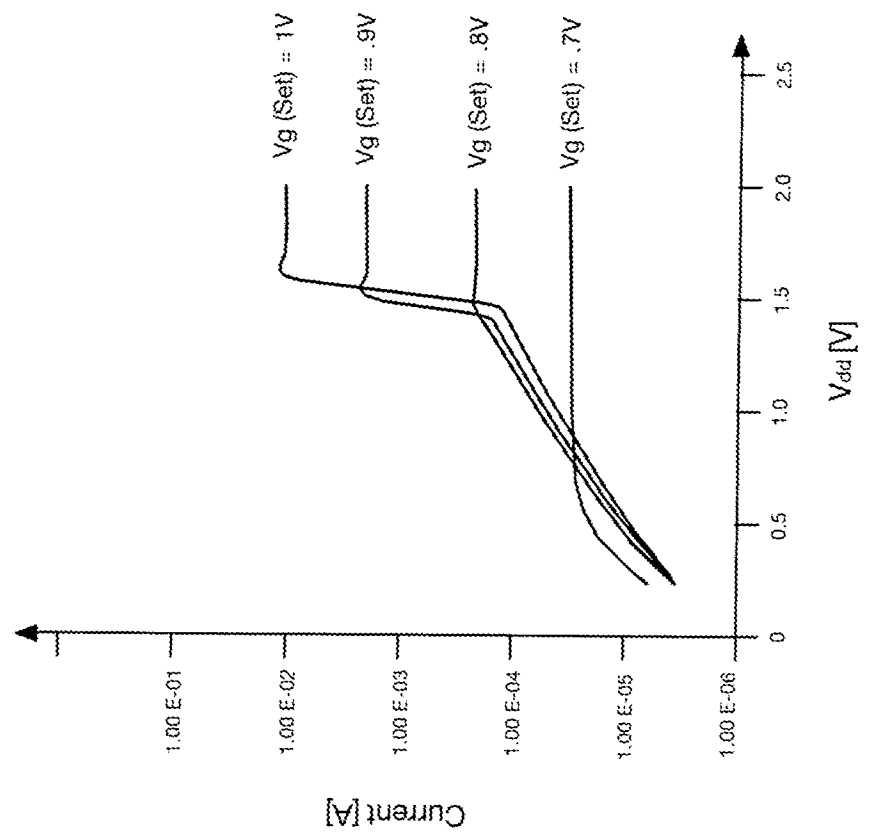

800
Vg (Set) = 1V
Vg (Set) = .9V
Vg (Set) = .8V
Vg (Set) = .7V
1.00 E-01
1.00 E-02
1.00 E-03
1.00 E-04
1.00 E-05
1.00 E-06
Current [A]
0
0.5
1.0
1.5
2.0
2.5
Vdd [V]

FIG. 8

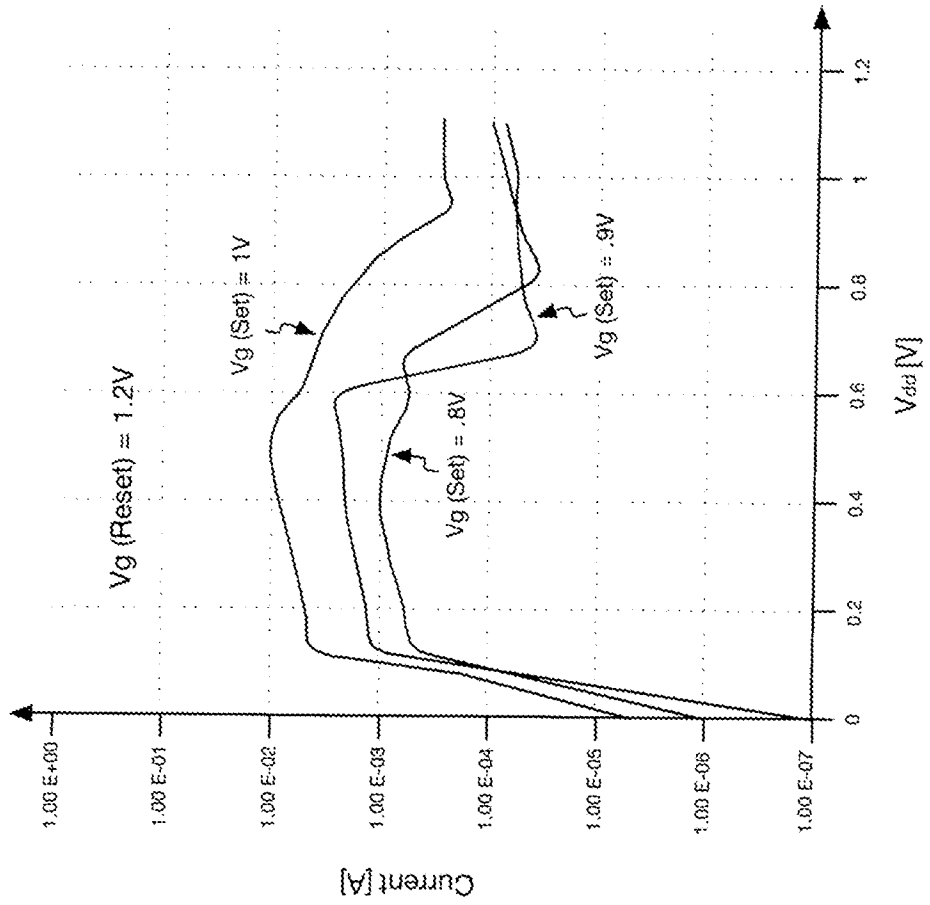

900
Vg (Reset) = 1.2V
Vg (Set) = 1V
Vg (Set) = .8V
Vg (Set) = .9V
Current [A]
1.00 E+00
1.00 E-01
1.00 E-02
1.00 E-03
1.00 E-04
1.00 E-05
1.00 E-06
1.00 E-07
0
0.2
0.4
0.6
0.8
1
1.2
V_{dd} [V]

FIG. 9

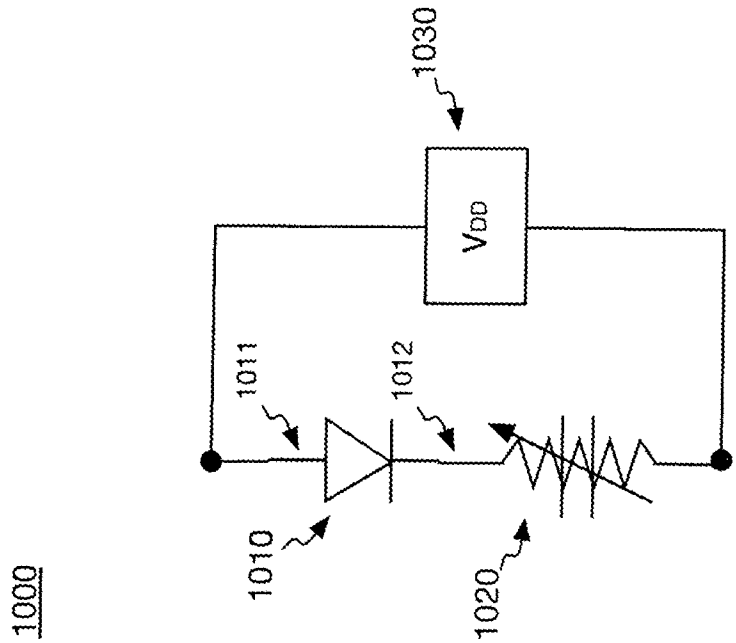


FIG. 10

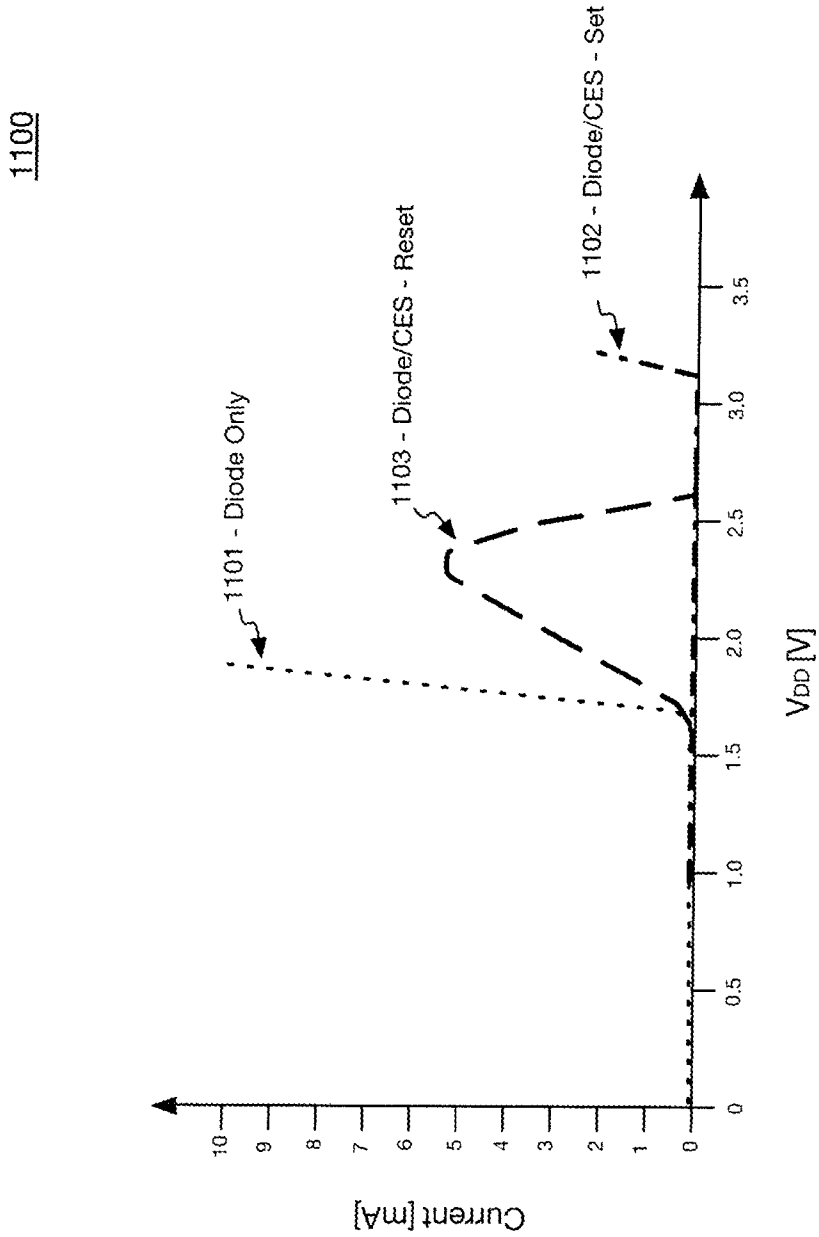

1100
1101 - Diode Only
1103 - Diode/CES - Reset
1102 - Diode/CES - Set
Current [mA]
0
1
2
3
4
5
6
7
8
9
10
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
VDD [V]

FIG. 11

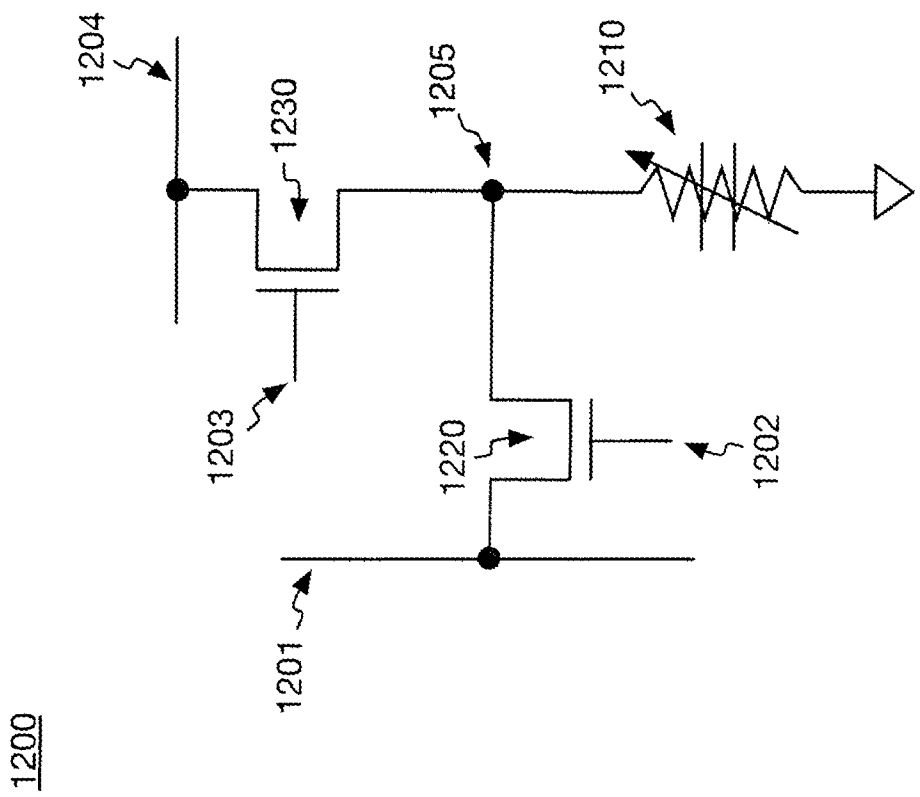


FIG. 12

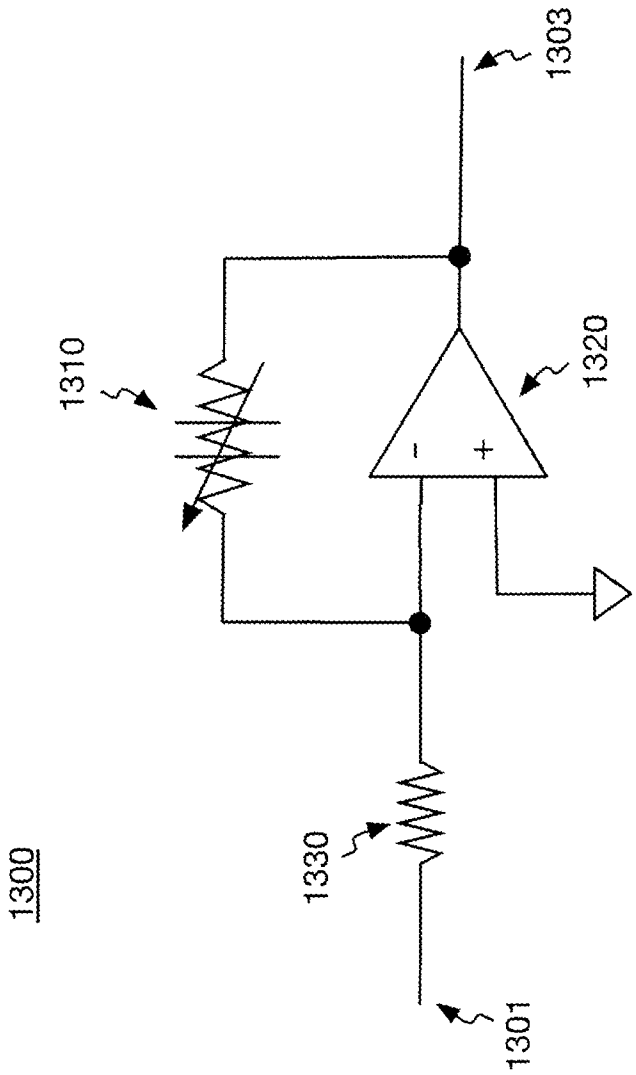


FIG. 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2016/052365

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L45/00 G11C13/00 H01L49/00 H03H7/01 H03K19/20
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G11C H03H H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CELINSKA JOLANTA ET AL: "Material and process optimization of correlated electron random access memories", JOURNAL OF APPLIED PHYSICS, AMERICAN INSTITUTE OF PHYSICS, US, vol. 109, no. 9, 13 May 2011 (2011-05-13), pages 91603-91603, XP012148990, ISSN: 0021-8979, DOI: 10.1063/1.3581197 page 2, left-hand column, line 6 - page 6, right-hand column, line 24; figures 1,3,6-8	1-25
X	WO 2008/058264 A2 (SYMETRIX CORP [US]; PAZ DE ARAUJO CARLOS A [US]; BRUBAKER MATTHEW D [U) 15 May 2008 (2008-05-15) page 17, line 15 - page 18, line 9; figures 1,2 page 42, line 13 - line 30; figures 31-33	1-25

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 October 2016	20/10/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Gröger, Andreas

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2016/052365

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	INOUE I H ET AL: "Strong electron correlation effects in non-volatile electronic memory devices", NON-VOLATILE MEMORY TECHNOLOGY SYMPOSIUM, 2005 DALLAS, TX, USA 7-10 NOV. 2005, PISCATAWAY, NJ, USA,IEEE, 7 November 2005 (2005-11-07), pages 131-136, XP010854267, ISBN: 978-0-7803-9408-7 page 133, right-hand column, line 7 - page 134, right-hand column, line 29; figure 5	1-25
X	WO 2008/054055 A1 (KOREA ELECTRONICS TELECOMM [KR]; LIM JUNGWOOK [KR]; YUN SUN-JIN [KR];) 8 May 2008 (2008-05-08) paragraph [0044] - paragraph [0051]; figures 1,2 paragraph [0003]	1-4, 6-23,26
X	WO 2006/088323 A1 (UTE ELECTRONICS & TELECOMMUNICATIONS RES INST [KR]; KIM HYUN-TAK [KR];) 24 August 2006 (2006-08-24) paragraph [0044] - paragraph [0046]; figure 2	1-4, 6-23,27
X	WO 2006/098560 A1 (KOREA ELECTRONICS TELECOMM [KR]; KIM HYUN-TAK [KR]; KANG KWANG-YONG [K) 21 September 2006 (2006-09-21) paragraph [0033] - paragraph [0039]; figure 1	1-4, 6-23,27

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2016/052365

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2008058264 A2	15-05-2008	BR PI0719055 A2	26-11-2013
		CN 101681911 A	24-03-2010
		EP 2082426 A2	29-07-2009
		JP 5156023 B2	06-03-2013
		JP 2010522424 A	01-07-2010
		KR 20090078370 A	17-07-2009
		WO 2008058264 A2	15-05-2008
WO 2008054055 A1	08-05-2008	NONE	
WO 2006088323 A1	24-08-2006	CN 101164166 A	16-04-2008
		EP 1851802 A1	07-11-2007
		JP 2008530815 A	07-08-2008
		KR 20060093266 A	24-08-2006
		US 2010134936 A1	03-06-2010
		WO 2006088323 A1	24-08-2006
WO 2006098560 A1	21-09-2006	JP 2008533736 A	21-08-2008
		KR 20060101208 A	22-09-2006
		US 2008197916 A1	21-08-2008
		WO 2006098560 A1	21-09-2006