(54) Title: METHOD OF MAKING DEVICE

START

FORM BOTTOM ELECTRODE ASSEMBLY

FORM MAGNETIC JUNCTION ASSEMBLY

FORM TOP ELECTRODE ASSEMBLY

STOP

(57) Abstract: A method for forming MRAM (magnetoresistive random access memory) devices is provided. A bottom electrode assembly is formed. A magnetic junction assembly is formed, comprising, depositing a magnetic junction assembly layer over the bottom electrode assembly, forming a patterned mask over the magnetic junction assembly layer, etching the magnetic junction assembly layer to form the magnetic junction assembly with gaps, gap filling the magnetic junction assembly, and planarizing the magnetic junction assembly. A top electrode assembly is formed.
Declarations under Rule 4.17:
— as to the applicant’s entitlement to claim the priority of the earlier application (Rule 4.17(Hi))
— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

Published:
— with international search report (Art. 21(3))
METHOD OF MAKING DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS


BACKGROUND OF THE INVENTION

[0002] The present invention relates to forming a semiconductor device. More specifically, the present invention relates to forming a magnetoresistive random-access memory (MRAM) device.

[0003] During semiconductor wafer processing, features may be etched through a metal containing layer. In the formation of magnetoresistive random-access memory (MRAM) a plurality of thin metal layers or films may be sequentially etched.

SUMMARY OF THE INVENTION

[0004] To achieve the foregoing and in accordance with the purpose of the present invention, a method for forming MRAM (magnetoresistive random access memory) devices is provided. A bottom electrode assembly is formed. A magnetic junction assembly is formed. A top electrode assembly is formed.

[0005] In another manifestation of the invention, a method for forming MRAM (magnetoresistive random access memory) devices is provided. A bottom electrode assembly is formed, comprising depositing a bottom electrode assembly layer over a substrate, forming a patterned mask over the bottom electrode assembly layer, etching the bottom electrode assembly layer to form the bottom electrode assembly with gaps, gap filling the gaps in the bottom electrode assembly, stripping the patterned mask over the bottom electrode assembly, and planarizing the bottom electrode assembly. A magnetic junction assembly is formed, comprising depositing a magnetic junction assembly layer over the planarized bottom electrode assembly, forming a patterned mask over the magnetic junction assembly layer, etching the magnetic junction assembly layer to form the magnetic junction assembly with gaps, gap filling the magnetic junction assembly, stripping the patterned mask over the magnetic junction assembly, and planarizing the magnetic junction assembly. A top electrode assembly
is formed, comprising depositing a top electrode assembly layer over the planarized magnetic junction assembly, forming a patterned mask over the top electrode assembly layer, etching the top electrode assembly layer to form the top electrode assembly with gaps, and gap filling the top electrode assembly.

[0006] In another manifestation of the invention, a magnetoresistive random access memory device is provided. A bottom electrode assembly is formed. A magnetic junction assembly is formed. A top electrode assembly is formed.

[0007] These and other features of the present invention will be described in more detail below in the detailed description of the invention and in conjunction with the following figures.

**BRIEF DESCRIPTION OF THE DRAWINGS**

[0008] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

[0009] FIG. 1 is a high level flow chart of an embodiment of the invention.

[0010] FIGS. 2A-K are schematic views of a stack processed according to an embodiment of the invention.

[0011] FIG. 3 is a more detailed flow chart of a step of forming a bottom electrode assembly.

[0012] FIG. 4 is a more detailed flow chart of a step of forming a magnetic junction assembly.

[0013] FIG. 5 is a more detailed flow chart of the step of forming a top electrode assembly.

[0014] FIGS. 6A-B are schematic views of a stack processed according to the prior art.

**DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

[0015] The present invention will now be described in detail with reference to a few preferred embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures
have not been described in detail in order to not unnecessarily obscure the present invention.

To facilitate understanding, FIG. 1 is a high level flow chart of a process used in an embodiment. A bottom electrode assembly is formed over a substrate with a layer with contacts (step 104). A magnetic junction assembly is formed over the bottom electrode assembly (step 108). A top electrode assembly is formed over the magnetic junction assembly (step 112).

Embodiments

In an embodiment, a bottom electrode assembly is formed (step 104). FIG. 2A is a cross-sectional view of a stack 200 with a substrate 204 over which a contact layer 208 with contacts 212 has been formed. One or more layers may be between the substrate 204 and the contact layer 208. FIG. 3 is a more detailed flow chart of the step of forming the bottom electrode assembly (step 104). A bottom electrode assembly layer 216 is deposited over the contact layer 208 (step 304). In this embodiment, the bottom electrode assembly layer 216 is a multiple layer of an adhesion layer over which an electrode layer is placed, over which a capping layer is placed. In an example of this embodiment, the bottom electrode assembly layer 216 is formed from layers of titanium nitride (TiN), tantalum (Ta), and ruthenium, (Ru).

A bottom electrode assembly mask 220 is formed over the bottom electrode assembly layer 216 (step 308). In one example, the bottom electrode assembly mask 220 is a carbon based lithographic material, such as photoresist. In another example, the bottom electrode assembly mask 220 is a metal or dielectric hardmask material formed in a multiple step process, such as forming a patterned photoresist mask over the hardmask layer and patterning the hardmask layer using the patterned photoresist mask.

The bottom electrode assembly layer 216 is etched to form a bottom electrode assembly of bottom electrodes (step 312). FIG. 2B is a cross-sectional view of the stack 200 after the bottom electrode assembly layer 216 (FIG. 2A) has been etched to form the bottom electrodes 224 of the bottom electrode assembly. In various embodiments, a reactive ion etch or a wet etch may be used for etching the bottom electrode assembly layer 216. Preferably, the etching of the bottom electrode assembly layer 216 is performed by a dry etch, such as a reactive ion etch. The
bottom electrode assembly mask 220 is stripped (step 316). In alternative embodiments of the invention, the bottom electrode assembly mask 220 is not stripped at this step, since the bottom electrode assembly mask 220 may be stripped during other steps. FIG. 2C is a cross-sectional view of the stack 200 after the bottom electrode assembly mask 220 (FIG. 2B) has been stripped. Gaps 228 are between the bottom electrodes 224 of the bottom electrode assembly. An optional clean step may be provided after the stripping or etching.

[0020] The gaps 228 are filled (step 320). Preferably, the gaps 228 are filled with a dielectric material. The dielectric material is planarized (step 324). FIG. 2D is a cross-sectional view of the stack 200 after the gaps 228 (FIG. 2C) have been filled with a dielectric filler 232, which has been planarized. In this example, the planarization is accomplished using chemical mechanical polishing (CMP). In embodiments where the bottom electrode assembly mask 220 is not stripped, the bottom electrode assembly mask 220 may be removed by the CMP.

[0021] The magnetic junction assembly is formed (step 108). FIG. 4 is a more detailed flow chart of the step of forming the magnetic junction assembly (step 108). A magnetic junction assembly layer is deposited over the bottom electrodes 224 and the dielectric filler 232 (step 404). FIG. 2E is a cross-sectional view of the stack 200 after the magnetic junction assembly layer 236 has been deposited. In this embodiment, the magnetic junction assembly layer 236 comprises a bottom magnetic layer 240, a tunnel oxide layer 244 over the bottom magnetic layer 240, and a top magnetic layer 248 over the tunnel oxide layer 244. In an embodiment, the bottom magnetic layer 240 and the top magnetic layer 248 are pinned magnets. In another embodiment, the bottom magnetic layer 240 is a pinned magnet and the top magnetic layer 248 is a free magnet layer and an anti ferromagnetic layer. Other embodiments may provide additional adhesion, capping, lattice matching, and work function matching layers.

[0022] A magnetic junction assembly mask 252 is formed over the magnetic junction assembly layer 236 (step 408). In one example, the magnetic junction assembly mask 252 is a carbon based lithographic material, such as photoresist. In another example, the magnetic junction assembly mask 252 is a metal or dielectric hardmask material formed in a multiple step process, such as forming a patterned
photoresist mask over the hardmask layer and patterning the hardmask layer using the patterned photoresist mask.

**[0023]** The magnetic junction assembly layer 236 is etched to form a magnetic junction assembly of magnetic junctions (step 412). FIG. 2F is a cross-sectional view of the stack 200 after the magnetic junction assembly layer has been etched to form the magnetic junctions 256 of the magnetic junction assembly. In various embodiments, a reactive ion etch or a wet etch may be used for etching the magnetic junction assembly layer. Preferably, the etch is non volatile, where all of the etch byproducts are non volatile. Preferably the etching of the magnetic junction assembly layer 236 is performed by a dry etch, such as a reactive ion etch. The magnetic junction assembly mask 252 is stripped (step 416). In alternative embodiments of the invention, the magnetic junction assembly mask 252 is not stripped at this step, since the magnetic junction assembly mask 252 may be stripped during other steps. FIG. 2G is a cross-sectional view of the stack 200 after the magnetic junction assembly mask has been stripped. Gaps 260 are between the magnetic junctions 256 of the magnetic junction assembly. An optional clean step may be provided after the stripping or etching.

**[0024]** The gaps 260 are filled (step 420). Preferably, the gaps 260 are filled with a dielectric material. The dielectric material is planarized (step 424). FIG. 2H is a cross-sectional view of the stack 200 after the gaps have been filled with a dielectric filler 264, which has been planarized. In this example, the planarization is accomplished using chemical mechanical polishing (CMP). In embodiments where the magnetic junction assembly mask 252 is not stripped, the magnetic junction assembly mask 252 may be removed by the CMP.

**[0025]** A top electrode assembly is formed (step 112). FIG. 5 is a more detailed flow chart of the step of forming the top electrode assembly (step 112). A top electrode assembly layer is deposited over the magnetic junctions 256 (step 504). FIG. 2I is a cross-sectional view of the stack 200 after the top electrode assembly layer 268 has been deposited over the magnetic junctions 256. In this embodiment, the top electrode assembly layer 268 is a multiple layer of an adhesion layer over which an electrode layer is placed, over which a capping layer is placed. In an example of this embodiment, the top electrode assembly layer 268 is formed from layers of tungsten (W), titanium nitride (TiN), and ruthenium (Ru), or tantalum (Ta),
titanium nitride (TiN), and ruthenium (Ru), or tungsten (W) and titanium nitride (TiN), or tantalum (Ta) and titanium nitride (TiN), or tantalum (Ta). Other embodiments may provide additional adhesion, capping, lattice matching, work function matching, and antiferromagnetic layers.

5 [0026] A top electrode assembly mask 272 is formed over the top electrode assembly layer 268 (step 508). In one example, the top electrode assembly mask 272 is a carbon based lithographic material, such as photoresist. In another example, the top electrode assembly mask 272 is a metal or dielectric hardmask material formed in a multiple step process, such as forming a patterned photoresist mask over the hardmask layer and patterning the hardmask layer using the patterned photoresist mask.

[0027] The top electrode assembly layer 268 is etched to form a top electrode assembly of top electrodes (step 512). FIG. 2J is a cross-sectional view of the stack 200 after the top electrode assembly layer 268 (FIG. 2I) has been etched to form the top electrodes 276 of the top electrode assembly with gaps 280 between the top electrodes 276. In various embodiments, a reactive ion etch or a wet etch may be used for etching the top electrode assembly layer 268. In an embodiment, the etch is a non volatile etch. Preferably the etching of the top electrode assembly layer 268 is performed by a dry etch, such as a reactive ion etch. An optional clean step may be provided after the etching.

[0028] The gaps 280 are filled (step 516). Preferably, the gaps 280 are filled with a dielectric material. FIG. 2K is a cross-sectional view of the stack 200 after the gaps 280 (FIG. 2J) have been filled with a dielectric filler 284. In this embodiment, the top electrode assembly mask 272 is not stripped and the dielectric filler 284 is not planarized. The stripping of the top electrode assembly mask 272 and the planarization of the dielectric filler 284 may occur in subsequent steps. In other embodiments, the top electrode assembly mask 272 may be stripped before the deposition of the dielectric filler 284. In other embodiments, the planarization and the removal of the top electrode assembly mask 272 may be performed by a CMP process.

[0029] These embodiments minimize exposure of the sidewalls of the stack to sputtered metallic deposition. In addition, these embodiments minimize exposure of the sidewalls of the magnetic junctions 256 to sputtered metallic deposition.
FIG. 6A is a cross-sectional view of a stack 600 processed according to the prior art. In such a stack, over a substrate layer 604 a contact layer 608 with contacts 610 is formed. A lower electrode assembly layer 612 is formed over the contact layer 608 with contacts 610. A magnetic assembly layer 616 is formed over the lower electrode assembly layer 612. The magnetic assembly layer 616 comprises a bottom magnetic layer 620, a tunnel oxide layer 624, and a top magnetic layer 628. An upper electrode assembly layer 632 is formed over the magnetic assembly layer 616. A patterned mask 636 is formed over the upper electrode assembly layer 632.

The patterned mask 636 is used to etch the upper electrode assembly layer 632, the magnetic assembly layer 616, and the lower electrode assembly layer 612. FIG. 6B is a cross-sectional view of the stack 600 after the upper electrode assembly layer 632, the magnetic assembly layer 616, and the lower electrode assembly layer 612 have been etched. The etching forms sidewalls 640 on sides of the stack 600. Due to the high aspect ratio of the etched spaces, removal of the sidewalls 640 is difficult. The sidewalls 640 may cause electrical shorts between different layers. In addition, sidewalls 640 formed from materials from the bottom magnetic layer 620 or top magnetic layer 628 may be magnetic, which would further interfere with the electrical operations of the stack 600. In addition, the tunnel oxide layer 624 is exposed to an etching plasma during the etching of the tunnel oxide layer 624, the bottom magnetic layer 620, and the lower electrode assembly layer 612.

By individually etching each layer and then filling the gaps before a subsequent etch, exposure of each layer to an etch plasma or sidewall deposition is minimized. Such metallic deposition may cause electrical shorts in the metallic junctions. If sputtered metallic deposition comes from the magnetic junctions, the resulting sidewalls may be magnetic, which may interfere with the functioning of the resulting devices. In addition, embodiments of the invention minimizes the exposure of the tunnel oxide to plasma, which reduces damage to the tunnel oxide. Such damage degrades device electrical behavior. Sidewalls on resulting high aspect ratio devices are difficult to clean. Therefore, the embodiments that reduce such sidewalls provide improved devices. Other embodiments may provide steps in other orders, as long as a gap fill is provided before a subsequent etch.

While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, modifications, and various
substitute equivalents, which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and various substitute equivalents as fall within the true spirit and scope of the present invention.
CLAIMS

What is claimed is:

1. A method for forming MRAM (magnetoresistive random access memory) devices, comprising:
   5  forming a bottom electrode assembly;
   forming a magnetic junction assembly; and
   forming a top electrode assembly.

2. The method, as recited in claim 1, wherein the forming the bottom electrode assembly, comprises:
   10  depositing a bottom electrode assembly layer over a substrate;
   forming a patterned mask over the bottom electrode assembly layer;
   etching the bottom electrode assembly layer to form the bottom electrode assembly with gaps;
   gap filling the gaps in the bottom electrode assembly; and
   planarizing the bottom electrode assembly.

3. The method, as recited in claim 2, wherein the forming the magnetic assembly, comprises:
   15  depositing a magnetic junction assembly layer over the planarized bottom electrode assembly;
   forming a patterned mask over the magnetic junction assembly layer;
   etching the magnetic junction assembly layer to form the magnetic junction assembly with gaps;
   gap filling the magnetic junction assembly; and
   planarizing the magnetic junction assembly.

4. The method, as recited in claim 3, wherein the forming the top electrode assembly, comprises:
   20  depositing a top electrode assembly layer over the planarized magnetic junction assembly;
   forming a patterned mask over the top electrode assembly layer;
   etching the top electrode assembly layer to form the top electrode assembly with gaps; and
   gap filling the top electrode assembly.
5. The method, as recited in claim 4, further comprising:
stripping the patterned mask over the bottom electrode assembly; and
stripping the patterned mask over the magnetic junction assembly.

6. The method, as recited in claim 5, wherein the etching the bottom electrode assembly layer is performed by a dry etch.

7. The method, as recited in claim 6, wherein the etching the magnetic junction assembly layer is performed by a dry etch.

8. The method, as recited in claim 7, wherein the etching the top electrode assembly layer is performed by a dry etch.

9. The method, as recited in claim 8, wherein the depositing the magnetic junction assembly layer, comprises:
depositing a bottom magnetic layer over the planarized bottom electrode assembly;
depositing a tunnel oxide layer over the bottom magnetic layer; and
depositing a top magnetic layer over the tunnel oxide layer.

10. The method, as recited in claim 9, wherein the gap filling fills the gaps with a dielectric material.

11. The method, as recited in claim 2, wherein the etching the bottom electrode assembly layer is performed by a dry etch.

12. The method, as recited in claim 1, wherein the forming the magnetic assembly, comprises:
depositing a magnetic junction assembly layer over the bottom electrode assembly;
forming a patterned mask over the magnetic junction assembly layer;
etching the magnetic junction assembly layer to form the magnetic junction assembly with gaps;
gap filling the magnetic junction assembly; and
planarizing the magnetic junction assembly.

13. The method, as recited in claim 12, wherein the etching the magnetic junction assembly layer is performed by a dry etch.

14. The method, as recited in claim 12, wherein the depositing the magnetic junction assembly layer, comprises:
depositing a bottom magnetic layer over the bottom electrode assembly;
depositing a tunnel oxide layer over the bottom magnetic layer; and
depositing a top magnetic layer over the tunnel oxide layer.

15. The method, as recited in claim 12, wherein the gap filling fills the gaps with a dielectric material.

16. The method, as recited in claim 1, wherein the forming the top electrode assembly, comprises:
   depositing a top electrode assembly layer over the magnetic junction assembly;
   forming a patterned mask over the top electrode assembly layer;
   etching the top electrode assembly layer to form the top electrode assembly with gaps; and
   gap filling the top electrode assembly.

17. The method, as recited in claim 15, wherein the etching the top electrode assembly layer is performed by a dry etch.

18. A method for forming MRAM (magnetoresistive random access memory) devices, comprising:
   forming a bottom electrode assembly, comprising:
   depositing a bottom electrode assembly layer over a substrate;
   forming a patterned mask over the bottom electrode assembly layer;
   etching the bottom electrode assembly layer to form the bottom electrode assembly with gaps;
   gap filling the gaps in the bottom electrode assembly;
   stripping the patterned mask over the bottom electrode assembly; and
   planarizing the bottom electrode assembly;
   forming a magnetic junction assembly, comprising
   depositing a magnetic junction assembly layer over the planarized bottom electrode assembly;
   forming a patterned mask over the magnetic junction assembly layer;
   etching the magnetic junction assembly layer to form the magnetic junction assembly with gaps;
   gap filling the magnetic junction assembly;
   stripping the patterned mask over the magnetic junction assembly; and
   planarizing the magnetic junction assembly; and
forming a top electrode assembly, comprising

depositing a top electrode assembly layer over the planarized magnetic
junction assembly;
forming a patterned mask over the top electrode assembly layer;
etching the top electrode assembly layer to form the top electrode
assembly with gaps; and
gap filling the top electrode assembly.

19. A magnetoresistive random access memory device formed by the method,
comprising:

forming a bottom electrode assembly;
forming a magnetic junction assembly; and
forming a top electrode assembly.

20. The method, as recited in any of claims 1-2, wherein the forming the magnetic
assembly, comprises:

depositing a magnetic junction assembly layer over the bottom electrode
assembly;
forming a patterned mask over the magnetic junction assembly layer;
etching the magnetic junction assembly layer to form the magnetic junction
assembly with gaps;
gap filling the magnetic junction assembly; and
planarizing the magnetic junction assembly.

21. The method, as recited in any of claims 1-2 and 20, wherein the forming the top electrode assembly, comprises:

depositing a top electrode assembly layer over the magnetic junction
assembly;
forming a patterned mask over the top electrode assembly layer;
etching the top electrode assembly layer to form the top electrode assembly
with gaps; and
gap filling the top electrode assembly.

22. The method, as recited in any of claims 20-21, further comprising:
stripping the patterned mask over the bottom electrode assembly; and
stripping the patterned mask over the magnetic junction assembly.
23. The method, as recited in any of claims 2 and 20-22, wherein the etching the bottom electrode assembly layer is performed by a dry etch.

24. The method, as recited in any of claims 20-23, wherein the etching the magnetic junction assembly layer is performed by a dry etch.

25. The method, as recited in any of claims 20-23, wherein the etching the top electrode assembly layer is performed by a dry etch.

26. The method, as recited in any of claims 20-25, wherein the depositing the magnetic junction assembly layer, comprises:
   - depositing a bottom magnetic layer over the bottom electrode assembly;
   - depositing a tunnel oxide layer over the bottom magnetic layer; and
   - depositing a top magnetic layer over the tunnel oxide layer.

27. The method, as recited in any of claims 2 and 20-26, wherein the gap filling fills the gaps with a dielectric material.
START

FORM BOTTOM ELECTRODE ASSEMBLY 104

FORM MAGNETIC JUNCTION ASSEMBLY 108

FORM TOP ELECTRODE ASSEMBLY 112

STOP

FIG. 1

START

DEPOSIT TOP ELECTRODE ASSEMBLY 504

FORM TOP ELECTRODE ASSEMBLY MASK 508

ETCH TOP ELECTRODE ASSEMBLY 512

FILL GAP 516

STOP

FIG. 5
START

DEPOSIT MAGNETIC JUNCTION ASSEMBLY 404

FORM MAGNETIC JUNCTION ASSEMBLY MASK 408

ETCH MAGNETIC JUNCTION ASSEMBLY 412

STRIP MASK 416

FILL GAP 420

PLANARIZE MAGNETIC JUNCTION ASSEMBLY 424

STOP

FIG. 4
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

G11C 1/15(2006.01), HOIL 27/115(2006.01), HOIL 21/8247(2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 11/15; HOIL 21/8246; G11C 7/02; HOIL 29/76; HOIL 23/552; G11C 11/00; HOIL 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: Magnetoresistive, RAM, MRAM, form, electrode, assembly, magnetic, junction, disposition, and similar terms.

c. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<td>X</td>
<td>US 2010-00472929 Al (LIUBO HONG et a l.) 25 February 2010</td>
<td>1, 19</td>
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<td></td>
<td>See paragraphs 35-37, 40, 47, 53; figures 4-5; and claim 1.</td>
<td>2-18, 20</td>
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<td>See paragraphs 44-46; figures 11-12; and claim 1.</td>
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Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:
  "A" document defining the general state of the art which is not considered to be of particular relevance
  "E" earlier application or patent but published on or after the international filing date
  "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
  "O" document referring to an oral disclosure, use, exhibition or other means
  "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
15 April 2013 (15.04.2013)

Date of mailing of the international search report
16 April 2013 (16.04.2013)

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongna-ro, Seo-gu, Daejeon Metropolitan City 302-70 1, Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
BYUN, Sung Cheal
Telephone No. 82-42-481-8262

Form PCT/ISA/210 (second sheet) (My 2009)
This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
   because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 21-27
   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☒ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest
☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
☒ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
☐ No protest accompanied the payment of additional search fees.
<table>
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