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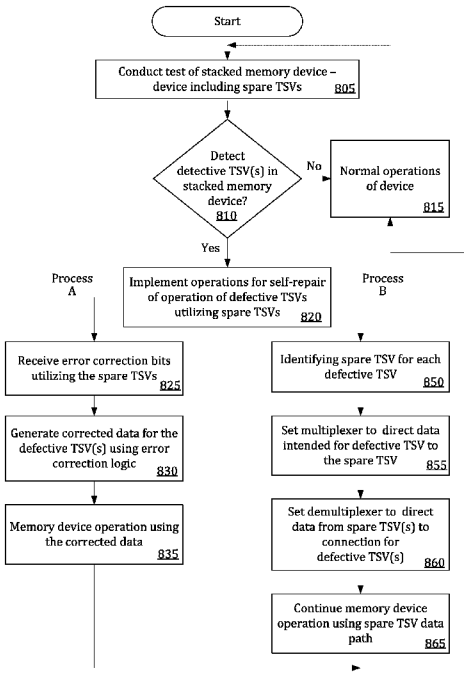


Fig. 8

(57) Abstract: Self-repair logic for stacked memory architecture. An embodiment of a memory device includes a memory stack having one or more memory die elements, including a first memory die element, and a system element coupled with the memory stack. The first memory die element includes multiple through silicon vias (TSVs), the TSVs including data TSVs and one or more spare TSVs, and self-repair logic to repair operation of a defective TSV of the plurality of data TSVs, the repair of operation of the defective TSV including utilization of the one or more spare TSVs.

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SELF-REPAIR LOGIC FOR STACKED MEMORY ARCHITECTURE

TECHNICAL FIELD

[0001] Embodiments of the invention generally relate to the field of electronic devices and, more particularly, to self-repair logic for stacked memory architecture.

BACKGROUND

[0002] To provide more dense memory for computing operations, concepts involving memory devices (which may be referred to as 3D stacked memory, or stacked memory) having a plurality of closely coupled memory elements have been developed. A 3D stacked memory may include coupled layers or packages of DRAM (dynamic random-access memory) memory elements, which may be referred to as a memory stack. Stacked memory may be utilized to provide a great amount of computer memory in a single device or package, where the device or package may also include certain system components, such as a memory controller and CPU (central processing unit).

[0003] However, there may a significant cost in the manufacture of 3D stacked memory, in comparison with the cost of simpler memory elements. In the construction of stacked memory devices, a memory die that is without flaws when fabricated may develop flaws in the manufacture of the 3D stacked memory package. Because of this, the cost of defective memory devices may be significant for device manufacturers, or for customers who purchase electronic devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

[0005] **Figure 1** illustrates an embodiment of a 3D stacked memory;

[0006] **Figure 2** illustrates an embodiment of a self-repair apparatus or system that provides for replacement of defective TSV operation using generation of error correction code;

[0007] **Figure 3** is an illustration of the generation of error correction code in an embodiment of an apparatus or system;

[0008] **Figure 4** illustrates an embodiment of error correction elements for a apparatus or system providing self-repair of defective TSV operation;

[0009] **Figure 5** is an illustration of an apparatus or system providing for self-repair of TSV operation using substitution of defective TSVs with spare TSVs;

[0010] **Figure 6** is an illustration of an embodiment of an apparatus or system providing for use of data of spare TSVs to substitute for data from defective TSVs;

[001 1] **Figure 7** is an illustration of an embodiment of identification of defective TSVs in a device or system;

[0012] **Figure 8** is a flowchart to illustrate an embodiment of a process for using spare TSVs in a stacked memory device to repair operations of defective TSVs;

[0013] **Figure 9** is an illustration of an embodiment of an apparatus or system including elements for repair of operations of defective TSVs using spare TSVs; and

[0014] **Figure 10** illustrates an embodiment of a computing system including stacked memory having elements for repair of operations of defective TSVs using spare TSVs.

DETAILED DESCRIPTION

[0015] Embodiments of the invention are generally directed to self-repair logic for a stacked memory architecture.

[00 16] As used herein:

[0017] "3D stacked memory" (where 3D indicates three-dimensional) or "stacked memory" means a computer memory including one or more coupled memory die layers, memory packages, or other memory elements. The memory may be vertically stacked or horizontally (such as side-by-side) stacked, or otherwise contain memory elements that are coupled together. In particular, a stacked memory DRAM device or system may include a memory device having a plurality of DRAM die layers. A stacked memory device may also include system

elements in the device, which may be referred to herein as a system layer or element, where the system layer may include elements such as a CPU (central processing unit), a memory controller, and other related system elements. The system layer may include a system on chip (SoC). In some embodiments, the logic chip may be an application processor or graphics processing unit (GPU).

[0018] With the advent of the stacked DRAM standard (such as the WidelO standard), the DRAM wafer may be stacked with a system element such as a system on chip (SoC) wafer in the same package with a memory stack. The stacked memory may utilize through silicon via (TSV) manufacturing techniques, where vias are produced through silicon dies to provide signal paths through the memory stack.

[0019] TSV manufacturing technique is used to interconnect the stacked silicon chips through direct contact. However, this technique may create a significant yield loss when TSVs are defective. The stacked memory assembling process and TSV manufacturing may potentially introduce defects into stacked memory devices. This may result in an increase in manufacturing and test cost increase, and may create yield problem in manufacturing. Defective TSVs are a critical element in stacked memory manufacturing because the existence of defective TSVs will directly impact manufacturing yield. If each device having defective TSVs is discarded, the resulting cost would be significantly greater in comparison with defects in conventional single die memory because in a stacked memory both a stacked DRAM package and an SoC will be lost. In conventional memory, a repair process may include replacement of an entire row or column by extra row or column, but this does not assist in circumstances in which connecting TSVs are defective.

[0020] In some embodiments, an apparatus, system, or method includes self-repair logic utilizing spare TSVs to dynamically perform a repair process for defective TSVs. In some embodiments, in order to improve reliability, reduce costs, and increase manufacturing yield, spare TSVs are included among TSVs in a stacked memory device to allow for repairing the defective TSVs. However, repair logic in a stacked memory should be minimized or reduced to avoid excessive hardware overhead for stacked memory devices.

[0021] In some embodiments, self-repair logic, such as error correcting code (ECC) and redirection of data, may be adopted for repair of defective TSVs operation using spare TSVs. In some embodiments, a TSV repair technique enables the dynamic repair of defective TSV by replacing the operation of defective TSVs, thus enhance the manufacturing yield and reliability of devices by allowing full operation of stacked memory devices having TSV defects. In some embodiments, a self-repair technique does not require re-routing of devices or shifting operations to different elements to replace defective TSVs.

[0022] In some embodiments, the testing to identify defective TSVs and the self-repair of the operation of defective TSVs may occur at various times, and may occur multiple times in the lifespan of a memory device. Testing and self-repair may be either static in initial testing, or dynamic in operation. For example, testing and self-repair of TSV operation may occur in the manufacturing of stacked memory devices, and may occur in the manufacture of an apparatus or system including stacked memory. Further, testing and self-repair may occur in the operation of such apparatus or system. In an example, testing and self-repair may occur at each power up cycle for the apparatus or system.

[0023] In some embodiments, an apparatus, system, or method provides for error correction of data transferred by the TSVs of a memory device. In some embodiments, a stacked memory device includes self-repair logic utilizing error correcting code. In this approach, on a transmitting side, a check bit (or other error correcting code) is generated based on data to be transferred by a plurality of TSVs. For example, every data byte may be utilized in the generation of check bits. The data is transferred via the TSVs, with the check bits being transferred via spare TSVs.

[0024] On a receiving side, decodes the data (the raw data and the check bit(s)) and corrects the corrupted data, such that correct data is provided by the stacked memory device regardless of the defective TSV channel. Thus, even though there is a defective TSV, the error correcting logic corrects the corrupted data from the channels and thus provides for replacement of the TSV operation.

[0025] In certain implementations, certain errors may be detected and corrected, or certain errors may be detected if not corrected, such as in

circumstances in which there are excessive numbers of defective TSVs. For example, logic may provide for single error correction and double-error detection (SEC-DED), single-error-correction and double adjacent error correction (SEC-DAEC), and other correction and detection operations. In one example, SEC-DAEC may be particularly useful in TSV operation because defects in a device may cause issues for adjacent TSVs, and thus there may be particular value in correcting double adjacent errors.

[0026] Multiple different kinds of self-repair logic may be utilized in an embodiment of an apparatus, system, or method, with error correcting codes and error detecting codes being common examples. For example, for single-bit error correcting code, check bits are generated using the data word. If the size of the data word is D and the number of required check bits to have SEC-DEC capability is C, then C is determined when D and C meet the requirements of Equation 1:

$$2^C \geq D + C + 1 \quad [1]$$

[0027] Hence, if the data words are 32 bits, 64 bits, and 128 bits, then, 6, 7, and 8 bits of check bits are required to perform single error correction, respectively. Every 32 TSVs, 64TSVs, or 128TSVs may thus have 6, 7, or 8 spare TSVs to perform the repair process using error correcting code.

[0028] In some embodiments, an apparatus, system, or method utilizes the redirection of data from a defective TSV to a spare TSV to provide for repair to TSV operation. In some embodiments, a hardware mapping process maps a defective TSV channel to a spare channel to perform the self-repair process. In this approach, on the transmitting side a mapping multiplexer may be used, where selection bits for the multiplexer may be dynamically or statically generated. In some embodiments, on the receiving side de-multiplexing logic is implemented and selection bits may be generated in the same manner. In a dynamic approach, Built-in Self Test (BIST) logic may be run to identify one or more defective TSVs. In some embodiments, static and dynamic repair is performed by utilizing hardware mapping logic in the transmitting side and the receiving side. In some embodiments, the static and dynamic repair processes use multiplexer/de-multiplexer logic or other similar logic to route a defective TSV to a spare TSV.

[0029] In some embodiments, a memory device includes a memory stack having one or more memory die elements, including a first memory die element, and a system element coupled with the memory stack. The first memory die element includes multiple TSVs, the TSVs including data TSVs and one or more spare TSVs, and self-repair logic to repair operation of a defective TSV of the plurality of data TSVs, the repair of operation of the defective TSV including utilization of the one or more spare TSVs.

[0030] In some embodiments, a method includes conducting a test of a stacked memory device, the stacked memory stack including one or more memory die elements, a system element coupled with the memory stack, and a plurality of TSVs; detecting one or more defective TSVs of the plurality of TSVs; and repairing operation of the one or more defective TSVs, the repair of operation including utilization of the one or more spare TSVs.

[003 1] In some embodiments, a system includes a processor to process data of the system; a transmitter, receiver, or both coupled with an omnidirectional antenna to transmit data, receive data, or both; and a memory to store data, the memory including a stacked memory device. In some embodiments, the stacked memory device includes a memory stack having one or more memory die elements, including a first memory die element, and a system element coupled with the memory stack, wherein the first memory die element includes a plurality of TSVs, the plurality of TSVs including a plurality of data TSVs and one or more spare TSVs, and self-repair logic to repair operation of a defective TSV of the plurality of data TSVs, the repair including utilization of the one or more spare TSVs.

[0032] **Figure 1** illustrates an embodiment of a 3D stacked memory. In this illustration, a 3D stacked memory device 100, such as a WidelO memory device, includes a system element 110 coupled with one or more DRAM memory die layers 120, also referred to herein as the memory stack. In some embodiments, the system element may be a system on chip (SoC) or other similar element. In this illustration, the DRAM memory die layers include four memory die layers, these layers being a first memory die layer 130, a second memory die layer 140, a third memory die layer 150, and a fourth memory die layer 160. However, embodiments are not limited to any particular number of memory die layers in the memory stack

120, and may include a greater or smaller number of memory die layers. Each die layer may include one or more slices or portions, and may have one or more different channels. Each die layer may include a temperature compensated self-refresh (TCSR) circuit to address thermal issues, where the TCSR and a mode register (MR) may be a part of management logic of the device, and where the MC may include thermal offset bit(s) for adjustment of refresh rate by the TCSR. The die layers and the system element may be thermally coupled together.

[0033] Among other elements, the system element 110 may include a memory controller 112, such as a WidelO memory controller, for the memory stack 120. In some embodiments, each memory die layer (with the possible exception of the top (or outermost) memory die layer, such as the fourth memory die layer 160 in this illustration) includes a plurality of through silicon vias (TSVs) 105 to provide paths through the memory die layers, as well as one or more spare TSVs 107.

[0034] In some embodiments, the stacked memory device 100 provides for self-repair of TSV operations utilizing the spare TSVs 107. In some embodiments, one or more of the memory die layers 120 includes detection logic (such as detection 132 illustrated in the first memory die layer 130) to detect defective TSVs. The detection logic 132 may include BIST elements of the memory die layer. In some embodiments, one or more of the memory die layers 120 includes spare TSV self-repair logic (such as the self-repair logic 132 illustrated in the first memory die layer 130) to provide for repair of the TSV operation for defective TSVs. In some embodiments, the self-repair logic 132 may include error correction logic utilizing the spare TSVs, where the error correction logic corrects errors generated by one or more defective TSVs. In some embodiments, the spare TSV logic may include multiplexing and de-multiplexing operations to allow for the rerouting of data of defective TSVs through spare TSVs.

[0035] **Figure 2** illustrates an embodiment of a self-repair apparatus or system that provides for replacement of defective TSV operation using generation of error correction code. Figure 2 illustrates an embodiment of hardware architecture to generate check bits based on a received data word. However, embodiments are not limited to any particular error correction structure. In some

embodiments, regardless of the location of defective TSV, corrupted data may be restored by the ECC scheme.

[0036] In this illustration, a memory apparatus or system 200 includes a plurality of TSVs 210, where the plurality of TSVs includes one or more spare TSVs 215. The non-spare TSVs intended to receive data may be referred to herein as data TSVs. As illustrated, at some point in time, a TSV 220 has become defective. As illustrated, inputs to the data TSVs of the plurality of TSVs 210 are also connected to a check bit generator 225 (or other error correction code generator, including error correction code generator 300 in Figure 3). In some embodiments, the check bit generator 225 generates check bits for transmission via the spare TSVs 215, where the check bits are used in the correction of data that has been corrupted by the defective TSV 220.

[0037] **Figure 3** is an illustration of the generation of error correction code in an embodiment of an apparatus or system. In some embodiments, a error correction code generator 300 (such as check bit generator 225 illustrated in Figure 2) receives each data bit input 305 intended for a plurality of TSVs (such as the data TSVs of the plurality of TSVs 210 illustrated in Figure 2).

[0038] In this particular implementation, the error correction code generator 300 includes a plurality of exclusive OR elements (XOR 320, 325, 330, and 335) to generate check bits 350 for use in the self-repair process for TSVs. However, embodiments of a memory apparatus or system are not limited to any particular error correction code generator implementation.

[0039] **Figure 4** illustrates an embodiment of error correction elements for a apparatus or system providing self-repair of defective TSV operation. In some embodiments, a memory apparatus or system 400 includes error correction logic 450 to provide for self-repair of defective TSV operation. In some embodiments, the correction logic will receive data from a plurality of TSVs 410 coupled to connections 425, where the TSVs include spare TSVs 415, the spare TSVs being utilized to provide generated error correction code based on the data transmitted via the non-spare TSVs.

[0040] In this example, the TSVs include one or more defective TSVs, such as a defective TSV 420. In some embodiments, the memory apparatus or

system utilizes the error correction logic to provide self-repair of the operation of the defective TSV 420 by generating corrections for errors caused by the defective TSV.

[0041] **Figure 5** is an illustration of an apparatus or system providing for self-repair of TSV operation using substitution of defective TSVs with spare TSVs. In some embodiments, a hardware mapping process, which may be utilized in static and dynamic repairs, utilize multiplexer/de-multiplexer logic to route data intended for a defective TSV to a spare TSV.

[0042] In some embodiments, a memory apparatus or system 500 receives a plurality of functional values 505 that are intended for a set of TSVs 510, where the TSVs of the apparatus or system 500 also include one or more spare TSVs 515. In some embodiments, the apparatus or system includes a multiplexer 530, where the multiplexer is used to choose a data line for which there is a defective TSV such that the data for the defective TSV is routed to a spare TSV. In some embodiments, the transmission of the data via the spare TSV allows for self-repair of the operation of the defective TSV in transmission of the relevant data.

[0043] Figure 5 illustrates a particular implementation is which a multiplexer element is used to re-route data to a spare channel. However, embodiments are not limited to this particular implementation, and may utilize any elements that provide for the selection of the data of a defective TSV for transmission using a spare TSV. For example, the multiplexer logic may be implemented using standard cell, pass transistor, or primitive logic gates. If a pass transistor logic implementation is chosen in an embodiment, then the pass transistor logic may be added to all channels of the memory device for delay balancing.

[0044] In a particular example, if the third TSV of a plurality of TSVs is determined to be defective (such as shown in Figure 5), a defect location may be identified by fusing for a static operation, where a fuse 540 is illustrated for each transmission TSV. The fusing is represented in Figure 5 as ‘1' or '0' (where ' 1' indicates a defect location and '0' indicates a location having no defect). In this implementation, defect location bits are used as mux/demux selection bits. However, embodiments are not limited to this particular implementation of the selection data for the multiplexer and de-multiplexer operations.

[0045] **Figure 6** is an illustration of an embodiment of an apparatus or system providing for use of data of spare TSVs to substitute for data from defective TSVs. In some embodiments, a memory apparatus or system 600 includes a plurality of TSVs 610 to transfer functional values 605, where the TSVs include one or more spare TSVs 615 for use in the self-repair of defective TSV operation. In this illustration, TSV 620 is defective, and as a result the data intended for such TSV has instead been transmitted via a substitute TSV of the one or more spare TSVs 615. In some embodiments, the apparatus or system 600 includes a demultiplexer 650 for use in directing the data received from the spare TSVs 615 to the correct location for the defective TSV 620. While not included in this illustration, the selection of for the demultiplexer may include fusing as illustrated in Figure 5.

[0046] **Figure 7** is an illustration of identification of defective TSVs in a device or system. In this illustration, a plurality of TSVs 710 may include one or more defective 720 TSVs. At a point in time, a test of the TSVs may occur, where the testing may include the use of BIST circuitry in the memory die elements of the apparatus of system. In this illustration, a test sequence may include the input of various inputs 705, including all T . In this illustration, the defective TSV 720 provides an erroneous '0' value in outputs 735. In some embodiments, the apparatus or system operates to identify the TSV 720 as defective, and to utilize such information to provide for self-repair of the operation of the TSV.

[0047] In some embodiments, for dynamic repair a BIST engine may be run as a part of the initial firmware bring up/Reset sequence. In some embodiments, hardware may be implemented to detect the failing channel dynamically. For example, the hardware implementation may include a counter to keep track of a number of read mismatches, and a comparator is implemented to compare expected number of reads with total read mismatches. If the number of mismatches equals the expected number, then the failing TSV channel can be identified. As an example, a DRAM may have four entries with each entry having a width of 32. In this example, the BIST engine writes all 1's to each entry and reads each entry of the 4 entries back. If read mismatch = 4 and if all the mismatches are indicated to the same failing bit (say data bit 25), then the TSV channel corresponding to data bit 25

is the failing and needs to be replaced. In some embodiments, once the failing channel location is identified, mux/demux select bits may be programmed in one of multiple different ways such as firmware, uCode, or any other data bit programming method.

[0048] **Figure 8** is a flowchart to illustrate an embodiment of a process for using spare TSVs in a stacked memory device to repair operations of defective TSVs. In this illustration, testing may be conducted for a stacked memory device 805, where the stacked memory device includes spare TSVs and logic to provide for self-repair of defective TSV operation. In some embodiments, there may be testing to determine whether one or more defective TSVs have been identified in the stacked memory device 810. If no defective TSVs have been identified, normal operation may be commenced or continued 815, which, depending on the implementation, may be followed by period retesting of the memory device 805, such as testing on start up of the apparatus or system containing the memory device.

[0049] In some embodiments, the testing of TSVs may vary depending on the self-repair implementation. In some embodiments, the testing may include the generation of error correction bits for transmission via the one or more spare TSVs. In some embodiments, the testing may include testing utilizing BIST circuitry of the memory device.

[0050] In some embodiments, if one or more defective TSVs are identified 810, then operations are implemented to provide self-repair of the operation of the defective TSVs using the one or more spare TSVs 820.

[005 1] In some embodiments (shown as Process A), the self-repair includes receiving the generated error correction bits that are transmitted via the spare TSVs 825. In some embodiments, corrected data for the defective TSVs is generated using error correction logic 830, where the corrected data is based upon the received data and error correction data. The memory device operation then proceeds using the corrected data 835, allowing commencement or continuation of normal operation of the memory device 815.

[0052] In some embodiments (shown as Process B), the self-repair includes identifying a spare TSV for each defective TSV 850, and setting a multiplexer (or other logic elements) to direct data intended for the defective TSV to

the spare TSV 855. In some embodiments, a demultiplexer is set to direct data from the identified spare TSVs to the appropriate data connections for the one or more defective TSVs 860. The memory device operation then proceeds using the spare TSV data path 865, allowing commencement or continuation of normal operation of the memory device 815.

[0053] **Figure 9** is an illustration of an embodiment of an apparatus or system including elements for repair of operations of defective TSVs using spare TSVs. Computing device 900 represents a computing device including a mobile computing device, such as a laptop computer, a tablet computer (including a device having a touchscreen without a separate keyboard; a device having both a touchscreen and keyboard; a device having quick initiation, referred to as "instant on" operation; and a device that is generally connected to a network in operation, referred to as "always connected"), a mobile phone or smart phone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain of the components are shown generally, and not all components of such a device are shown in device 900. The components may be connected by one or more buses or other connections 905.

[0054] Device 900 includes processor 910, which performs the primary processing operations of device 900. Processor 910 can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 910 include the execution of an operating platform or operating system on which applications, device functions, or both are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, operations, or both related to connecting device 900 to another device. The processing operations may also include operations related to audio I/O, display I/O, or both.

[0055] In one embodiment, device 900 includes audio subsystem 920, which represents hardware (such as audio hardware and audio circuits) and software (such as drivers and codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker, headphone, or both such audio output, as well as microphone input. Devices for such functions can be

integrated into device 900, or connected to device 900. In one embodiment, a user interacts with device 900 by providing audio commands that are received and processed by processor 910.

[0056] Display subsystem 930 represents hardware (such as display devices) and software (such as drivers) components that provide a display having visual, tactile, or both elements for a user to interact with the computing device. Display subsystem 930 includes display interface 932, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 932 includes logic separate from processor 910 to perform at least some processing related to the display. In one embodiment, display subsystem 930 includes a touch screen device that provides both output and input to a user.

[0057] I/O controller 940 represents hardware devices and software components related to interaction with a user. I/O controller 940 can operate to manage hardware that is part of audio subsystem 920, a display subsystem 930, or both such subsystems. Additionally, I/O controller 940 illustrates a connection point for additional devices that connect to device 900 through which a user might interact with the system. For example, devices that can be attached to device 900 might include microphone devices, speaker or stereo systems, video systems or other display device, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0058] As mentioned above, I/O controller 940 may interact with audio subsystem 920, display subsystem 930, or both such subsystems. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of device 900. Additionally, audio output can be provided instead of or in addition to display output. In another example, if display subsystem includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 940. There can also be additional buttons or switches on device 900 to provide I/O functions managed by I/O controller 940.

[0059] In one embodiment, I/O controller 940 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in device 900. The input can be part of direct user

interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0060] In one embodiment, device 900 includes power management 950 that manages battery power usage, charging of the battery, and features related to power saving operation.

[0061] In some embodiments, memory subsystem 960 includes memory devices for storing information in device 900. The processor 910 may read and write data to elements of the memory subsystem 960. Memory can include nonvolatile (having a state that does not change if power to the memory device is interrupted), volatile (having a state that is indeterminate if power to the memory device is interrupted) memory devices, or both such memories. Memory 960 can store application data, user data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of system 900.

[0062] In some embodiments, the memory subsystem 960 may include a stacked memory device 962, where the stacked memory device includes one or more memory die layers and a system element. In some embodiments, the stacked memory device 962 include spare TSV self-repair logic 964, where the self-repair logic 964 provides for replacement of the operation of defective TSVs using the spare TSVs of the stacked memory device.

[0063] Connectivity 970 includes hardware devices (e.g., connectors and communication hardware for wireless communication, wired communication, or both) and software components (e.g., drivers, protocol stacks) to enable device 900 to communicate with external devices. The device could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[0064] Connectivity 970 can include multiple different types of connectivity. To generalize, device 900 is illustrated with cellular connectivity 972 and wireless connectivity 974. Cellular connectivity 972 refers generally to cellular network connectivity provided by wireless carriers, such as provided via 4G/LTE (Long Term Evolution), GSM (global system for mobile communications) or

variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity 974 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth), local area networks (such as WiFi), wide area networks (such as WiMax), and other wireless communications. Connectivity may include one or more omnidirectional or directional antennas 976.

[0065] Peripheral connections 980 include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that device 900 could both be a peripheral device ("to" 982) to other computing devices, as well as have peripheral devices ("from" 984) connected to it. Device 900 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (such as downloading, uploading, changing, or synchronizing) content on device 900. Additionally, a docking connector can allow device 900 to connect to certain peripherals that allow device 900 to control content output, for example, to audiovisual or other systems.

[0066] In addition to a proprietary docking connector or other proprietary connection hardware, device 900 can make peripheral connections 980 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other type.

[0067] **Figure 10** illustrates an embodiment of a computing system including stacked memory having elements for repair of operations of defective TSVs using spare TSVs. The computing system may include a computer, server, game console, or other computing apparatus. In this illustration, certain standard and well-known components that are not germane to the present description are not shown. Under some embodiments, the computing system 1000 comprises an interconnect or crossbar 1005 or other communication means for transmission of data. The computing system 1000 may include a processing means such as one or more processors 1010 coupled with the interconnect 1005 for processing

information. The processors 1010 may comprise one or more physical processors and one or more logical processors. The interconnect 1005 is illustrated as a single interconnect for simplicity, but may represent multiple different interconnects or buses and the component connections to such interconnects may vary. The interconnect 1005 shown in Figure 10 is an abstraction that represents any one or more separate physical buses, point-to-point connections, or both connected by appropriate bridges, adapters, or controllers.

[0068] In some embodiments, the computing system 1000 further comprises a random access memory (RAM) or other dynamic storage device or element as a main memory 1012 for storing information and instructions to be executed by the processors 1010. RAM memory includes dynamic random access memory (DRAM), which requires refreshing of memory contents, and static random access memory (SRAM), which does not require refreshing contents, but at increased cost. In some embodiments, main memory may include active storage of applications including a browser application for using in network browsing activities by a user of the computing system. DRAM memory may include synchronous dynamic random access memory (SDRAM), which includes a clock signal to control signals, and extended data-out dynamic random access memory (EDO DRAM). In some embodiments, memory of the system may include certain registers or other special purpose memory.

[0069] In some embodiments, the main memory 1012 includes stacked memory 1014, wherein the stacked memory includes spare TSV self-repair logic 1015.

[0070] The computing system 1000 also may comprise a read only memory (ROM) 1016 or other static storage device for storing static information and instructions for the processors 1010. The computing system 1000 may include one or more non-volatile memory elements 1018 for the storage of certain elements.

[0071] In some embodiments, the computing system 1000 includes one or more input devices 1030, where the input devices include one or more of a keyboard, mouse, touch pad, voice command recognition, gesture recognition, or other device for providing an input to a computing system.

[0072] The computing system 1000 may also be coupled via the interconnect 1005 to an output display 1040. In some embodiments, the display 1040 may include a liquid crystal display (LCD) or any other display technology, for displaying information or content to a user. In some environments, the display 1040 may include a touch-screen that is also utilized as at least a part of an input device. In some environments, the display 1040 may be or may include an audio device, such as a speaker for providing audio information.

[0073] One or more transmitters or receivers 1045 may also be coupled to the interconnect 1005. In some embodiments, the computing system 1000 may include one or more ports 1050 for the reception or transmission of data. The computing system 1000 may further include one or more omnidirectional or directional antennas 1055 for the reception of data via radio signals.

[0074] The computing system 1000 may also comprise a power device or system 1060, which may comprise a power supply, a battery, a solar cell, a fuel cell, or other system or device for providing or generating power. The power provided by the power device or system 1060 may be distributed as required to elements of the computing system 1000.

[0075] In the description above, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some of these specific details. In other instances, well-known structures and devices are shown in block diagram form. There may be intermediate structure between illustrated components. The components described or illustrated herein may have additional inputs or outputs which are not illustrated or described.

[0076] Various embodiments may include various processes. These processes may be performed by hardware components or may be embodied in computer program or machine-executable instructions, which may be used to cause a general-purpose or special-purpose processor or logic circuits programmed with the instructions to perform the processes. Alternatively, the processes may be performed by a combination of hardware and software.

[0077] Portions of various embodiments may be provided as a computer program product, which may include a non-transitory computer-readable storage medium having stored thereon computer program instructions, which may be used to program a computer (or other electronic devices) for execution by one or more processors to perform a process according to certain embodiments. The computer-readable medium may include, but is not limited to, floppy diskettes, optical disks, compact disk read-only memory (CD-ROM), and magneto-optical disks, read-only memory (ROM), random access memory (RAM), erasable programmable read-only memory (EPROM), electrically-erasable programmable read-only memory (EEPROM), magnet or optical cards, flash memory, or other type of computer-readable medium suitable for storing electronic instructions. Moreover, embodiments may also be downloaded as a computer program product, wherein the program may be transferred from a remote computer to a requesting computer.

[0078] Many of the methods are described in their most basic form, but processes can be added to or deleted from any of the methods and information can be added or subtracted from any of the described messages without departing from the basic scope of the present invention. It will be apparent to those skilled in the art that many further modifications and adaptations can be made. The particular embodiments are not provided to limit the invention but to illustrate it. The scope of the embodiments of the present invention is not to be determined by the specific examples provided above but only by the claims below.

[0079] If it is said that an element "A" is coupled to or with element "B," element A may be directly coupled to element B or be indirectly coupled through, for example, element C. When the specification or claims state that a component, feature, structure, process, or characteristic A "causes" a component, feature, structure, process, or characteristic B, it means that "A" is at least a partial cause of "B" but that there may also be at least one other component, feature, structure, process, or characteristic that assists in causing "B." If the specification indicates that a component, feature, structure, process, or characteristic "may", "might", or "could" be included, that particular component, feature, structure, process, or characteristic is not required to be included. If the specification or claim

refers to "a" or "an" element, this does not mean there is only one of the described elements.

[0080] An embodiment is an implementation or example of the present invention. Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. It should be appreciated that in the foregoing description of exemplary embodiments of the present invention, various features are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims are hereby expressly incorporated into this description, with each claim standing on its own as a separate embodiment of this invention.

CLAIMS

What is claimed is:

1. A memory device comprising:
a memory stack having one or more memory die elements, including a first memory die element; and
a system element coupled with the memory stack;
wherein the first memory die element includes:
a plurality of through silicon vias (TSVs), the plurality of TSVs including a plurality of data TSVs and one or more spare TSVs, and
self-repair logic to repair operation of a defective TSV of the plurality of data TSVs, the repair of operation of the defective TSV including utilization of the one or more spare TSVs.

2. The memory device of claim 1, wherein the self-repair logic includes an error correction code generator to generate an error correction code based on data for the data TSVs, the error correction code to be transferred via the one or more spare TSVs.

3. The memory device of claim 2, wherein the self-repair logic further includes error correction logic to generate corrected data for the defective TSV.

4. The memory device of claim 1, wherein the self-repair logic includes a detection element to detect the defective TSV.

5. The memory device of claim 4, wherein the self-repair logic includes a multiplexer element to direct data intended for the defective TSV to a first spare TSV.

6. The memory device of claim 5, wherein the self-repair logic further includes a demultiplexer element to direct data received on the first spare TSV to a connection for the defective TSV.

7. The memory device of claim 1, wherein the self-repair logic provides for static repairs of operation of defective TSVs in manufacture of the memory device.

8. The memory device of claim 1, wherein the self-repair logic provides for dynamic repairs of operation of defective TSVs in operation of the memory device.

9. The memory device of claim 1, wherein the memory device is a WidelO compatible device.

10. A method comprising:

conducting a test of a stacked memory device, the stacked memory stack including one or more memory die elements, a system element coupled with the memory stack, and a plurality of through silicon vias (TSVs);

detecting one or more defective TSVs of the plurality of TSVs; and

repairing operation of the one or more defective TSVs, the repair of operation including utilization of the one or more spare TSVs.

11. The method of claim 10, wherein repairing operation of the one or more defective TSVs includes generating an error correction code based on data for the data TSVs.

12. The method of claim 11, further comprising transferring the error correction code via the one or more spare TSVs.

13. The method of claim 10, further comprising generating corrected data for the one or more defective TSVs.

14. The method of claim 10, wherein repairing the operation of the one or more defective TSVs includes directing data intended for a first defective TSV to a first spare TSVs

15. The method of claim 14, wherein repairing the operation of the one or more defective TSVs further includes directing data received on the first spare TSV to a connection for the first defective TSV.

16. The method of claim 10, wherein repairing the operation of the one or more defective TSVs includes static repair in manufacture of the stacked memory device.

17. The method of claim 10, wherein repairing the operation of the one or more defective TSVs includes dynamic in operation of the memory device.

18. A system comprising:
a processor to process data of the system;
a transmitter, receiver, or both coupled with an omnidirectional antenna to transmit data, receive data, or both; and
a memory to store data, the memory including a stacked memory device, the stacked memory device including:
a memory stack having one or more memory die elements, including a first memory die element, and
a system element coupled with the memory stack, wherein the first memory die element includes:
a plurality of through silicon vias (TSVs), the plurality of TSVs including a plurality of data TSVs and one or more spare TSVs, and
self-repair logic to repair operation of a defective TSV of the plurality of data TSVs, the repair including utilization of the one or more spare TSVs.

19. The system of claim 18, wherein the self-repair logic includes an error correction code generator to generate an error correction code based on data for the data TSVs, the error correction code to be transferred via the one or more spare TSVs.

20. The system of claim 19, wherein the self-repair logic further includes error correction logic to generate corrected data for the defective TSV.

21. The system of claim 18, wherein the self-repair logic includes a detection element to detect the defective TSV.

22. The system of claim 21, wherein the self-repair logic includes a multiplexer element to direct data intended for the defective TSV to a first spare TSV.

23. The system of claim 22, wherein the self-repair logic further includes a demultiplexer element to direct data received on the first spare TSV to a connection for the defective TSV.

24. The system of claim 18, wherein the system is a mobile device.

25. The system of claim 24, wherein the mobile device is a tablet computer.

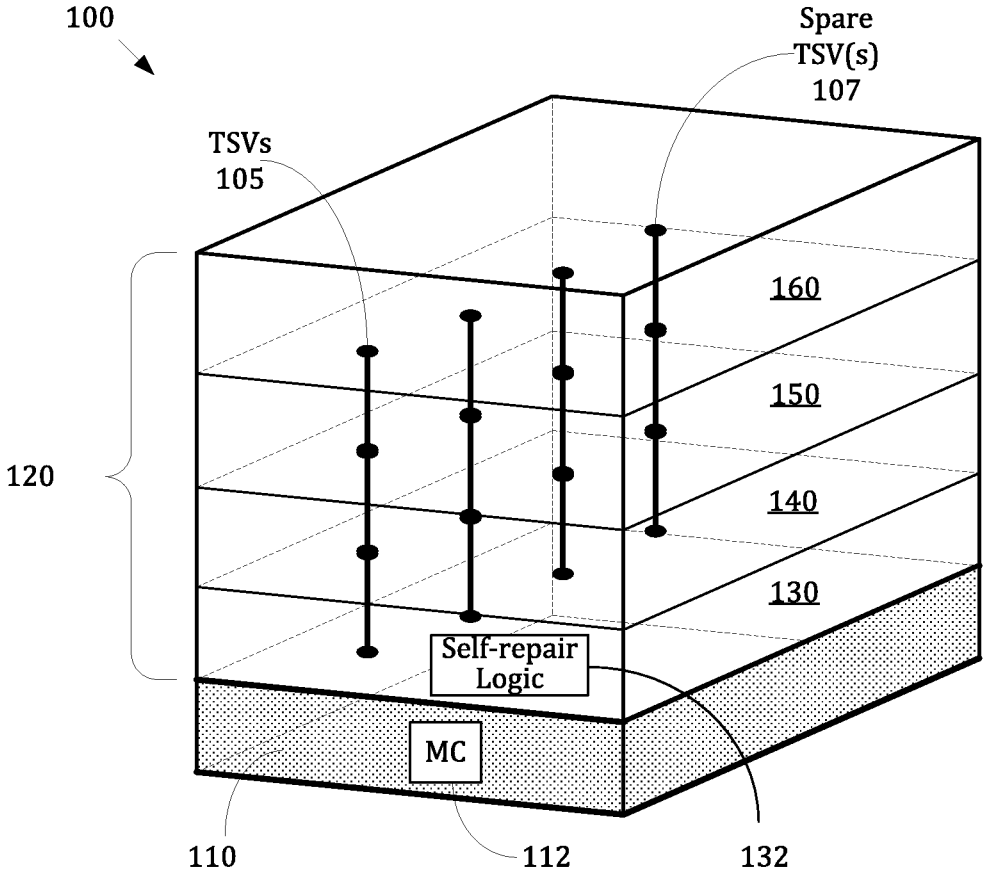

100
Spare
TSV(s)
107
TSVs
105
160
150
140
130
120
Self-repair
Logic
MC
110
112
132

Fig. 1

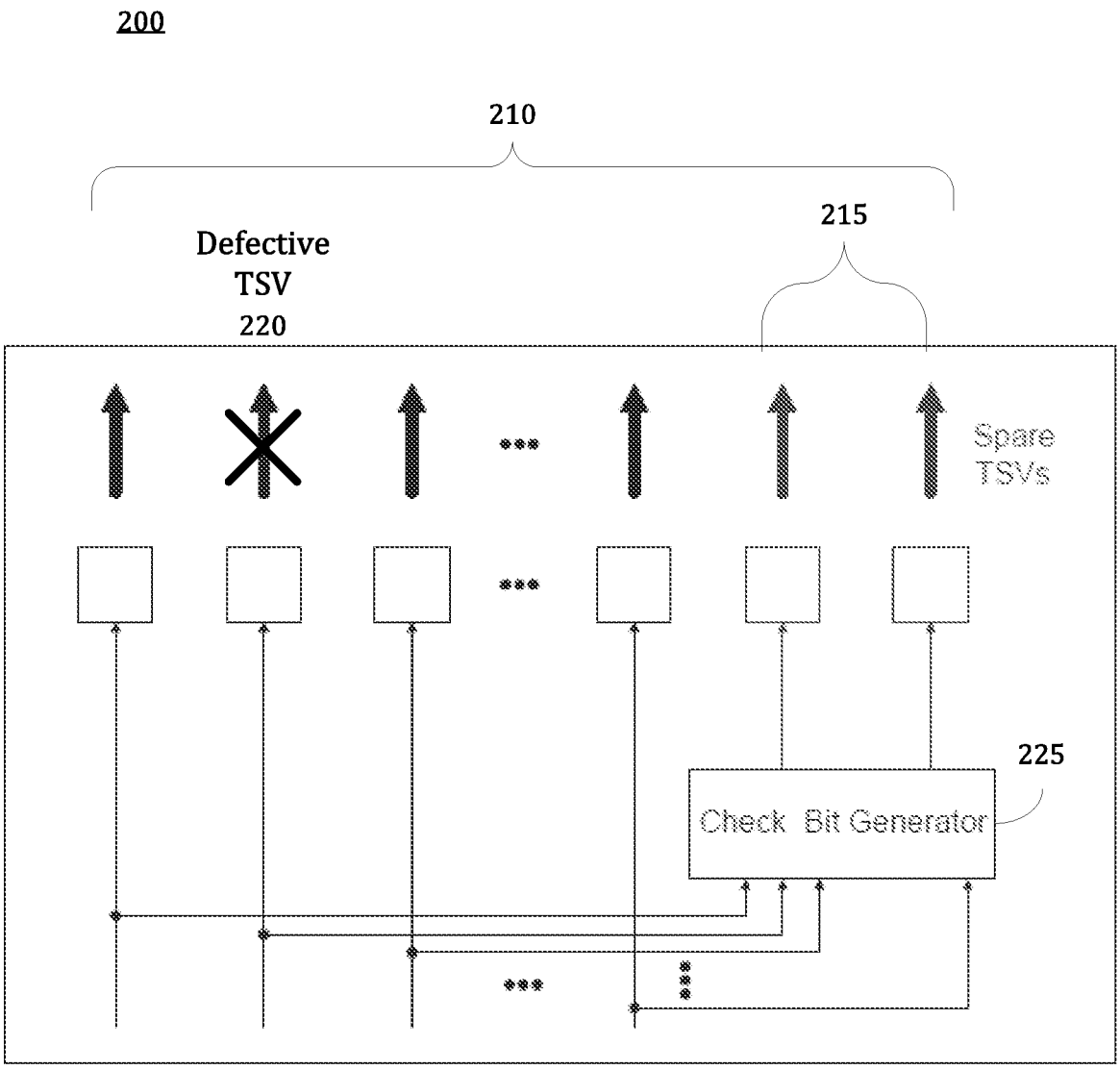

200
210
215
Defective
TSV
220
Spare
TSVs
225
Check Bit Generator

Fig. 2

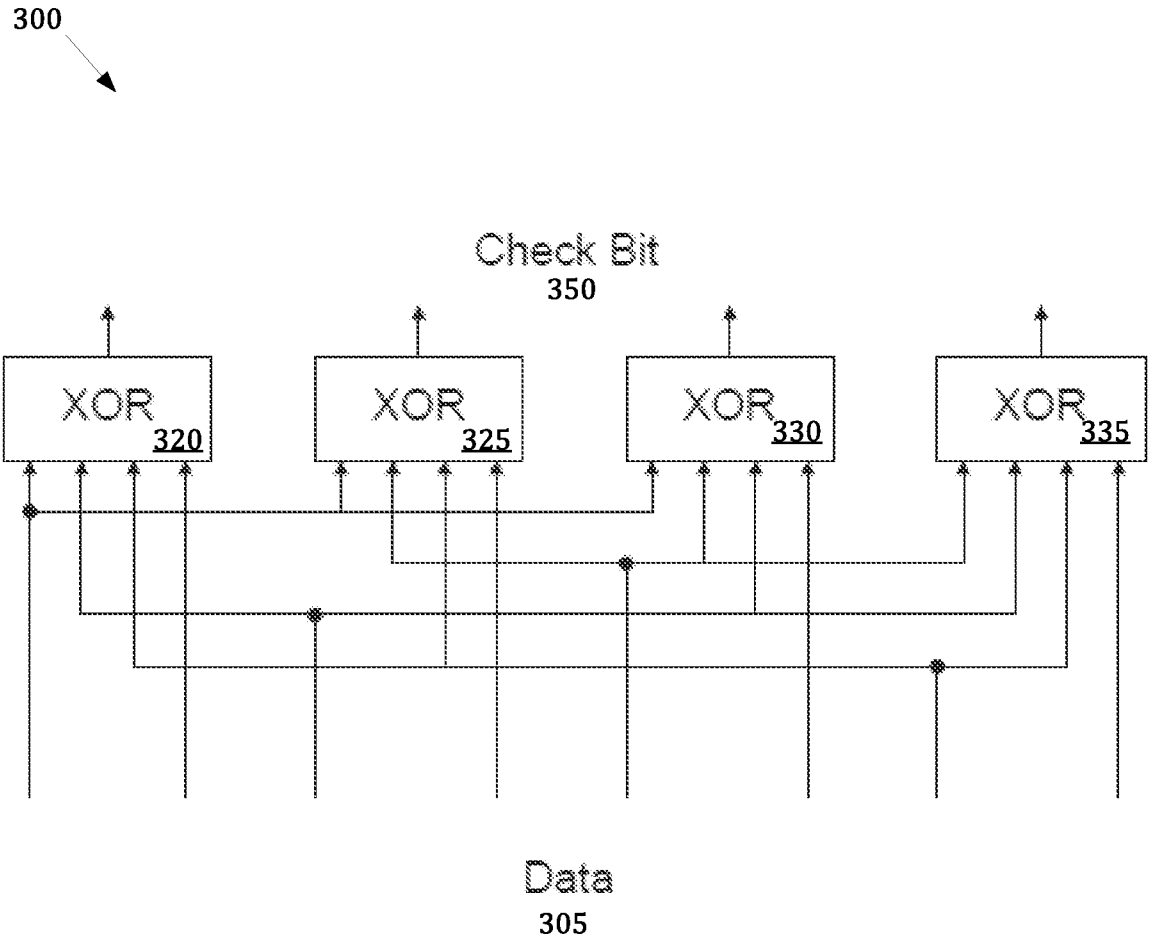


Fig. 3

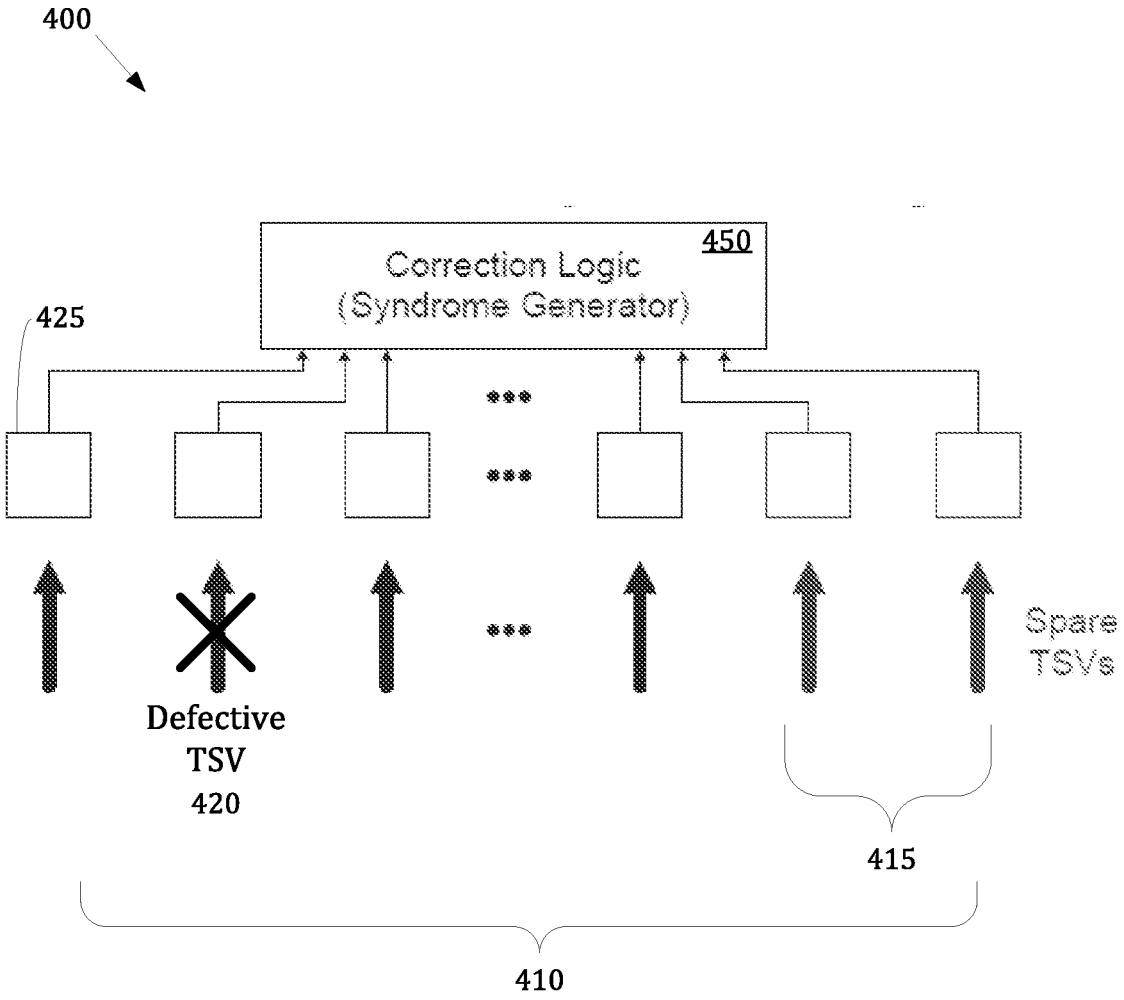

400
450
Correction Logic
(Syndrome Generator)
425
Spare
TSVs
Defective
TSV
420
415
410

Fig. 4

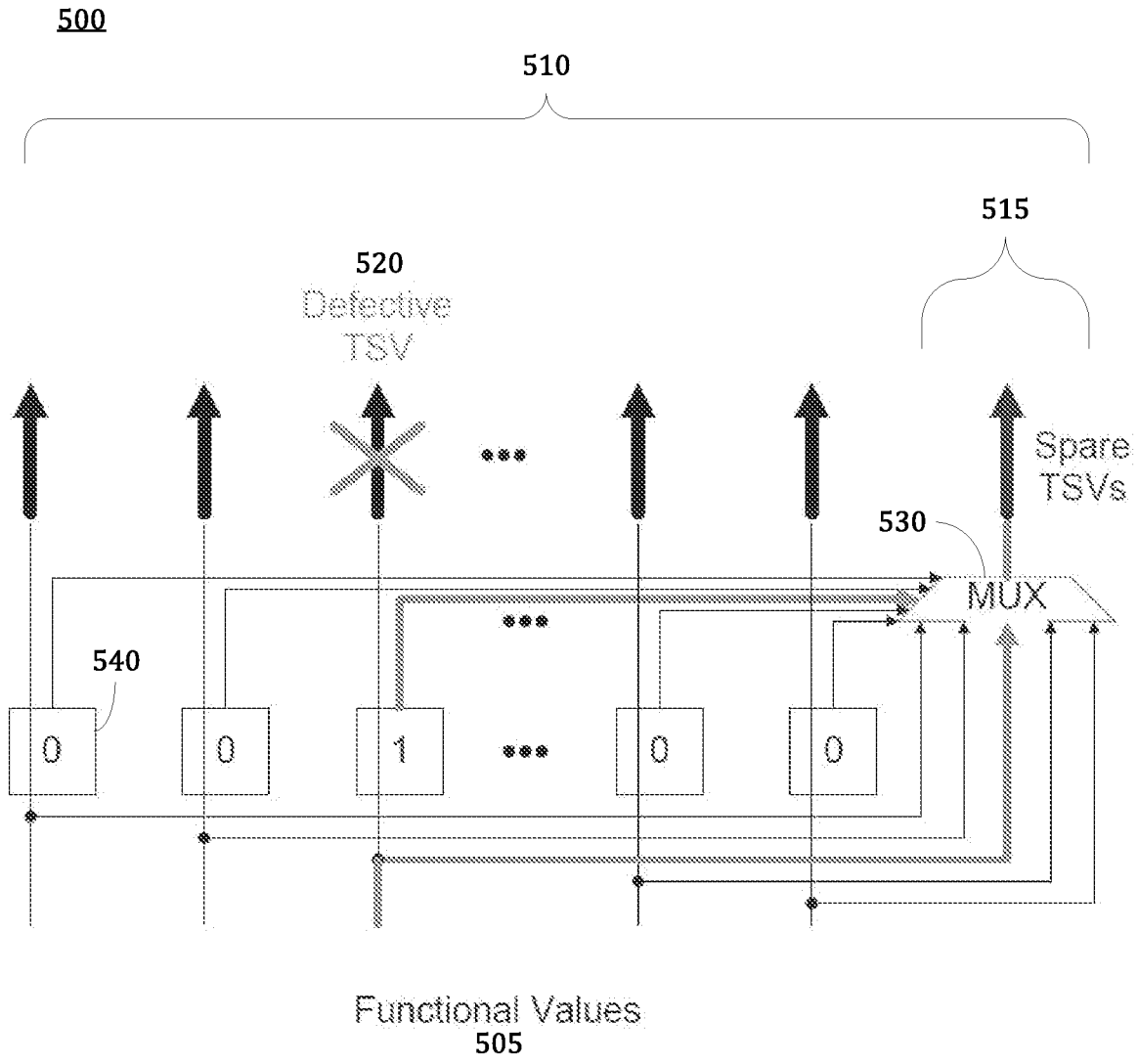

500
510
515
520
Defective TSV
Spare TSVs
530
MUX
540
0
0
1
0
0
Functional Values
505

Fig. 5

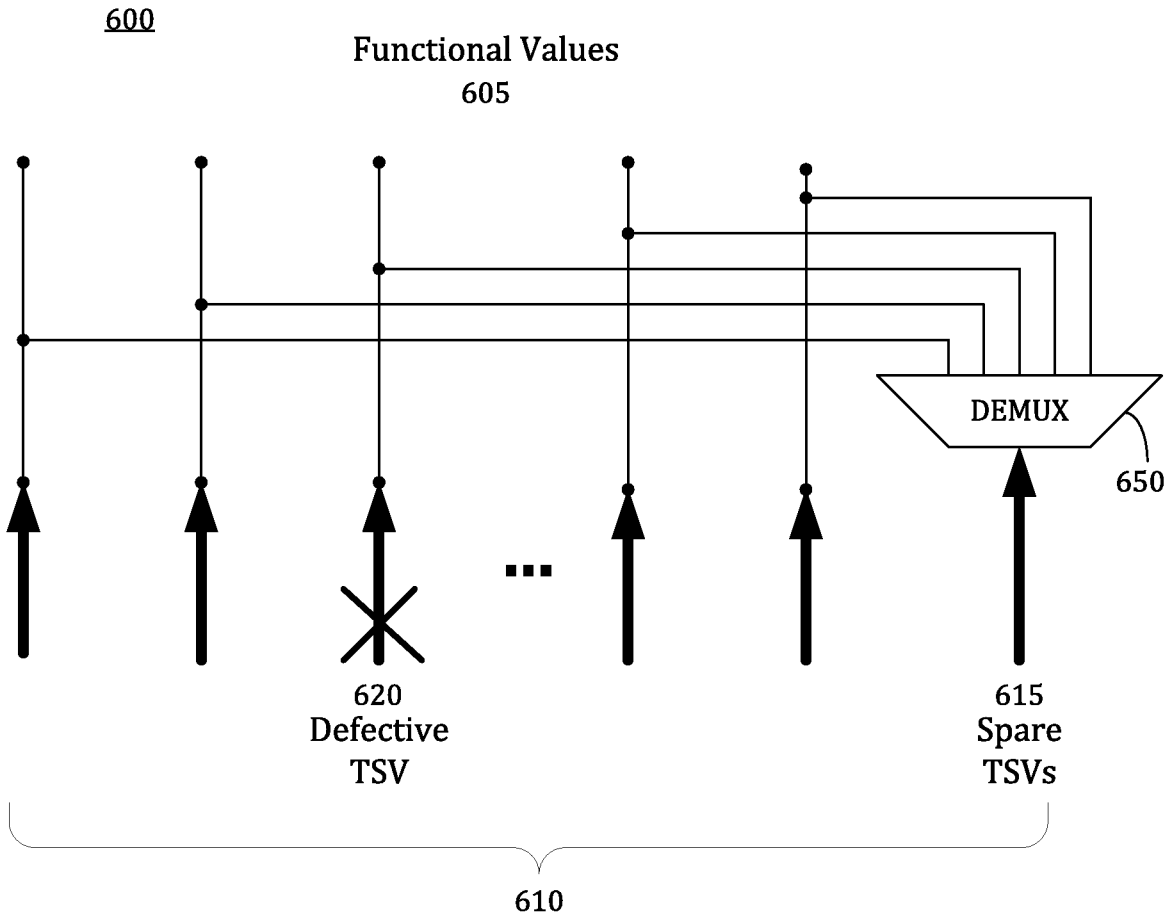

600
Functional Values
605
DEMUX
650
620
Defective
TSV
615
Spare
TSVs
610

Fig. 6

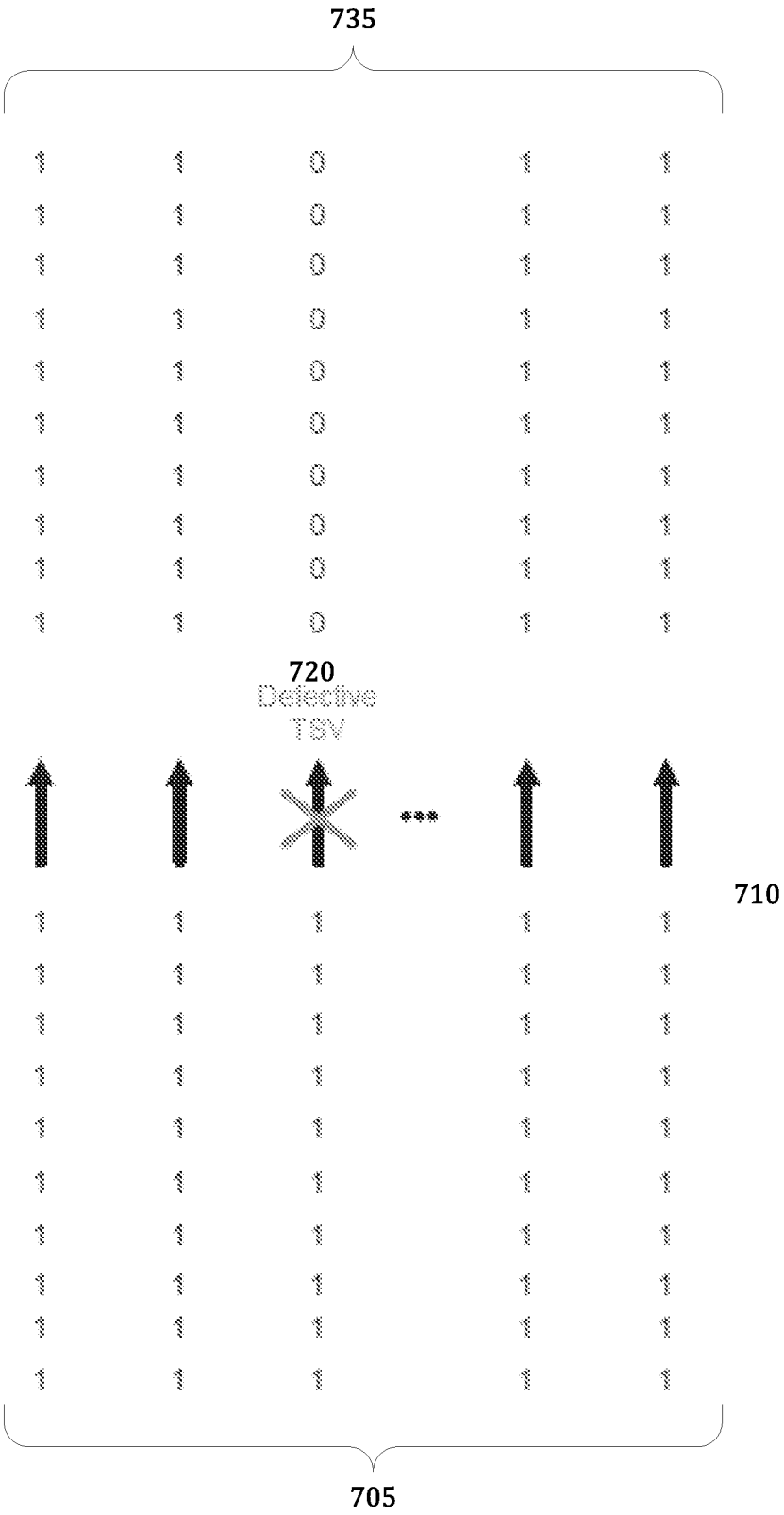

735
1 1 0 1 1
1 1 0 1 1
1 1 0 1 1
1 1 0 1 1
1 1 0 1 1
1 1 0 1 1
1 1 0 1 1
1 1 0 1 1
1 1 0 1 1
1 1 0 1 1
720
Defective
TSV
710
1 1 1 1 1
1 1 1 1 1
1 1 1 1 1
1 1 1 1 1
1 1 1 1 1
1 1 1 1 1
1 1 1 1 1
1 1 1 1 1
1 1 1 1 1
1 1 1 1 1
705

Fig. 7

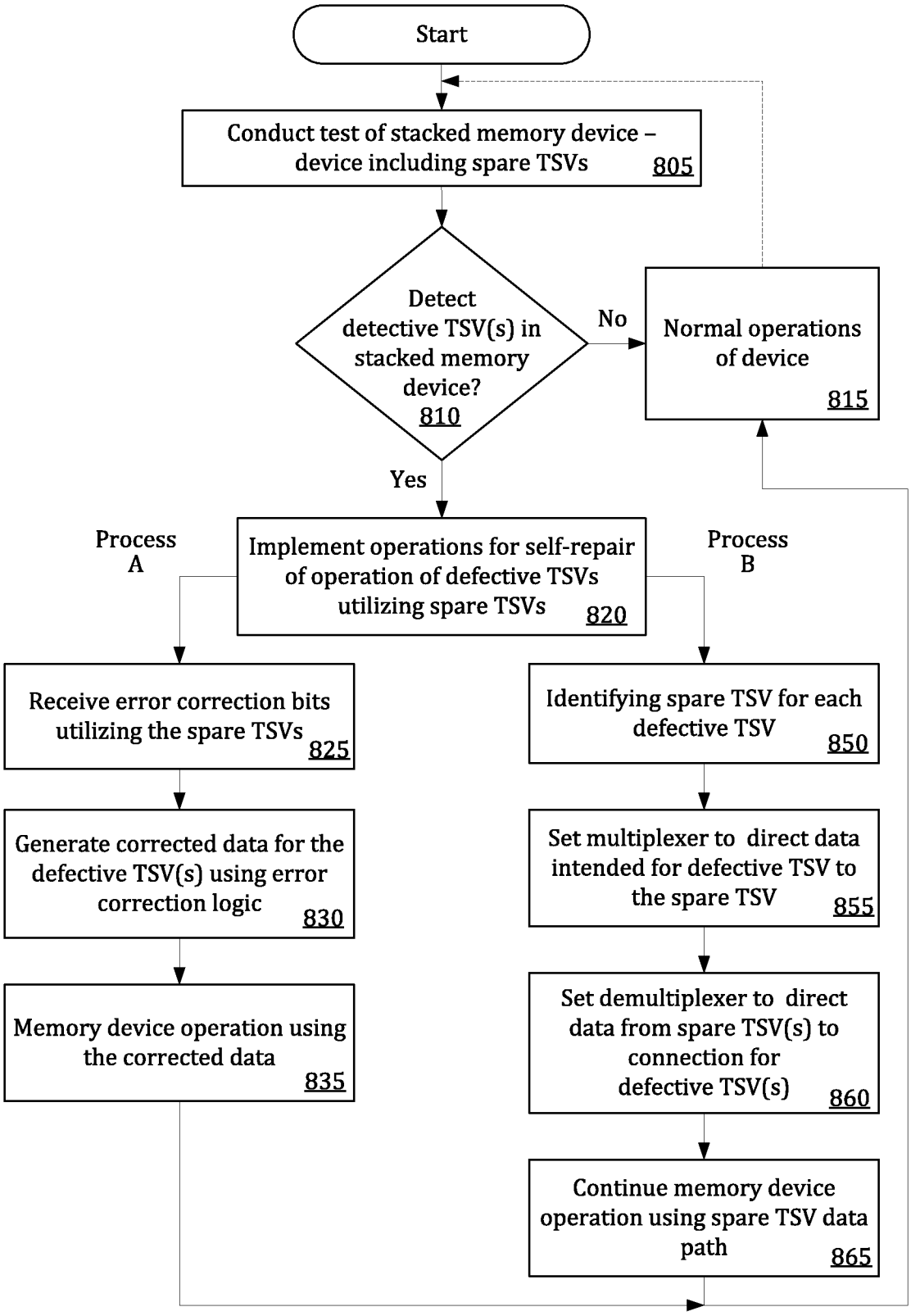

Start
Conduct test of stacked memory device – device including spare TSVs 805
Detect detective TSV(s) in stacked memory device? 810
No
Normal operations of device 815
Yes
Process A
Implement operations for self-repair of operation of defective TSVs utilizing spare TSVs 820
Process B
Receive error correction bits utilizing the spare TSVs 825
Generate corrected data for the defective TSV(s) using error correction logic 830
Memory device operation using the corrected data 835
Identifying spare TSV for each defective TSV 850
Set multiplexer to direct data intended for defective TSV to the spare TSV 855
Set demultiplexer to direct data from spare TSV(s) to connection for defective TSV(s) 860
Continue memory device operation using spare TSV data path 865

Fig. 8

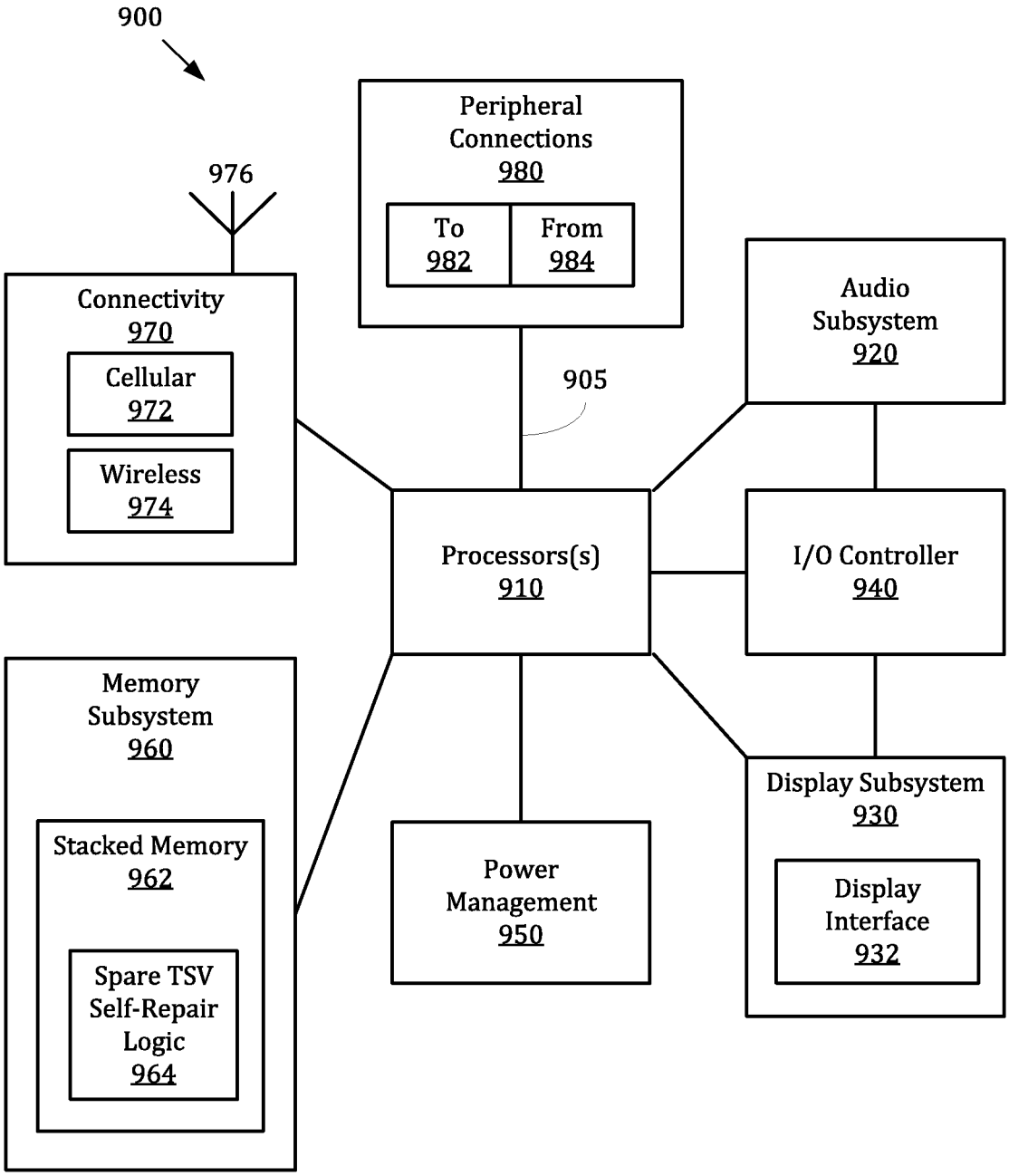

900
976
Peripheral Connections 980
To 982
From 984
Audio Subsystem 920
Connectivity 970
Cellular 972
Wireless 974
905
Processors(s) 910
I/O Controller 940
Memory Subsystem 960
Stacked Memory 962
Spare TSV Self-Repair Logic 964
Power Management 950
Display Subsystem 930
Display Interface 932

Fig. 9

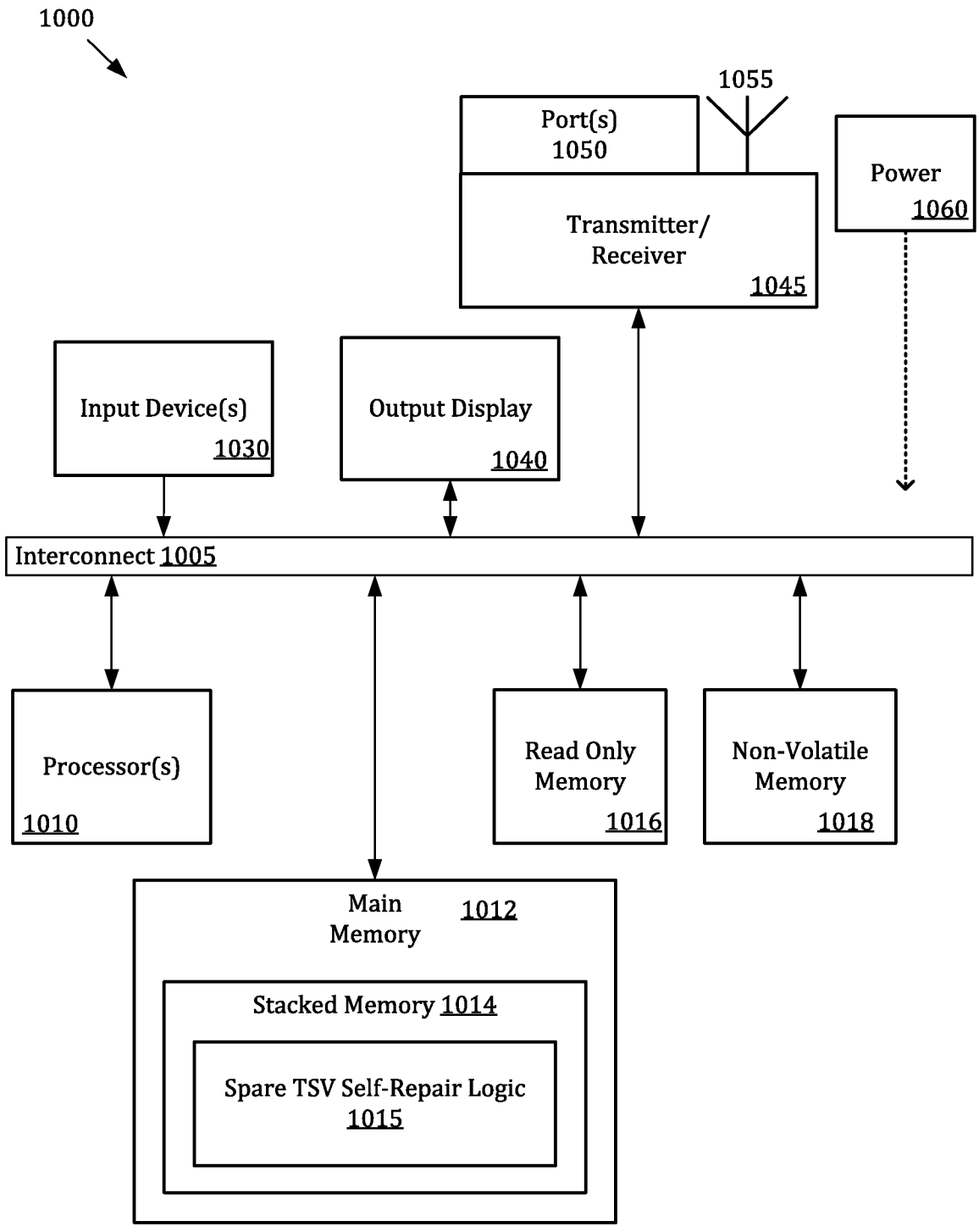

1000
1055
Port(s)
1050
Power
1060
Transmitter/
Receiver
1045
Input Device(s)
1030
Output Display
1040
Interconnect 1005
Processor(s)
1010
Read Only
Memory
1016
Non-Volatile
Memory
1018
Main
Memory
1012
Stacked Memory 1014
Spare TSV Self-Repair Logic
1015

Fig. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US20 11/067283

A. CLASSIFICATION OF SUBJECT MATTER

GllC 29/00(2006.01)i, GllC 29/42(2006.01)1, HOIL 23/48(2006.01)1, GllC 5/02(2006.01)1, GllC 5/06(2006.01)1

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 29/00; H03M 13/09; G01R 31/26; G06F 12/06; GllC 5/02; G06F 11/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:memory,stack,error,defect*,repair*,correct*,recover,TSV,via,die

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010-0005376 Al (LABERGE PAUL A. et al.) 07 January 2010 See Paragraphs [0012H0031] and Figures 1-3.	1-25
A	US 2008-0101104 Al (IKEDA HIROAKI) 01 May 2008 See Paragraphs [0047H0064] and Figure 3A.	1-25
A	US 2009-0096478 Al (KEETH BRENT) 16 April 2009 See Paragraphs [0024H0065] and Figures 4, 7.	1-25
A	US 2010-0070696 Al (BLANKENSHIP DENNIS) 18 March 2010 See Paragraphs [0021H0039], Claim 13 and Figures 2-3.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 AUGUST 2012 (29.08.2012)	**30 AUGUST 2012 (30.08.2012)**

Name and mailing address of the ISA/KR

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Facsimile No. 82-42-472-7140

Authorized officer

Son, June Young

Telephone No. 82-42-481-5720

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US20 11/067283

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