



(51) International Patent Classification:

H05K 3/34 (2006.01) H05K 1/11 (2006.01)

H05K 3/12 (2006.01) H05K 1/09 (2006.01)

(21) International Application Number:

PCT/US2023/017446

(22) International Filing Date:

04 April 2023 (04.04.2023)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

17/714,837 06 April 2022 (06.04.2022) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT,

(54) Title: MICRO SOLDER JOINT AND STENCIL APERTURE DESIGN

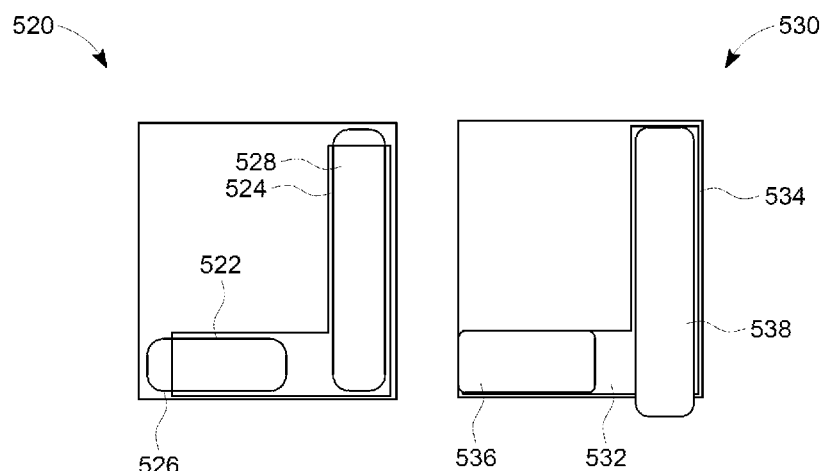


FIG. 13

(57) Abstract: Micro solder joint and stencil design. In one embodiment, a stencil for depositing solder on a printed circuit board (PCB) includes a plurality of stencil apertures, a first stencil aperture of the plurality of apertures having an aperture wall defining an aperture perimeter. The aperture wall is configured to not extend beyond an outer edge of a PCB pad provided on the printed circuit board, the aperture wall is also configured to not extend beyond an outer edge of a terminal of a surface mount component, and the first stencil aperture is configured to receive solder paste to form a non-convex solder joint between the PCB pad and the terminal.

LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE,
SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- *with international search report (Art. 21(3))*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

MICRO SOLDER JOINT AND STENCIL APERTURE DESIGN

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims the benefit of and hereby incorporates by reference, for all purposes, the entirety of the contents of U.S. Nonprovisional Application No. 17/714,837, filed April 6, 2022, and entitled “MICRO SOLDER JOINT AND STENCIL APERTURE DESIGN”.

FIELD

[0002] This application relates generally to a solder paste stencil and, more particularly, to a solder paste stencil with an aperture that has the same length as a surface-mount circuit component to provide a non-convex micro solder joint.

BACKGROUND

[0003] FIG. 1 is a crack formation image 100 illustrating a crack 101 in a convex solder joint 102. The reliability of solder joints is a common issue in the surface-mount technology (SMT) process, and in particular, in power management integrated circuits (PMIC), due to the miniaturization of the solder joints. As illustrated in FIG. 1, a terminal 104 of a quad-flat-no-lead (QFN) package is surface mounted to a printed circuit board (PCB) pad 106 via solder paste. Commonly, the solder paste contacts a non-solderable side surface of the terminal 104. During a reflow process, the solder is heated to form a bond between the QFN terminal 104 and the PCB pad 106.

[0004] During repeated thermal cycles, the crack 101 of the crack formation image 100 of FIG. 1 is formed due to thermal expansion and contraction. For example, the crack may be formed after 500 thermal cycles. The crack 101 formed at the interface of the convex solder joint 102 and QFN terminal 104 and propagated inward further along the interface and, in some cases, the crack may propagate along a surface of the terminal 104 that is parallel to and facing a surface of the PCB pad 106. The convex solder joint 102 may lead to excessive stress on the interface as well as reduction in performance.

[0005] FIG. 2 is an image 110 illustrating another example of the convex solder joint 112. A side surface 111 of a QFN package and QFN terminals 114 is not plated with a tin (Sn) coating like a surface of the QFN package 114 that faces the PCB pad, thus a copper (Cu) region is exposed to the solder joint 112 during a reflow process. The side surface 111 may be prone to oxide formations as a result of oxidation during storage and shipment of the QFN package. The oxide formations may inhibit a metallurgical reaction during soldering, thus, promoting cracking of the convex solder joint 112. Additionally, during thermal cycles, the interface of the solder

joint 112 and the terminal 114 may react with one another causing a brittle intermetallic compound (e.g., Ni_3Sn , Ni_3Sn_2 , Ni_3Sn_4 , NiSn_3 , Cu_6Sn_5 , Cu_3Sn) to be produced. The crack may then propagate due to the expansion direction of the convex shape of the solder joint 112, thus, causing a disruption in the electrical functionality (i.e., a reduction in performance) of the QFN package. For example, the QFN package may be used as the main power input source on a circuit board. Consequently, a faulty connection may be a result of the crack forming and increasing on the convex solder joint 112.

SUMMARY

[0006] To overcome the crack from forming and propagating along an interface of the terminal of the QFN package and the solder joint, a solder paste stencil aperture that leads to a concave solder joint is needed to improve the performance of the solder joint, and therefore, the performance of the QFN package. A curvature of a solder fillet influences the stress state of the solder joint. The curvature of the solder fillet may be controlled by parameters such as dimensions of a stencil aperture and application of solder paste to a surface of the terminal that faces the PCB pad, and not to a side surface of the terminal. It is advantageous to provide a stencil aperture with dimensions that ensures a concave solder fillet (instead of the typical convex solder fillet), which in turn, provides a minimized stress concentration, thus, providing an increase in performance of the QFN package. The stencil aperture of the present disclosure may lead to a reduction in cost because the performance of the QFN package is increased.

[0007] This disclosure provides a method of assembling an electronic device using a stencil. The method includes depositing a solder paste at a plurality of stencil apertures on a printed circuit board (PCB) pad, wherein the PCB pad has a first predefined area and one stencil aperture of the plurality of stencil apertures has an aperture wall defining a second predefined area that is less than or equal to the first predefined area. The method further includes providing a surface mount circuit component on top of the solder paste, wherein the surface mount circuit component includes at least one terminal with a non-solderable side surface. The method also includes performing a reflow process to form a non-convex solder joint between the at least one terminal and the PCB pad.

[0008] Further, this disclosure provides a stencil for depositing solder on a printed circuit board (PCB). The stencil includes a plurality of stencil apertures, a first stencil aperture of the plurality of apertures having an aperture wall defining an aperture perimeter. The aperture wall is configured to not extend beyond an outer edge of a PCB pad provided on the printed circuit board, the aperture wall is configured to not extend beyond an outer edge of a terminal of a

surface mount component, and the first stencil aperture is configured to receive solder paste to form a non-convex solder joint between the PCB pad and the terminal.

[0009] Further, this disclosure provides an electronic device assembled using a stencil. The electronic device includes a printed circuit board (PCB) including a substrate defining a plurality of PCB pads with a first predefined area, a surface mount circuit component including at least one terminal, and a non-convex solder joint between the at least one terminal and one of the plurality of PCB pads.

[0010] In this manner, various aspects of the disclosure provide for improvements in at least the technical fields of solder paste stencils and assembling with solder paste stencils. The foregoing introduction is intended solely to give a general idea of various aspects of the disclosure and does not limit the scope of the disclosure in any way.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The patent or application file contains at least one drawing executed in color. Copies of this patent or patent application publication with color drawing(s) will be provided by the Office upon request and payment of the necessary fee.

[0012] FIG. 1 is a crack formation image illustrating a crack in an example convex solder joint.

[0013] FIG. 2 is an image illustrating an example convex solder joint.

[0014] FIG. 3 is a schematic diagram illustrating a cross-section of a concave solder joint.

[0015] FIG. 4 is a schematic diagram illustrating a cross-section of a straight solder joint.

[0016] FIG. 5 is a schematic diagram illustrating a cross-section of a convex solder joint.

[0017] FIG. 6 is a graph illustrating a comparison of principal stress levels exerted by the solder joints of FIGS. 3-5.

[0018] FIG. 7 is an image illustrating a cross-section of a higher-stress stencil aperture design.

[0019] FIG. 8 is an image illustrating a cross-section of a lower-stress stencil aperture design.

[0020] FIG. 9 is an image illustrating a higher-stress stencil aperture design.

[0021] FIG. 10 is a table illustrating ratios of the higher-stress stencil aperture design of FIG. 9.

[0022] FIG. 11 is an image illustrating a lower-stress stencil aperture design.

[0023] FIG. 12 is a table illustrating ratios of the lower-stress stencil aperture design of FIG. 11.

[0024] FIG. 13 is an image illustrating a higher-stress stencil aperture design and a lower-stress stencil aperture design.

[0025] FIG. 14 is an image illustrating a cross-section of an exemplary concave solder joint.

[0026] FIG. 15 is an image illustrating a cross-section of an exemplary concave solder joint.

[0027] FIG. 16 is a graph illustrating an accumulated creep strain of the concave solder joint of FIG. 15.

[0028] FIG. 17 is a graph illustrating creep work in the concave solder joint of FIG. 15.

[0029] FIG. 18 is a flowchart method for creating a concave solder joint, in accordance with some embodiments of the disclosure.

DETAILED DESCRIPTION

[0030] FIG. 3 is a schematic diagram illustrating a cross-section 200 of a concave solder joint 204. The concave solder joint 204 solders a terminal 202 of a surface-mount circuit component to a PCB board 206. The concave solder joint 204 includes a solder alloy (e.g., SnAgCu). The terminal 202 of the component that contacts the solder, thus creating the concave solder joint 204, may be comprised of copper (Cu). Copper may be prone to severe oxidation, leading to poor solder wetting and, thus, solder defects when the solder joint is a higher-stress shape (i.e., a convex shape) relative to a low stress shape (i.e., a non-convex shape). The PCB board 206 may include a copper substrate. The concave solder joint 204 is one example of the lower-stress shape because the concave solder joint 204 is a non-convex shape.

[0031] The solder alloy and the terminal 202 may have different coefficients of thermal expansion (CTE) from one another. For example, the CTE of SnAgCu is 21 parts per million per degrees (Celsius) (ppm/°C) and the CTE of Cu is 17 ppm/°C. The differing CTE between the solder alloy and the terminal 202 leads the expansion and contraction at differing rates during thermal cycles, thus producing principal stress on the concave solder joint 204. In some embodiments, thermal cycles is designed to impose defects to the surface-mount circuit component.

[0032] For example, a surface-mount circuit component, and in particular solid-state devices (SSD), includes an approximate acceptance failure risk of 0.1%. The achievement of the concave shape of the concave solder joint 204 will be described below with respect to FIGS. 8 and 10.

[0033] FIG. 4 is a schematic diagram illustrating a cross-section 210 of a straight solder joint 214. The straight solder joint 214 solders a terminal 212 of a surface-mount circuit component to a PCB board 216. The straight solder joint 214 may include a similar solder alloy as the concave solder joint 204 (FIG. 3). More importantly, the straight solder joint 214 is another example of the lower-stress shape because the straight solder joint 214 is a non-convex shape.

[0034] FIG. 5 is a schematic diagram illustrating a cross-section 220 of a convex solder joint 224, similar to the convex solder joint of FIGS. 1 and 2. The convex solder joint 224 solders a terminal 222 of a surface-mount circuit component to a PCB board 226. The convex solder joint 224 may include a similar solder alloy as concave solder joint 204 (FIG. 3). The convex solder joint 224 is an example of the higher-stress shape because the convex shoulder joint is a convex shape.

[0035] FIG. 6 is a graph 300 illustrating a comparison of principal stress levels exerted by the concave solder joint 204, the straight solder joint 214, and the convex solder joint 224 with respect to the distance from the terminals 202, 212, 222 of the surface-mounted components. The curvature of the solder joint influences the stress state in the concave solder joint 204, the straight solder joint 214, and the convex solder joint 224.

[0036] As illustrated in the graph 300, the convex solder joint 224 produces the highest stress with a maximum stress level that is about 75% larger than that for the concave solder joint 204 at a location near the terminal 202, 222. The principal stress level exerted by the concave solder joint 204 may be at a maximum about 0.125 millimeters (mm) from the terminal 202. For example, the maximum value may be 30 mega-pascal (MPa). The principal stress level exerted by the concave solder joint 204 may once again peak at 0.2mm from the terminal 202. As shown in the graph 300, the principal stress level exerted by the concave solder joint 204 may be greater than the principal stress level exerted by the convex solder joint 224 at 0.2mm from the terminal 202, 222. Thus, the curvature of the solder joint may transfer the stress to a location that is further from the terminal such that cracking is minimized at the interface of the solder joint and the terminal.

[0037] The concave solder joint 204 may result in the least amount of stress relative to the straight solder joint 214 and the convex solder joint 224. However, both the concave solder joint 204 and the straight solder joint 214 are lower in overall stress than the convex solder joint 224.

[0038] FIG. 7 is an image illustrating a cross-section of a higher-stress stencil aperture design 400. The higher-stress stencil aperture design 400 includes a QFN terminal 402, solder paste 404, and a PCB pad 406. The solder paste 404 extends past the edge of the QFN terminal 402 by a first predetermined amount. In some embodiments, the higher-stress stencil aperture design 400 leads to a convex solder joint 224 when the reflow process takes place due to the solder paste 404 expanding to contact the edge of the QFN terminal 402. In some embodiments, the higher-stress stencil aperture design 400 may include solder paste 404 that contacts the side edge of the QFN terminal 402.

[0039] FIG. 8 is an image illustrating a cross-section of a lower-stress stencil aperture design 410. The lower-stress stencil aperture design 410 includes a QFN terminal 412, solder paste 414, and a PCB pad 416. The solder paste 414 has the same length as the bottom of the QFN terminal 412. In some embodiments, a stencil is laid on the PCB pad 416. The stencil includes a plurality of stencil apertures. For example, a first stencil aperture of the plurality of stencil apertures has an aperture wall defining an aperture perimeter that has a first area. The first stencil aperture may receive the solder paste 414 and the solder paste 414 may have the same area as the first area.

[0040] In some embodiments, an edge of the solder paste 414 may be parallel to an edge of the QFN terminal 412 prior to the reflow process taking place due to the wall of the stencil aperture aligning with the edge of the QFN terminal 412. The edge of the solder paste 414 and the edge of the QFN terminal 412 combine to provide a single, combined side surface in a first direction prior to the reflow process. The lower-stress stencil aperture design 410 leads to a concave solder joint 204 when the reflow process takes place. The lower-stress stencil aperture design 410 does not include solder paste 414 contacting the side edge of the QFN terminal 412. The absence of solder paste 414 at the side edge of the QFN terminal 412 minimizes the risk of a solder joint cracking at the side edge of the QFN terminal 412, especially during thermal cycles.

[0041] FIG. 9 is an image illustrating a higher-stress stencil aperture design 500. The higher-stress stencil aperture design 500 includes a plurality of PCB pads 502 (individually PCB pads 502A–502N), a stencil 501 with a plurality of stencil apertures 504 (individually stencil apertures 504A–504N), and a component layout 506. In some embodiments, the higher-stress stencil aperture design 500 receives a surface-mount circuit component that includes terminals that are configured to be electrically connected to the plurality of PCB pads 502 via solder paste that is placed using the plurality of stencil apertures 504. For example, the surface-mount circuit component may be a QFN package. However, alternative surface-mount circuit component may be also contemplated. Accordingly, in some examples, the area of the PCB pad 502A and the area of the

stencil aperture 504A are substantially the same in the higher-stress stencil aperture design 500. For example, during the reflow process, the solder paste is unable to wick due to the equivalent areas of the PCB pad 502A and the stencil aperture 504A that allows an equivalent area of solder paste to be laid on the PCB pad 502A.

[0042] FIG. 10 is a table 508 illustrating ratios between the PCB pad 502 and the stencil aperture 504 and the component terminals and the stencil aperture 504 of the higher-stress stencil aperture design 500. For example, dimensions of the PCB pad 502 corresponding to a first lead may be 0.2 millimeters (mm) wide by 0.8mm long and dimensions of the corresponding stencil aperture 504 may be 0.17mm wide by 0.84mm long. In the current example, the ratio of the PCB pad 502 to the stencil aperture 504 would be 1:0.89 and the ratio of the terminal of the surface-mount component to the stencil aperture 504 would be 1:1.428.

[0043] FIG. 11 is an image illustrating a lower-stress stencil aperture design 510 that has lower-stresses relative to the higher-stress stencil aperture design 500. The lower-stress stencil aperture design 510 includes a plurality of PCB pads 512 (individually PCB pads 512A–512N), a stencil 511 with a plurality of stencil apertures 514 (individually, stencil apertures 514A–514N) and a component layout 516. In some embodiments, each of the plurality of stencil apertures 514 is formed by cutting a stencil using electroforming. In some embodiments, a first stencil aperture 514A of the plurality of stencil apertures 514 includes a rectangular aperture wall with a first lengthwise wall, a second lengthwise wall that is parallel to the first lengthwise wall, a first widthwise wall, and a second widthwise wall that is parallel to the first widthwise wall. Similar to the higher-stress stencil aperture design 500, in some embodiments, the lower-stress stencil aperture design 510 receives a surface-mount circuit component that includes terminals that are configured to be electrically connected to a first PCB pad 512A of the plurality of PCB pads 512 via solder paste that has an area corresponding to the first stencil aperture 514A. For example, solder paste may be deposited on the stencil such that the solder paste contacts the PCB pad 512A at the first stencil aperture 514A. In some embodiments, the first PCB pad 512A may be a first predetermined area comprised of copper (Cu). In some embodiments, the first stencil aperture 514A and the corresponding solder paste is a second predetermined area that is less than the first predetermined area. For example, the second predetermined area may be a 1:0.8 to 1:1.2 ratio of an area of the terminals of the surface-mount circuit component.

[0044] In some embodiments, the surface-mount circuit component may include various sized terminals. The first stencil aperture 514A and the corresponding solder paste of the lower-stress stencil aperture design 510 may correspond to the various sized terminals, such that the solder

paste is the same area as the various sized terminals, and is less than the area of each of the plurality of PCB pads 512.

[0045] In some embodiments, the first stencil aperture 514A allows for an increased height of solder paste. The lower-stress stencil aperture design 510 significantly reduces the potential for cracking between the solder paste and the terminal during a reflow process by allowing the solder paste to wick when heated, thus, creating a concave solder joint.

[0046] FIG. 12 is a table 518 illustrating ratios between the PCB pad 512 and the stencil aperture 514 and the component terminals and the stencil aperture 514 of the lower-stress stencil aperture design 510. For each corresponding lead of the higher-stress stencil aperture design 500, the leads of the lower-stress stencil aperture design 510 include a smaller ratio between both the PCB pad 512 and the stencil aperture 514 and the component terminals and the stencil aperture 514. This allows for the solder paste to wick during the reflow process, thus, creating a concave solder joint. For example, dimensions of the PCB pad 512 corresponding to a first lead may be 0.2 millimeters (mm) wide by 0.8mm long and dimensions of the corresponding stencil aperture 514 may be 0.2mm wide by 0.48mm long. In the current example, the ratio of the PCB pad 512 to the stencil aperture 514 would be 1:0.725 and the ratio of the terminal of the surface-mount component to the stencil aperture 514 would be 1:1.2.

[0047] In some embodiments, the lower-stress stencil aperture design 510 may produce a reduction in volume of solder paste used compared to the higher-stress stencil aperture design 500. For example, the volume of solder used at each lead may be reduced between 1 and 15%. In the illustrated embodiment, the volume reduction of the first lead is 18.9%. Alternatively, in some embodiments, the volume of solder paste used may increase less than 1% compared to the higher-stress stencil aperture design 500. For example, the height of the solder paste and/or the width of the stencil aperture 514 may increase. The values in the table 518 are merely exemplary and may include any number of values that produce ratios that are less than the ratios of table 508.

[0048] FIG. 13 is an image illustrating a higher-stress stencil aperture design 520 and a lower-stress stencil aperture design 530. The higher-stress stencil aperture design 520 includes a first PCB pad 522, a second PCB pad 524, a first stencil aperture 526, and a second stencil aperture 528. The dimensions of the higher-stress stencil aperture design 520 are provided in Table 1, below. The dimensions are provided as a width and a length in millimeters (mm). The first stencil aperture 526 extends paste an edge of the first PCB pad 522 by 0.08 millimeters (mm). The second stencil aperture 528 extends paste an edge of the second PCB pad 524 by 0.05mm.

	First PCB Pad (mm)	Second PCB Pad (mm)	First Stencil Aperture (mm)	Second Stencil Aperture (mm)
Higher-Stress Design	0.20 x 0.60	0.20 x 0.80	0.18 x 0.44	0.18 x 0.83

Table 1

[0049] The lower-stress stencil aperture design 530 increases the stand-off height of a surface-mount surface component (e.g., QFN package), thus increasing board level reliability (BLR). The lower-stress stencil aperture design 530 includes a first PCB pad 532, a second PCB pad 534, a first stencil aperture 536, and a second stencil aperture 538. The dimensions of the lower-stress stencil aperture design 530 are provided in Table 2, below. The dimensions are provided as a width and a length in millimeters (mm). In the lower-stress stencil aperture design 530, the first stencil aperture 536 does not extend past the first PCB pad 532 in a length direction. The second stencil aperture 538 extends past the second PCB pad 534 in a direction opposite the extension of second stencil aperture 528 of higher-stress stencil aperture design 520. In the lower-stress stencil aperture design 530, no excess solder paste is on the PCB pads 532, 534. The stand-off height of the surface-mount surface component is increased due to solder surface tension pulling back onto the PCB pads 532, 534 during the reflow process.

	First PCB Pad (mm)	Second PCB Pad (mm)	First Stencil Aperture (mm)	Second Stencil Aperture (mm)
Lower-Stress Design	0.20 x 0.60	0.20 x 0.80	0.18 x 0.39 or 0.19 x 0.38	0.18 x 0.83

Table 2

[0050] FIG. 14 is an image illustrating a cross-section 600 of an exemplary concave solder joint 606. The concave solder joint 606 results from employing the lower-stress stencil aperture designs 410, 510 (FIG. 8; FIG. 11) to electrically connect a terminal 602 of a QFN package to a PCB pad 604. For example, solder paste is deposited on the PCB pad 604 such that the solder paste does not contact the side of the terminal and a stencil aperture is created that allows solder wicking during a reflow process. In some embodiments, the concave solder joint 606 uses a lower volume of solder paste compared to alternative solder joints (e.g., convex).

[0051] FIG. 15 is an image illustrating a cross-section 700 of an exemplary concave solder joint 706. The cross-section 700 may be a zoomed in view of the cross-section 600 (FIG. 6). The concave solder joint 706 electrically connects a terminal 702 of a QFN Package to a PCB pad 704.

The concave solder joint 706 has undergone thermal cycling, resulting in a crack 708 propagating. In some embodiments, the crack 708 appeared between 500 and 1000 thermal cycles. The crack 708 may have begun in the concave solder joint 706 section near the bottom corner of the terminal 702 and propagated in different directions. In some embodiments, the crack propagates away from the terminal 702, thus, lessening any potential detriment to the electrical connection between the terminal 702 and the PCB pad 704. The crack 708 formed by the concave solder joint 706 may exert lower stress levels during thermal cycling than a crack formed by a convex solder joint. Accordingly, the crack 708 reduces a crack propagation magnitude compared to cracks formed by a convex solder joint. The crack 708 may be the result of creep deformation during thermal cycling.

[0052] FIG. 16 is a graph 710 illustrating an accumulated creep strain of the concave solder joint 706. The graph 710 uses data that was collected when the concave solder joint 706 underwent a temperature change of -40°C to 100°C. The data may be collected using a finite element analysis to evaluate critical points of damage initiation. As illustrated in the graph 710, a maximum creep strain occurs at the lower corner of the concave solder joint 706, as evidenced by the light blue coloring. The location of the maximum creep strain in the graph 710 allows for a minimum strain along a side surface of the terminal 702. Creep is a time-dependent deformation when a material is subjected to a stress for a prolong period of time.

[0053] FIG. 17 is a graph illustrating creep work in the concave solder joint 706. The graph 720 uses data that was collected when the concave solder joint 706 underwent a temperature change of -40°C to 100°C. The data may be collected using a finite element analysis to evaluate critical points of damage initiation. As illustrated in the graph 720, the creep work is at a maximum at the lower corner of the concave solder joint 706, as evidenced by the red and yellow coloring. Along the side surface of the terminal 702, the creep work is at a minimum, as evidenced by the dark blue coloring.

[0054] FIG. 18 is a flowchart method 800 for creating a concave solder joint, in accordance with some embodiments of the disclosure. The method 800 includes providing a solder paste to a PCB pad (at block 802). In some embodiments, the PCB pad is an exposed area of a stencil aperture. In some embodiments, the PCB pad is a first predetermined area and the stencil aperture is a second predetermined area that is less than the first predetermined area.

[0055] The method 800 includes providing a circuit component on top of the solder paste (at block 804). In some embodiments, the circuit component is a QFN package with terminals that are the

same area on the bottom as the solder paste. Alternatively, in some embodiments, the circuit component is any surface-mounted circuit component.

[0056] The method 800 also includes performing a reflow process to form a non-convex solder joint (at block 806). In some embodiments, during the reflow process, the solder wicks and forms a concaved solder joint. The concaved solder joint provides an electrical connection between the terminal of the QFN package and the PCB pad.

[0057] The following are enumerated examples of methods, stencils, and electronic devices described herein. Example 1: a method of assembling an electronic device using a stencil, the method comprising: depositing a solder paste at a plurality of stencil apertures on a printed circuit board (PCB) pad, wherein the PCB pad has a first predefined area and one stencil aperture of the plurality of stencil apertures has an aperture wall defining a second predefined area that is less than or equal to the first predefined area; providing a surface mount circuit component on top of the solder paste, wherein the surface mount circuit component includes at least one terminal with a non-solderable side surface; and performing a reflow process to form a non-convex solder joint between the at least one terminal and the PCB pad.

[0058] Example 2: the method of Example 1, wherein the solder paste has a first side surface and the at least one terminal has a second side surface that is substantially parallel to the first side surface, and wherein, prior to performing the reflow process, the first side surface and the second side surface combine to form a combined side surface in a first direction.

[0059] Example 3: the method of any of Examples 1 or 2, wherein the non-convex solder joint is a concave solder joint.

[0060] Example 4: The method of any of Examples 1 or 3, wherein the non-convex solder joint is a straight solder joint.

[0061] Example 5: The method of any of Examples 1 through 4, wherein the surface mount circuit component is a quad flat no-lead (QFN) package.

[0062] Example 6: The method of any of Examples 1 through 5, wherein the PCB pad is a copper material.

[0063] Example 7: The method of any of Examples 1 through 6, wherein a maximum principal stress level exerted by the non-convex solder joint is less than or equal to 42 megapascal (MPa).

[0064] Example 8: The method of Example 7, wherein the maximum principal stress level exerted by a concave solder joint is approximately equal to 30 MPa.

[0065] Example 9: The method of any of Examples 1 through 8, wherein a width of the solder paste is 0.2 millimeters (mm) prior to the reflow process.

[0066] Example 10: A stencil for depositing solder on a printed circuit board (PCB), the stencil comprising: a plurality of stencil apertures, a first stencil aperture of the plurality of stencil apertures having an aperture wall defining an aperture perimeter, wherein the aperture wall is configured to not extend beyond an outer edge of a PCB pad provided on the PCB, wherein the aperture wall is configured to not extend beyond an outer edge of a terminal of a surface mount component, and wherein the first stencil aperture is configured to receive solder paste to form a non-convex solder joint between the PCB pad and the terminal.

[0067] Example 11: The stencil of Example 10, wherein the non-convex solder joint is a concave solder joint.

[0068] Example 12: The stencil of Example 10, wherein the non-convex solder joint is a straight solder joint.

[0069] Example 13: The stencil of any of Examples 10 through 12, wherein a maximum principal stress level exerted by the non-convex solder joint is less than or equal to 42 megapascal (MPa).

[0070] Example 14: The stencil of Example 13, wherein the non-convex solder joint is a concave solder joint, wherein the maximum principal stress level exerted by the concave solder joint is approximately equal to 30 MPa.

[0071] Example 15: The stencil of any of Examples 10 through 14, wherein a portion of the aperture perimeter defined by the aperture wall has a width of approximately 0.2 millimeters (mm).

[0072] Example 16: The stencil of any of Examples 10 through 15, wherein the surface mount component is a quad flat no-lead (QFN) package.

[0073] Example 17: The stencil of any of Examples 10 through 16, wherein the first stencil aperture is configured to receive the solder paste that contacts the PCB pad and only a surface of the terminal that faces the PCB pad.

[0074] Example 18: An electronic device assembled using a stencil, the electronic device comprising: a printed circuit board (PCB) including a substrate defining a plurality of PCB pads

with a first predefined area; a surface mount circuit component including at least one terminal; and a non-convex solder joint between the at least one terminal and one of the plurality of PCB pads.

[0075] Example 19: The electronic device of Example 18, wherein the non-convex solder joint is a concave solder joint.

[0076] Example 20: The electronic device of any of Examples 18 or 19, wherein the non-convex solder joint contacts the one of the plurality of PCB pads and contacts only a surface of the at least one terminal that faces the one of the plurality of PCB pads.

[0077] Example 21: The electronic device of Example 18, wherein the non-convex solder joint is a straight solder joint.

[0078] Example 22: The electronic device of any of Examples 18 through 21, wherein the surface mount circuit component is a quad flat no-lead (QFN) package.

[0079] Example 23: The electronic device of any of Examples 18 through 22, wherein the substrate is a copper material.

[0080] Example 24: The electronic device of any of Examples 18 through 23, wherein a maximum principal stress level exerted by the non-convex solder joint is less than or equal to 42 megapascal (MPa).

[0081] Example 25: The electronic device of Example 24, wherein the maximum principal stress level exerted by a concave solder joint is approximately equal to 30 MPa.

[0082] Example 26: The electronic device of any of Examples 18 through 25, wherein a creep strain of the non-convex solder joint is at a maximum at a bottom corner of the at least one terminal.

[0083] Example 27: The electronic device of any of Examples 18 through 26, wherein a width of the solder paste is 0.2 millimeters (mm).

[0084] Example 28: The electronic device of any of Examples 18 through 28, wherein the non-convex solder joint is formed after a reflow process is performed on the electronic device.

[0085] In the above description, numerous details are set forth, such as providing a stencil aperture for solder paste to exclusively contact of a portion of a terminal that is parallel to the a PCB board of a surface-mount component prior to a reflow process and allowing for wicking of the solder paste to form a non-convex solder joint, and the like, in order to provide an understanding of one or more aspects of the present disclosure. It will be readily apparent to one skilled in the art that

these specific details are merely exemplary and not intended to limit the scope of this application. This description is intended solely to give a general idea of various aspects of the disclosure and does not limit the scope of the disclosure in any way.

[0086] Accordingly, it is to be understood that the above description is intended to be illustrative and not restrictive. Many embodiments and applications other than the examples provided would be apparent upon reading the above description. The scope should be determined, not with reference to the above description, but should instead be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled. It is anticipated and intended that future developments will occur in the technologies discussed herein, and that the disclosed systems and methods will be incorporated into such future embodiments. In sum, it should be understood that the application is capable of modification and variation.

[0087] All terms used in the claims are intended to be given their broadest reasonable constructions and their ordinary meanings as understood by those knowledgeable in the technologies described herein unless an explicit indication to the contrary is made herein. In particular, use of the singular articles such as “a,” “the,” “said,” etc. should be read to recite one or more of the indicated elements unless a claim recites an explicit limitation to the contrary.

[0088] The Abstract is provided to allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. In addition, in the foregoing Detailed Description, it can be seen that various features are grouped together in various embodiments for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed embodiments require more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus, the following claim is hereby incorporated into the Detailed Description and standing on its own as a separately claimed subject matter.

CLAIMS

What is claimed is:

1. A method of assembling an electronic device using a stencil, the method comprising:
 - depositing a solder paste at a plurality of stencil apertures on a printed circuit board (PCB) pad, wherein the PCB pad has a first predefined area and one stencil aperture of the plurality of stencil apertures has an aperture wall defining a second predefined area that is less than or equal to the first predefined area;
 - providing a surface mount circuit component on top of the solder paste, wherein the surface mount circuit component includes at least one terminal with a non-solderable side surface; and
 - performing a reflow process to form a non-convex solder joint between the at least one terminal and the PCB pad.
2. The method of claim 1, wherein the solder paste has a first side surface and the at least one terminal has a second side surface that is substantially parallel to the first side surface, and
 - wherein, prior to performing the reflow process, the first side surface and the second side surface combine to form a combined side surface in a first direction.
3. The method of claim 1, wherein the non-convex solder joint is a concave solder joint.
4. The method of claim 1, wherein the non-convex solder joint is a straight solder joint.
5. The method of claim 1, wherein the surface mount circuit component is a quad flat no-lead (QFN) package.
6. The method of claim 1, wherein the PCB pad is a copper material.
7. The method of claim 1, wherein a maximum principal stress level exerted by the non-convex solder joint is less than or equal to 42 megapascal (MPa).
8. The method of claim 7, wherein the maximum principal stress level exerted by a concave solder joint is approximately equal to 30 MPa.

9. The method of claim 1, wherein a width of the solder paste is 0.2 millimeters (mm) prior to the reflow process.
10. A stencil for depositing solder on a printed circuit board (PCB), the stencil comprising:
 - a plurality of stencil apertures, a first stencil aperture of the plurality of stencil apertures having an aperture wall defining an aperture perimeter,
 - wherein the aperture wall is configured to not extend beyond an outer edge of a PCB pad provided on the PCB,
 - wherein the aperture wall is configured to not extend beyond an outer edge of a terminal of a surface mount component, and
 - wherein the first stencil aperture is configured to receive solder paste to form a non-convex solder joint between the PCB pad and the terminal.
11. The stencil of claim 10, wherein the non-convex solder joint is a concave solder joint.
12. The stencil of claim 10, wherein the non-convex solder joint is a straight solder joint.
13. The stencil of claim 10, wherein a maximum principal stress level exerted by the non-convex solder joint is less than or equal to 42 megapascal (MPa).
14. The stencil of claim 13, wherein the non-convex solder joint is a concave solder joint, wherein the maximum principal stress level exerted by the concave solder joint is approximately equal to 30 MPa.
15. The stencil of claim 10, wherein a portion of the aperture perimeter defined by the aperture wall has a width of approximately 0.2 millimeters (mm).
16. The stencil of claim 10, wherein the surface mount component is a quad flat no-lead (QFN) package.
17. The stencil of claim 10, wherein the first stencil aperture is configured to receive the solder paste that contacts the PCB pad and only a surface of the terminal that faces the PCB pad.

18. An electronic device assembled using a stencil, the device comprising:
 - a printed circuit board (PCB) including a substrate defining a plurality of PCB pads with a first predefined area;
 - a surface mount circuit component including at least one terminal; and
 - a non-convex solder joint between the at least one terminal and one of the plurality of PCB pads.
19. The electronic device of claim 18, wherein the non-convex solder joint is a concave solder joint.
20. The electronic device of claim 18, wherein the non-convex solder joint contacts the one of the plurality of PCB pads and contacts only a surface of the at least one terminal that faces the one of the plurality of PCB pads.

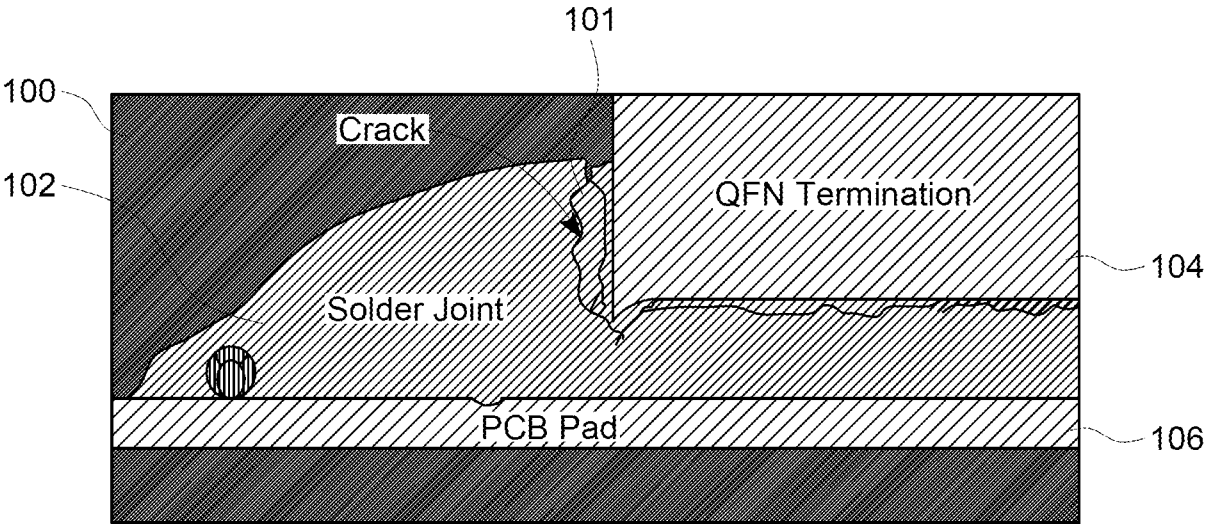


FIG. 1

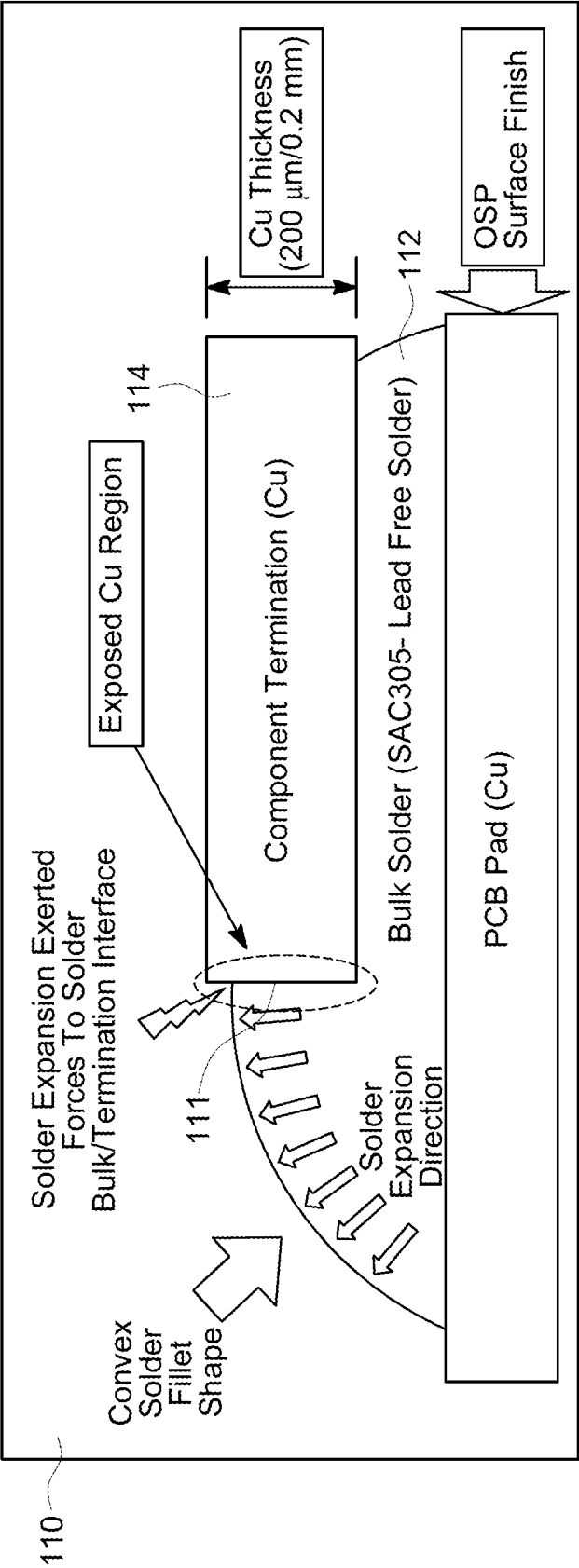


FIG. 2

200

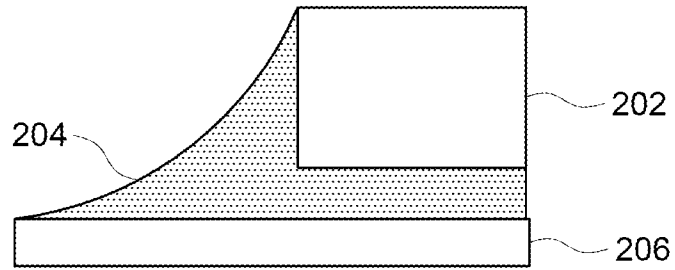


FIG. 3

210

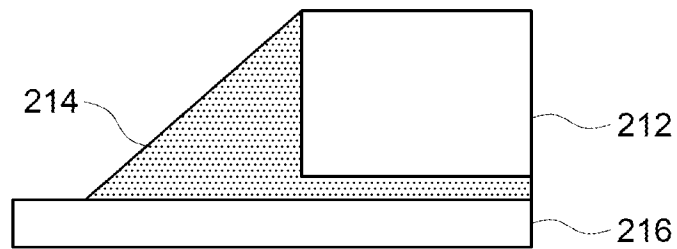


FIG. 4

220

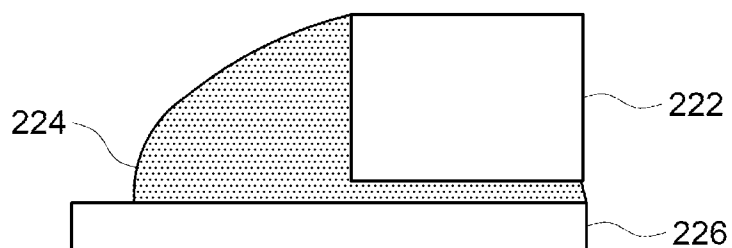


FIG. 5

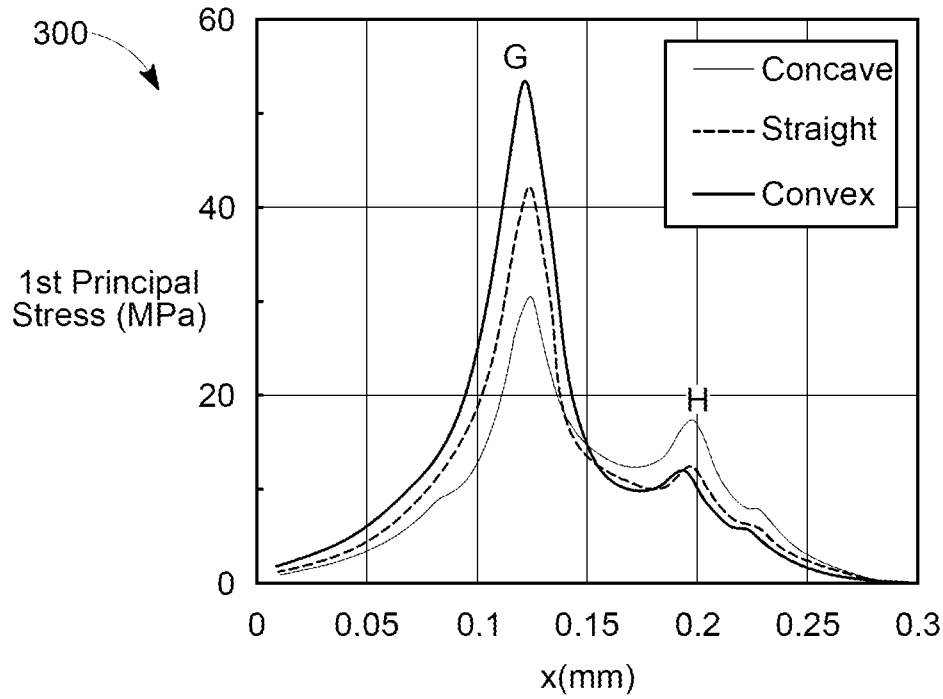


FIG. 6

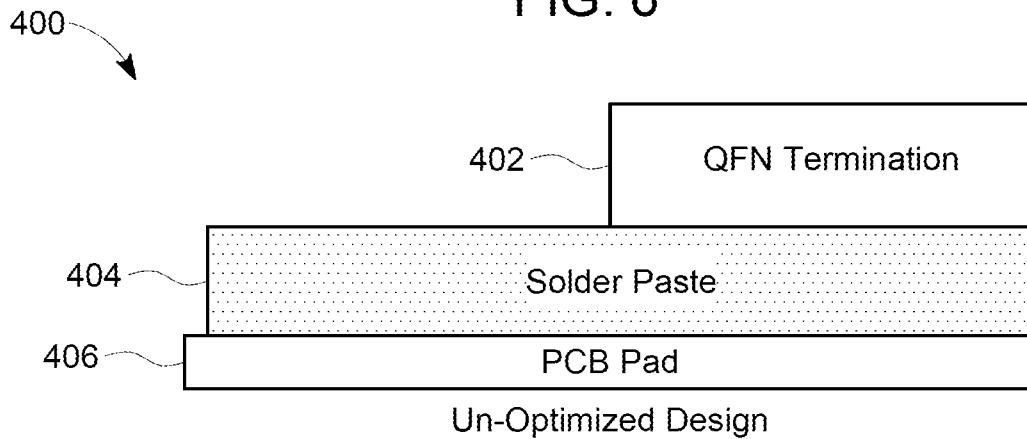


FIG. 7

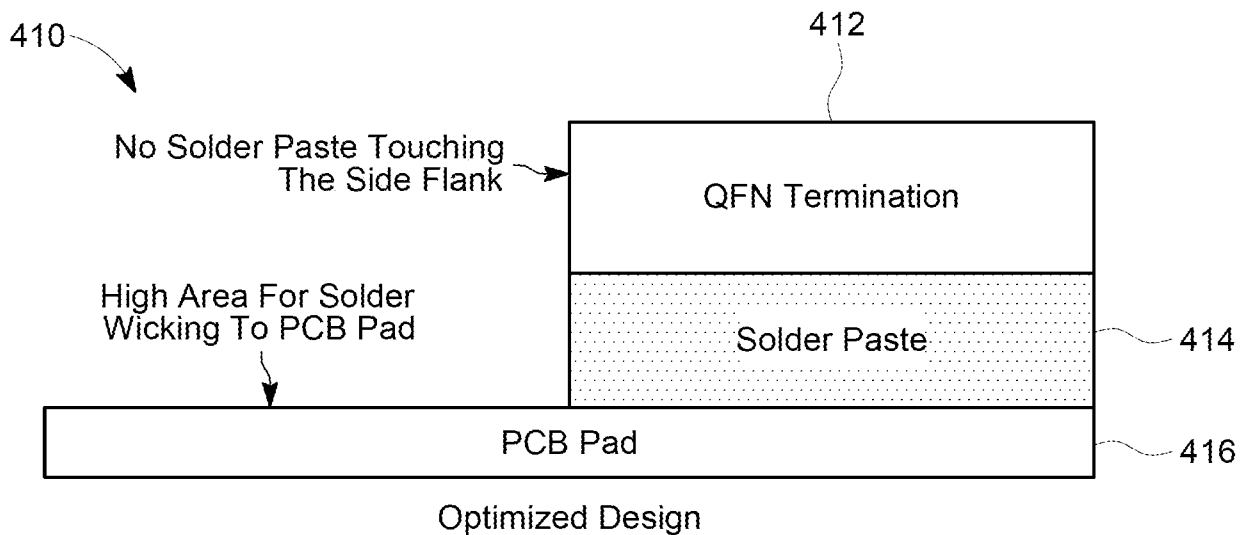


FIG. 8

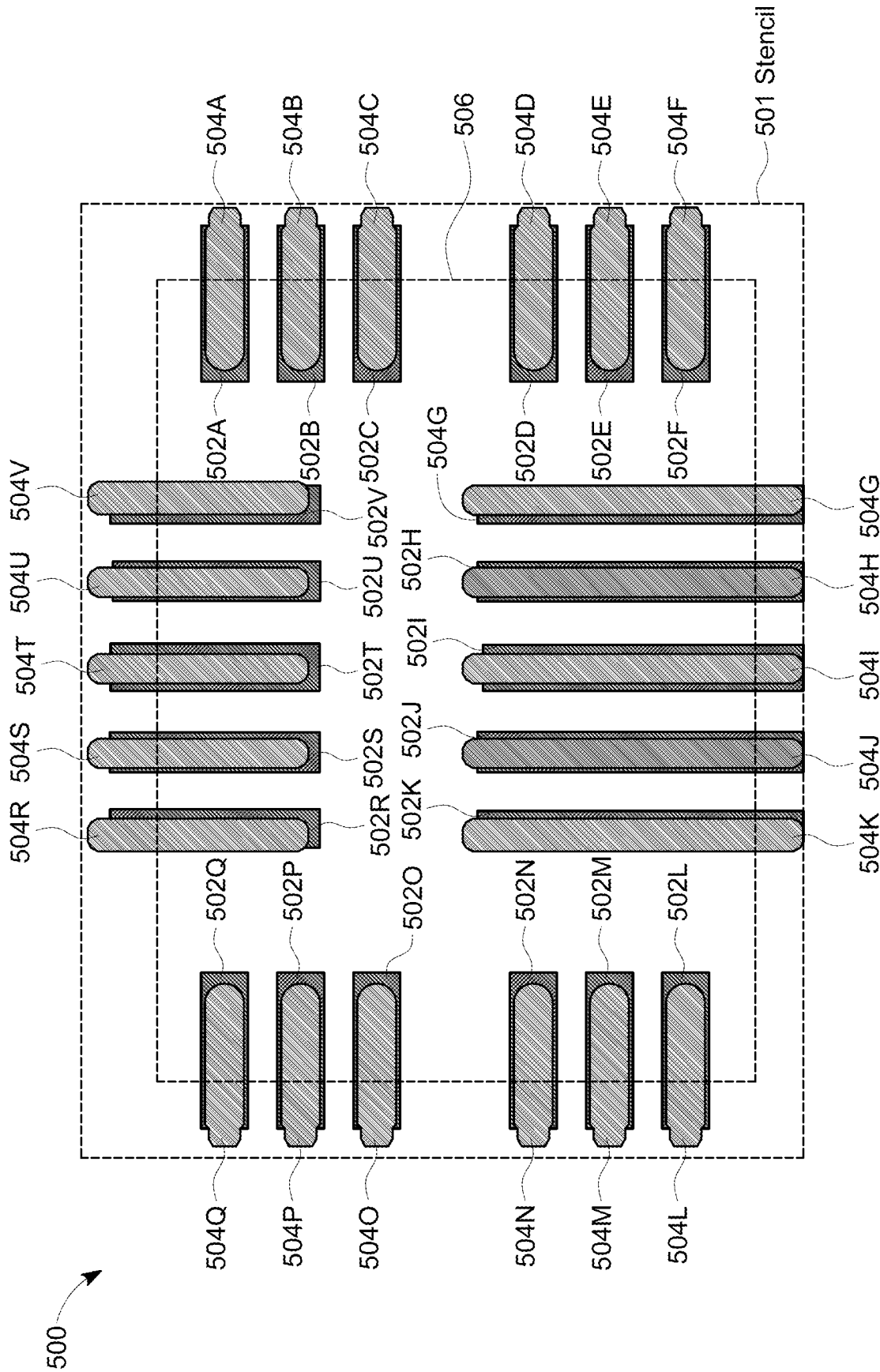
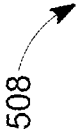


FIG. 9

508



Lead	PCB Pad	Stencil Opening	Radio PCB Pad: Stencil Aperture	Radio Component Termination: Stencil Aperture	Area Ratio	Theoretical Volume (mm ³)
1	0.2mm × 0.8mm	0.17mm × 0.84mm	1:0.89	1:1.428	0.71	0.0143
2	0.2mm × 1mm	0.17mm × 1.14mm	1:0.97	1:1.21	0.737	0.0194
3	0.25mm × 1mm	0.18mm × 1.14mm	1:0.82	1:1.03	0.796	0.0206
4	0.2mm × 1.7mm	0.17mm × 1.75mm	1:0.87	1:1.06	0.766	0.0298
5	0.25mm × 1.7mm	0.18mm × 1.75mm	1:0.74	1:0.9	0.83	0.0315

FIG. 10

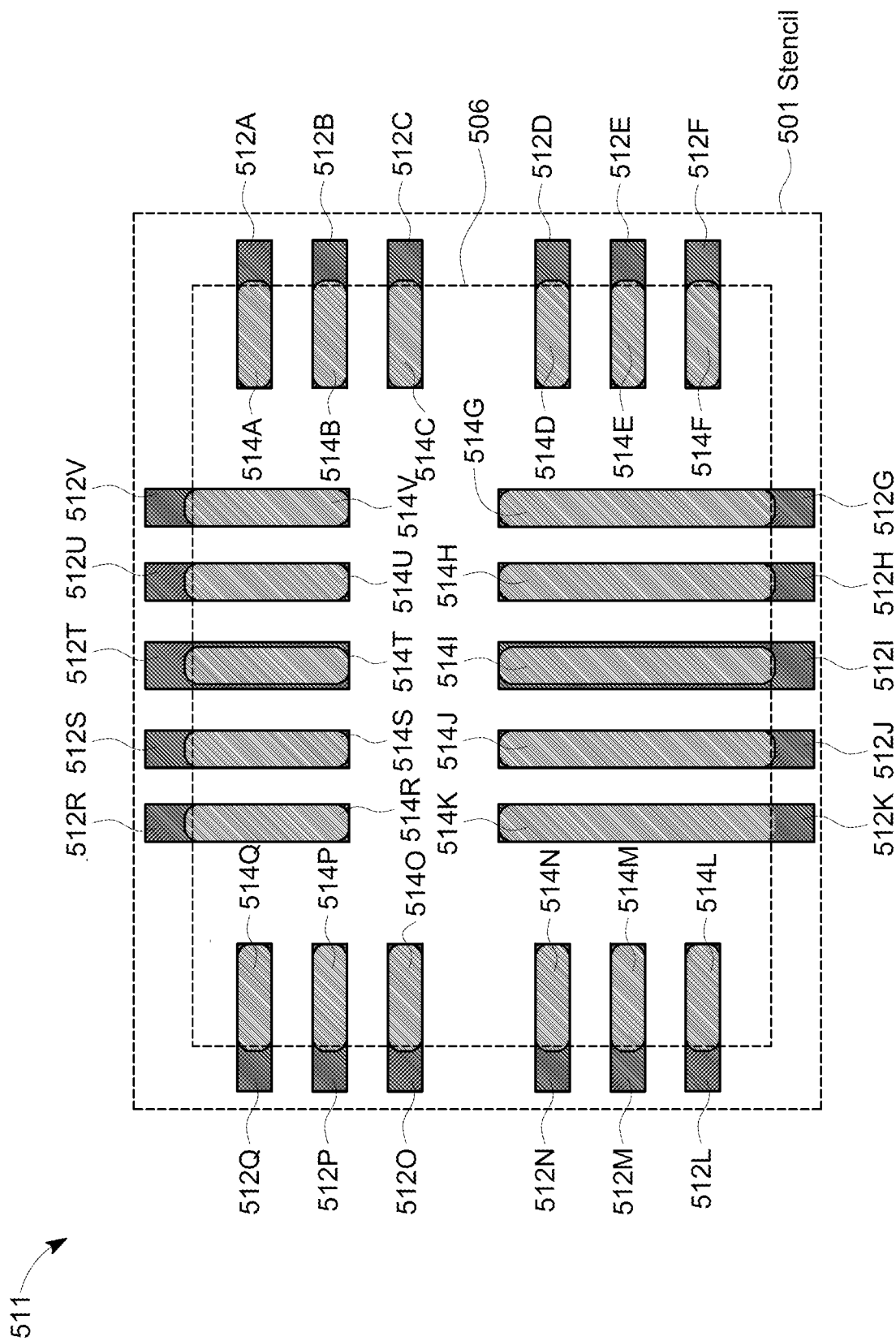


FIG. 11

518



Lead	New Opening (mm)	Area Ratio	Radio PCB Pad: Stencil Aperture	Radio Component Termination: Stencil Aperture	Theoretical Volume (mm ³)
1	0.58 × 0.2	0.77	1:0.725	1:1.2	0.0116
2	0.883 × 0.2	0.839	1:0.88	1:1.1	0.0177
3	0.883 × 0.2	0.839	1:0.71	1:0.8	0.0177
4	1.482 × 0.2	0.898	1:0.87	1:1.1	0.0297
5	1.482 × 0.2	0.898	1:0.7	1:0.85	0.0297

FIG. 12

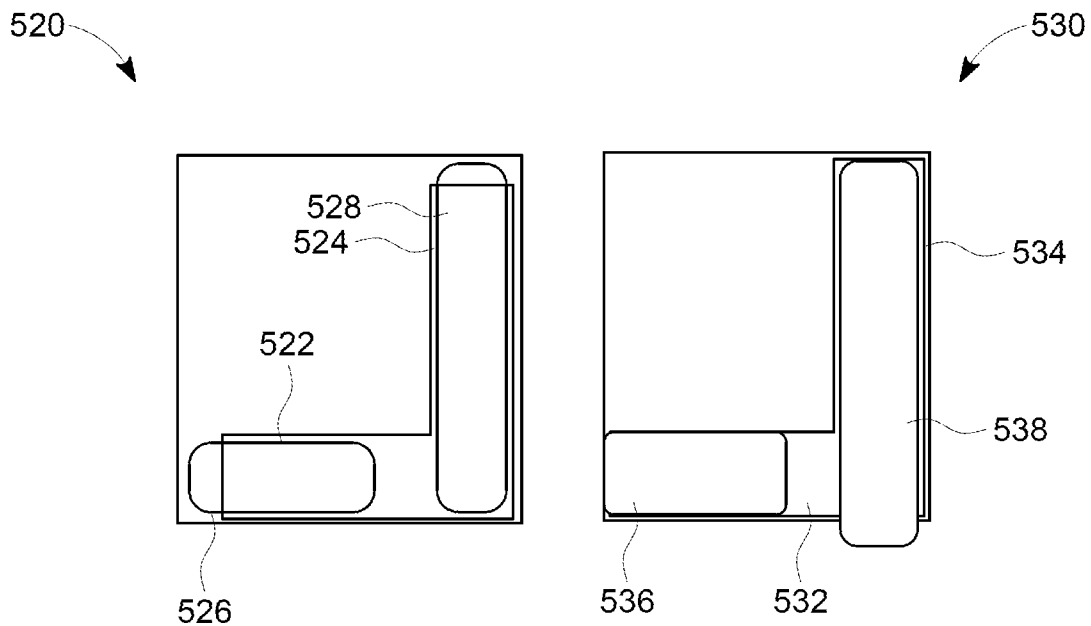


FIG. 13

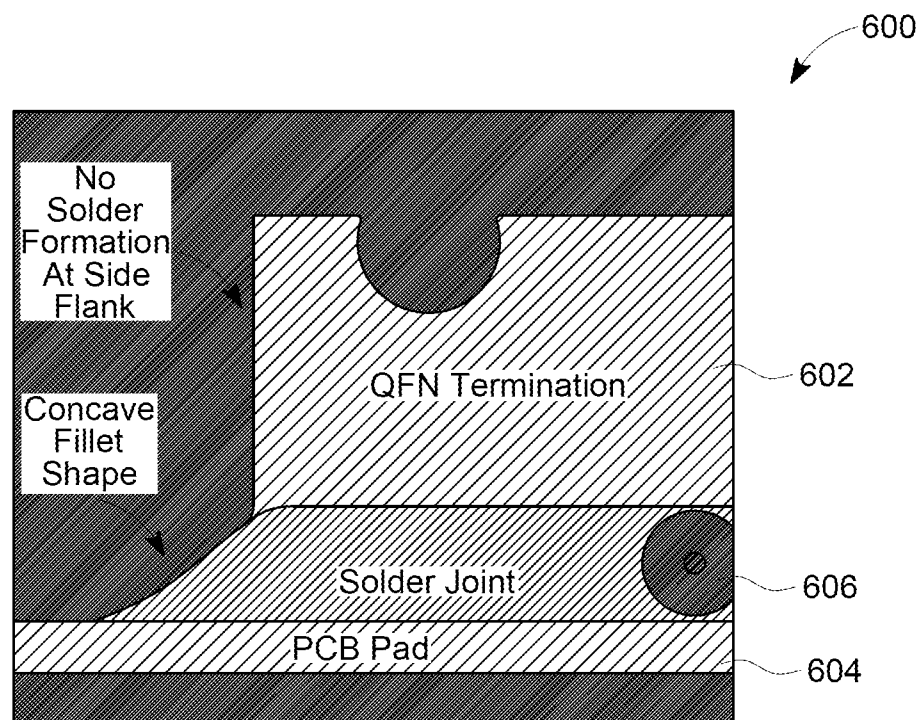


FIG. 14

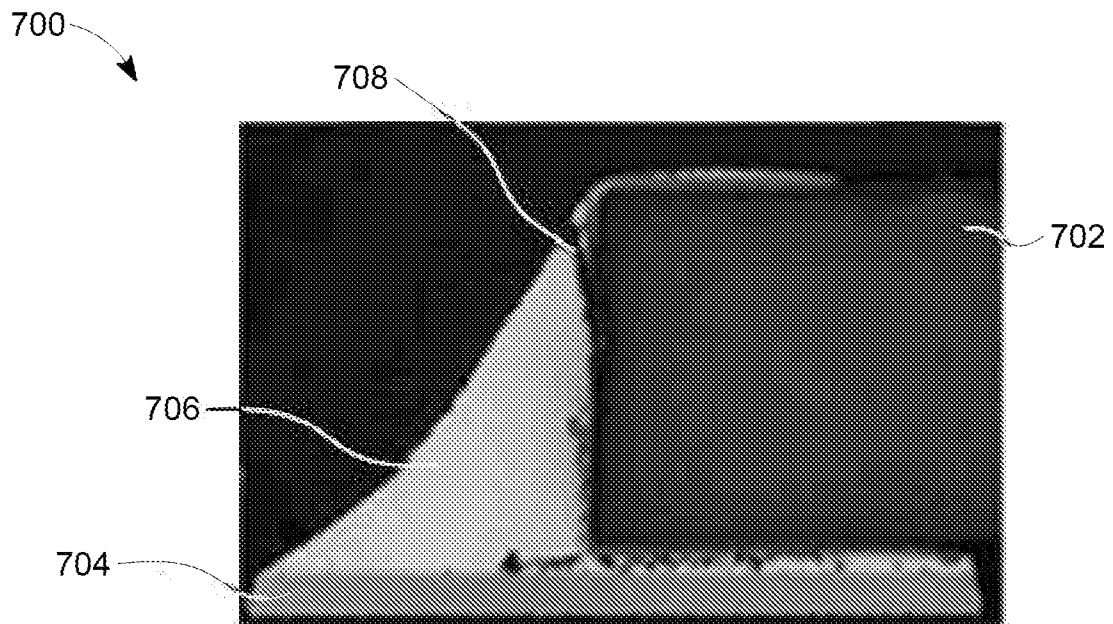


FIG. 15

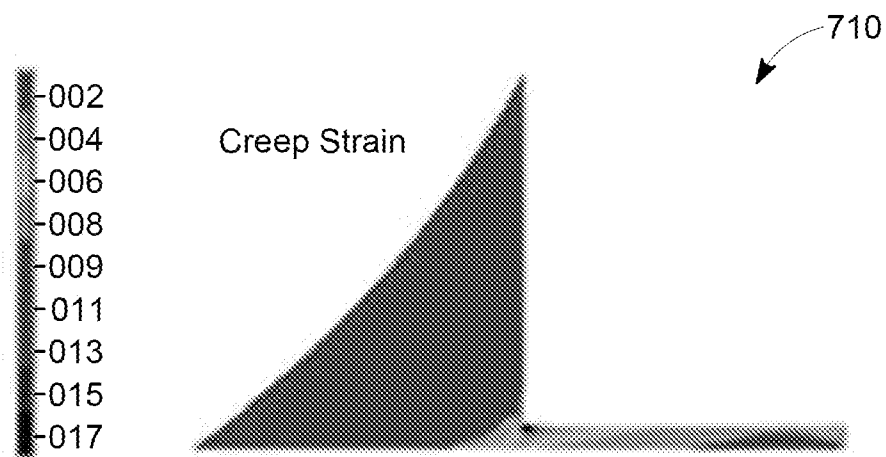


FIG. 16

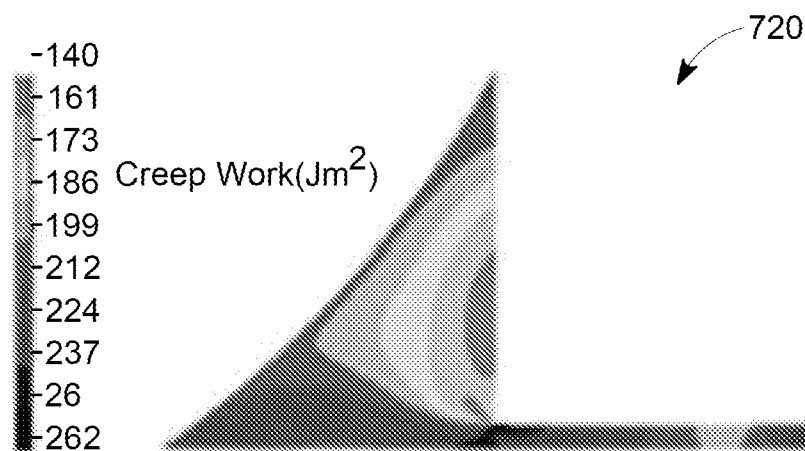


FIG. 17

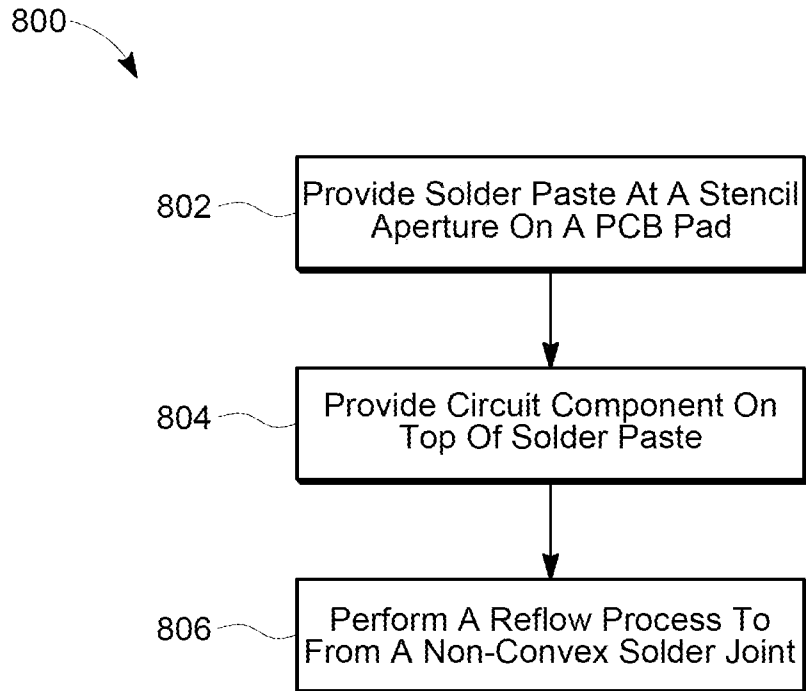


FIG. 18

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2023/017446

A. CLASSIFICATION OF SUBJECT MATTER H05K 3/34(2006.01)i; H05K 3/12(2006.01)i; H05K 1/11(2006.01)i; H05K 1/09(2006.01)i According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H05K 3/34(2006.01); B23K 35/22(2006.01); H05K 1/11(2006.01) Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: stencil, solder paste, printed circuit board pad, surface mount circuit component, terminal, non-convex solder joint		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 06-232544 A (MITSUBISHI ELECTRIC CORP.) 19 August 1994 (1994-08-19) See paragraphs [0014]-[0039] and figures 1, 5, 7-8.	1-20
A	US 5743007 A (HIROAKI ONISHI et al.) 28 April 1998 (1998-04-28) See column 2, line 55 - column 5, line 29 and figures 1A-7B.	1-20
A	US 2001-0011676 A1 (RICHARD REGNER et al.) 09 August 2001 (2001-08-09) See paragraphs [0019]-[0026] and figures 1-4.	1-20
A	JP 10-154870 A (KOKUSAI ELECTRIC CO., LTD.) 09 June 1998 (1998-06-09) See paragraphs [0009]-[0013] and figures 1-4.	1-20
A	US 2013-0206456 A1 (SONY CORPORATION) 15 August 2013 (2013-08-15) See paragraphs [0051]-[0071] and figures 1-7.	1-20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 01 August 2023		Date of mailing of the international search report 01 August 2023
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer PARK, Hye Lyun Telephone No. +82-42-481-3463

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2023/017446

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				US	6094832	A	01 August 2000
				US	6248452	B1	19 June 2001
				US	6391468	B2	21 May 2002
JP	10-154870	A	09 June 1998	None			
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				CN	103260346	B	10 April 2018
				JP	2013-168517	A	29 August 2013
				JP	6396633	B2	26 September 2018
				KR	10-2013-0094235	A	23 August 2013
				US	9113564	B2	18 August 2015